

## Frequency Control Word Setting Procedure for 8V19N850D

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### 1. Overview

The 8V19N850D DPLL0 and DPLL1 DCO frequency can be controlled by Frequency Control Word (FCW). This document provides an 8V19N850D general procedure of setting FCW. Examples are provided to show the register setting and expected results of the output frequencies for initial setting and subsequent FCW update. In these examples, DPLL1 is used. The same principles can be applied to DPLL0 with equivalent registers.

### 2. Convert ppm to FCW for Register

In write Frequency Mode, the APLL VCO is tuned by the FCW as follows:

$$F_{VCO} = F_{XO} \times N \times (1 + FCW)$$

Where:

- $F_{VCO}$  is the APLL VCO frequency.
- $F_{XO}$  is the OSCI/XO\_DPLL frequency which is fixed.
- N is the nominal APLL feedback divider ratio.
- FCW is the tuning word which is 42 bit 2's complement and LSB is  $2^{-53}$
- FCW is calculated as follows:
  - $FCW = FFO \times 10^{-6} \times 2^{53}$  (Convert this FCW from decimal to HEX for registers).
  - FFO is the target fraction frequency in ppm.

### 3. General FCW Setting Procedure

1. Write Frequency Enable = 1.  
For DPLL1, R1A4, D5 = 1  
(For DPLL0, R124, D5 = 1)
2. Integrator Enable = 1.  
For DPLL1, R1A4, D3 = 1  
(For DPLL0, R124, D3=1)
3. Combo Enable = 1.  
For DPLL1, R1A5, D4 = 1  
(For DPLL0, R125, D4 = 1)
4. Direct Write Mode = 1.  
For DPLL1, R1A6, D0 = 1  
(For DPLL0, R126, D0 = 1)
5. Write Frequency.  
Using the equation shown above to convert ppm to hex, load the hex data to the following registers:  
For DPLL1, R1B5[1:0] = [41:40], R1B4[7:0] to 1B0[7:0] = [39:0]  
(For DPLL0, R135[1:0] = [41:40], R134[7:0] to 130[7:0] = [39:0])

### 4. Examples

#### 4.1 Setting Register for Write Frequency

DPLL1 can be either free-running and lock to the local OCXO, or can be a slave of DPLL0. RFPLL locked DPLL1. For simplicity, assume the local OCXO is perfect frequency with 0 error. The Output R0 = 491.52MHz

**Write register 0x1a4 = 28h** (i.e., 00101000b)

D5 = 1, Write Frequency Enable,

D3 = 1 Integrator Enable,

**Write register 0x1a5 = 10h** (i.e., 00000001b)

D4 = 1, Combo\_EN\_DPLL1 Mode

**Write register 0x1a6 = 03h** (i.e., 00000011b)

D0 = 1, Direct Write Mode

D1 = 1 (Default = 1, FCW works either 0 or 1)

**Write registers 0x1B0, 1B1, 1B2, 1B3, 1B4, 1B5 = 00 00 00 00 00 00** (0.0 ppm). At this point, the FCW is not yet applied.

Assume the OCXO has no frequency error

FCW = 0 or FWC is not yet activated, expect Output R0 = 491.520000MHz (nominal, assume the OCXO frequency does not have an error).

## 4.2 Update FCW

Update Frequency Control Word = 0.320ppm

Control Word in decimal =  $(0.320 * 10^{-6}) * 2^{53} = 2882303761.517$

Convert 2882303762 to hex for Register Data Write frequency field = AB CC 77 12 Hex

**Write registers 0x1B0, 1B1, 1B2, 1B3, 1B4, 1B5 = 12 77 CC AB 00 00** (0.320 ppm calculated and converted from the above equation)

Expect frequency R0 = 491.520000MHz + 0.320ppm

## 4.3 Subsequent Update FCW

Update Frequency Control Word = 5.76ppm

Control Word in decimal =  $(5.76 * 10^{-6}) * 2^{53} = 51881467707.308$

Convert 51881467707 to hex for Register Data Write frequency field = C 14 60 5F 3B Hex

**Write registers 0x1B0, 1B1, 1B2, 1B3, 1B4, 1B5 = 3B 5F 60 14 0C 00** (5.76 ppm calculated and converted from the above equation)

Expect frequency R0 = 491.520000MHz + 5.76ppm

## 5. Revision History

Revision	Date	Description
1.0	Mar 17, 2021	Initial release.

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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