FemtoClock3 Power Supply Filtering Recommendation

This document provides a power supply filtering recommendation for the FemtoClock3 (FC3) family of devices including the RC32312, RC22312, RC32308, and RC22308. The recommendation is based on our the FC3's evaluation board designs.

Power supply noise will have an impact on the phase noise and jitter performance of FC3's output clocks. The intended audience of this document is board designers who are seeking a power supply filtering scheme.

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1. Power Supply Block Diagram

The power supply noise typically comes external sources like the switching frequency of the power supply and internal sources like coupling between the power supply pins from different domains (like digital and RF).

The PCB designer should not supply power directly from such a noisy power supply to any noise-sensitive timing or clock ICs. Renesas recommends using local LDOs combined with a power decoupling filter to distribute the power to each pin on the clock device.

Low-noise LDOs offer high power supply rejection ratio (PSRR) to block the incoming noise, and are preferred over a large stronger filter due to the board size advantage.

The LDO's outputs are connected to the device through the recommended filter.

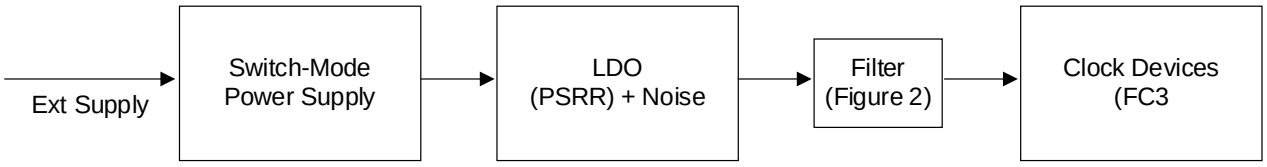

Figure 1. Power Supply Block Diagram

2. Filtering Circuit Topology

The power supply filtering circuit recommended for each power rail are displayed in Figure 2 and Figure 3. The figures show the power trails of the RC32312 and RC32308, respectively. Separate filters should be used for VDDOs with different frequency families, while a common filter can be shared between VDDOs with the same frequency family.

Also recommended is to never combine the VCO rail with any other rails, and to make sure all decoupling capacitors are grounded through their own individual vias.'' Do not share the same ground via.

In general, all VDDO pins should be connected to the power sources even if the output is not used.

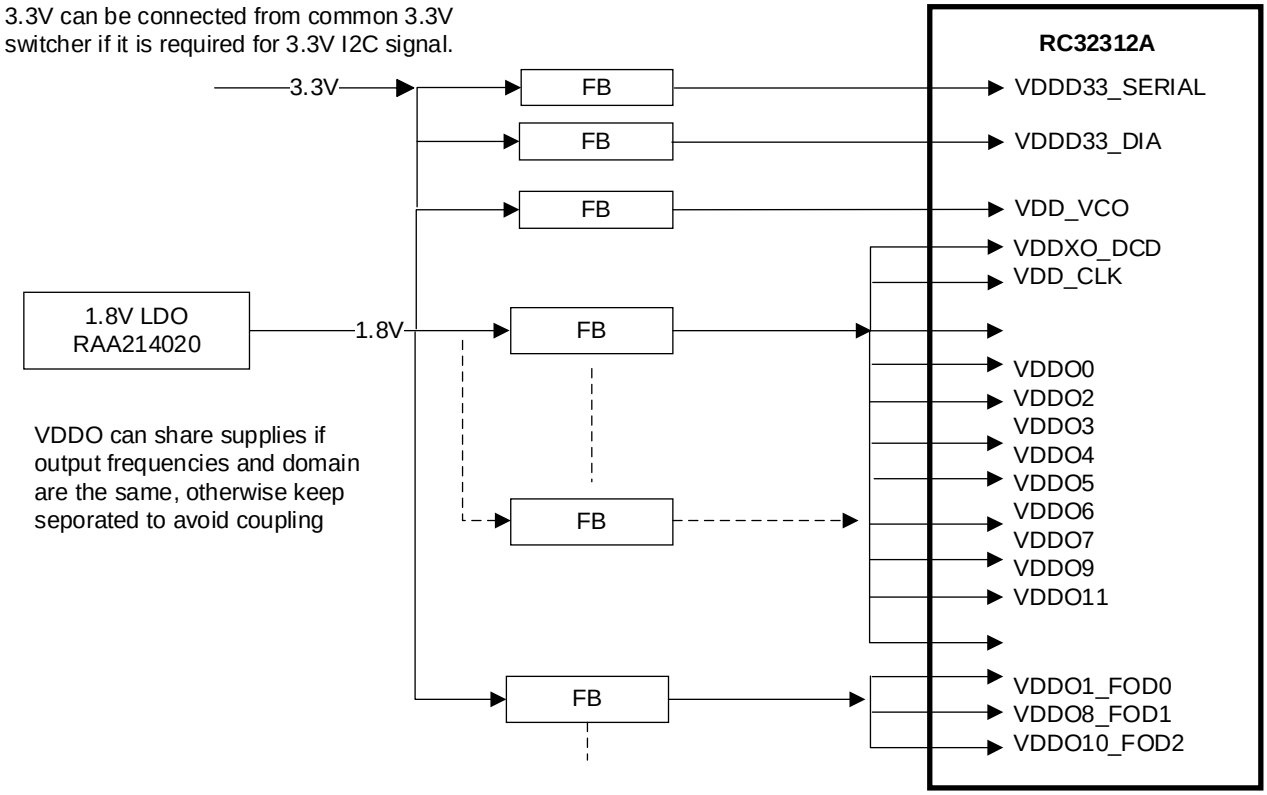

Figure 2. RC32312A Power Trails and Supply Options

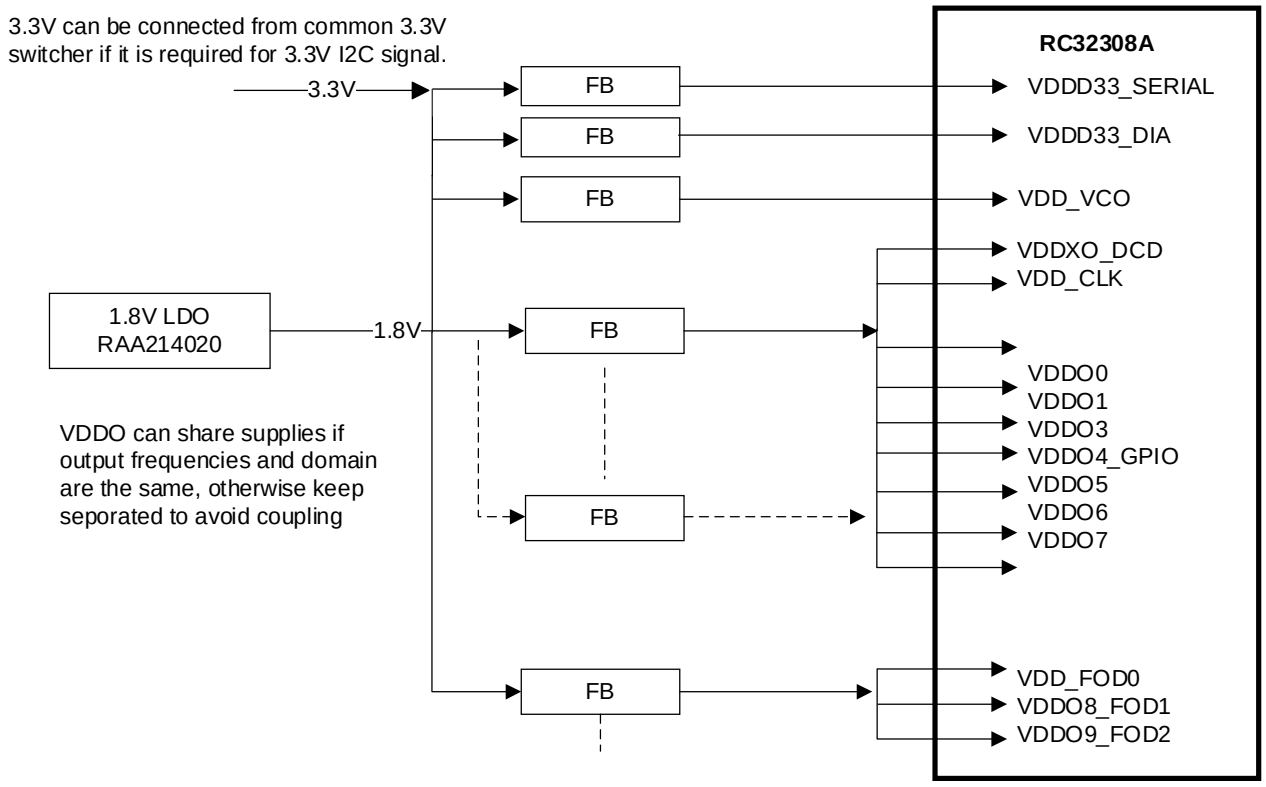

Figure 3. RC32308A Power Trails and Supply Options

A π(pi)-shape filtering network consists of decoupling capacitors of 0.1uF and 10uF with a ferrite bead, as shown in Figure 4. The right-side decoupling capacitors should be placed as close as possible to each power supply pin. A list of recommended ferrite beads is provided in Table 1.

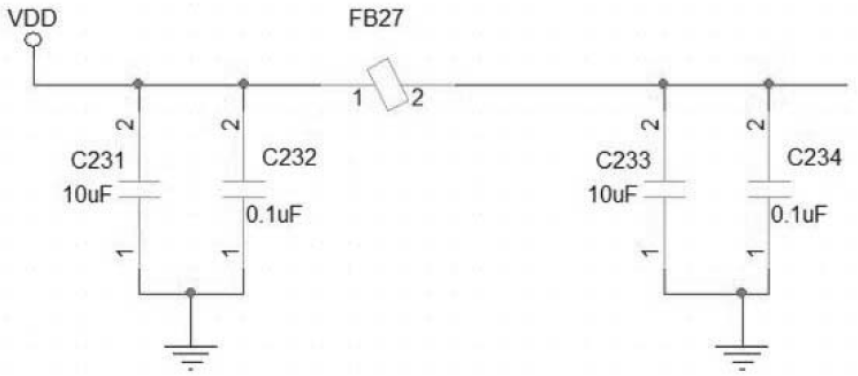

Figure 4. Recommended Filter Topology

Table 1. Ferrite Bead Selection [1]

Part Number	Category	Specification Summary
BLM18BB221SN1D	General use	220 Ohms at 100MHz 1 Ferrite Bead 0603 (1608 Metric) 500mA 250mOhm
BLM18PG221SN1D	For DC power Line	220 Ohms at 100MHz 1 Power Line Ferrite Bead 0603 (1608 Metric) 1.4A 100mOhm
BLM18KG221SN1D	For DC power Line	220 Ohms at 100MHz 1 Power Line Ferrite Bead 0603 (1608 Metric) 2.2A 50mOhm
BLM18BD221SN1D	For high-speed signal line	220 Ohms at 100MHz 1 Signal Line Ferrite Bead 0603 (1608 Metric) 200mA 450mOhm

1. For more information, see AN-805 Recommended Ferrite Beads.

3. Revision History

Revision	Date	Description
1.00	March 22, 2023	Initial release.

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