FemtoClock 4 and FemtoClock 4 Wireless Frequency Planning

Introduction

This document describes how to configure the FemtoClock®4 (FC4) and FemtoClock 4 Wireless (FC4W) devices to achieve the best performance in terms of phase noise with the lowest crosstalk. Included is an example using the GUI in Synthesizer Mode.

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1. Overview

FemtoClock 4 (FC4) and FemtoClock 4 Wireless (FC4W) devices are a family of telecom-integrated circuits that are low-phase noise jitter attenuators. These include the RC38616/RC38412 for FC4W and the RC32412/RC32418 for FC4.

The jitter attenuators (JA) consist of inputs, a DPLL to perform the filtering, an APLL, and outputs. The synthesizers (Synth) do not have any inputs or DPLLs; only an APLL and outputs. The parameters for optimizing for low-phase noise will be slightly different for JA mode versus Synth mode. Some commonalities also exist during the optimization process. This document focuses on the commonalities of the devices.

Figure 1 shows a block diagram of an FC4W device (RC38616) in JA mode.

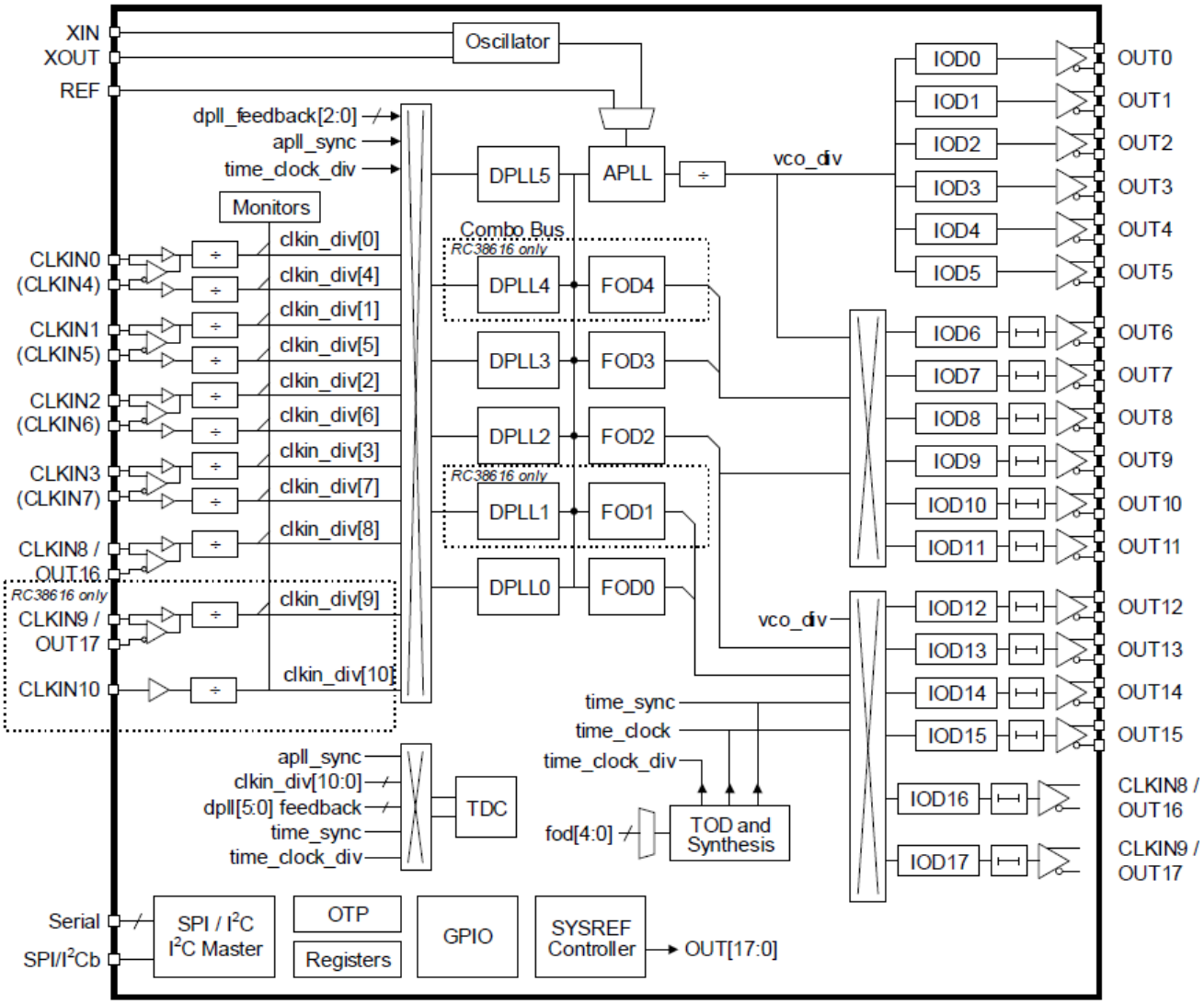


Figure 1. Block Diagram of an FC4W Device

Figure 2 shows a block diagram of an FC4 device (RC32418) in JA mode.

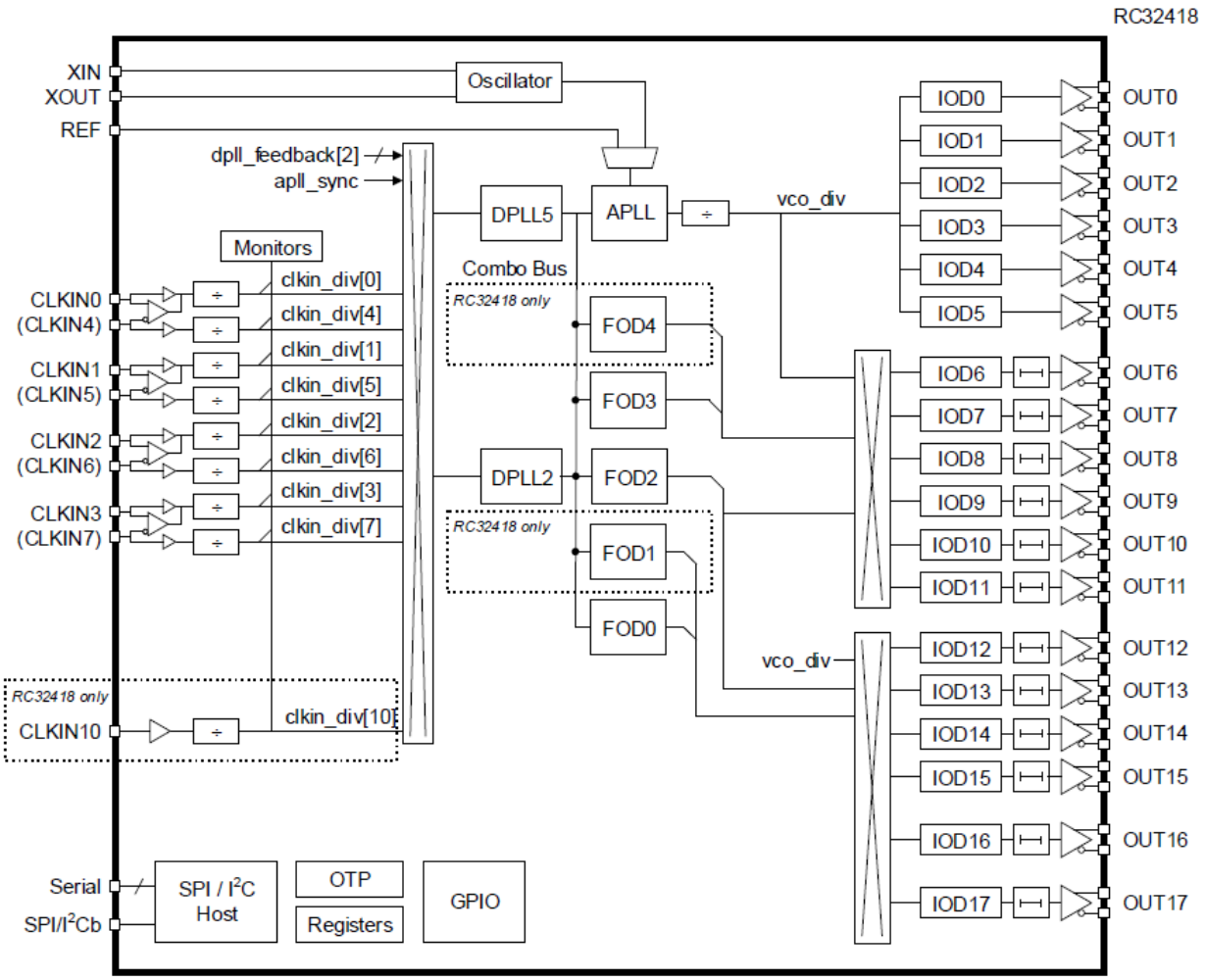


Figure 2. Block Diagram of an FC4 Device

The major differences between FC4 and FC4W are more DPLLs for FC4W, and the addition of the TDC and Time Sync block. In terms of frequency planning, the same rules and recommendations apply to both.

2. XTAL Frequency Selection

Use the following guidelines for choosing the correct XTAL when optimizing for phase noise:

1. Selection to be based upon the device datasheet specifications for frequency, CL, ESR, and drivel level.
2. The higher the XTAL frequency, the better the phase noise. This also helps in filtering out reference feedthrough (a specific type of spur).
3. Choose an appropriate frequency based on the mode, the output frequency plan, and the VCO frequency.
   a. For Synth mode applications, choose a XTAL that **is** an integer multiple of the VCO frequency. For example, VCO = 10GHz, XTAL = 62.5MHz and 50MHz are valid values (62.5MHz is the better value).
   b. For JA mode applications, choose a XTAL that **is not** an integer of the VCO or the output frequency. Also calculate the harmonics to ensure they are outside the integration range of interest. For example, VCO = 10GHz, XTAL = 68MHz.

3. Output Selection

FC4/W has Integer Output Dividers (IOD) and Fractional Output Dividers (FOD) as shown in Figure 3. Outputs 0 to 5 are divided by a fixed divide by 4 directly from the APLL followed by the IOD. Outputs 6 to 17 have the option of being divided by 4 from the APLL or to be divided by an FOD, followed by the IOD. These latter outputs also go through a mux before the IOD.

For best phase noise, use Outputs 0 to 5 as they go through the path of least circuitry. If more outputs are necessary, they can be used simultaneously with Outputs 0 to 5 but will have more noise compared to Outputs 0 to 5.

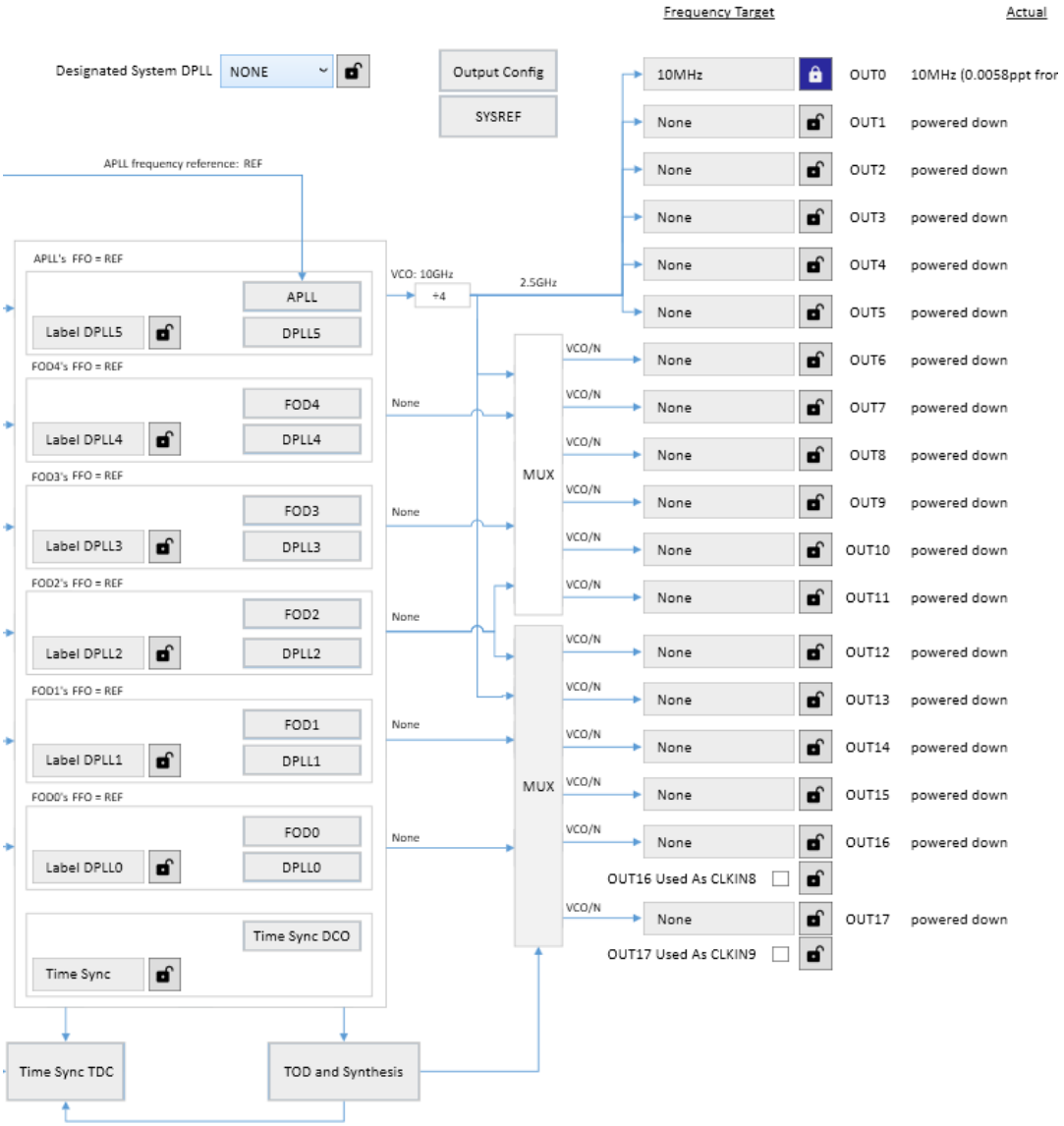


Figure 3. GUI Diagram Showing the Various FC4 Outputs

4. Fractional Output Dividers (FOD)

Fractional output frequencies are sometimes necessary. FC4/W has up to five FODs depending on the variant. To avoid integer boundary spurs using the FODs, the fractional portion of the divide ratio should be between 0.2 and 0.8 as shown in Figure 4. This applies to both FC4 and FC4W. Depending on the configuration, a divide ratio between 0.2 and 0.8 is not guaranteed.

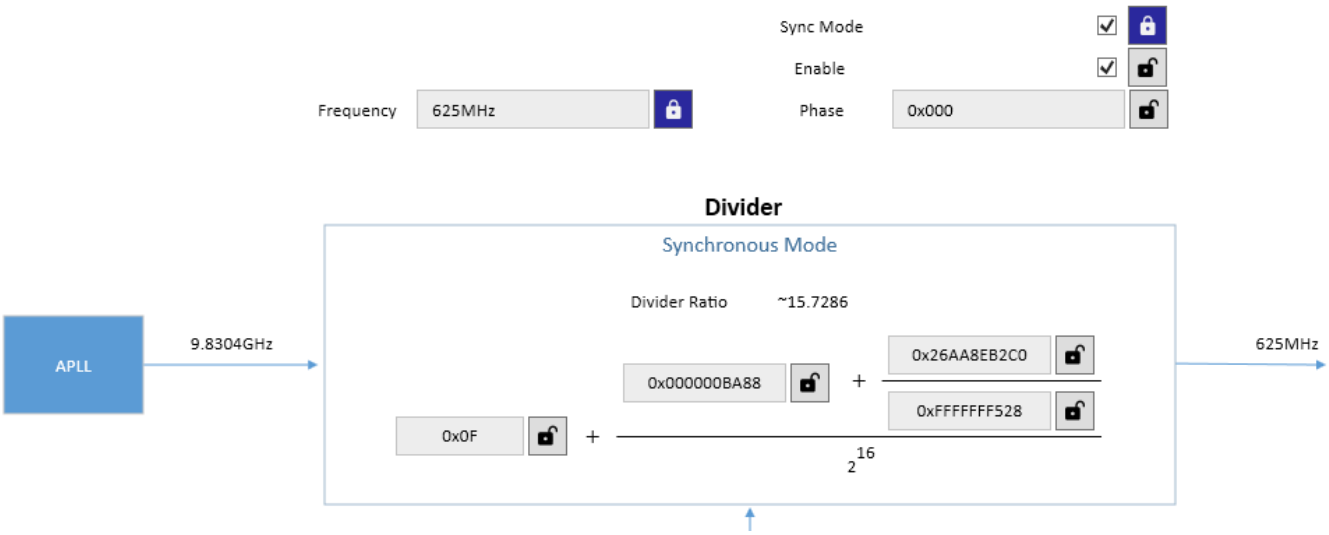


Figure 4. GUI Diagram of the FOD Block Showing the Divider Ratio

5. Output to FOD Grouping

FODx pair best with outputs that have nearby pins to VDD_FODx. Certain outputs and FODs can be grouped to reduce the amount of coupling between FOD rails and outputs. (see Figure 5). These types of optimizations can be found for both 144 BGA die and the 100 BGA die. The 144 BGA die is shown in Figure 5.

- **Out11** can be grouped with **FOD3/4**
- **Out12** can be grouped with **FOD2**
- **Out13** can be grouped with **FOD1/2**
- **Out14** can be grouped with **FOD1**
- **Out15** can be grouped with **FOD0**

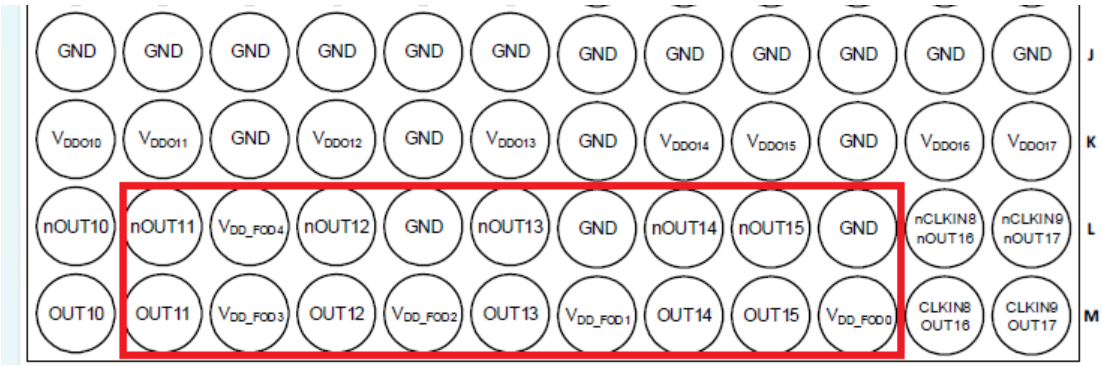


Figure 5. 144 BGA Die Showing OUTx and VDD_FODx Groupings

6. REF_CLK Coupling to Out16/nOUT16 (100 BGA die only)

For the 100 BGA packages (RC38412 and RC32412), there is coupling from the REF_CLK to Out16 (see Figure 6) due to the pad locations of REF_CLK relative to Out16. Therefore, unless output/REF_CLK is an integer relationship and in Synth mode, Out16 cannot have a sensitive clock output. The 144 BGA die does not have the same issue.

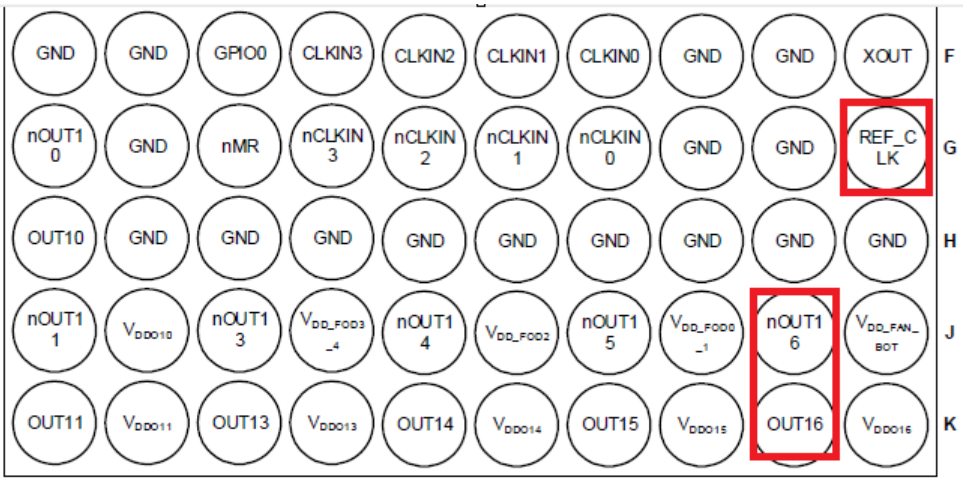


Figure 6. 100 BGA Die Pad Locations for REF_CLK and OUT16/nOUT16

7. Output-to-Output Coupling

The outputs of an FC4W (RC38616) 144 BGA package start at the top of the package and then increment serially in counterclockwise rotation as shown in Figure 7. The FC4 (RC32418) 144 BGA package has a similar package orientation. The location of the outputs gives an indication of where to place certain frequencies to avoid coupling of the fundamental frequency or even the harmonics of adjacent outputs.

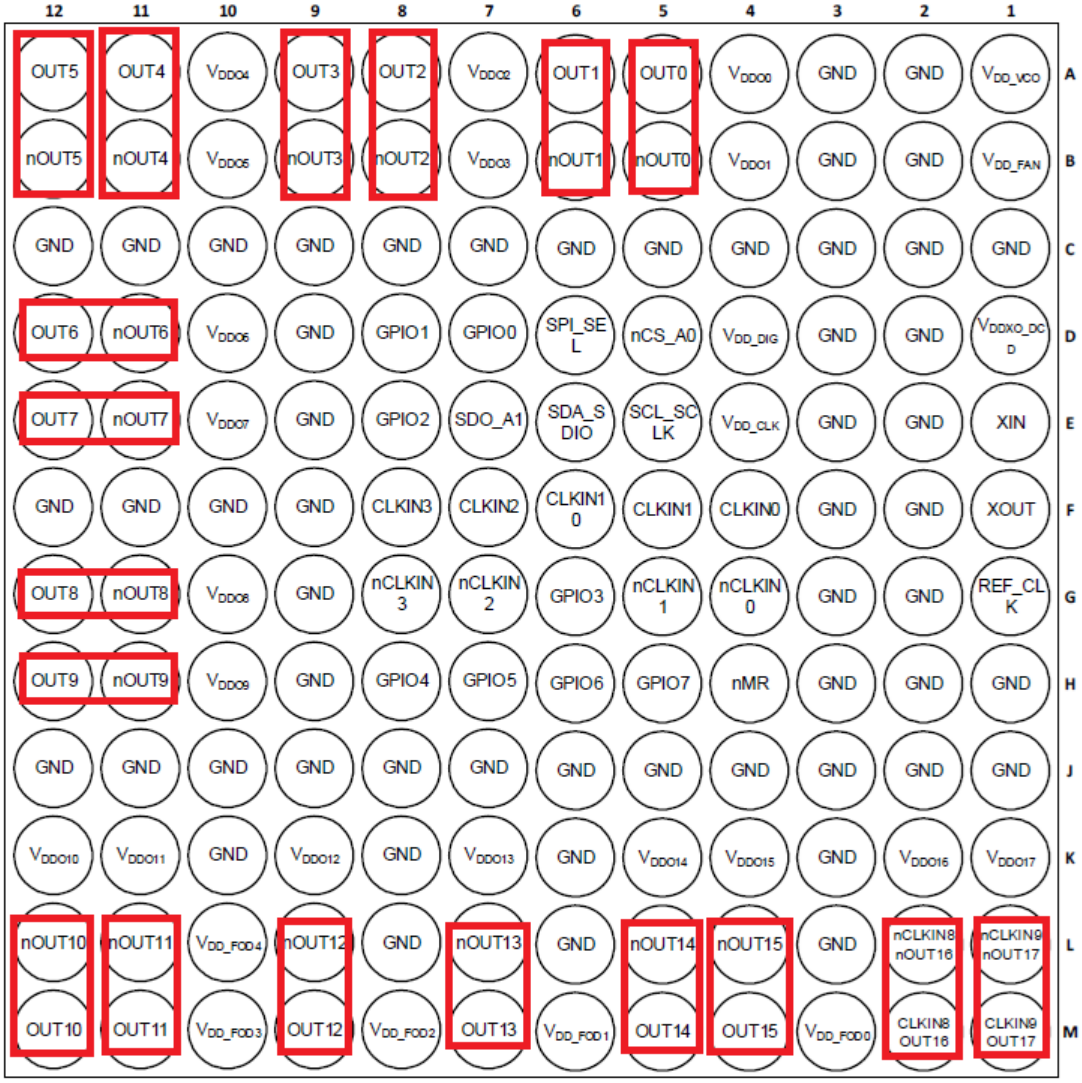


Figure 7. FC4W (RC38616) 144 BGA Die Pad Locations for the Outputs

The outputs of the FC4W (RC38412) 100 BGA package are shown in Figure 8. The outputs start at the top of the package and then increment serially in counterclockwise rotation. The FC4 (RC32412) 100 BGA package has a similar package orientation. Similarly to the 144 BGA, the location of the outputs gives an indication of where to place certain frequencies to avoid coupling of the fundamental frequency or even the harmonics of adjacent outputs.



Figure 8. FC4W (RC38412) 100 BGA Die Pad Locations for the Outputs

8. FC4 Synthesizer Configuration Example

Due to the similarities between FC4 and FC4W, only an FC4W example is shown below. The GUI configuration was created with the following details:

- XTAL = 62.5MHz
- 1x 25MHz HCSL
- 1x 156.25MHz HCSL
- 1x 312.5MHz HCSL

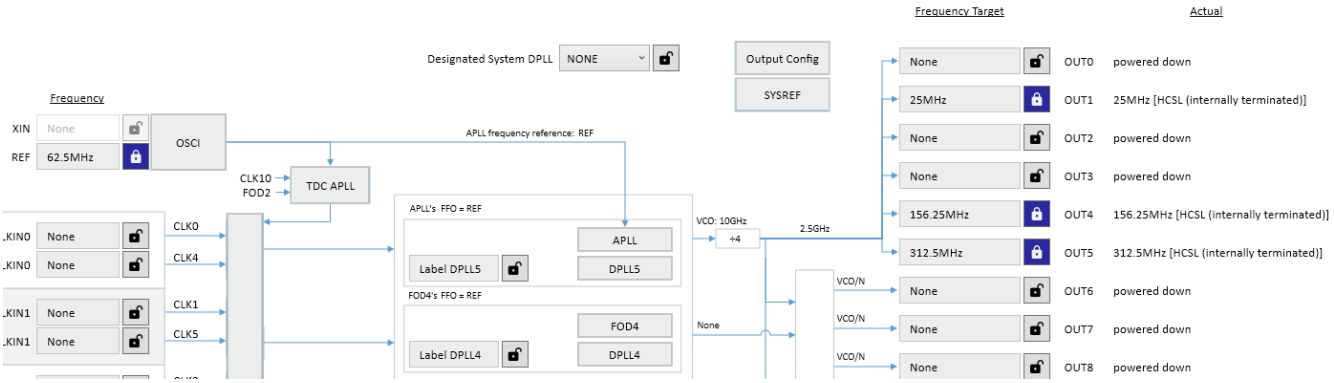


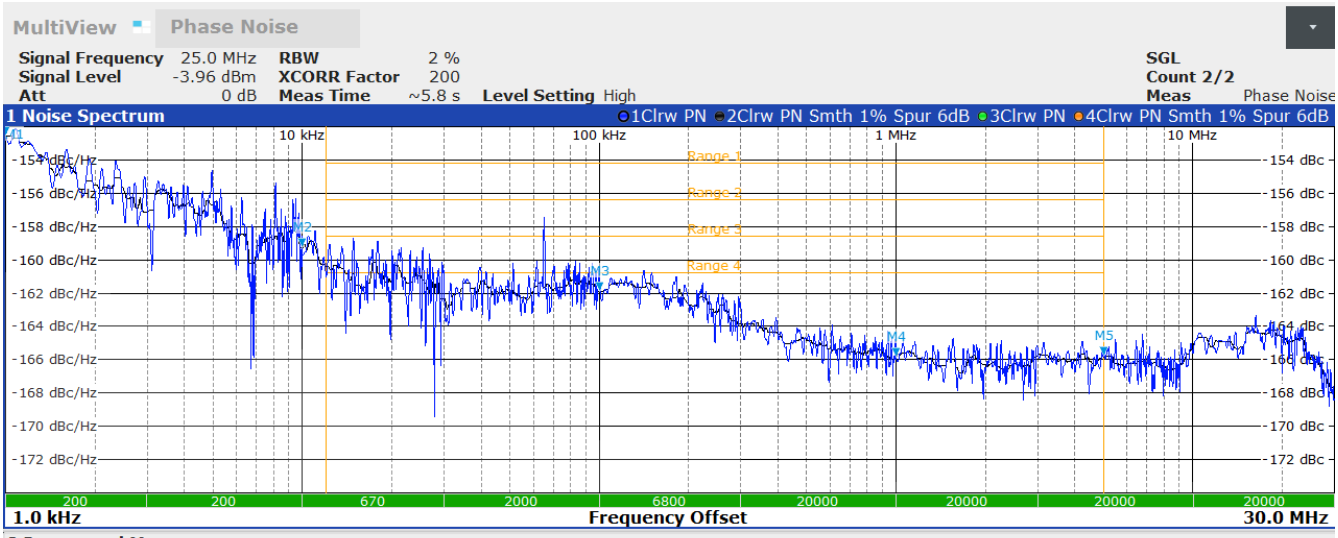
Figure 9. GUI Diagram of the FC4W Synthesizer Configuration Example

As shown in Figure 9, an APLL VCO frequency of 10GHz is chosen because it is a multiple of 62.5MHz. In Synthesizer mode, the best phase noise is achieved when the VCO frequency is a multiple of the XTAL frequency.

All the outputs are common factors of 10GHz and use a divide-by-4 followed by an IOD. If they were not common factors of 10GHz, the FODs would need to be used. FODs give higher jitter and can cause additional spurs. Outputs 6 to 17 go through an additional mux that Outputs 0 to 5 do not see, so higher jitter is expected.

There is potential crosstalk between the 25MHz with the 156.25MHz/312.5MHz. For example, 156.25MHz - 6 × 25MHz = 6.25MHz. This produces a 6.25MHz spur on the 156.25MHz and 312.5MHz outputs due to harmonic coupling. This crosstalk is unavoidable.

For the phase noise plots, see Figure 10 (25MHz output), Figure 11 (156.25MHz output), and Figure 12 (312.5MHz output).



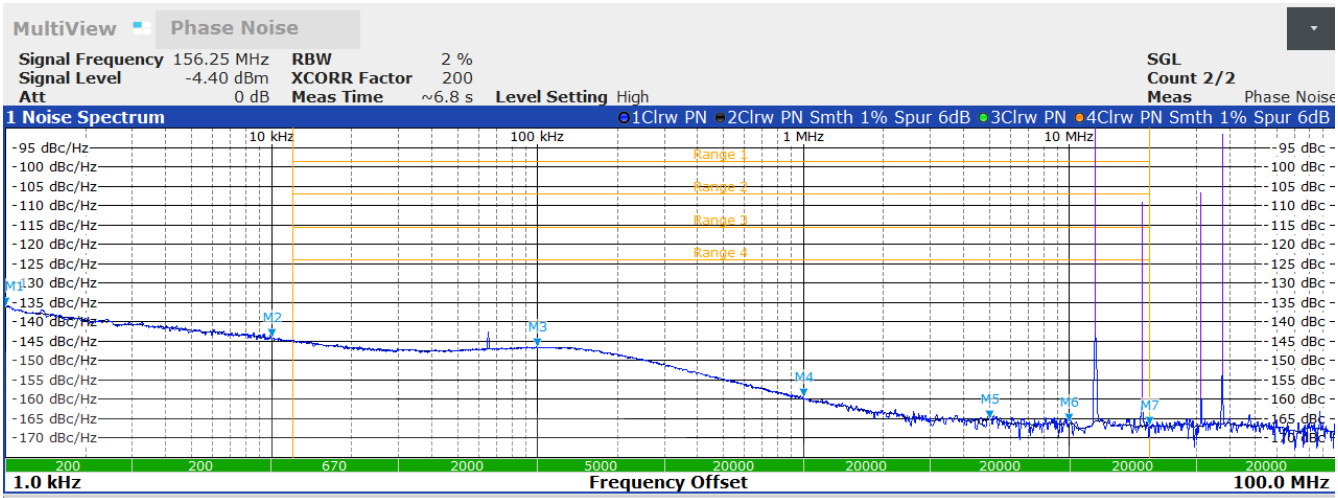
2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	5.000 MHz		-98.59 dBc	952.87 µ°/16.63 µrad	45.376 Hz	105.875 fs
2	2	12.000 kHz	5.000 MHz		-98.59 dBc	952.87 µ°/16.63 µrad	45.376 Hz	105.875 fs
3	3	12.000 kHz	5.000 MHz	4M HPF	-104.91 dBc	460.25 µ°/8.03 µrad	31.037 Hz	51.138 fs
4	4	12.000 kHz	5.000 MHz	4M HPF	-104.91 dBc	460.25 µ°/8.03 µrad	31.037 Hz	51.138 fs

3 Marker Table

Type	Ref	Trace	X-value	Y-value
M1		2	1.0 kHz	-152.57 dBc/Hz
M2		2	10.0 kHz	-159.29 dBc/Hz
M3		2	100.0 kHz	-161.9 dBc/Hz
M4		2	1.0 MHz	-165.85 dBc/Hz
M5		2	5.0 MHz	-165.78 dBc/Hz

Figure 10. Phase Noise Plot of 25MHz Output



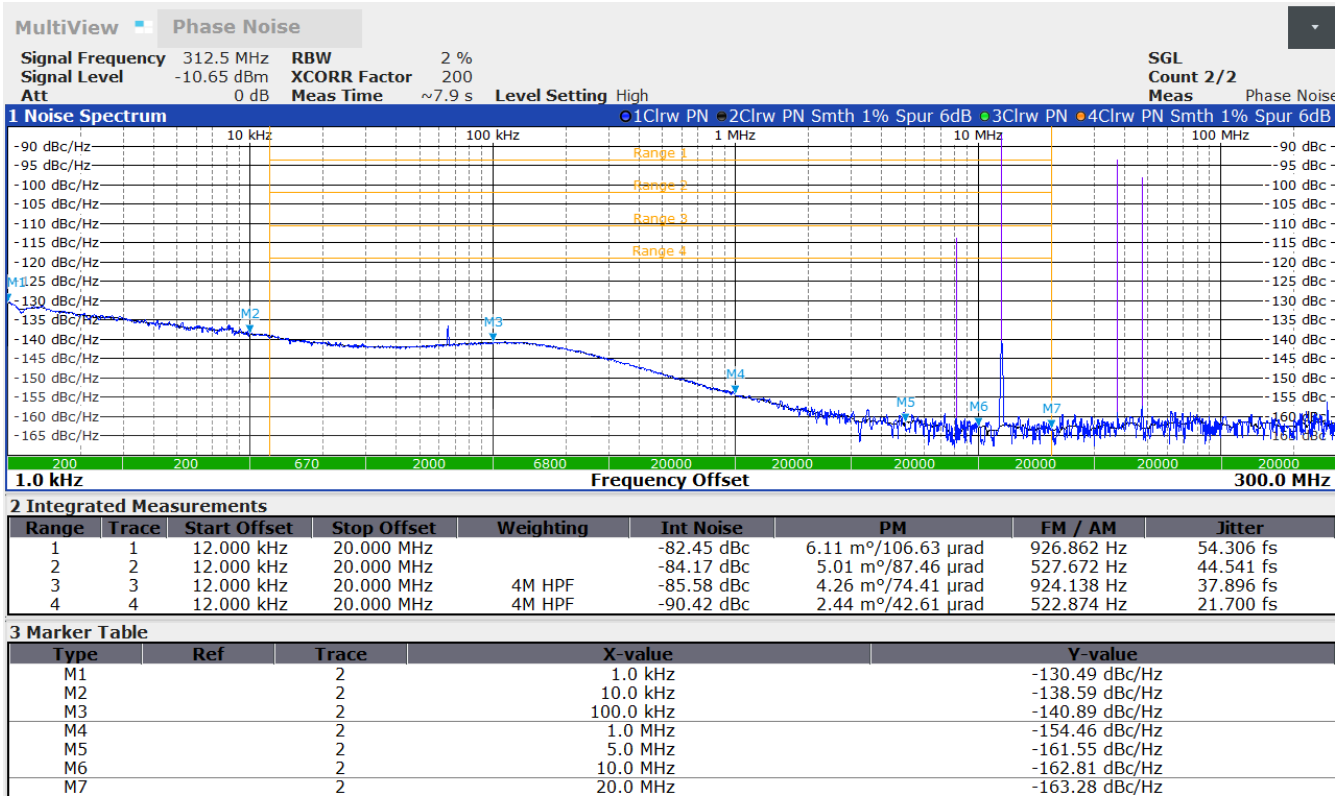
2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	20.000 MHz		-86.73 dBc	3.73 m°/65.16 µrad	650.702 Hz	66.374 fs
2	2	12.000 kHz	20.000 MHz		-89.34 dBc	2.77 m°/48.27 µrad	343.475 Hz	49.170 fs
3	3	12.000 kHz	20.000 MHz	4M HPF	-88.74 dBc	2.96 m°/51.73 µrad	649.384 Hz	52.693 fs
4	4	12.000 kHz	20.000 MHz	4M HPF	-94.20 dBc	1.58 m°/27.57 µrad	340.972 Hz	28.084 fs

3 Marker Table

Type	Ref	Trace	X-value	Y-value
M1		2	1.0 kHz	-136.06 dBc/Hz
M2		2	10.0 kHz	-144.37 dBc/Hz
M3		2	100.0 kHz	-146.65 dBc/Hz
M4		2	1.0 MHz	-159.74 dBc/Hz
M5		2	5.0 MHz	-165.17 dBc/Hz
M6		2	10.0 MHz	-166.13 dBc/Hz
M7		2	20.0 MHz	-167.01 dBc/Hz

Figure 11. Phase Noise Plot of 156.25MHz Output



2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	12.000 kHz	20.000 MHz		-82.45 dBc	6.11 m°/106.63 µrad	926.862 Hz	54.306 fs
2	2	12.000 kHz	20.000 MHz		-84.17 dBc	5.01 m°/87.46 µrad	527.672 Hz	44.541 fs
3	3	12.000 kHz	20.000 MHz	4M HPF	-85.58 dBc	4.26 m°/74.41 µrad	924.138 Hz	37.896 fs
4	4	12.000 kHz	20.000 MHz	4M HPF	-90.42 dBc	2.44 m°/42.61 µrad	522.874 Hz	21.700 fs

3 Marker Table

Type	Ref	Trace	X-value	Y-value
M1		2	1.0 kHz	-130.49 dBc/Hz
M2		2	10.0 kHz	-138.59 dBc/Hz
M3		2	100.0 kHz	-140.89 dBc/Hz
M4		2	1.0 MHz	-154.46 dBc/Hz
M5		2	5.0 MHz	-161.55 dBc/Hz
M6		2	10.0 MHz	-162.81 dBc/Hz
M7		2	20.0 MHz	-163.28 dBc/Hz

Figure 12. Phase Noise Plot of 312.5MHz Output

9. Revision History

Revision	Date	Description
1.00	Sep 25, 2026	Initial release

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