FemtoClock™3 Wireless O-RU (Open Radio Unit) Synchronization Clock Tree

Introduction

Open Radio Access Network (O-RAN) is a disruptive approach to the traditional RAN, enabling interoperability between different vendors and promoting software-defined implementations. The Open Radio Unit (O-RU) is a critical component of Open-RAN, responsible for handling radio transmission and reception. A fundamental requirement of O-RU design is precise time synchronization which is achieved through an optimized clock tree. This document explores the synchronization clock tree in O-RU design, discusses the implementation of synchronization protocols, and reviews open-source drivers compatible with Linux PTP (ptp4l) for time synchronization.

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1. Overview

Synchronization is a key requirement in RANs, ensuring seamless communication between base stations and users. In an O-RAN, synchronization is achieved over the fronthaul network using PTP and SyncE or by GNSS connected directly to the O-RU.

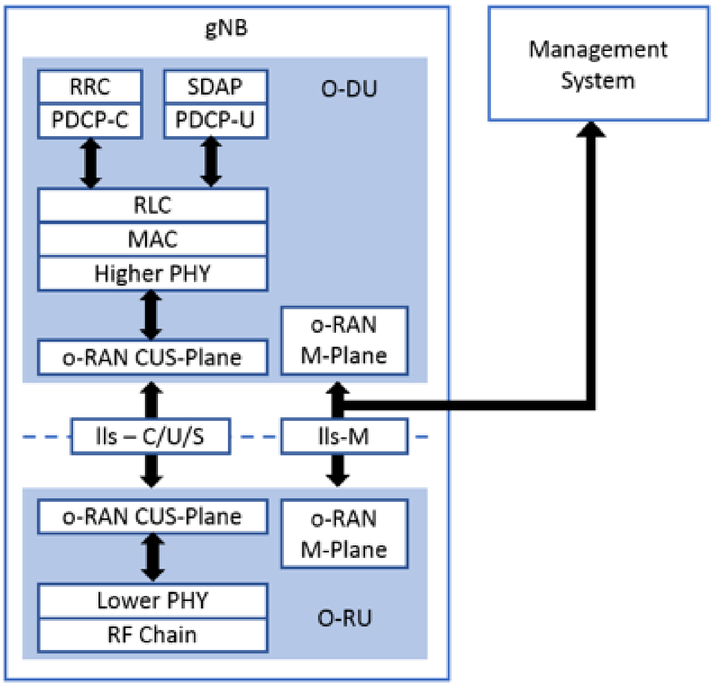

Figure 1. O-RAN Fronthaul Functional Split

(Figure from O-RAN.WG4.TS.MP.0)

In an O-RU, a well-structured clock tree distributes precise timing to different components of the radio unit. The primary sources of synchronization in an O-RU include:

- **Precision Time Protocol (PTP - IEEE 1588v2)**: Distributes time over Ethernet, a means to maintain time/phase synchronization.
- **Synchronous Ethernet (SyncE)**: Maintains frequency synchronization; also referred to as Physical Layer Frequency Support (PLFS).
- **Local Oscillators and Phase-Locked Loops (PLLs)**: Ensures stable phase/frequency reference and holdover.
- **Global Navigation Satellite System (GNSS)**: Provides absolute time reference.

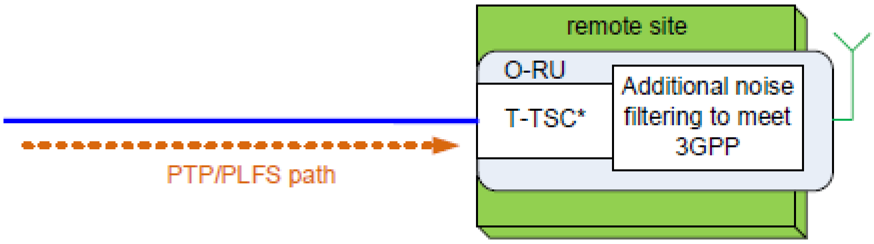

Figure 2. O-RAN S-Plane for O-RU

(Figure from O-RAN.WG4.CUS.0)

This document explores the clock tree requirements for an O-RU, how PLL silicon supports these requirements, and design considerations to meet O-RAN S-Plane specifications.

2. O-RU Synchronization

The O-RU synchronization clock tree is structured to ensure robust and accurate distribution of timing signals. The primary components include:

- **Primary Clock Source**: GNSS (for example, GPS, GLONASS) or IEEE 1588 PTP Grandmaster provides the initial timing reference. SyncE distributes the frequency reference if available.
- **Master Clock Unit (MCU)**: The MCU receives the primary clock input and generates a high-stability reference clock. A high-precision oven-controlled crystal oscillator (OCXO) or rubidium clock is used to maintain accuracy.
- **Clock Distribution Network**: Multiple PLLs and clock synthesizers distribute reference signals to different O-RU components. PLLs filter out jitter and ensure a stable reference clock.
- **Synchronization Interface**: The O-RU interfaces with IEEE 1588 PTP and SyncE to maintain phase and frequency synchronization. Hardware timestamping is used to achieve nanosecond-level accuracy.
- **Timing Recovery Mechanism**: The O-RU must recover timing from SyncE or PTP in the event of GNSS failure. Holdover performance is critical for maintaining synchronization during link failures.

2.1 Benefits of Phase-Locked Loops (PLLs)

Phase-Locked Loops (PLLs) play a crucial role in O-RU clock design by maintaining precise frequency and phase synchronization across the network. The benefits of PLLs in an O-RU synchronization clock tree include:

- **Jitter Reduction**: PLLs filter out both low-frequency (wander) and high-frequency (jitter) noise in the timing signal, ensuring a cleaner clock source. This is crucial for high-performance radio transmission where signal integrity is essential.
- **Frequency Multiplication and Division**: PLLs can generate higher or lower frequency signals derived from a reference clock. This allows O-RUs to generate different clock frequencies needed for various components such as baseband processing and radio transmission.
- **Holdover Stability**: In the event of a synchronization failure (for example, GNSS signal loss), PLLs provide stable timing using a high-quality oscillator, ensuring continued network operation even under degraded conditions.
- **Phase Synchronization**: PLLs ensure that the output clock remains phase-aligned with the reference clock, thus minimizing timing drift. This is particularly important in 5G networks where tight phase synchronization is required for time-division duplexing (TDD) operations.
- **Adaptive Filtering and Locking**: Modern PLLs incorporate adaptive filtering techniques to dynamically adjust to changing network conditions. This enhances the resilience of the O-RU against timing disturbances.
- **Integration with IEEE 1588 and SyncE**: PLLs work in conjunction with PTP and SyncE to align the local clock with the network's master clock. Hardware-assisted PLLs further improve timestamping accuracy in Linux PTP implementations.

By leveraging PLLs effectively, O-RUs can achieve a stable and precise clock signal, ensuring reliable communication and synchronization across Open-RAN networks.

2.2 AMD ZCU670 Solution

The AMD Zynq RFSoC DFE (XCZU67DR-2FSVE1156I) is an advanced FPGA-based platform optimized for 5G and Open-RAN applications. It provides robust hardware timestamping capabilities and, along with a high-accuracy PLL, ensures precise time synchronization in O-RUs.

Features of AMD RFSoC for synchronization:

- **Integrated IEEE 1588 PTP Timestamping**: Ensures nanosecond-level synchronization accuracy.
- **Programmable Logic with Dedicated Timing Blocks**: Enables real-time clock corrections and phase alignment.
- **Multiple Clock Inputs**: Supports GNSS, SyncE, and IEEE 1588 PTP timing sources.
- **High-Performance PLLs**: Provides wander and jitter filtering and frequency synthesis for stable clock distribution.
- **Hardware-Assisted PTP Processing**: Reduces CPU load by offloading timestamping to the FPGA.

3. Role of FemtoClock 3 Wireless in a Clock Tree Design

FC3W (FemtoClock 3 Wireless) is a critical component in the clock tree, enabling precise frequency synthesis, phase alignment, and noise filtering. It serves as the cornerstone for generating and distributing synchronized clock signals within the O-RU.

3.1 Core Functions of FemtoClock 3 Wireless

FC3W performs several core functions:

- **Frequency synthesis**: Converts the reference clock frequency to desired output frequencies with high accuracy. It supports fractional-N synthesis for non-integer frequency ratios, enhancing flexibility.
- **Jitter filtering**: Suppresses high-frequency noise from the reference signal, delivering a clean output and ensuring low phase noise to meet timing precision requirements.
- **Phase alignment**: Aligns the output clock phase with the reference signal, maintaining synchronization, and supports phase adjustment to compensate for delay variations in the distribution clock tree.
- **Dynamic reconfiguration**: Enables on-the-fly adjustment of output frequencies and phases, supporting adaptive systems that respond to changes in synchronization conditions.
- **Precise clock measurement in picosecond resolution**: Accurately monitors and calibrates the accuracy of clock signals.

3.2 Advantages of FemtoClock 3 Wireless in O-RUs

FC3W offers several advantages in O-RUs:

- Provides high precision with femtosecond jitter performance for ultra-precise timing
- Low power consumption makes it optimized for energy efficiency, which is essential for embedded systems
- Compact integration combines multiple PLLs on a single chip, reducing board space
- Flexibility supports a wide range of reference frequencies and output configurations

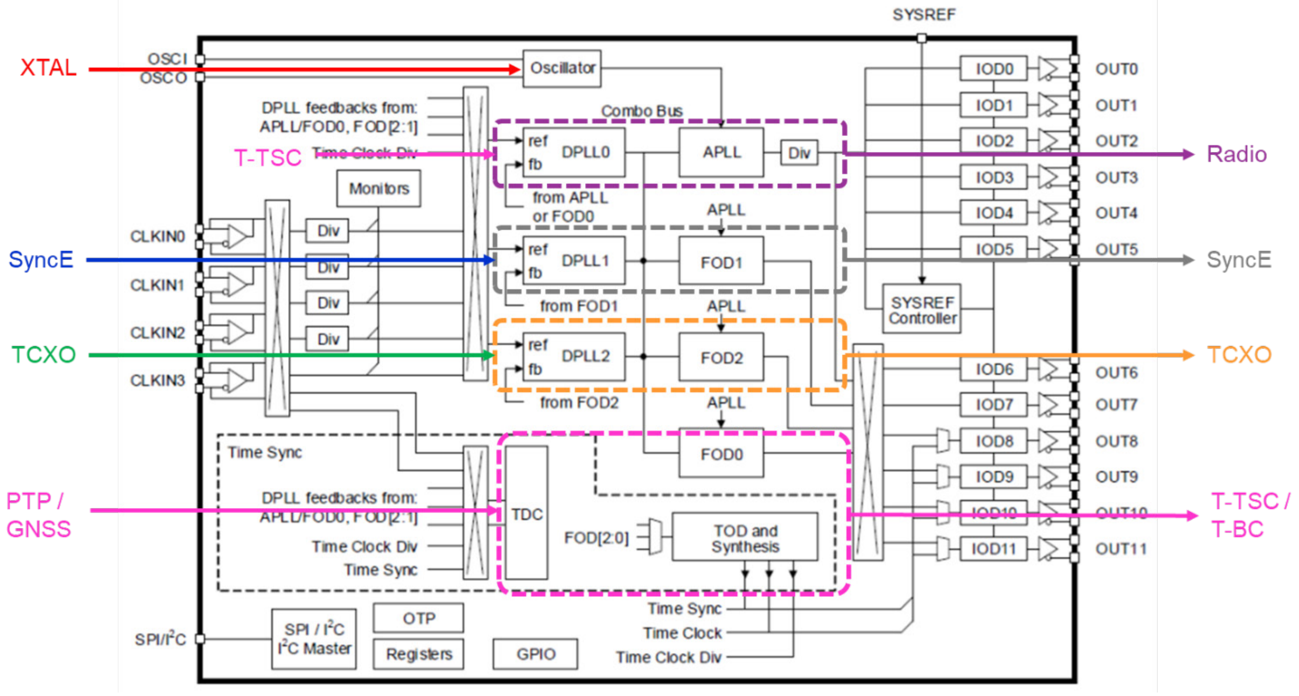

Figure 3. Radio Clock Synchronized by Fronthaul

FC3W supports multiple clock input and output options for clocking and adheres to many synchronization standards and recommendations. Available Linux-based drivers based on the PTP Hardware Clock (PHC) subsystem allow for quick integration of software on the host, supporting open-source software such as Linux PTP (ptp4l).

4. Clock Tree Design using FemtoClock 3 Wireless

An O-RU requires synchronization to either a network time clock or a GNSS reference, and the synthesis of multiple output frequencies, including 156.25 MHz for high-speed communication links and RF frequencies such as 122.88MHz. The system must achieve sub-nanosecond synchronization accuracy.

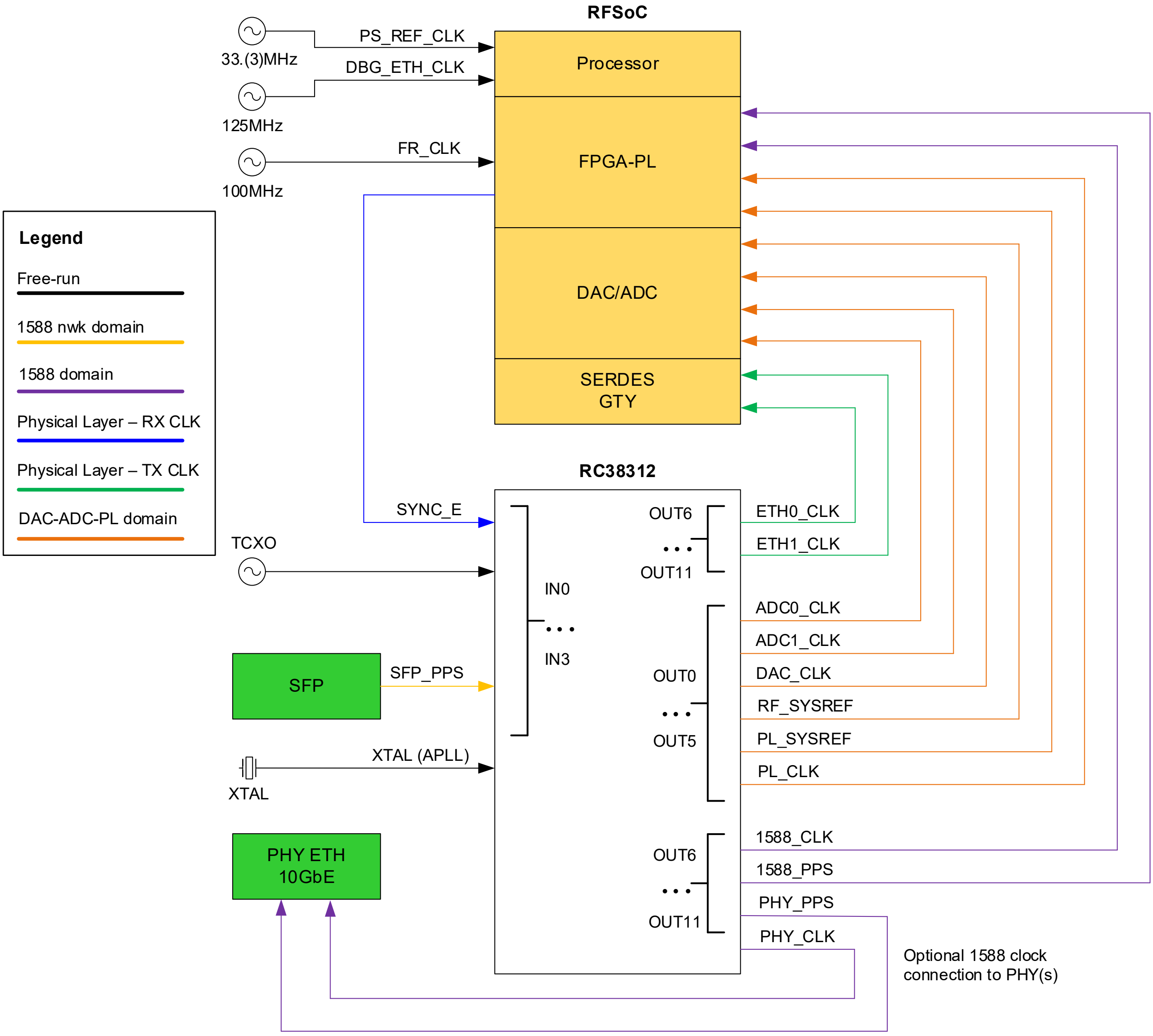

Figure 4. Example Clock Tree for Fronthaul Synchronization to O-RU

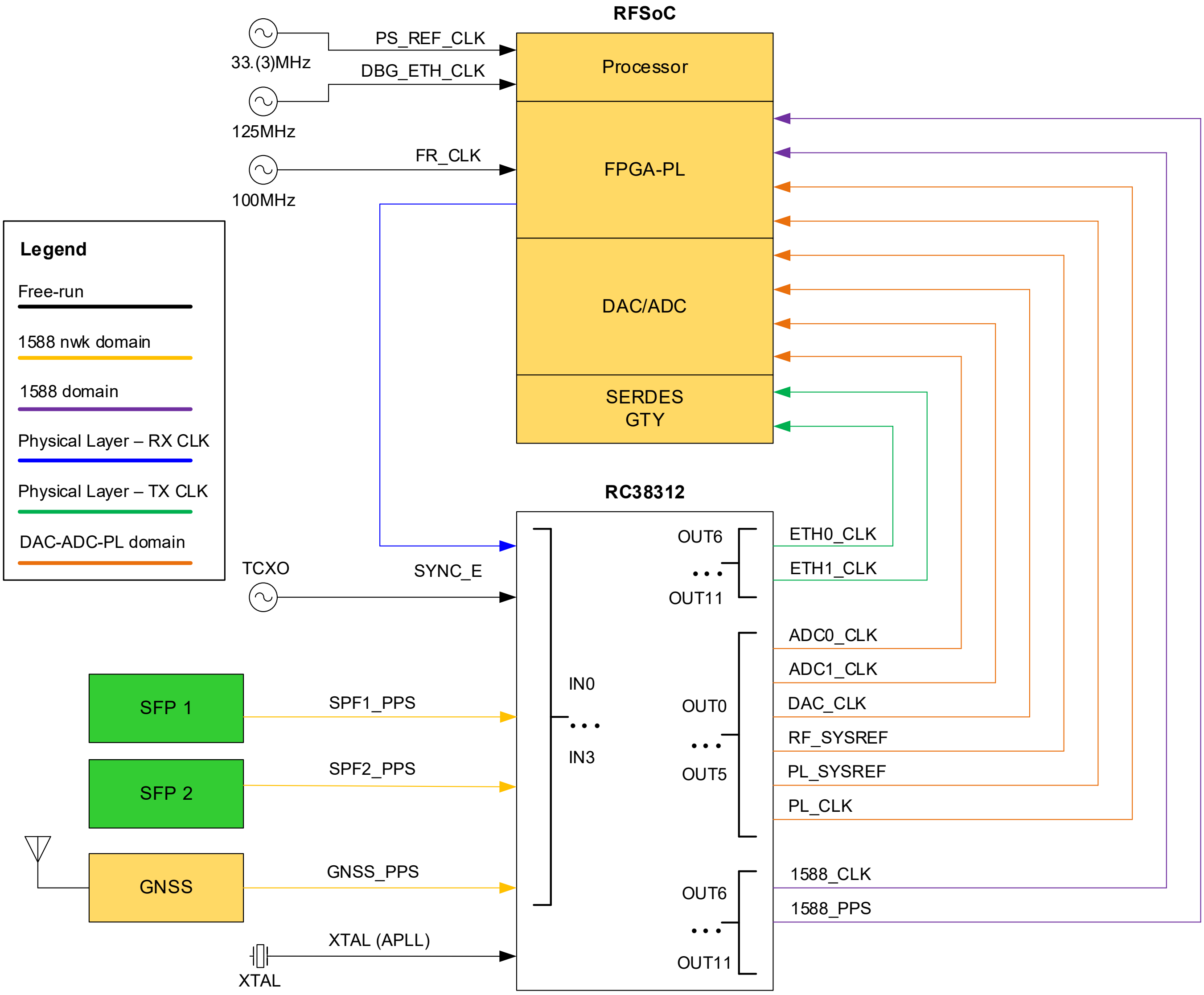

Figure 5. Example Clock Tree for GNSS/1PPS to O-RU

To design a robust clock tree for an O-RU, the process begins with defining the following system requirements:

- Input reference signal characteristics, such as frequency, stability, and jitter, must be determined
- Output frequencies for all subsystems need to be identified
- Timing accuracy targets for jitter, phase noise, and synchronization precision should be established, along with redundancy plans for backup reference sources and failover mechanisms

This includes multi-output capability for simultaneous generation of multiple frequencies, low jitter performance for clean and stable clock signals, a wide frequency range to cover the desired input and output frequencies, and dynamic reconfiguration for real-time adjustments to maintain synchronization.

Designing the clock distribution network involves:

- Using low-skew buffers and fanout devices to distribute clock signals without introducing significant delay or noise
- Minimizing trace lengths and using controlled impedance routing helps reduce signal degradation, and termination resistors are included to match impedance and prevent signal reflections.
- Implementing monitoring and feedback mechanisms involves integrating phase detectors and drift correction units to monitor synchronization accuracy, along with feedback loops to dynamically adjust PLL parameters based on reference signal variations.

- Finally, validating and optimizing the design involves performing simulations to evaluate jitter, phase noise, and frequency stability under different conditions, conducting hardware testing to verify performance and compliance with O-RAN Alliance O-RU requirements, and optimizing power consumption and thermal performance.

5. Conclusion

Synchronization is a fundamental aspect of Open-RAN O-RU design, ensuring accurate timing for efficient network operation. The synchronization clock tree in O-RU consists of GNSS, PTP, SyncE, PLLs, and oscillators to maintain stable and precise timing. Open-source drivers provide hardware timestamping support for Linux PTP (ptp4l). Implementing Linux PTP for synchronization in O-RU requires configuring ptp4l, phc2sys, and monitoring synchronization status. As Open-RAN continues to evolve, further advancements in synchronization technologies will enhance network performance and reliability.

6. Revision History

Revision	Date	Description
1.00	Apr 14, 2025	Initial release.

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