

FemtoClock3 (FC3) and FemtoClock3 Wireless (FC3W) EEPROM Programming

This document describes the connections for the EEPROM hardware, discusses instructions for programming the EEPROM with the FemtoClock™3 (FC3) and FemtoClock™3 Wireless (FC3W) devices, provides the GUI instructions on how to program the EEPROM, and provides a list of recommended EEPROM vendors.

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1. EEPROM Overview

The FC3 and FC3W product line is primarily designed to use internal resources for initialization and operation. However, there are scenarios whereby integrating an external I²C serial EEPROM is beneficial or required to access alternative configurations during device resets.

The FC3 and FC3W devices can load a configuration automatically from internal one-time programmable (OTP) memory. These configurations can be assigned (by a dash code number) differently for configuration(s) or tailored to specific customers. A dash code is defined as a factory programmed custom device. Alternatively, after reset, the I²C master interface can automatically load a configuration from an external EEPROM.

The device will poll the I²C bus for the EEPROM at power-up only if the OTP is configured to look for an EEPROM. The FC3 and FC3W devices then become the I²C bus master to perform this polling. This is optional (configured in OTP) and may require the bus to be temporarily isolated to allow the FC3 and FC3W devices to be a temporary bus master (controller), then switch the I²C bus over to slave (target) mode.

The load time varies based on the size, EEPROM speed, and number of configurations loading from the EEPROM. Both FC3 and FC3W support EEPROM I²C access speeds of 100kHz, 400kHz, and 1MHz, as well as a single configuration in the EEPROM. Where FC3 and FC3W differ is in the size of the EEPROM payload. The EEPROM payload size for FC3 is approximately 4kB, while for FC3W the EEPROM payload size is approximately 2kB. Since FC3 and FC3W require an OTP configuration to enable the EEPROM load and set the EEPROM slave (target) address, it cannot be assumed that device is at default before applying the EEPROM register sequence. This means that all registers need to be written as part of the EEPROM load, thus the payload size is constant for any EEPROM configuration. EEPROM start-up time can be calculated using [Equation 1](#). This equation includes a 10% margin. After the device boots from EEPROM, there is an additional calibration time of approximately 5ms before the device outputs start up.

$$\text{Start Up Time (sec)} = 1.1 * ((\text{Payload_in_Bytes}) * 74/6 + (\text{user_config_offset} + 1) * 290 + (\text{number_of_valid_configs})) * 74) / (\text{EEPROM_I2C_Speed_in_Hz}))$$

Equation 1: FC3 and FC3W EEPROM Start-Up Time Formula

As an example, suppose it is required to know how long after power cycle it will take for outputs to become active for a FC3W device, booting from EEPROM, with 1 configuration, and an EEPROM I²C speed of 400kHz. Since the device is an FC3W device, the EEPROM payload size will be 2kB. Since there is a single configuration, **user_config_offset** = 0. Plugging this information into [Equation 1](#) yields the following start up time.

$$\text{Start Up Time (sec)} = 1.1 * (((2000) * 74/6 + (0 + 1) * 290 + (1) * 74))/400000$$

$$\text{Start Up Time (sec)} = 0.06883 \text{ seconds}$$

$$\text{Start Up Time} = 68.83 \text{ ms}$$

It takes the device approximately 68.83ms to load the configuration from the EEPROM.

Note: There is a 5ms calibration time after the EEPROM contents are loaded to the device.

So, the time from power-up to outputs active will be approximately 68.83ms + 5ms = 73.83ms. [Figure 1](#) shows a scope capture for case described in the previous example. The measured time from power-up to output active is 73.397ms.

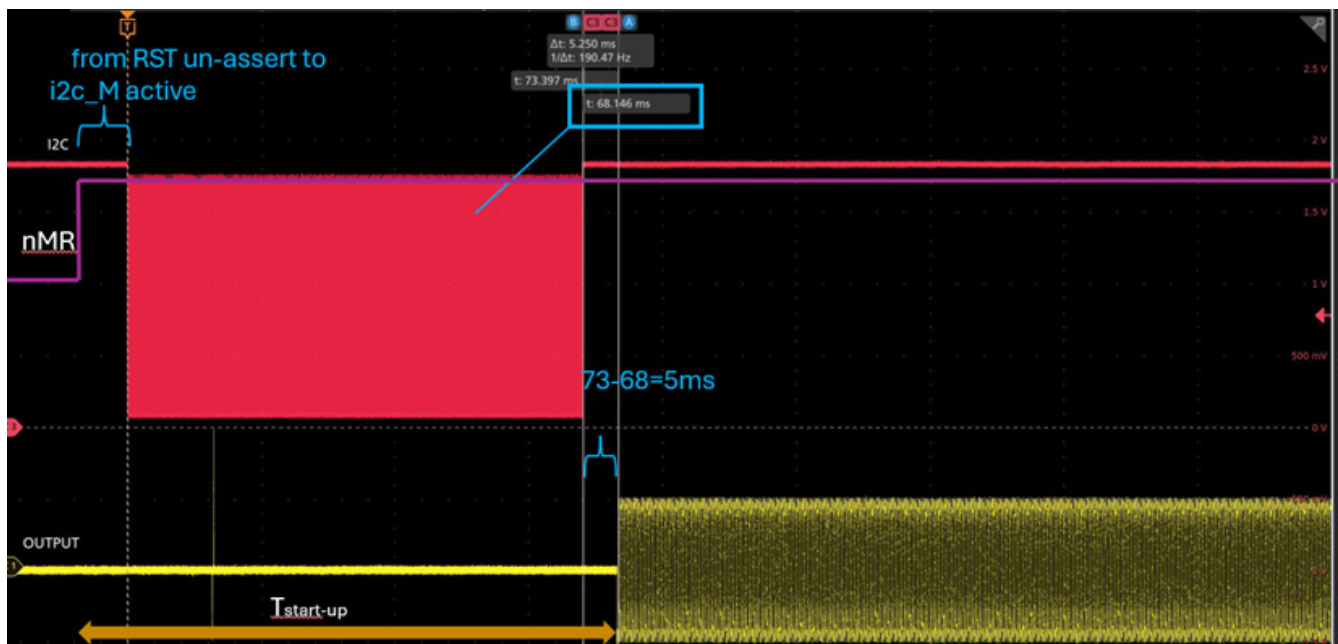


Figure 1. Scope Capture of Serial Data and Output After Power-Up

FC3 and FC3W devices have different status and event bits that enable checking of the OTP/EEPROM load status. Use “**TOP.GLOBAL.DEVICE_STS.eeprom_config_valid_sts**” to confirm if the loading is successful; however, there is no specific indicator for load failure.

For more information on saving or programming the EEPROM image using the evaluation board, see the [RC22308A/RC32308A Evaluation Board Manual](#) and [RICBox GUI Software for FemtoClock3 User Guide](#).

For information on the *FC3W EVK Manual*, contact the Renesas [Technical Support](#) team.

2. Hardware Setup

Figure 2 shows an example of an EEPROM schematic.

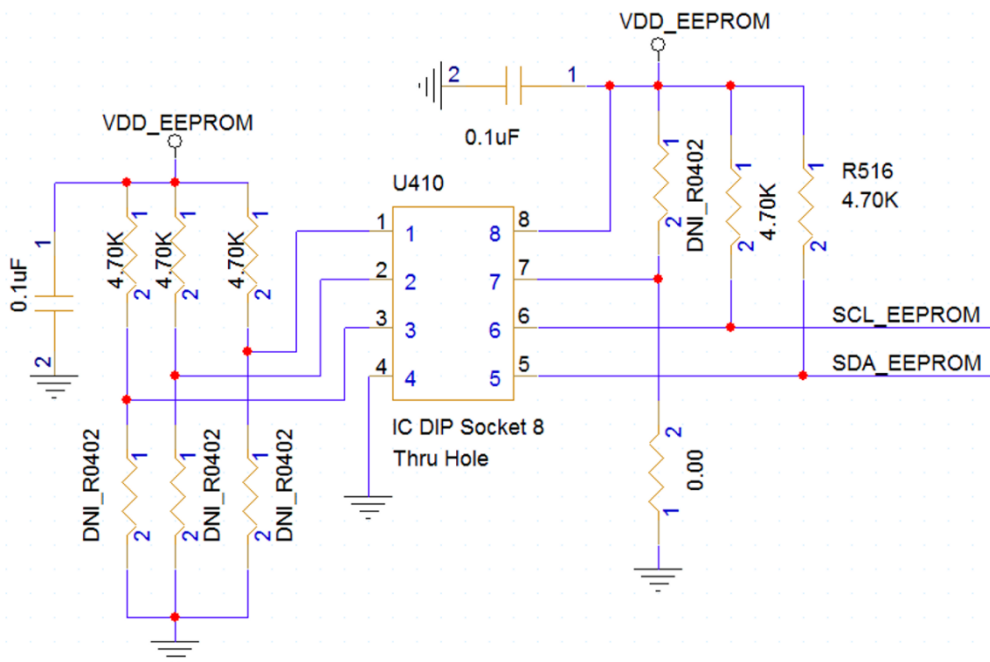


Figure 2. EEPROM Schematic Example

The EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or a write operation. The device address word consists of a 4-bit device code, 3-bit device address code, and 1-bit read/write (R/W) code. Figure 3 shows the device address word decode:

	Device address word (8-bit)							
	Device code (fixed)				Device address code			R/W code ^{*1}
64k	1	0	1	0	A2	A1	A0	R/W

Note: 1. R/W="1" is read and R/W = "0" is write.

Figure 3. R1EX24064ASAS0G Slave Address Word

R1EX24064ASAS0G address decode reference for Figure 3:

Device (U410) Slave Address: 1010A2A1A0 -> 1010111 -> 0x57

The symbol labeled as U410 in the Figure 2 schematic represents an EEPROM DIP socket footprint that is compatible with most 8-pin EEPROMs. Connect the SCL and SDA traces to the master I²C port of the FC3 device (SCK_SCK and SDA_SDIO).

The evaluation board (EVB) also supports an external EEPROM IC for loading of a device configuration programmed into the EEPROM as an option. To load the configurations from EEPROM, the EEPROM load enable bit must be set in device OTP. If the enable bit is not set, the EEPROM load will be skipped.

The EVB provides a socket of 8-lead DIP8 SOIC-8 socket (see Figure 4) so other EEPROM devices of different memory size can be tested.



Figure 4. EEPROM in Socket

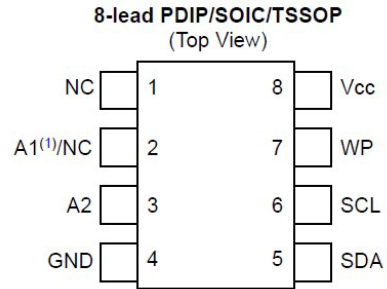


Figure 5. EEPROM Pin Description

2.1 FC3 Evaluation Board

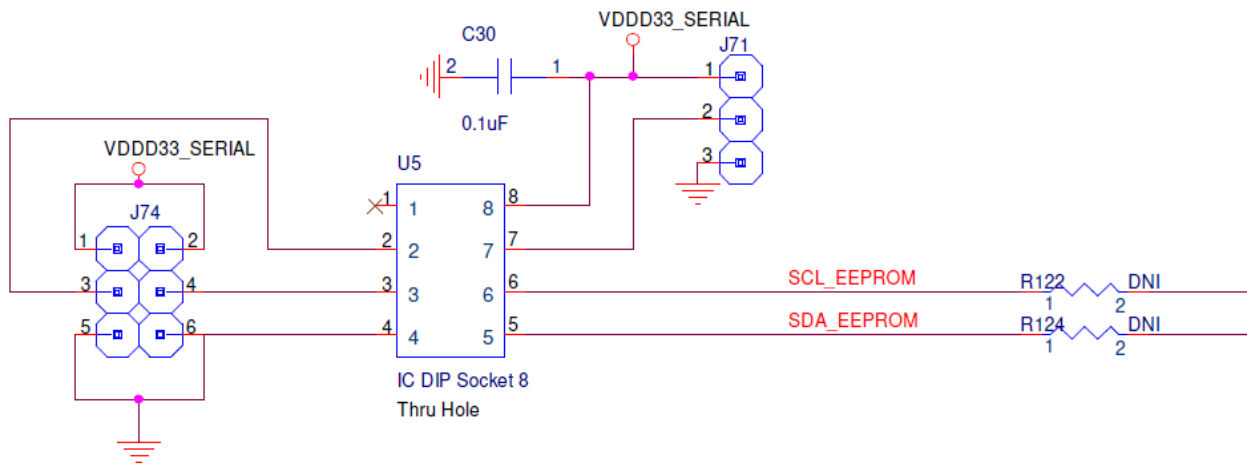


Figure 6. EEPROM Schematic

The A1 and A2 pins are the EEPROM address inputs that can be pulled either high or low using jumpers at J74 to define the device address. By default, jumpers can be removed so that A1 and A2 are left floating as they are internally pulled down to GND in most EEPROM devices.

The WP pin is the write-protect input. When the WP pin is pulled down to GND (Low), the EEPROM can have normal write operations. When it is pulled up directly to V_{CC} (High), all write operations are inhibited. The WP pin can be controlled with a jumper at J71.

To establish a connection to the EEPROM, the SDA and SCL traces must be connected to the FTDI communication path. Populate R122 and R124 with 0 Ohms to make the connection. This allows software features like RICBox to communicate with the EEPROM device.

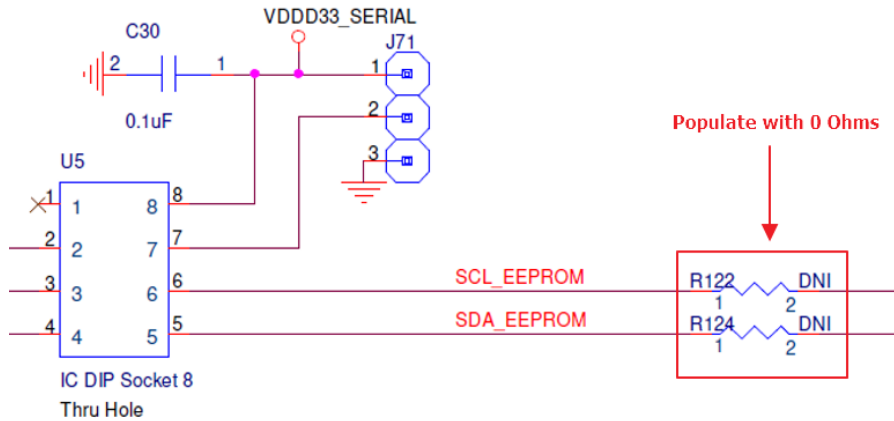


Figure 7. EEPROM Connection Resistors

When the device attempts to load an EEPROM configuration during start-up, the FTDI I²C controller can cause interference. The FTDI device can be removed from the I²C trace path by removing jumpers J61 and J62. This will also disconnect RICBox from communicating with the RC22312A/RC32312A device.

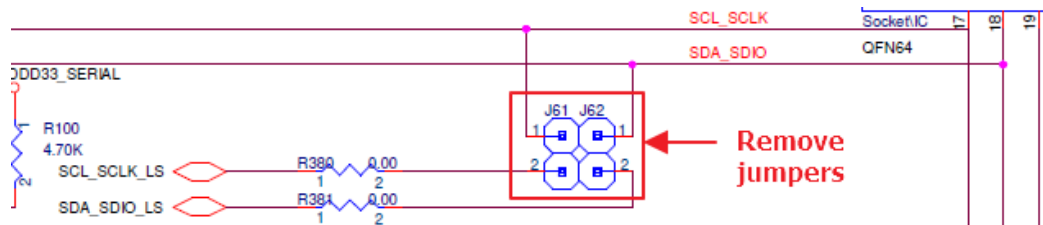


Figure 8. FTDI to I²C Communication Jumpers

2.2 FC3W Evaluation Board

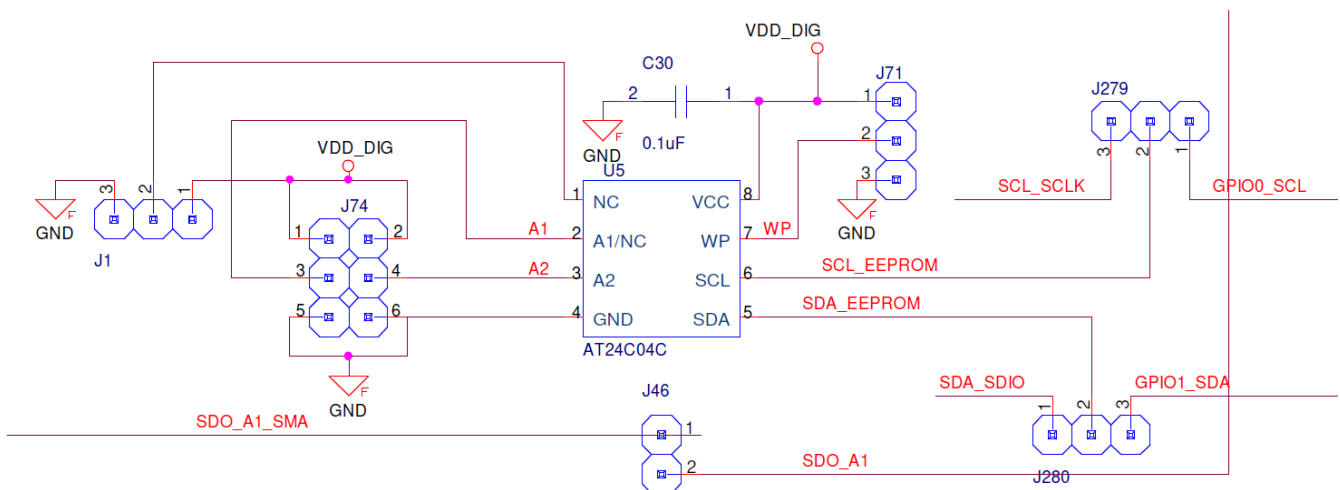


Figure 9. EEPROM Schematic

The A0 (Pin 1), A1 (Pin2) and A2 (Pin 3) are the EEPROM address inputs that can be pulled either high or low using jumpers at J74 and J1 to define the device address. By default, jumpers can be removed so that A0, A1 and A2 are left floating as they are internally pulled down to GND in most EEPROM devices.

The WP pin is the write-protect input. When the WP pin is pulled down to GND (Low), the EEPROM can have normal write operations. When it is pulled up directly to V_{CC} (High), all write operations are inhibited. The WP pin can be controlled with a jumper at J71.

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To establish a connection to the EEPROM, the SDA and SCL traces must be connected to the RC38312 SCL_SCLK/SDA_SDIO or GPIO0 and GPIO1 pins communication path through setting J279 and J280 as shown in Figure 10.

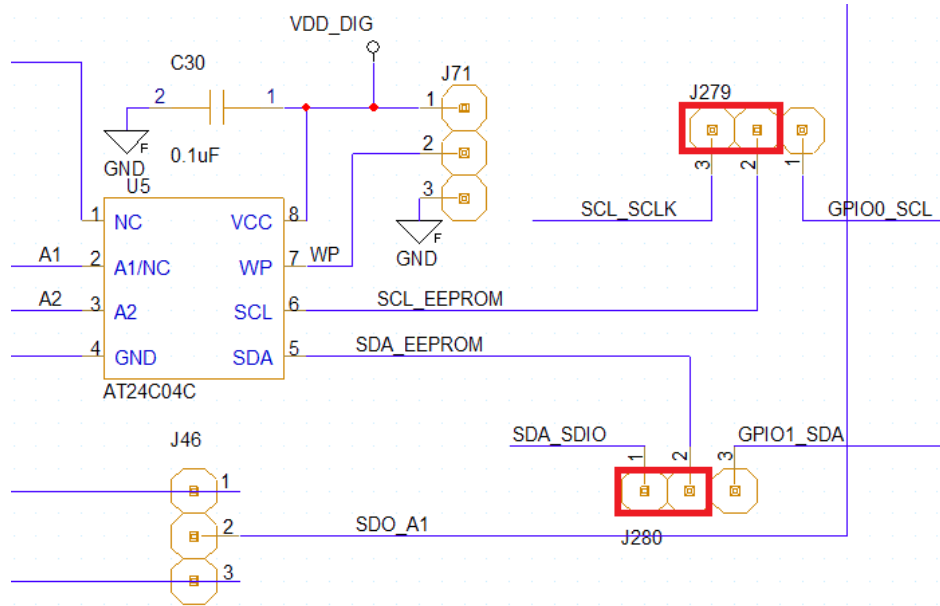


Figure 10. EEPROM Connection Jumpers for RC38312A SCL_SCLK and SDA_SDIO

For the EEPROM connected to the RC38312, the GPIO0 and GPIO1 pins communication path is established through setting J279 and J280 as shown in Figure 11. Install 0 Ohm on R567 and R568. Remove R562 and R563.

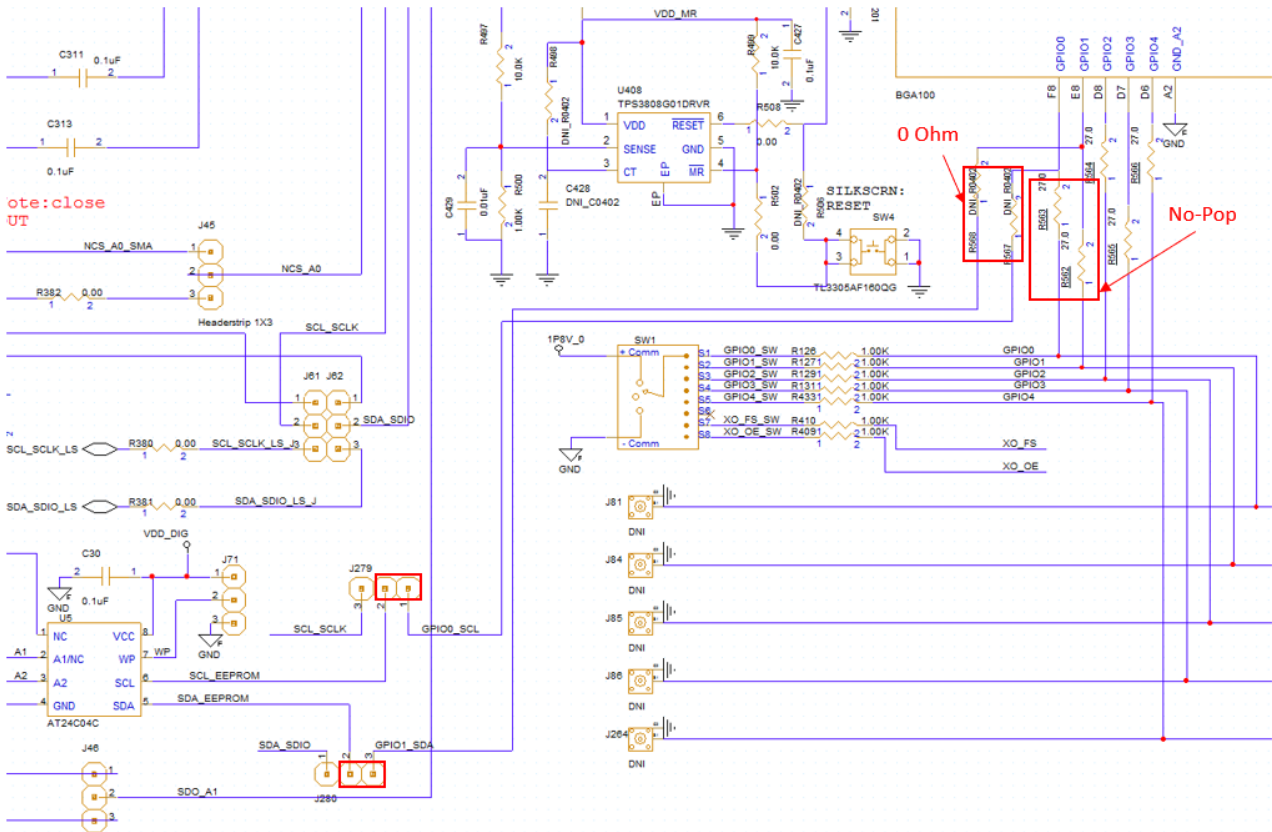


Figure 11. EEPROM Connection Jumpers for RC38312A GPIO

3. EEPROM Addressing

3.1 FC3 EEPROM Address Selection vs Dash Code

Each EEPROM configuration in the addendum that uses EEPROM loading has a dedicated EEPROM address. To select the EEPROM address accordingly, select the configuration by selecting GPIO0 and GPIO1 and the EEPROMs pins 1–3 (A0, A1, and A2).

Table 1 shows the available dash code versus the EEPROM address selection. The options for pull-up or pull-down of A0, A1, and A2 facilitate the configuration of the EEPROM address.

Table 1. FC3 Dash Code vs EEPROM Address Selection

Device	Dash Code	Configuration	GPIO for Configuration Selection	EEPROM Address	EEPROM Part Number
RCx2308A001	001	Config 0	00	0x51	R1EX24064ASA/ CAT24M01/ BR24G1M-3A
		Config 1	01	0x52	
		Config 2	10	0x53	
		Config 3	11	0x57	
RC32308A001	001	Config 0	00	0x51	
		Config 1	01	0x52	
		Config 2	10	0x53	
		Config 3	11	0x57	
RC22312A002	002	Config 2	10	0x50	
		Config 3	11	0x50	
RC32312A001	001	Config 2	00	0x50	
		Config 3	11	0x50	
RC32312A002	002	Config 0	00	0x51	
		Config 1	01	0x52	
		Config 2	10	0x53	
		Config 3	11	0x57	
RC22312A003	003	Config 2	10	0x50	
		Config 3	11	0x50	
RC32312A004	004	Config 1	10	0x50	
		Config 3	11	0x50	

3.2 FC3W EEPROM Address Selection and OTP Configuration Sequence

The EEPROM can be programmed using one of two methods, depending on the One-Time Programmable (OTP) configuration.

- Using the SCL_SCLK and SDA_SDIO pins of FC3W to load the EEPROM.
- Using GPIO0 (SCL) and GPIO1 (SDA) to load the EEPROM.

The method used is defined in OTP memory. Due to GPIO limitations, EEPROM operation is restricted to 1.8V signaling. A static EEPROM address can be defined, or GPIO2–GPIO4 can be used to dynamically select address bits (A0–A2). The selection between a static address and GPIO-based addressing is configured in OTP memory.

Note: If a dash code is using GPIO0 and GPIO1 for configuration selection and as the EEPROM load pins, configuration slot 3 or a single configuration must be used. This is because GPIO0 and GPIO1 require pull ups to function as I²C serial lines.

Table 2 shows the EEPROM address selection based on the state of GPIO2-4. The options for pull-up or pull-down of A0, A1, and A2 facilitate the configuration of the EEPROM address.

Table 2. FC3W EEPROM Address Selection

EEPROM Address	GPIO4 (A2)	GPIO3 (A1)	GPIO2 (A0)
0x50	0	0	0
0x51	0	0	1
0x52	0	1	0
0x53	0	1	1
0x54	1	0	0
0x55	1	0	1
0x56	1	1	0
0x57	1	1	1

Table 3 shows the configuration order for FC3W dash codes. A dash code containing a single config does not use GPIOs for config select as it always loads the same configuration.

Table 3. FC3W OTP Configuration Order

Configuration	GPIO1	GPIO0
Config0	0	0
Config1	0	1
Config2	1	0
Config3	1	1
Single Config	x	x

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Table 4 shows the available FC3W dash codes that support EEPROM loading.

Table 4. FC3W EEPROM Loading Dash Codes

Device	Dash Code	Configuration	EEPROM Load Pins	EEPROM Address	EEPROM Part Number
RC38108A100	-100	Config 3	GPIO0, GPIO1	0x50	R1EX24064ASA/ 24LC64
RC38108A104	-104	Single Config	SCL_SCLK, SDA_SDIO	0x50	R1EX24064ASA/ 24LC64
RC38108A200	-200	Config 3	GPIO0, GPIO1	0x50	R1EX24064ASA/ 24LC64
RC38108A204	-204	Single Config	SCL_SCLK, SDA_SDIO	0x50	R1EX24064ASA/ 24LC64
RC38208A100	-100	Config 3	GPIO0, GPIO1	0x50	R1EX24064ASA/ 24LC64
RC38208A104	-104	Single Config	SCL_SCLK, SDA_SDIO	0x50	R1EX24064ASA/ 24LC64
RC38208A200	-200	Config 3	GPIO0, GPIO1	0x50	R1EX24064ASA/ 24LC64
RC38208A204	-204	Single Config	SCL_SCLK, SDA_SDIO	0x50	R1EX24064ASA/ 24LC64
RC38112A100	-100	Config 3	GPIO0, GPIO1	GPIO2-4	R1EX24064ASA/ 24LC64
RC38112A104	-104	Single Config	SCL_SCLK, SDA_SDIO	GPIO2-4	R1EX24064ASA/ 24LC64
RC38112A200	-200	Config 3	GPIO0, GPIO1	GPIO2-4	R1EX24064ASA/ 24LC64
RC38112A204	-204	Single Config	SCL_SCLK, SDA_SDIO	GPIO2-4	R1EX24064ASA/ 24LC64
RC38312A100	-100	Config 3	GPIO0, GPIO1	GPIO2-4	R1EX24064ASA/ 24LC64
RC38312A104	-104	Single Config	SCL_SCLK, SDA_SDIO	GPIO2-4	R1EX24064ASA/ 24LC64
RC38312A200	-200	Config 3	GPIO0, GPIO1	GPIO2-4	R1EX24064ASA/ 24LC64
RC38312A204	-204	Single Config	SCL_SCLK, SDA_SDIO	GPIO2-4	R1EX24064ASA/ 24LC64

4. Saving/Programming EEPROM Images Using the GUI

1. Establish a connection to a device with the EEPROM attached.



Figure 12. Device Connection

2. Go to the OTP/EEPROM section of the block diagram.
3. Use the **Configuration Type** dropdown menu to select **SingleConfig** (see Figure 13).
4. Populate the **SingleConfig** drop-down menu with the configuration name that is being programmed to the EEPROM.
5. Click the **Program** button in the lower corner of the page.

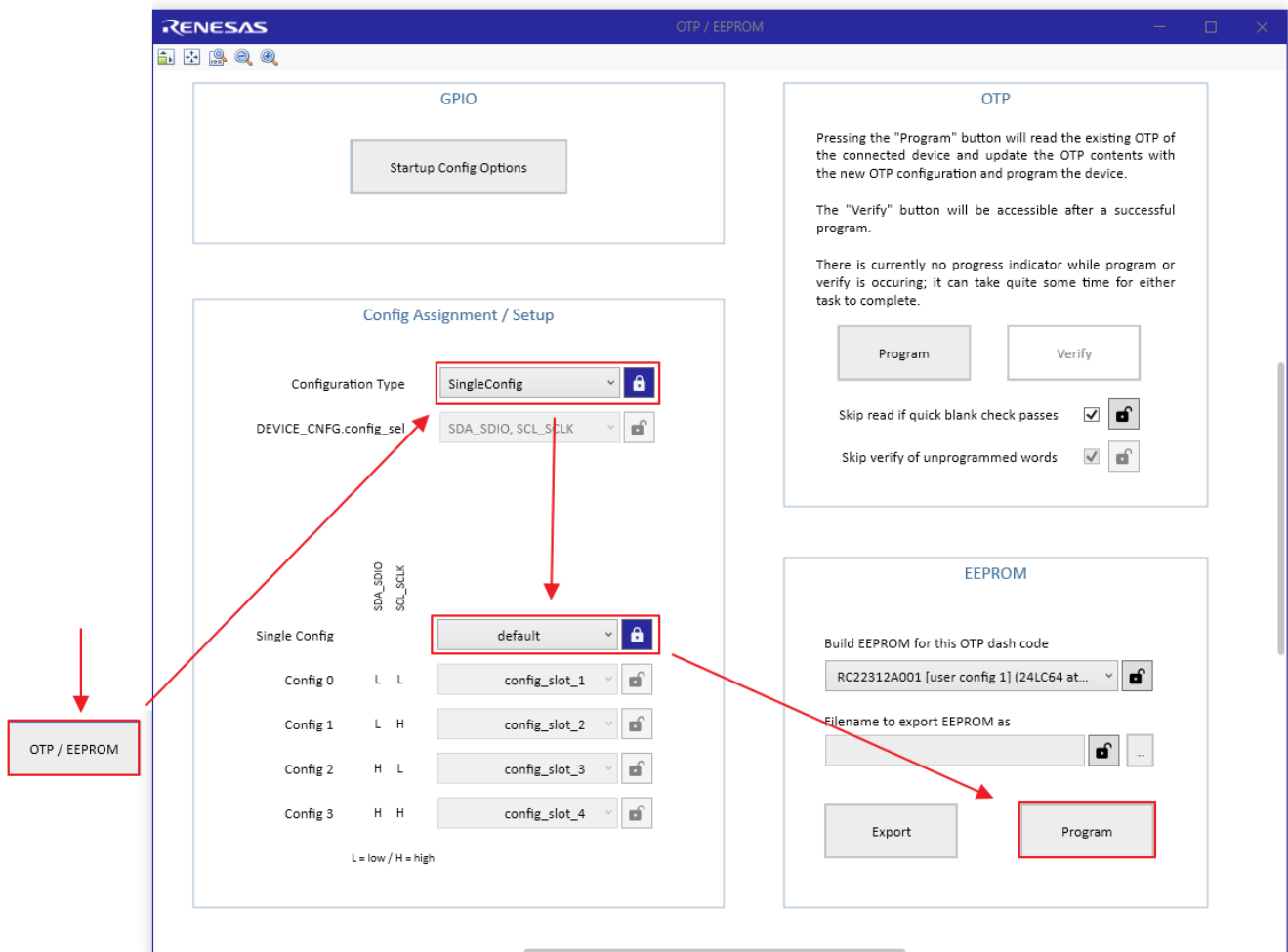


Figure 13. Programming a Connected EEPROM Device

Note: The *Adding Configurations to a Settings File* section in the document [RICBox GUI Software for FemtoClock3-Wireless User Guide](#) highlights configuration naming. Section 13 of the [RICBox Software Manual](#) discusses multiple configuration support.

Note: FemtoClock3 software only supports programming one configuration into EEPROM at a time.

6. Choose the **Save** location by clicking the button next to the EEPROM filename entry box.
7. Click the **Export** button to save the EEPROM image to the specified location.

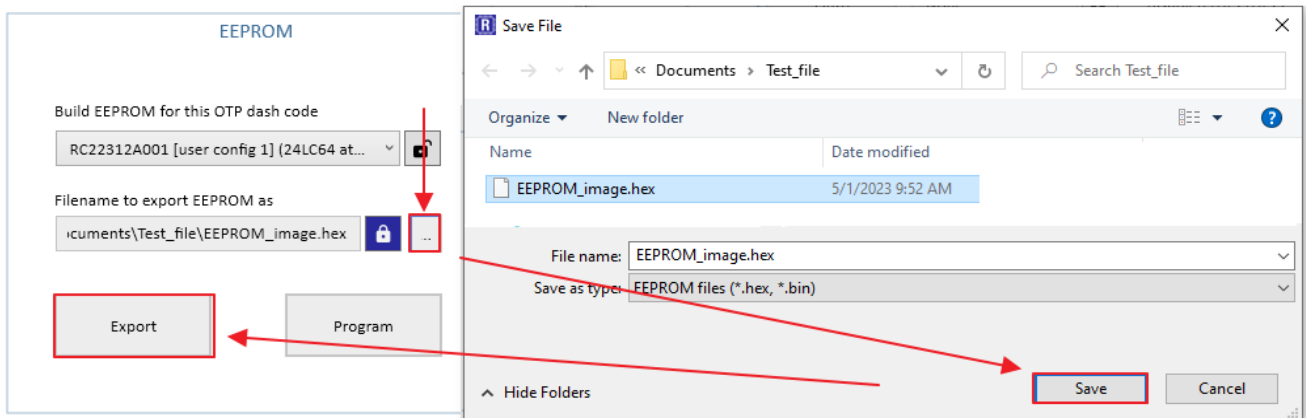


Figure 14. Saving EEPROM Image

Note: Ensure to specify the file extension as “.bin” or “.hex” when naming the file.

5. EEPROM Vendor Recommendations

Table 5 shows recommended EEPROM vendors and part numbers according to industry standards. This table highlights parts that have proven compatibility with the FC3 family of devices and is not a complete list of recommended vendors.

Table 5. Vendor Part Number Package Comments

Vendor Part Number	Vendor Name	Package Information	Comments
R1EX24064ASAS0I#S0	Renesas	SOP (8)	Datasheet
R1EX24064ATAS0I#S0	Renesas	TSSOP (8)	Datasheet
CAT24M01	On Semiconductor	-	A0 is not connected
BR24G1M-3A	Rohm	-	A0 is "don't use"

6. Revision History

Revision	Date	Description
1.05	May 22, 2026	Updated section 3.2.
1.04	May 7, 2025	Updated section 1.
1.03	Dec 16, 2024	<ul style="list-style-type: none"> ▪ Updated sections 2 and 3. ▪ Added new section 4.
1.02	Aug 19, 2024	<ul style="list-style-type: none"> ▪ Added sections 3.1 and 3.2. ▪ Completed other minor changes throughout.
1.01	May 20, 2024	Updated Table 2.
1.00	Nov. 28, 2024	Initial release.

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