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Renesas Electronics Corporation

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H8SX Family

External-Write-Data Buffer

Introduction

The external-write-data buffer is employed to execute external writing and internal access in parallel.

Target Device

H8SX/1653

Contents

1. Specification

- The external-write-data buffer is employed to execute external writing and internal access in parallel.
- One longword of data is consecutively written to external memory (SRAM) and internal RAM.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 16 MHz System clock (Iϕ): 32 MHz Peripheral module clock (Pϕ): 16 MHz External bus clock (Bϕ): 16 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)

3. Description of Functions Used

3.1 External Memory

SRAM is connected in area 3.

3.2 External-Write-Data Buffer

An H8SX/1653 microcontroller is equipped with a write-data buffer for the external data bus. Employing this external-write-data buffer in external writing and single-address transfer by the DMAC allow parallel execution of internal access. Setting the WDBE bit in BCR1 to 1 brings the external-write-data buffer into operation.

4. Principles of Operation

4.1 Timing when the External-Write-Data Buffer is Not in Use

Figure 1 shows an example of the timing when the external-write-data buffer function is not in use. When the WDBE bit in BCR1 is set to 0, the buffer is not in use. In this case, even if a cycle of external access or a single-address transfer by the DMAC is followed by internal access, internal access (reading or writing of internal registers or memory) will only be executed after the end of the external access or single-address transfer.

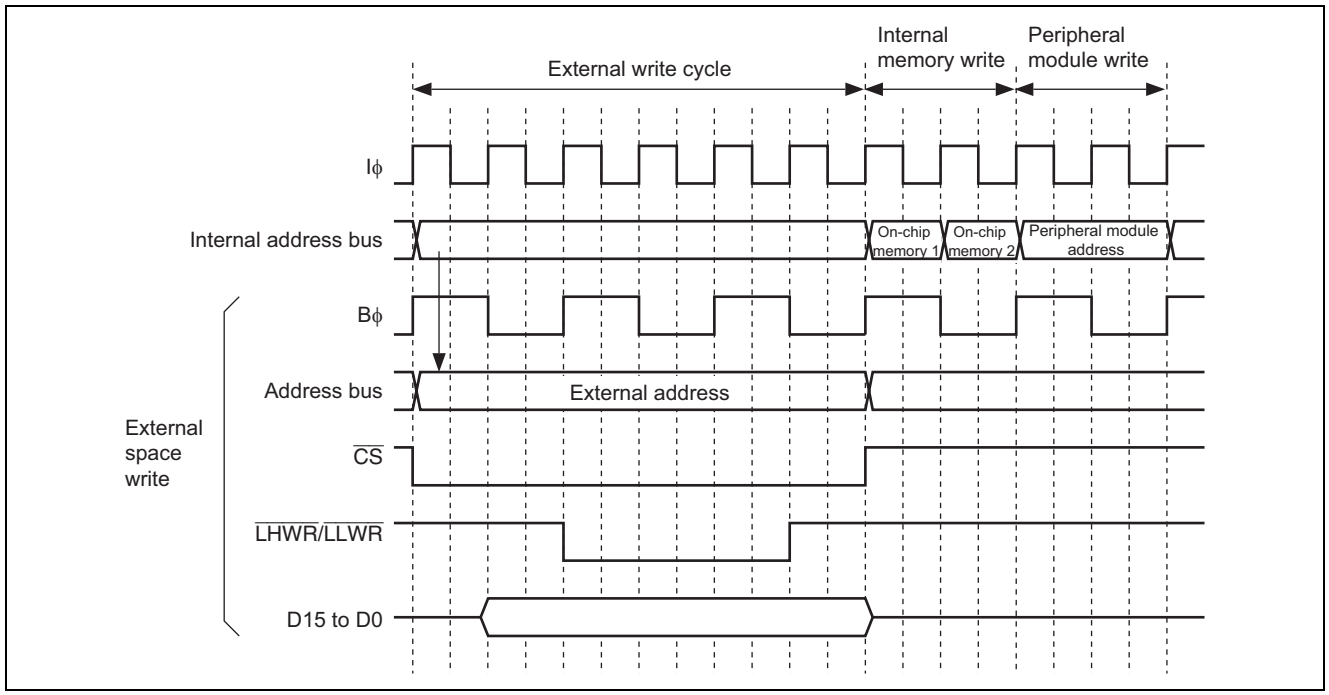


Figure 1 Example of Timing when the External-Write-Data Buffer is Not in Use (WDBE = 0)

4.2 Timing when the External-Write-Data Buffer is in Use

Figure 2 shows an example of the timing when the external-write-data buffer is in use. When the WDBE bit in BCR1 is set to 1, the buffer is in use. When this function is in use, if an external cycle or DMAC single-address transfer is followed by internal access and the external cycle or DMAC single-address transfer continues for two cycles or longer (cycles of the bus clock), the internal access (reading or writing of on-chip memory or an internal I/O register) is executed in parallel with access to the external address space from the next cycle onward, rather than being made to wait until the end of the external access.

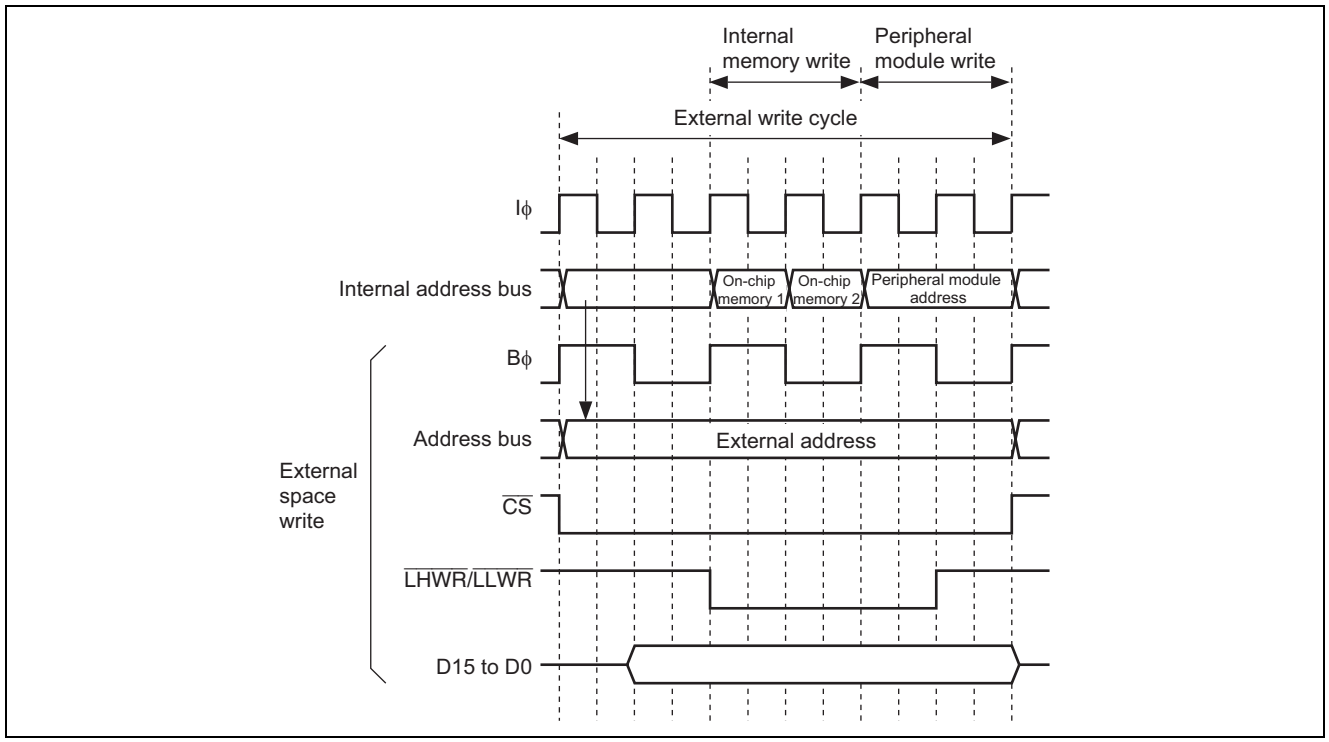


Figure 2 Example of Timing when the External-Write-Data Buffer is in Use (WDBE = 1)

5. Description of Software

5.1 Operating Environment

Table 2 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver.4.01.01
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler Ver.6.01.02 (manufactured by Renesas Technology)
Compiler options	-cpu = h8sxa:24:md, -code = machinecode, -optimize = 1, -regparam = 3 -speed = (register, shift, struct, expression)

Table 3 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'C00000	BCS3	Area 3, SRAM area
H'FF2000	B	Non-initialized data area (RAM area)

Table 4 Vector Table for Interrupt Exception Processing

Exception Processing Source	Vector No.	Vector Table Address	Destination Function
Reset	0	H'000000	init

5.2 List of Functions

Table 5 List of Functions in File main.c

Function Name	Function
init	Initialization routine Sets the CCR and configures the clocks, releases modules from the module stop mode, and calls the main function.
main	Main routine Calls the BscInit function and makes settings for the external-write-data buffer.
BscInit	Area 3 (SRAM) initialization

5.3 RAM Usage

Table 6 RAM Usage

Type	Name of Variable	Description	Used in Function
unsigned char	area3	Area 3 (SRAM area)	main
unsigned char	buf1, buf2	Internal RAM area	main

5.4 Description of Functions

5.4.1 Function init

1. Functional overview

Initialization routine, which releases the modules from module stop mode, configures the clocks, and calls the main function.

2. Arguments

None

3. Return value

None

4. Description of internal register usage

Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	Undefined*	R	Indicates the value set by a mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	Undefined*	R	Mode Select 3 to 0
10	MDS2	Undefined*	R	These bits indicate the operating mode selected by mode pins (MD2 to MD0; see table 7). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. The latches are released by a reset.
9	MDS1	Undefined*	R	
8	MDS0	Undefined*	R	

Note: * Determined by the settings on pins MD3 to MD0.

Table 7 Values of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to the CPU, DMAC, and DTC.
8	ICK0	1	R/W	001: Input clock × 2
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	1	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	0	R/W	010: Input clock × 1
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	1	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	010: Input clock × 1

- MSTPCRA, MSTPCRB and MSTPCRC control the module stop mode. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 releases the module from module stop mode.
- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Description
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current drawn by stopping operation of the bus controller and I/O ports when the CPU executes the SLEEP instruction after the module stop state has been set for all of the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timer unit (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timer unit (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	1	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

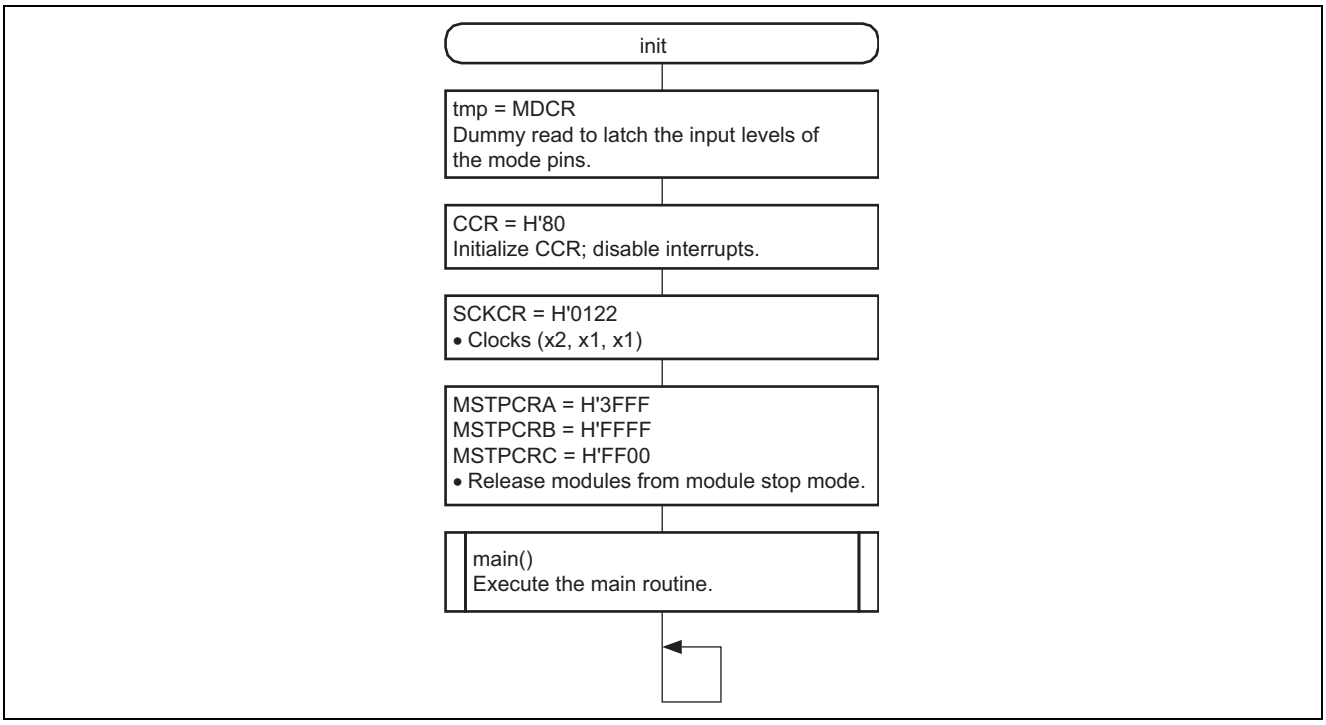
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Description
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus Interface_1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus Interface_0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Description
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5) , (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer unit (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer unit (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart


init
tmp = MDCR
Dummy read to latch the input levels of the mode pins.
CCR = H'80
Initialize CCR; disable interrupts.
SCKCR = H'0122
• Clocks (x2, x1, x1)
MSTPCRA = H'3FFF
MSTPCRB = H'FFFF
MSTPCRC = H'FF00
• Release modules from module stop mode.
main()
Execute the main routine.

5.4.2 Function main

1. Functional overview

Calls function BscInit and makes settings for the external-write-data buffer.

2. Arguments

None

3. Return value

None

4. Description of internal register usage

Usage of internal registers in this function of the sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Bus control register 1 (BCR1) Number of bits: 16 Address: H'FFFD92

Bit	Bit Name	Setting	R/W	Description
9	WDBE	1	R/W	Write Data Buffer Enable The write-data buffer is employed in cycles of external writing and single-address transfer by the DMAC. When this setting is changed, the change is reflected in the immediately subsequent external access. 0: The write-data buffer is not used. 1: The write-data buffer is used.

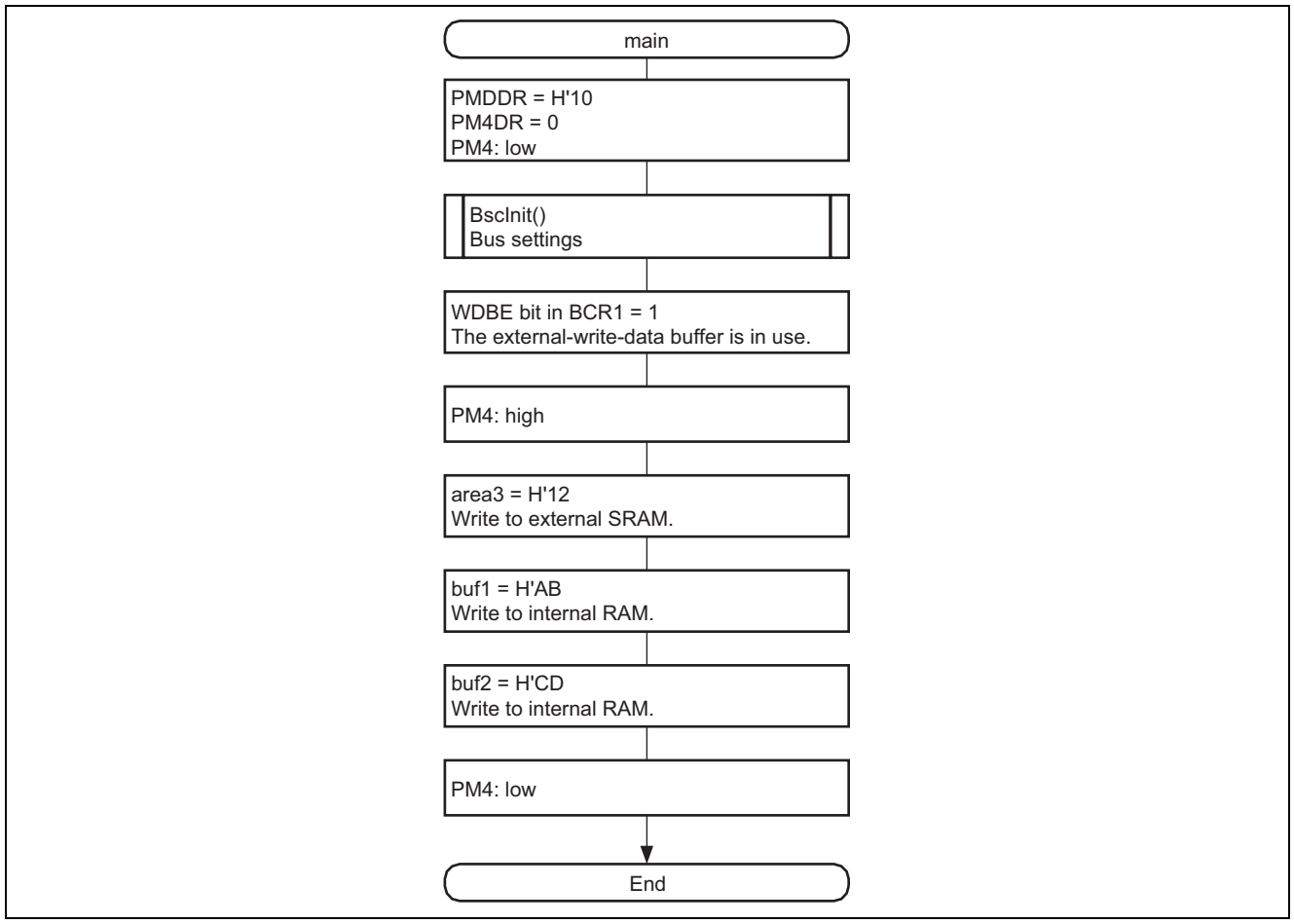
- Port M data direction register (PMDDR) Number of bits: 8 Address: H'FFEE50

Function: Sets pin PM4 as an output pin.
Setting: H'10

- Port M data register (PMDR) Number of bits: 8 Address: H'FFEE51

Bit	Bit Name	Setting	R/W	Description
4	PM4DR	1	R/W	0: The value 0 (low level) is output on pin PM4. 1: The value 1 (high level) is output on pin PM4.

5. Flowchart


main
PMDDR = H'10
PM4DR = 0
PM4: low
BscInit()
Bus settings
WDBE bit in BCR1 = 1
The external-write-data buffer is in use.
PM4: high
area3 = H'12
Write to external SRAM.
buf1 = H'AB
Write to internal RAM.
buf2 = H'CD
Write to internal RAM.
PM4: low
End

5.4.3 Function BscInit

1. Functional overview

Bus settings for area 3

2. Arguments

None

3. Return value

None

4. Description of internal register usage

Usage of internal registers in this sample task is described below. Note that the settings shown below are not the initial values but the values used in this sample task.

- Port D data direction register (PDDDR) Number of bits: 8 Address: H'FFFB8C

Function: Sets pins PD7 to PD0 as output pins for address output.
Value: H'FF

- Port E data direction register (PEDDR) Number of bits: 8 Address: H'FFFB8D

Function: Sets pins PE7 to PE0 as output pins for address output.
Value: H'FF

- Bus width control register (ABWCR) Number of bits: 16 Address: H'FFFD84

Function: Sets areas 7 to 0 for 16-bit access.
Value: H'00FF

- Access state-control register (ASTCR) Number of bits: 8 Address: H'FFFD86

Function: Sets areas 7 to 0 as spaces for access in three states (cycles of the bus clock).
Value: H'FF00

- Wait control register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Function: Sets the number for programmed waiting. Seven states (cycles of the bus clock) are inserted for access to area 3.
Value: H'7000

- Read strobe timing control register (RDNCR) Number of bits: 16 Address: H'FFFD8C

Function: For read access to areas 7 to 0, sets the timing for enabling RD and the timing of the end of read cycles.
Value: H'0000

- Port function control register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Setting	R/W	Description
7	CS7E	0	R/W	CS7–CS0 Enable
6	CS6E	0		These bits select enabling or disabling of the corresponding $\overline{CSn}$ output pins.
5	CS5E	0		0: Setting for an I/O port pin
4	CS4E	0		1: Setting for a $\overline{CSn}$ output pin (n = 7 to 0)
3	CS3E	1		
2	CS2E	0		
1	CS1E	0		
0	CS0E	0		

- Port function control register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Setting	R/W	Description
2	RDWRE	1	R/W	RD/$\overline{WR}$ Output Enable 0: Output of RD/$\overline{WR}$ is disabled. 1: Output of RD/$\overline{WR}$ is enabled.

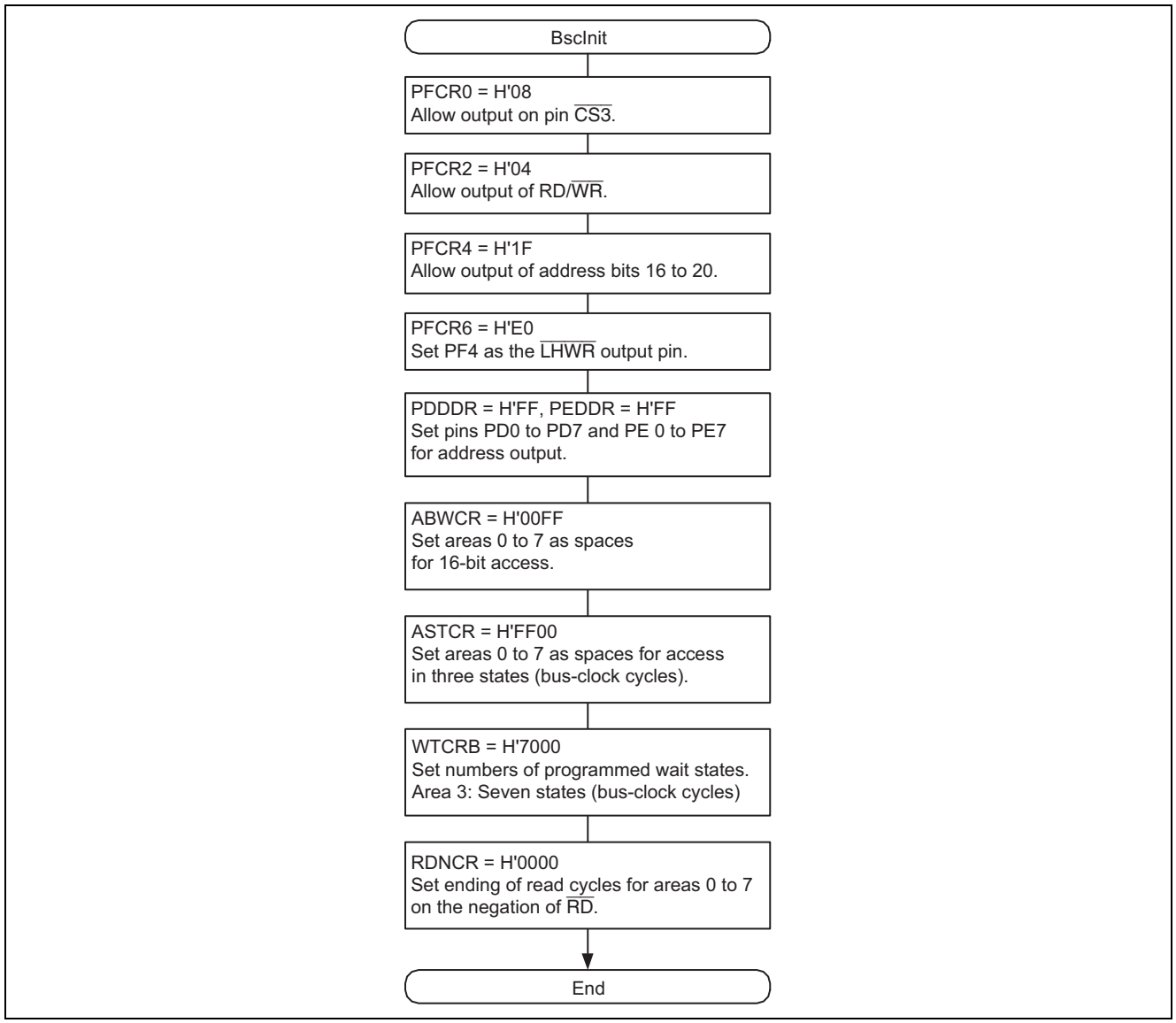
- Port function control register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Setting	R/W	Description
4	A20E	1	R/W	Address A20 Enable 0: Disables the A20 output. 1: Enables the A20 output.
3	A19E	1	R/W	Address A19 Enable 0: Disables the A19 output. 1: Enables the A19 output.
2	A18E	1	R/W	Address A18 Enable 0: Disables the A18 output. 1: Enables the A18 output.
1	A17E	1	R/W	Address A17 Enable 0: Disables the A17 output. 1: Enables the A17 output.
0	A16E	1	R/W	Address A16 Enable 0: Disables the A16 output. 1: Enables the A16 output.

- Port function control register 6 (PFCR6) Number of bits: 8 Address: H'FFFBC6

Bit	Bit Name	Setting	R/W	Description
6	LHWROE	1	R/W	$\overline{LHWR}$ Output Enable 0: Sets PA4 as an I/O port pin. 1: Sets PF4 as the $\overline{LHWR}$ output pin.

5. Flowchart


BscInit
PFCR0 = H'08
Allow output on pin CS3.
PFCR2 = H'04
Allow output of RD/WR.
PFCR4 = H'1F
Allow output of address bits 16 to 20.
PFCR6 = H'E0
Set PF4 as the LHWR output pin.
PDDDR = H'FF, PEDDR = H'FF
Set pins PD0 to PD7 and PE 0 to PE7
for address output.
ABWCR = H'00FF
Set areas 0 to 7 as spaces
for 16-bit access.
ASTCR = H'FF00
Set areas 0 to 7 as spaces for access
in three states (bus-clock cycles).
WTCRB = H'7000
Set numbers of programmed wait states.
Area 3: Seven states (bus-clock cycles)
RDNCR = H'0000
Set ending of read cycles for areas 0 to 7
on the negation of RD.
End

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jun.18.07	—	First edition issued
1.01	Feb.15.08	4	Section 4.2, “Timing when the External-Write-Data Buffer in Use” modified

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