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# M16C/80 Group
## External Buses

## 1. Abstract

The following article introduces external bus.

## 2. Introduction

The explanation of this issue is M16C/80 Group.

## 3. External Buses

### 3.1 Overview of External Buses

Memory and I/O external expansion can be connected to microcomputer easily by using external buses. When memory expansion mode or microprocessor mode is selected for processor mode, some of the pins function as the address bus, the data bus, and as control signals and this makes the external buses be able to operate.

You can select 8-bit or 16-bit for the width of the external data bus for external areas 0, 1, 2, and 3. When the data bus width bit of the external data bus width control register is “0”, the data bus width is 8 bits; when “1”, it is 16 bits. The width can be set for each of the external areas. 16-bit width is used to access an internal area, regardless of the data bus width bit of the external data bus width control register.

The default bus width for external area 3 is 16 bits when the BYTE pin is “L” after a reset, or 8 bits when the BYTE pin is “H” after a reset.

## 3.2 Data Access

### 3.2.1 Data Bus Width

If the data bus width bits in all areas of the external data bus width control register are “0”, the data bus width becomes 8 bits, and P10 (/D8) through P17 (/D15) can be used as I/O ports (Figure 3.2.1).
If any of the data bus width bits of the external data bus width control register is “1” , the data bus width becomes 16 bits, and P10 (/D8) through P17 (/D15) operate as a data bus (D8 through D15) (Figure 3.2.1).

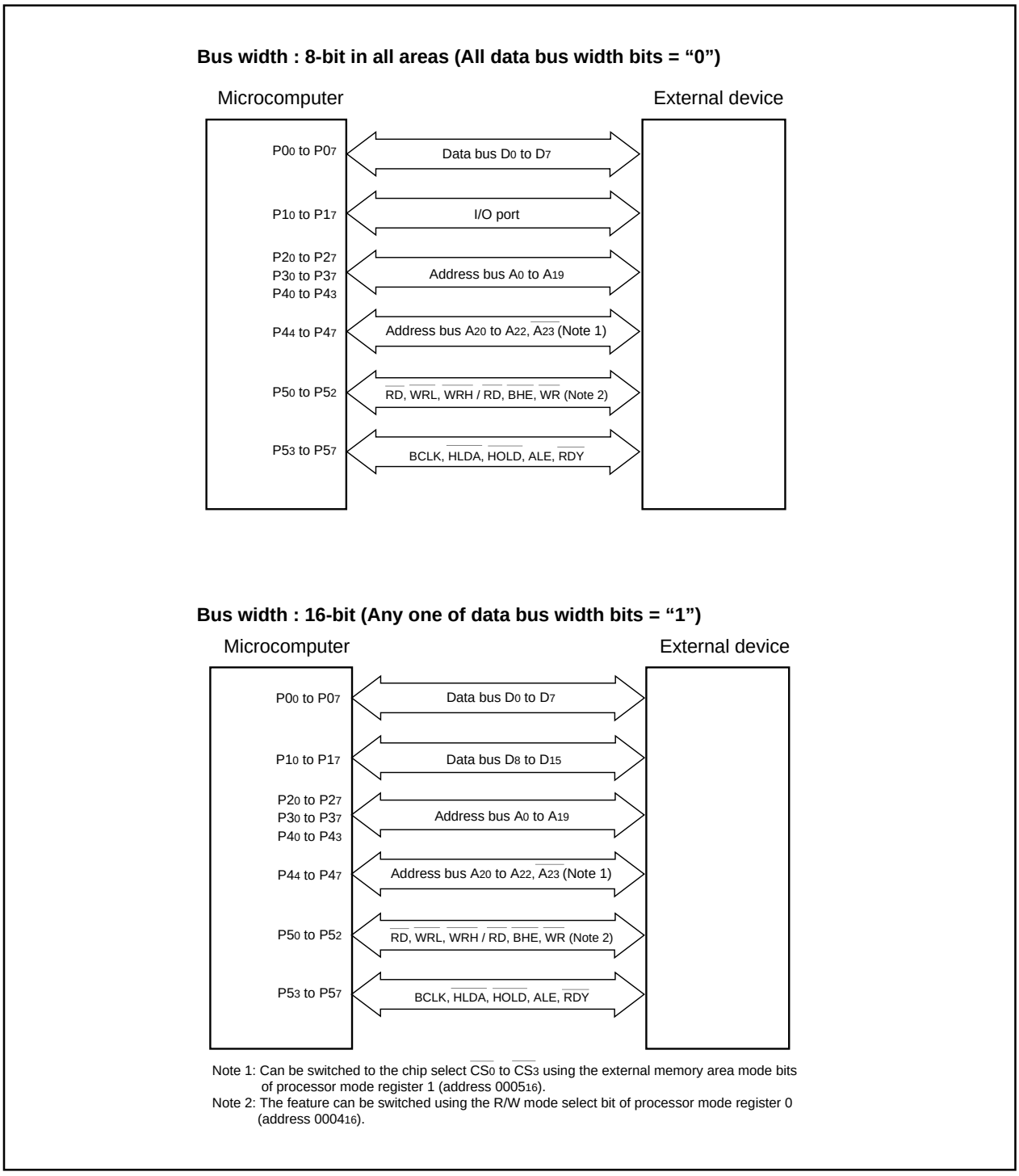
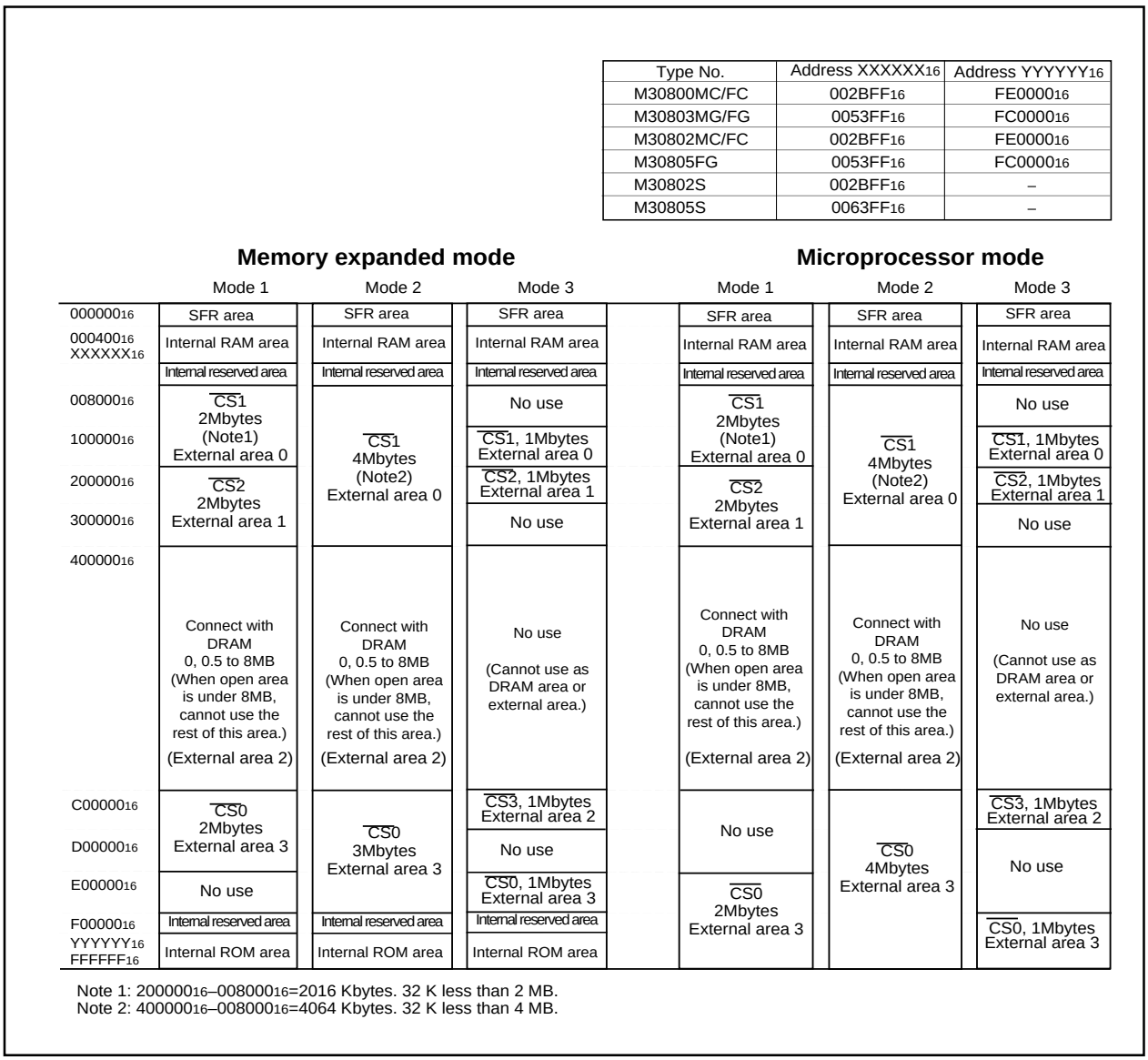



**Figure 3.2.1. Data bus width select bits and external data bus width**

### 3.2.2 Chip Selects and Address Bus

Chip selects (P44/$\overline{CS3}$ through P47/$\overline{CS0}$) share $A_0$ to $A_{22}$ and $\overline{A_{23}}$. Use bits 0 and 1 of the processor mode register 1 (address $0005_{16}$) to set the external area mode, then select the chip select area and number of address outputs. Figure 3.2.2 shows addresses in which chip selects become active ("L"). Since the extent of the internal area and the external area in memory expansion mode is different from those in microprocessor mode, there is a difference between areas for which $\overline{CS0}$ is output. When an internal ROM/RAM area is being accessed, no chip select is output, and the address bus does not change (the address of the external area that was accessed previously is held).

| Type No. | Address XXXXXX$_{16}$ | Address YYYYYY$_{16}$ |
|---|---|---|
| M30800MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30803MG/FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30805FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802S | 002BFF$_{16}$ | – |
| M30805S | 0063FF$_{16}$ | – |




Note 1: $200000_{16}$–$008000_{16}$=2016 Kbytes. 32 K less than 2 MB.
Note 2: $400000_{16}$–$008000_{16}$=4064 Kbytes. 32 K less than 4 MB.

**Figure 3.2.2. Addresses in which chip selects turn active ("L")**

### 3.2.3 Bus Types

The M16C/80 Group has two types of buses: a separate bus where separate pins are used for address output and data input/output and a multiplexed bus where pins are time- multiplexed and switched between address output and data input/output to save the number of pins used.
A separate bus is used to access devices such as ROM and RAM which have separate buses. The areas accessed via separate buses can be allocated for programs and data.
A multiplexed bus is used to access devices such as ASSPs which have multiplexed buses. The areas accessed via a multiplexed bus can only be allocated for data. Programs cannot be located in these areas.

The area accessed via a multiplex bus can be selected from three types of area $\overline{CS2}$ area, $\overline{CS1}$ area, and entire $\overline{CS}$ space by setting the multiplexed bus select bits (bits 4 and 5) of the processor mode register 0 (address $0004_{16}$). However, the entire space cannot be selected when operating in the microprocessor mode.
$\overline{CS}$ areas not accessed via multiplexed bus are accessed through separate buses.

When accessing an area set for access via a multiplexed bus the data bus is 8 bits wide, the data bus $D_0$ to $D_7$ is multiplexed with address bus $A_0$ to $A_7$.
If the data bus is 16 bits wide, the data bus $D_0$ to $D_{15}$ is multiplexed with address bus $A_0$ to $A_{15}$. In either case, the bus is switched between data and address separated only in time. When accessing memory using the multiplex bus configuration, two waits are inserted regardless of whether you select “No wait” or “1 wait’ in the appropriate bit of the wait control register.

### 3.2.4 R/W Modes

The read/write signal that is output when accessing an external area can be selected between the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ and the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ modes by setting the R/W mode select bit (bit 2) of the processor mode register 0 (address $0004_{16}$). Use the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ mode to access a 16-bit wide RAM and the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ mode to access an 8-bit wide RAM.
When the M16C/80 is reset, the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ mode is selected by default. To switch over the R/W mode, change the $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ to the $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ mode before accessing an external RAM.
Refer to the connection examples of $\overline{RD}$/$\overline{BHE}$/$\overline{WR}$ and $\overline{RD}$/$\overline{WRH}$/$\overline{WRL}$ shown in Section 3.4, "Connection Examples."

## 3.3 External Memory Area Mode

Here follows the description of the external memory area mode.

(1) Mode 0 • • • P44 to P47:A20 to A23

(2) Mode 1 • • • P44:A20, P45 to P47:$\overline{CS2}$ to $\overline{CS0}$

(3) Mode 2 • • • P44 to P45:A20 to A21, P46 to P47:$\overline{CS1}$ to $\overline{CS0}$

(4) Mode 3 • • • P44 to P47:$\overline{CS3}$ to $\overline{CS0}$

Use bits 1 and 0(PM11,PM10) of processor mode register 1 to select a desired mode. Figure 3.3.1 shows the processor mode register 1.

Processor mode register 1 (Note 1) :Mask ROM version
ROMless version (144-pin version)

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Symbol | Address | When reset |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0 | | | | PM1 | 000516 | 0016 |

| Bit symbol | Bit name | Function | R | W |
|---|---|---|---|---|
| PM10 | External memory area mode bit (Note 3) | b1 b0<br>0 0 : Mode 0 (P44 to P47 : A20 to $\overline{A23}$)<br>0 1 : Mode 1 (P44 : A20, P45 to P47 : $\overline{CS2}$ to $\overline{CS0}$)<br>1 0 : Mode 2 (P44, P45 : A20, A21, P46, P47 : $\overline{CS1}$, $\overline{CS0}$)<br>1 1 : Mode 3 (Note 2) (P44 to P47 : $\overline{CS3}$ to $\overline{CS0}$) | ○ | ○ |
| PM11 | | | | |
| PM12 | Internal memory wait bit | 0 : No wait state<br>1 : Wait state inserted | — | — |
| Reserved bit | | Must always be set to “0” | — | ○ |
| PM14 | ALE pin select bit (Note 3) | b5 b4<br>0 0 : No ALE<br>0 1 : P53/BCLK (Note 4)<br>1 0 : P56/$\overline{RAS}$<br>1 1 : P54/$\overline{HLDA}$ | ○ | ○ |
| PM15 | | | ○ | ○ |
| Nothing is assinged. When read, the content is indeterminate. | | | — | — |

Note 1: Set bit 1 of the protect register (address 000A16) to “1” when writing new values to this register.
Note 2: When mode 3 is selected, DRAMC is not used.
Note 3: Valid in memory expansion mode or in microprocessor mode.
Note 4: When selecting P53/BCLK, set bits 0 and 1 of system clock control register 0 (CM00, CM01) to "0".

Processor mode register 1 (Note 1) :Flash memory version

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Symbol | Address | When reset |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 0 | | | | PM1 | 000516 | 0016 |

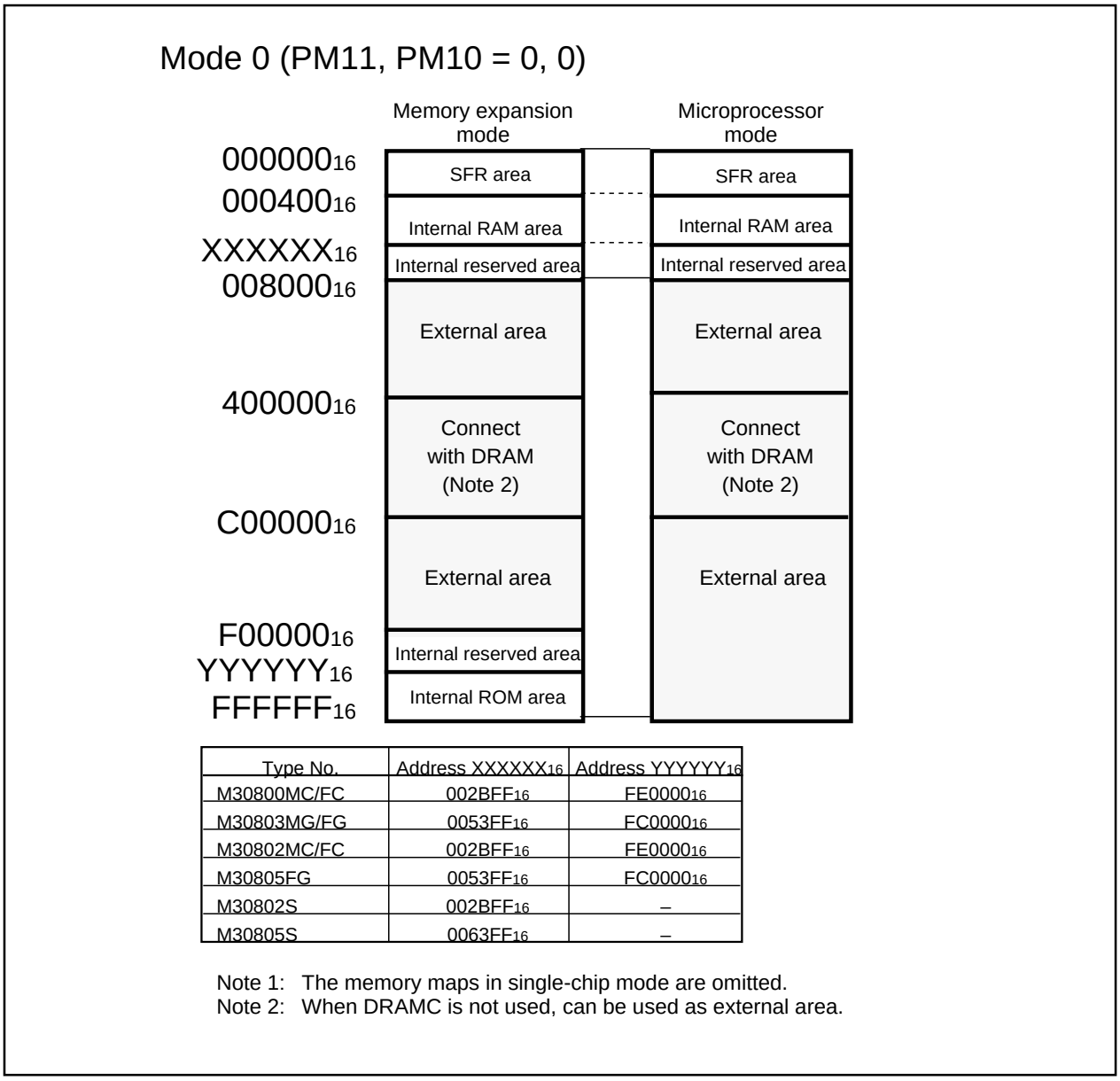
| Bit symbol | Bit name | Function | R | W |
|---|---|---|---|---|
| PM10 | External memory area mode bit (Note 3) | b1 b0<br>0 0 : Mode 0 (P44 to P47 : A20 to $\overline{A23}$)<br>0 1 : Mode 1 (P44 : A20, P45 to P47 : $\overline{CS2}$ to $\overline{CS0}$)<br>1 0 : Mode 2 (P44, P45 : A20, A21, P46, P47 : $\overline{CS1}$, $\overline{CS0}$)<br>1 1 : Mode 3 (Note 2) (P44 to P47 : $\overline{CS3}$ to $\overline{CS0}$) | ○ | ○ |
| PM11 | | | | |
| PM12 | Internal memory wait bit | 0 : No wait state<br>1 : Wait state inserted | — | — |
| Reserved bit | | Must always be set to “0” | — | ○ |
| PM14 | ALE pin select bit (Note 3) | b5 b4<br>0 0 : No ALE<br>0 1 : P53/BCLK (Note 4)<br>1 0 : P56/$\overline{RAS}$<br>1 1 : P54/$\overline{HLDA}$ | ○ | ○ |
| PM15 | | | ○ | ○ |
| Reserved bit | | Must always be set to “1” (Note 5) | ○ | ○ |

Note 1: Set bit 1 of the protect register (address 000A16) to “1” when writing new values to this register.
Note 2: When mode 3 is selected, DRAMC is not used.
Note 3: Valid in memory expansion mode or in microprocessor mode.
Note 4: When selecting P53/BCLK, set bits 0 and 1 of system clock control register 0 (CM00, CM01) to "0".
Note 5: Rewrite this bit when the main clock is in division by 8 mode.

**Figure 3.3.1. Processor mode register 1**

### 3.3.1 Mode 0

In mode 0, a maximum 16 Mbyte of memory space can be accessed in memory expansion and microprocessor modes. Programs and data can be located in any external area.




| Type No. | Address XXXXXX$_{16}$ | Address YYYYYY$_{16}$ |
|---|---|---|
| M30800MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30803MG/FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30805FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802S | 002BFF$_{16}$ | – |
| M30805S | 0063FF$_{16}$ | – |

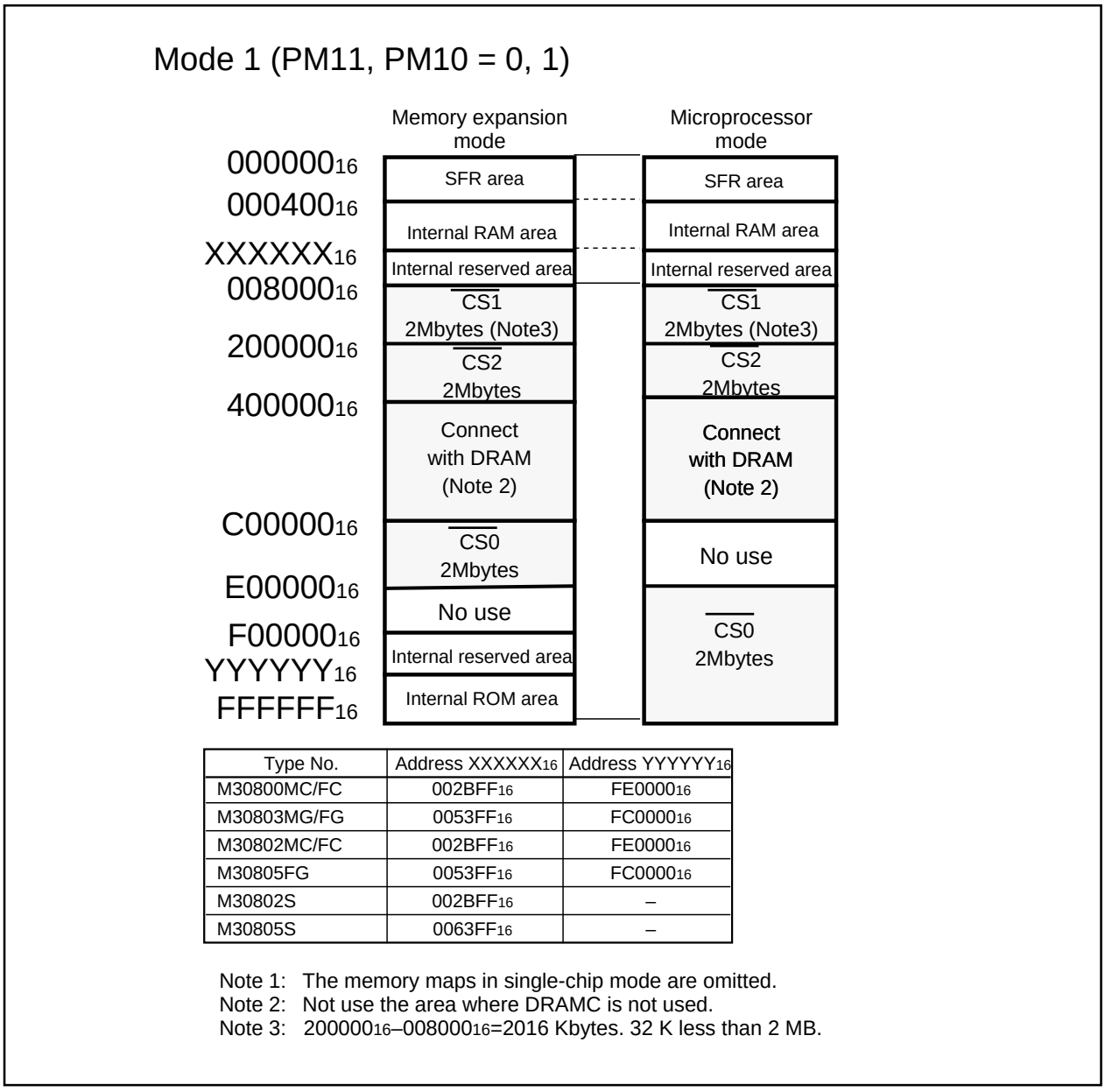
Note 1: The memory maps in single-chip mode are omitted.
Note 2: When DRAMC is not used, can be used as external area.

**Figure 3.3.2. Memory Map in Mode 0**

When accessing each external area, chip select signals $\overline{CS0}$ to $\overline{CS3}$ are not output. Instead, address signals A$_{20}$ to $\overline{A23}$ are output. $\overline{A23}$ is an inverted output of the MSB of the address.
The area consisting of these addresses 400000$_{16}$ through BFFFFF$_{16}$ can be used as external area when not connecting with DRAM. When connecting with DRAM, the rest of this area cannot be used.

### 3.3.2 Mode 1

In mode 1, the external area can be split into four and used as chip select signals and can be connected with DRAM.




| Type No. | Address XXXXXX$_{16}$ | Address YYYYYY$_{16}$ |
|---|---|---|
| M30800MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30803MG/FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30805FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802S | 002BFF$_{16}$ | – |
| M30805S | 0063FF$_{16}$ | – |

Note 1: The memory maps in single-chip mode are omitted.
Note 2: Not use the area where DRAMC is not used.
Note 3: 200000$_{16}$–008000$_{16}$=2016 Kbytes. 32 K less than 2 MB.

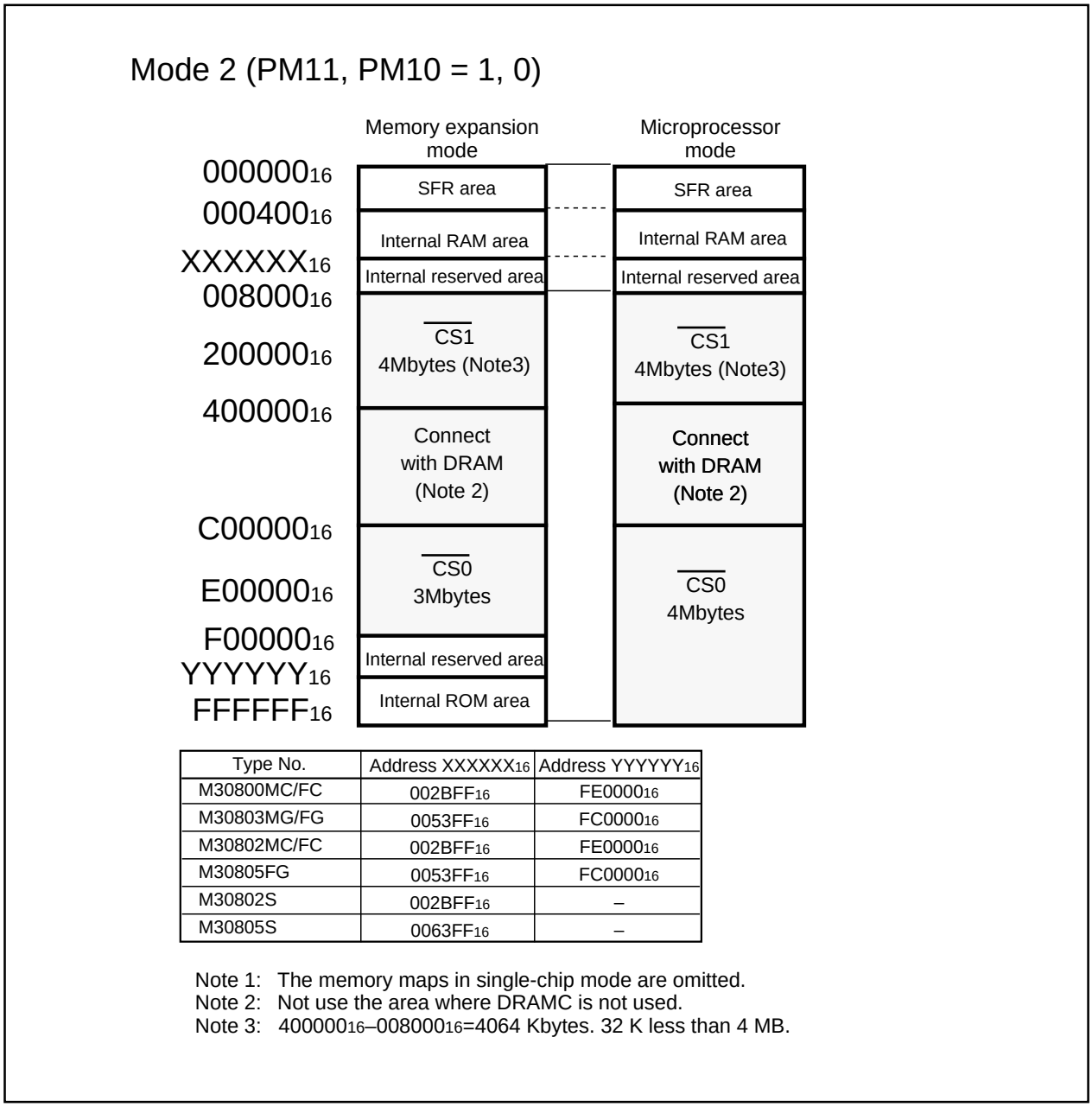
**Figure 3.3.3. Memory Map in Mode 1**

When accessing the area comprised of address 008000$_{16}$ through 1FFFFF$_{16}$, the CPU outputs $\overline{CS1}$ chip select signal. Similarly, when accessing the area comprised of address 200000$_{16}$ through 3FFFFF$_{16}$ and address C00000$_{16}$ through DFFFFF$_{16}$ (address E00000$_{16}$ through FFFFFF$_{16}$ in microprocessor mode), the CPU outputs $\overline{CS2}$ and $\overline{CS0}$ chip select signals respectively.

The area consisting of these addresses 400000$_{16}$ through BFFFFF$_{16}$ cannot be used when not connecting with DRAM. Similarly, when connecting with DRAM, the open area of these addresses cannot be used.

### 3.3.3 Mode 2

In mode 2, the external area can be split into three and used as chip select signals and can be connected with DRAM.




| Type No. | Address XXXXXX$_{16}$ | Address YYYYYY$_{16}$ |
|---|---|---|
| M30800MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30803MG/FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30805FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802S | 002BFF$_{16}$ | – |
| M30805S | 0063FF$_{16}$ | – |

Note 1: The memory maps in single-chip mode are omitted.
Note 2: Not use the area where DRAMC is not used.
Note 3: 400000$_{16}$–008000$_{16}$=4064 Kbytes. 32 K less than 4 MB.

**Figure 3.3.4. Memory Map in Mode 2**

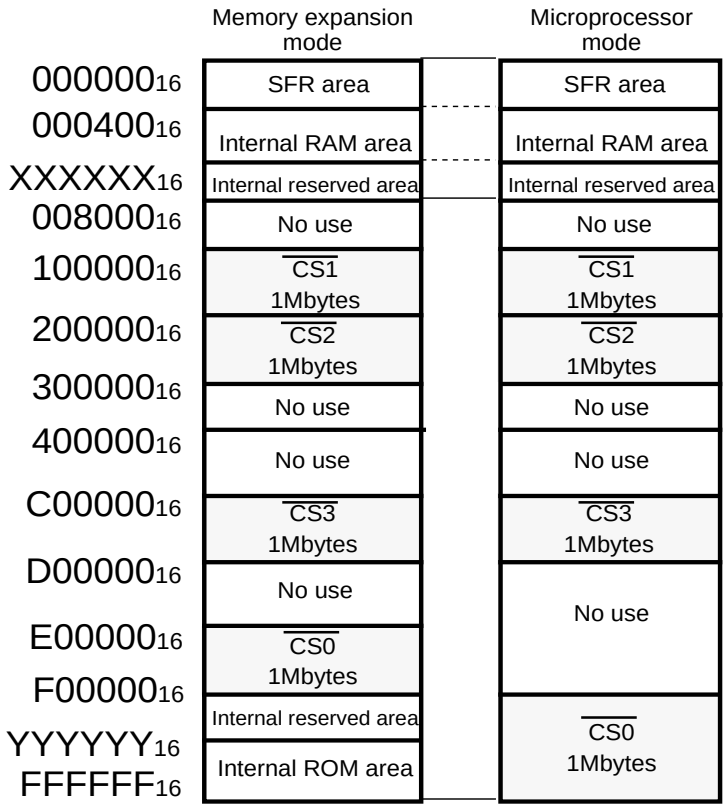
When accessing the area comprised of address 008000$_{16}$ through 3FFFFF$_{16}$, the CPU outputs $\overline{CS1}$ chip select signal. Similarly, when accessing the area comprised of address C00000$_{16}$ through EFFFFF$_{16}$ (address C00000$_{16}$ through FFFFFF$_{16}$ in microprocessor mode), the CPU outputs $\overline{CS0}$ chip select signal.

The area consisting of these addresses 400000$_{16}$ through BFFFFF$_{16}$ cannot be used when not connecting with DRAM. Similarly, when connecting with DRAM, the open area of these addresses cannot be used.

### 3.3.4 Mode 3

In mode 3, the external area can be split into three and used as chip select signals.

Mode 3 (PM11, PM10 = 1, 1)




| Type No. | Address XXXXXX$_{16}$ | Address YYYYYY$_{16}$ |
|---|---|---|
| M30800MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30803MG/FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802MC/FC | 002BFF$_{16}$ | FE0000$_{16}$ |
| M30805FG | 0053FF$_{16}$ | FC0000$_{16}$ |
| M30802S | 002BFF$_{16}$ | – |
| M30805S | 0063FF$_{16}$ | – |

Note : The memory maps in single-chip mode are omitted.

**Figure 3.3.5. Memory Map in Mode 3**

When accessing the area comprised of address 100000$_{16}$ through 1FFFFF$_{16}$, the CPU outputs $\overline{CS1}$ chip select signal. Similarly, when accessing the area comprised of address 200000$_{16}$ through 2FFFFF$_{16}$, C00000$_{16}$ through CFFFFF$_{16}$ and E00000$_{16}$ through EFFFFF$_{16}$ (address F00000$_{16}$ through FFFFFF$_{16}$ in microprocessor mode), the CPU outputs $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS0}$ chip select signals respectively.
The area consisting of these addresses 400000$_{16}$ through BFFFFF$_{16}$ cannot be used because DRAM cannot be connected in mode 3.

## 3.4 Connection Examples

### 3.4.1 16-bit Memory to 16-bit Width Data Bus Connection Example

Figure 3.4.1 shows an example of connecting M5M51016BTP (16-bit SRAM) to a 16-bit data bus.In this diagram, when reset the microcomputer operates in single-chip mode. Change the external area mode to mode 1 through mode 3, the external area 0 data bus width bit to 16-bit bus and the processor mode bit to memory expansion mode in a program.

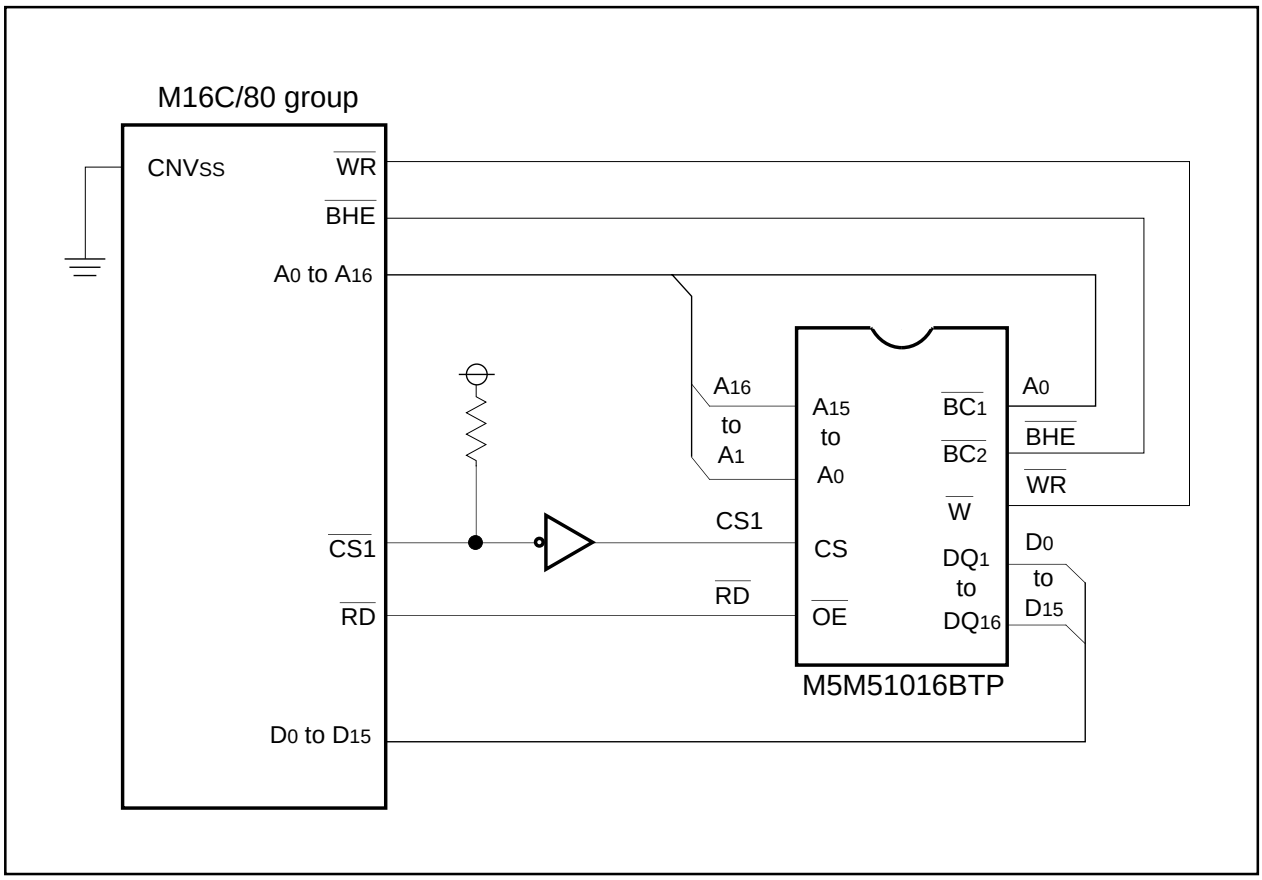



**Figure 3.4.1. Example of connecting M5M51016BTP to a 16-bit data bus**

### 3.4.2 8-bit Memory to 16-bit Width Data Bus Connection Example

Figure 3.4.2 shows an example of connecting two M5M5278DP (8-bit SRAM) to a 16-bit data bus.In this diagram, when reset the microcomputer operates in single-chip mode. Change the external area mode to mode 1 through mode 3, the external area 0 data bus width bit to 16-bit bus and the processor mode bit to memory expansion mode in a program.

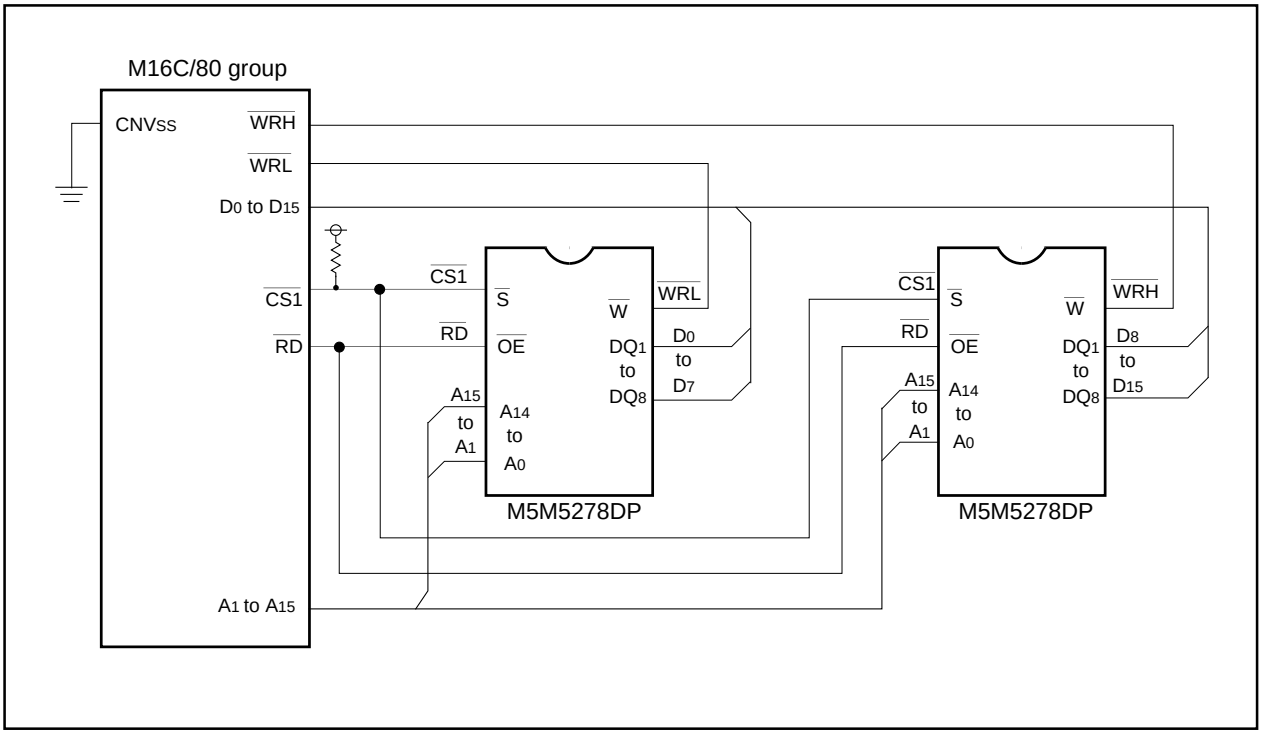



**Figure 3.4.2. Example of connecting two M5M5278's to a 16-bit data bus**

Figure 3.4.3 shows how to connect two M5M28F101AFP (8-bit flash memory). In 16-bit bus mode, the $\overline{BHE}$/$\overline{WRH}$ pin functions as $\overline{BHE}$ after reset. When connecting 8-bit flash memory chips to the 16-bit bus, make sure the microcomputer's $\overline{WRL}$ pin is connected to the $\overline{WR}$ pins on both flash memory chips, and that data is written to the flash memory in units of 16 bits beginning with an even address.

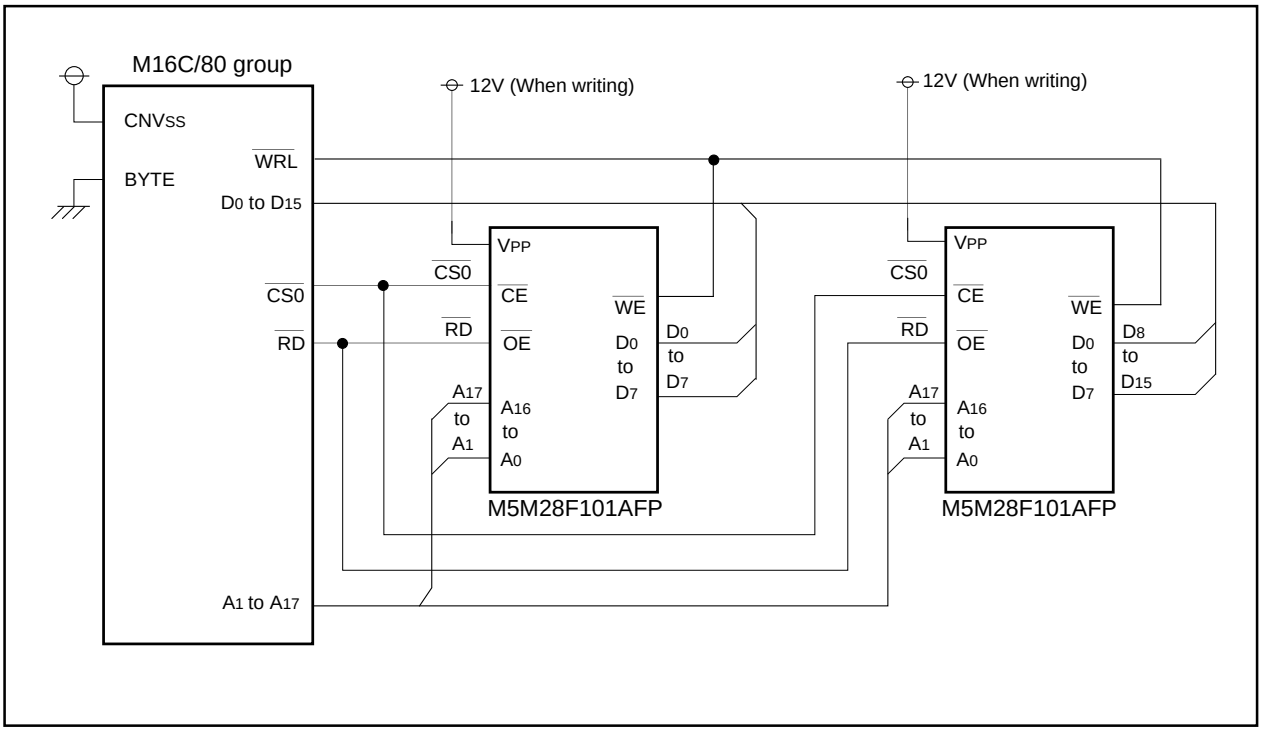



**Figure 3.4.3. Example of connecting two M5M28F101AFPs to a 16-bit data bus**

### 3.4.3 8-bit Memory to 8-bit Width Data Bus Connection Example

Figure 3.4.4 shows an example of connecting two M5M5278DP (8-bit SRAM) to an 8-bit data bus.In this diagram, when reset the microcomputer operates in single-chip mode. Change the external area mode to mode 1 through mode 3 and the processor mode bit to memory expansion mode in a program.

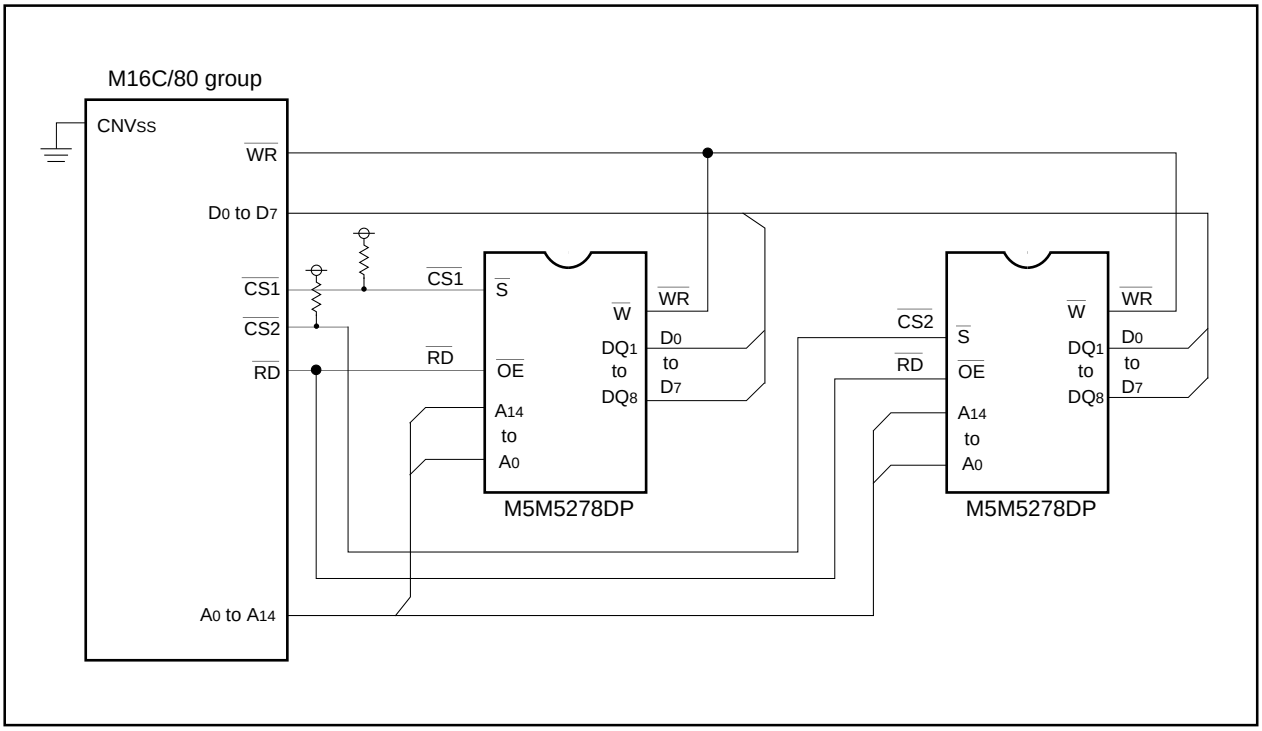



**Figure 3.4.4. Example of connecting two M5M5278's to an 8-bit data bus**

### 3.4.4 Two 8-bit and 16-Bit Memory to 16-Bit Width Data Bus Connection Example

Figure 3.4.5 shows an example of connecting M5M28F102 (16-bit flash memory) and two M5M5278DP (8-bit SRAM) to a 16-bit data bus. In this diagram, when reset the microcomputer operates in microprocessor mode. Change the external area mode to mode 1 through mode 3 and the external area 0 data bus width bit to 16-bit bus in a program. (The bus width of the external area 3 ($\overline{CS0}$ area) is 16-bit because the level of BYTE pin is "L".)

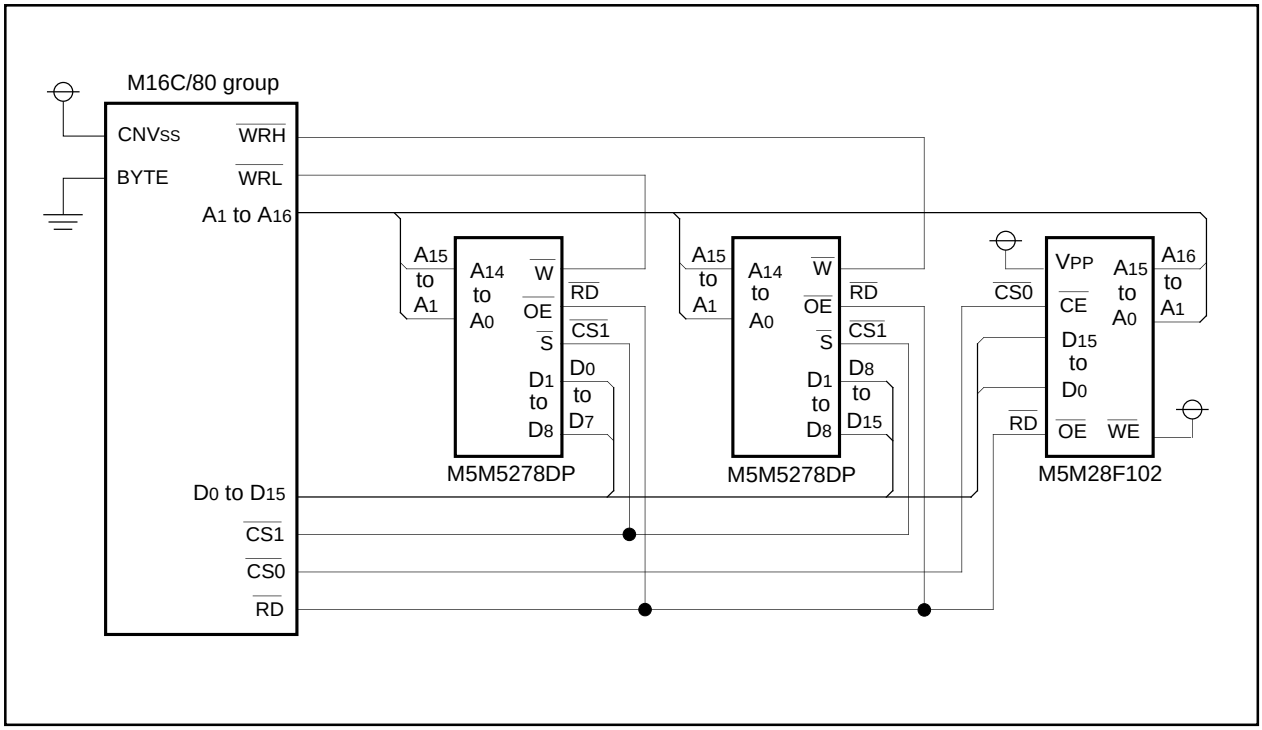



**Figure 3.4.5. Example of connection of two 8-bit memories and one 16-bit memory to 16-bit width data bus**

### 3.4.5 8-bit Memory to 8-bit Width Data Bus and 16-Bit Memory to 16-Bit Width Data Bus Connection Example

Figure 3.4.6 shows an example of connecting M5M28F102 (16-bit flash memory) and M5M5278DP (8-bit SRAM) to a 16-bit data bus and a 8-bit data bus respectively. In this diagram, when reset the microcomputer operates in microprocessor mode. Change the external area mode to mode 1 through mode 3 and the external area 0 data bus width bit to 8-bit bus in a program. (The bus width of the external area 3 ($\overline{CS0}$ area) is 16-bit because the level of BYTE pin is "L".) Write to the flash memory in 16-bit unit from even address.

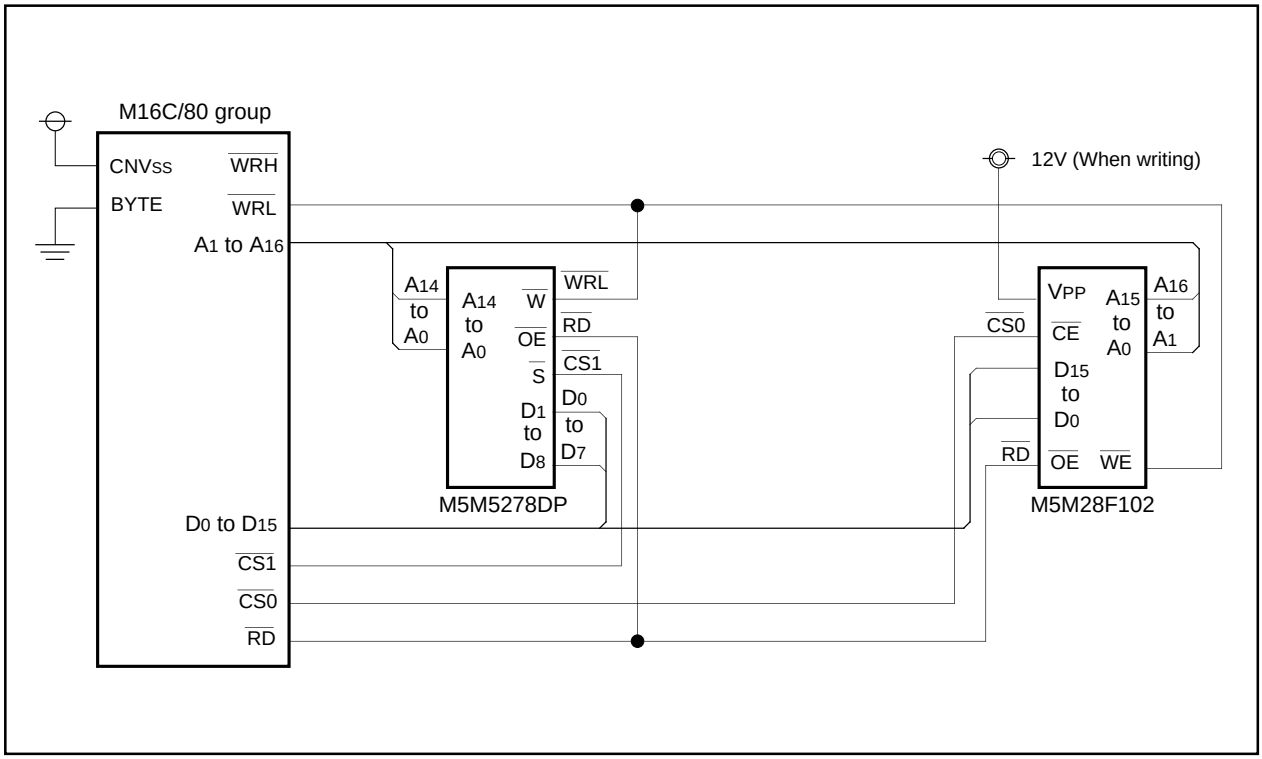



**Figure 3.4.6. Example of connection of 8-bit and 16-bit memory to 8-bit and 16-bit width data bus respectively**

### 3.4.6 Chip Selects and Address Bus

When there are insufficient chip select signals, it is necessary to generate chip selects externally. Figure 3.4.7 shows an example of a connection in which the $\overline{CS1}$ area is divided into eight 128K byte areas when the external area mode is selected for mode 3.

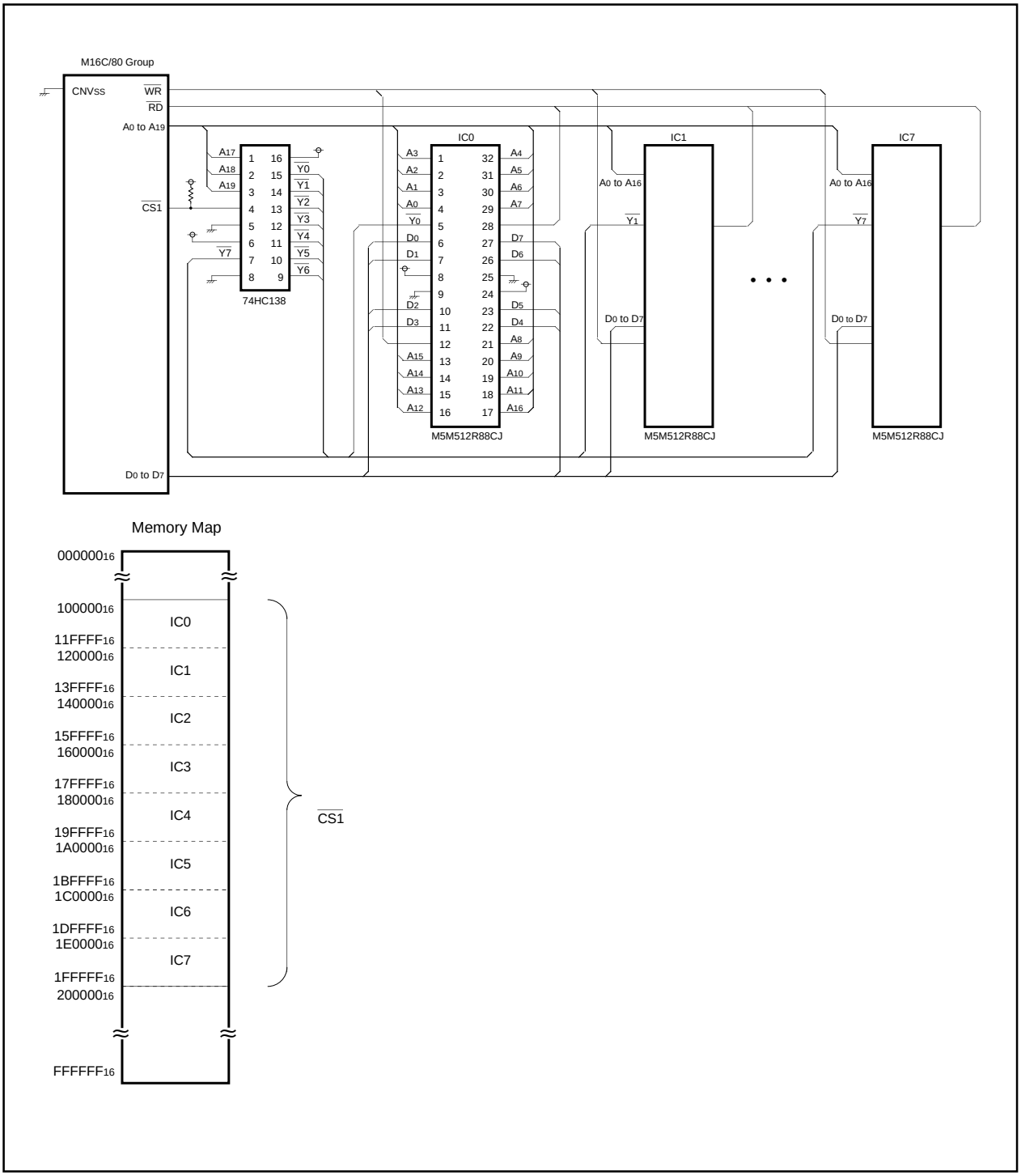



**Figure 3.4.7. Chip selects and address bus**

### 3.4.7 DRAM to 16-bit Width Data Bus Connection Example

Figure 3.4.8 shows an example of connecting M5M465160A (64 M-bit DRAM) to a 16-bit data bus. In this diagram, when reset the microcomputer operates in single-chip mode. Change the R/W mode select bit (bit 2 at address $0004_{16}$) to “1”, the external area mode to mode 0 through mode 2, the external area 2 data bus width bit to 16-bit bus and the processor mode bit to memory expansion mode in a program.

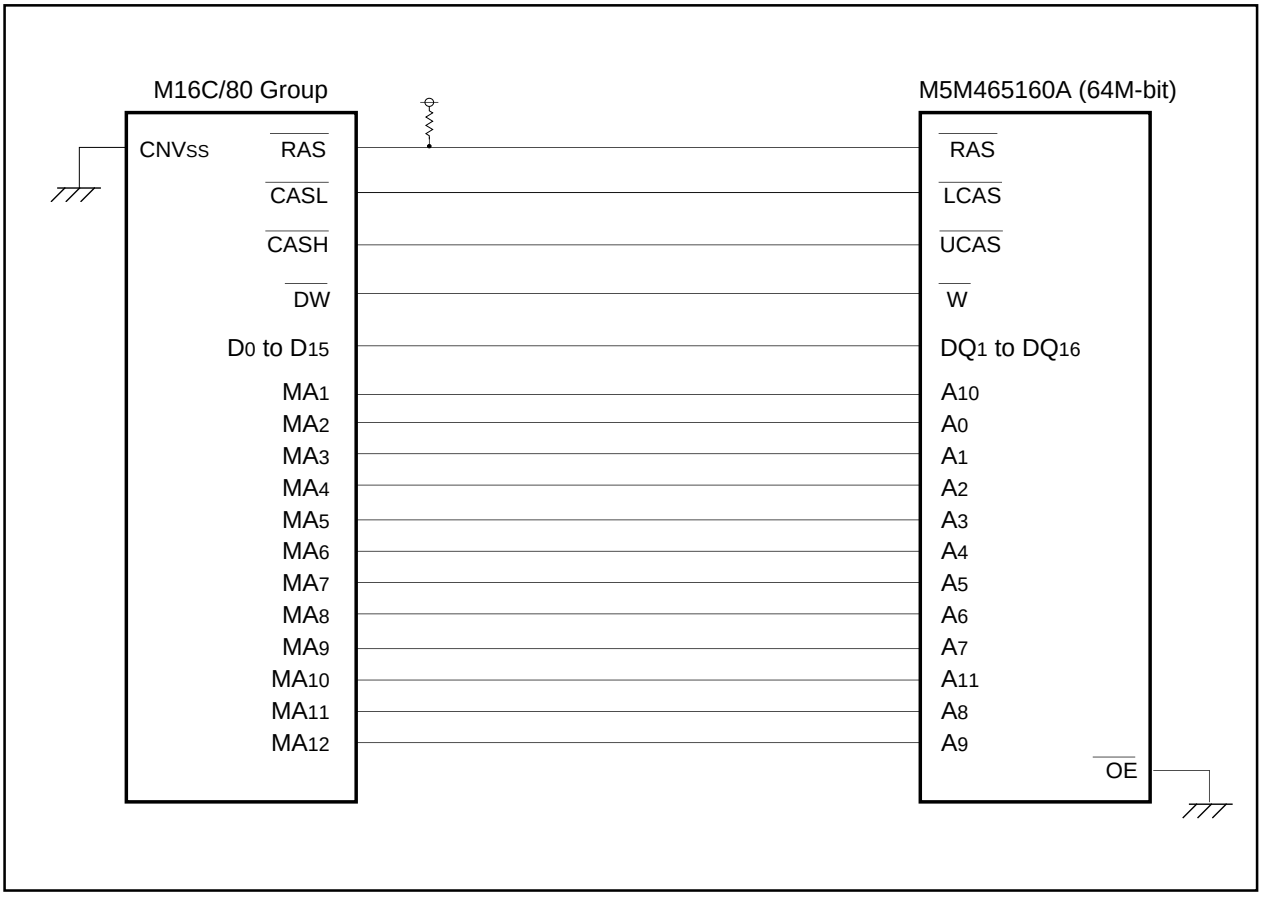



**Figure 3.4.8. Example of connecting DRAM to a 16-bit data bus**

## 3.5 Connectable Memories

### 3.5.1 Operation Frequency and Access Time

Connectable memories depend upon the BCLK frequency f(BCLK). f(BCLK) is contingent on the oscillator's frequency and on the settings in the main clock division register (bits 0 to 4 of address $000C_{16}$).

The following are the conditional equations for the connections. Meet these conditions minimally. Figures 3.5.1 and 3.5.2 show the relation between the frequency of BCLK and memory.

**(1) Read cycle time (tCR)/write cycle time (tCW)**

Read cycle time (tCR) and write cycle time (tCW) must satisfy the following conditional expressions:

- **With the Wait option cleared**

  $tCR < 10^9/f(BCLK)$ and $tCW < 2 \times 10^9/f(BCLK)$

- **With the Wait option selected**

  $tCR < m \times 10^9/f(BCLK)$ and $tCW < m \times 10^9/f(BCLK)$

  (m=2, 3, and 4 when 1wait, 2 waits and 3 waits, respectively)

**(2) Address access time [ta(A)]**

Address access time [ta(A)] must satisfy the following conditional expressions:

**(a) Vcc = 5V**

- **With the Wait option cleared**

  $ta(A) < 10^9/f(BCLK) - 35(ns)$*

- **With the Wait option selected**

  $ta(A) < m \times 10^9/f(BCLK) - 35(ns)$* (m=2, 3, and 4 when 1wait, 2 waits and 3 waits, respectively)

* 35(ns) = td(BCLK – AD) + tsu(DB – BCLK)
= (address output delay time) + (data input setup time)

**(b) Vcc = 3V**

- **With the Wait option cleared**

  $ta(A) < 10^9/f(BCLK) - 55(ns)$*

- **With the Wait option selected**

  $ta(A) < m \times 10^9/f(BCLK) - 55(ns)$* (m=2, 3, and 4 when 1wait, 2 waits and 3 waits, respectively)

* 55(ns) = td(BCLK-AD) + tsu(DB – BCLK)
= (address output delay time) + (data input setup time)

**(3) Chip select access time [ta(S)]**

Chip select access time [ta(S)] must satisfy the following conditional expressions:

**(a) Vcc = 5V**

- **With the Wait option cleared**

  $ta(S) < 10^9/f(BCLK) - 35(ns)$*

- **With the Wait option selected**

  $ta(S) < m \times 10^9/f(BCLK) - 35(ns)$* (m=2, 3, and 4 when 1wait, 2 waits and 3 waits, respectively)

* 35(ns) = td(BCLK – CS) + tsu(DB – BCLK)
= (chip select output delay time) + (data input setup time)

**(b) Vcc = 3V**

**• With the Wait option cleared**

ta(S) < $10^9$/f(BCLK) – 55(ns)*

**• With the Wait option selected**

ta(S) < m X$10^9$/f(BCLK) – 55(ns)* (m=2, 3, and 4 when 1wait, 2 waits and 3 waits, respectively)

* 55(ns) = td(BCLK – CS) + tsu(DB – BCLK)
= (chip select output delay time) + (data input setup time)

**(4) Output enable time [ta(OE)]**

Output enable time [ta(OE)] must satisfy the following conditional expressions:

**(a) Vcc = 5V**

**• With the Wait option cleared**

ta(OE) < $10^9$/(f(BCLK) X 2) – 35(ns) = tac1(RD-DB)

**• With the Wait option selected**

ta(OE) < m X $10^9$/(f(BCLK) X 2) – 35(ns) = tac2(RD-DB)
(m=3, 5, and 7 when 1wait, 2 waits and 3 waits, respectively)

**(b) Vcc = 3V**

**• With the Wait option cleared**

ta(OE) < $10^9$/(f(BCLK) X 2) – 42(ns) = tac1(RD-DB)

**• With the Wait option selected**

ta(OE) < m X$10^9$/(f(BCLK) X 2) – 42(ns) = tac2(RD-DB)
(m=3, 5, and 7 when 1wait, 2 waits and 3 waits, respectively)

**(5) Data setup time [tsu(D)]**

Data setup time [tsu(D)] must satisfy the following conditional expressions:

**(a) Vcc = 5V**

**• With the Wait option cleared**

tsu(D) < $10^9$/(f(BCLK)) – 20(ns) = td(DB-WR)

**• With the Wait option selected**

tsu(D) < n X$10^9$/f(BCLK) – 20(ns) = td(DB-WR) (n=number of wait)

**(b) Vcc = 3V**

**• With the Wait option cleared**

tsu(D) < $10^9$/(f(BCLK) – 40(ns) = td(DB-WR)

**• With the Wait option selected**

tsu(D) < n X$10^9$/f(BCLK) – 40(ns) = td(DB-WR) (n=number of wait)

**(6) Write pulse width [tw(W)]**

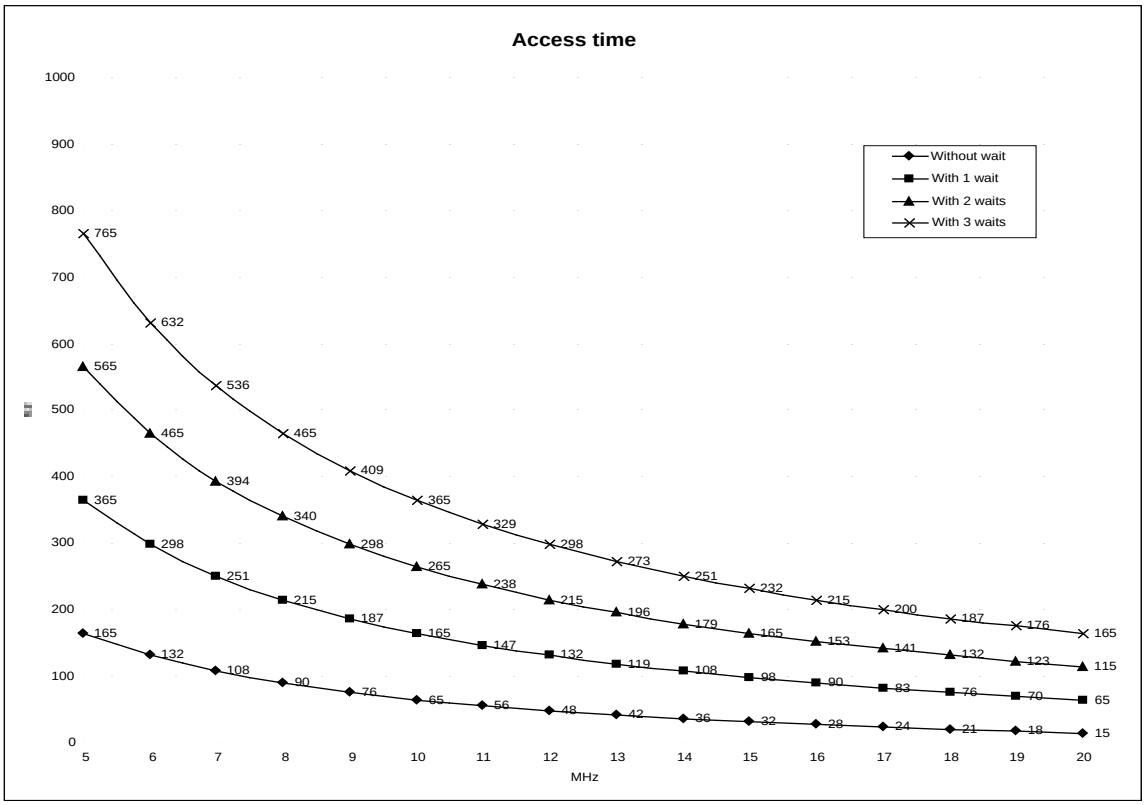
Write pulse width [tw(W)] is as following expressions:

**(a) Vcc = 5V**

tw(W) < n X $10^9$/(f(BCLK) X 2) – 15(ns)
(n=1, 1, 3 and 5 when no wait, 1wait, 2 waits and 3 waits, respectively)

**(b) Vcc = 3V**

tw(W) < n X $10^9$/(f(BCLK) X 2) – 20(ns)
(n=1, 1, 3 and 5 when no wait, 1wait, 2 waits and 3 waits, respectively)



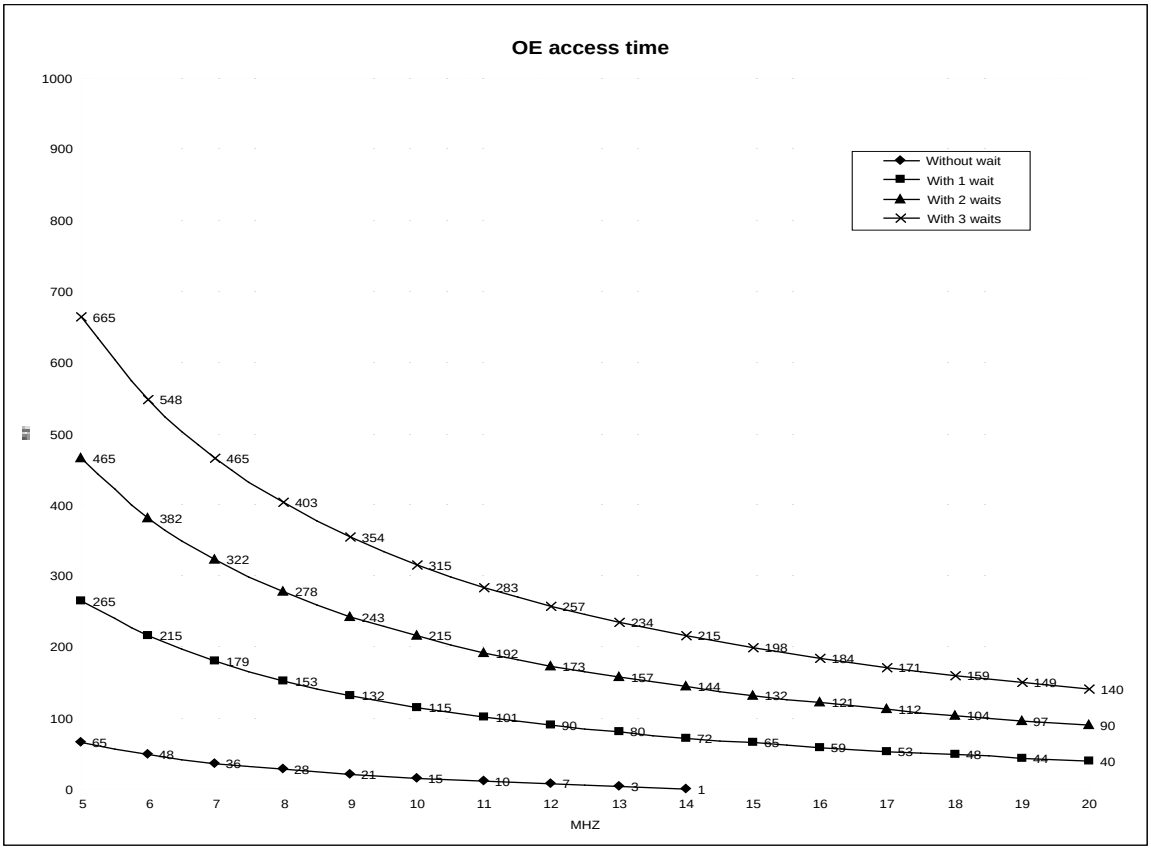
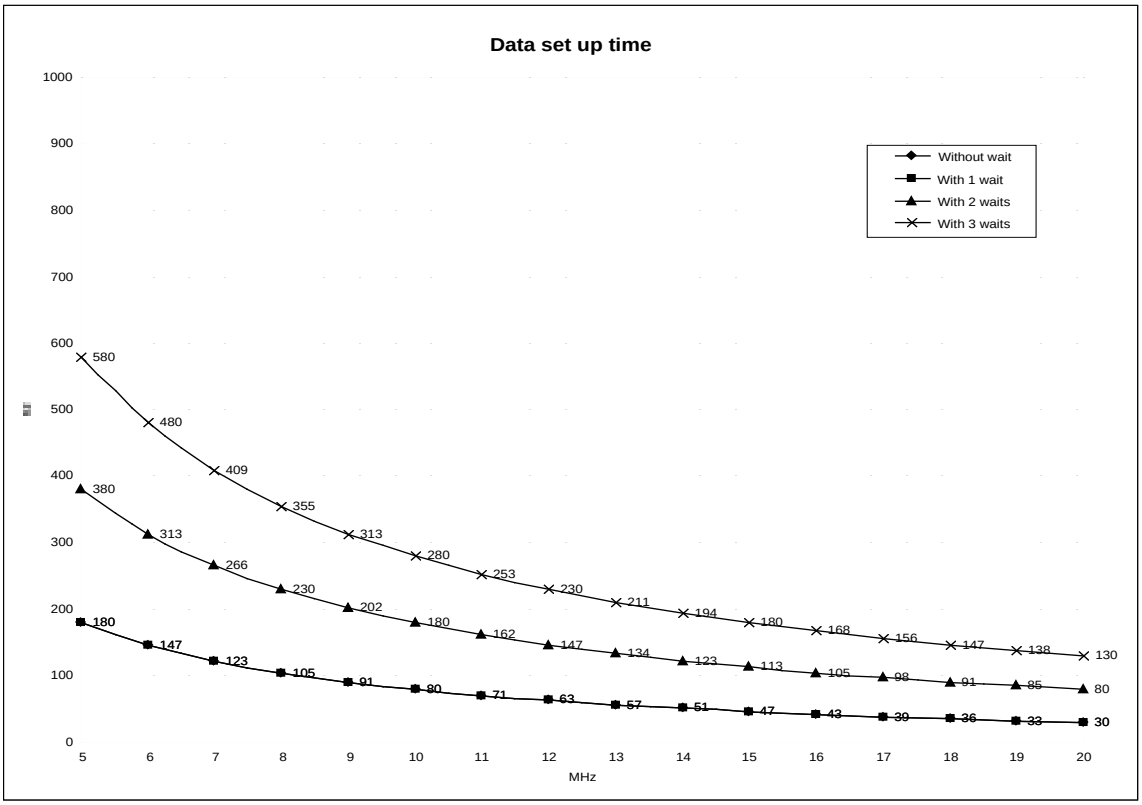




**Figure 3.5.1. Relation between the frequency of BCLK and memory (Vcc = 5V (1))**



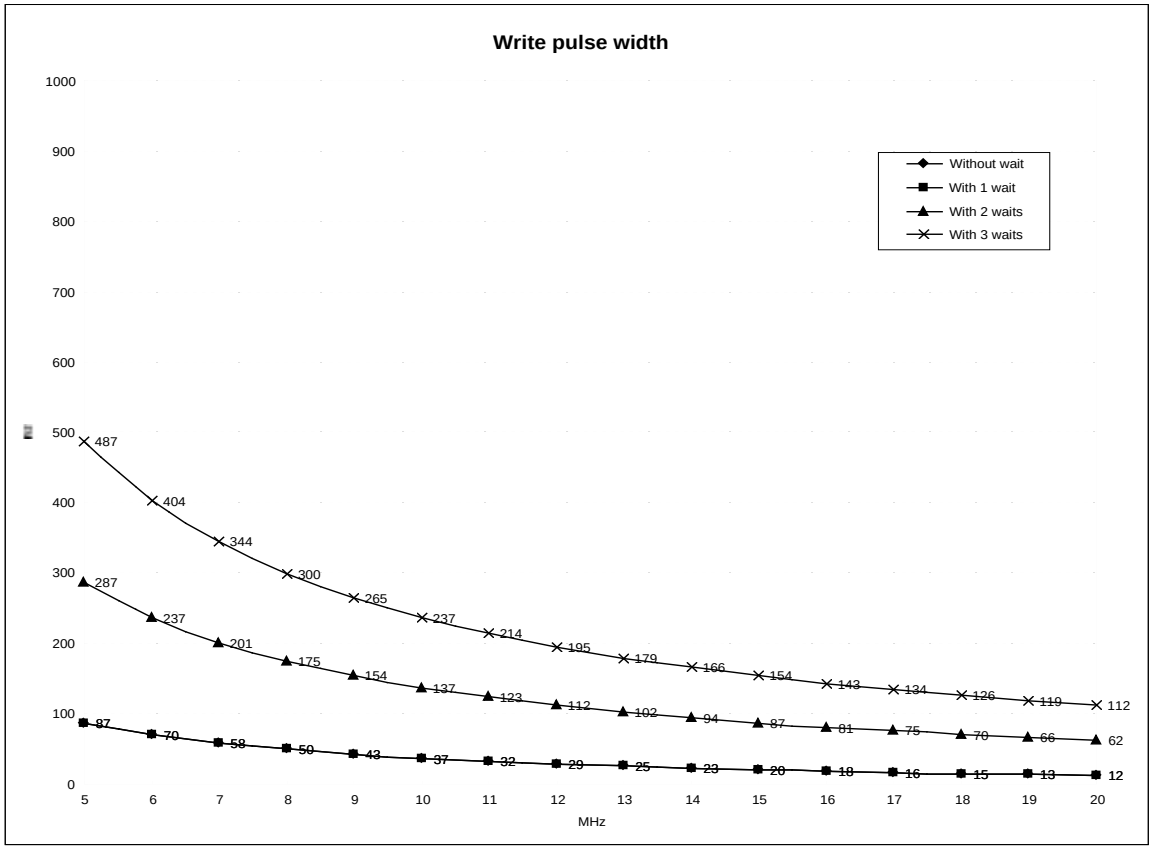




**Figure 3.5.2. Relation between the frequency of BCLK and memory (Vcc = 5V (2))**

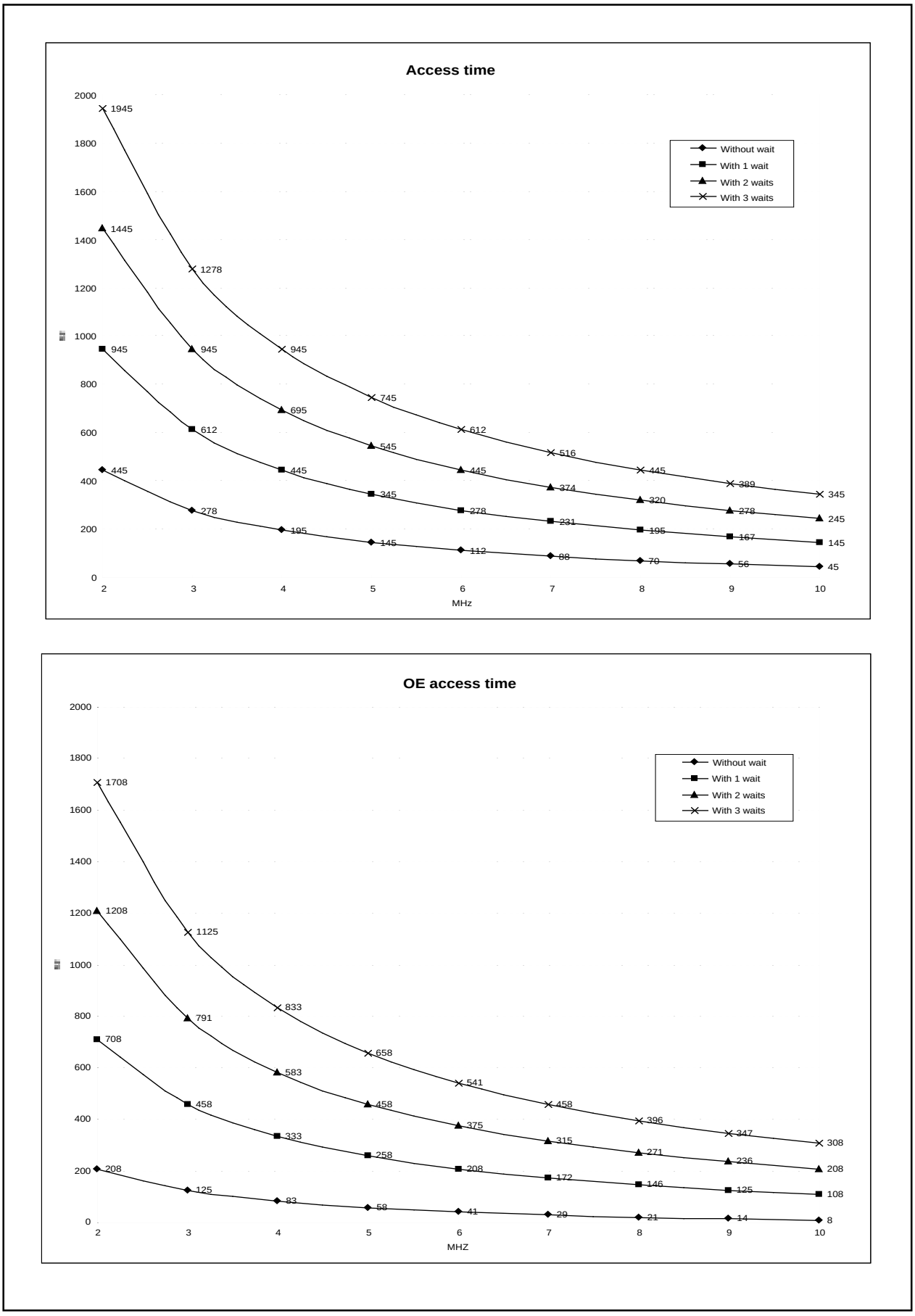
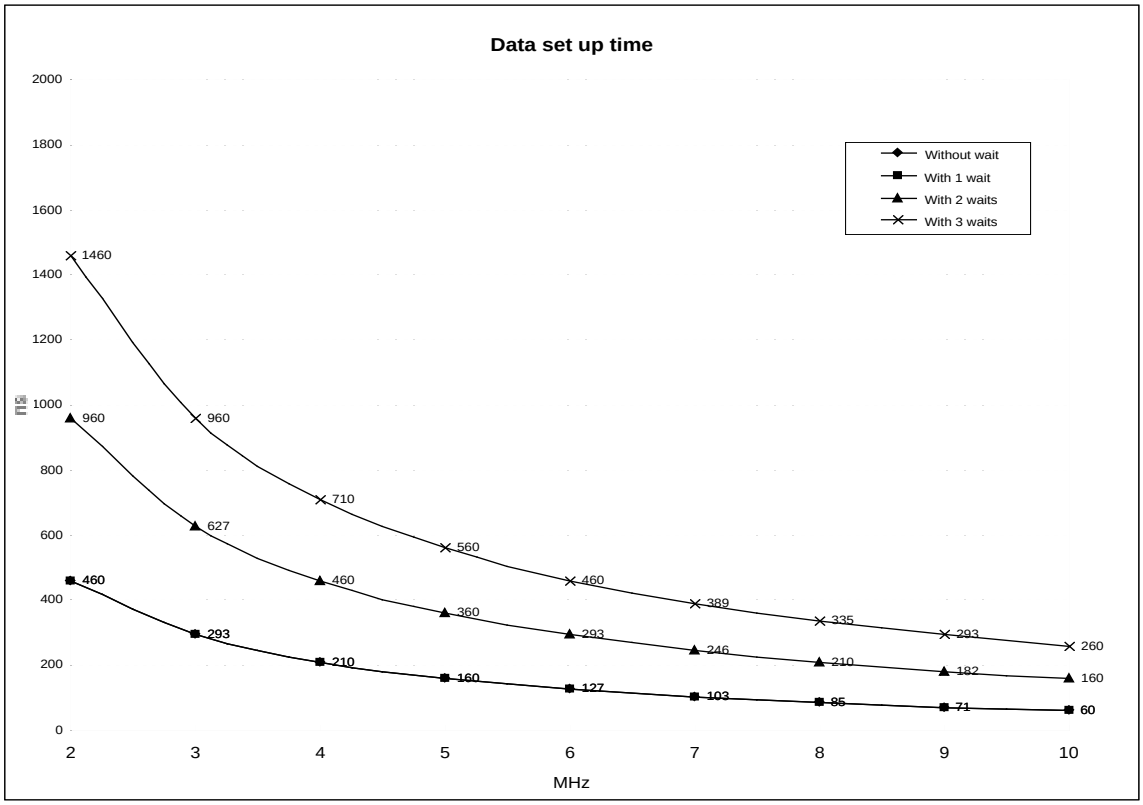



**Figure 3.5.3. Relation between the frequency of BCLK and memory (Vcc = 3V (1))**



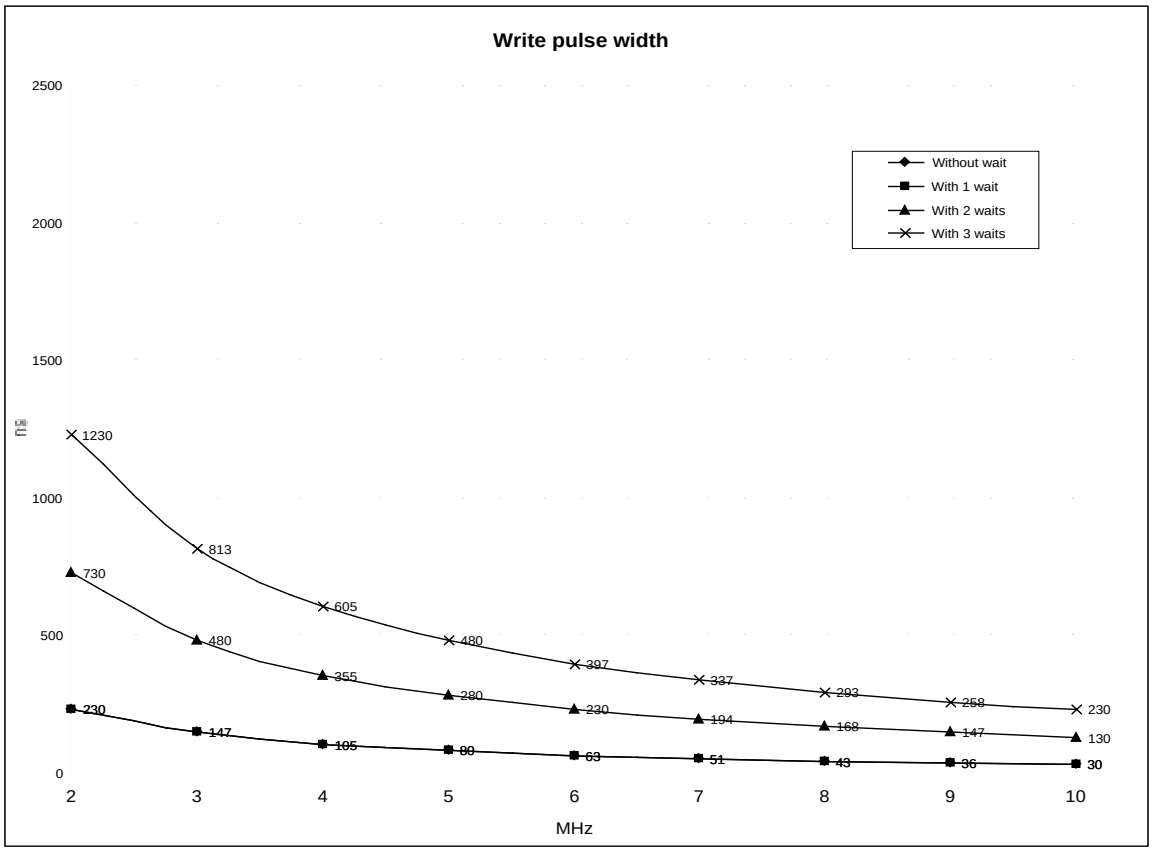




**Figure 3.5.4. Relation between the frequency of BCLK and memory (Vcc = 3V (2))**

### 3.5.2 Connecting Low-Speed Memory

To connect memory with long access time [ta(A)], either decrease the frequency of BCLK or set a software wait. Using the $\overline{RDY}$ feature allows you to connect memory having the timing that precludes connection though you set software wait.

#### (1) Using software wait

Set software wait by using the wait control register (WCR0 to WCR7). With software wait set, if an address space is accessed in which a separate bus is selected, the bus cycle for the external areas results in specified cycles (1 to 4) of the selected BCLK; if an address space in the external areas is accessed in which a multiplex bus is selected, the bus cycle results in three cycles of BCLK regardless of whether "No wait" or "1 wait" is selected.

If bit 2 (PM12) of processor mode register 1 is set to “Wait selected”, the microcomputer accesses the internal RAM and internal ROM with this option in effect. The SFR area is not affected by the setting of the internal memory wait bit and is always accessed in two cycles of BCLK. The number of software wait is set by setting the wait control register (WCR0 to WCR7). Figures 3.5.5 through 3.5.7 show relation of processor mode and the wait bit (PM12, WCRi).

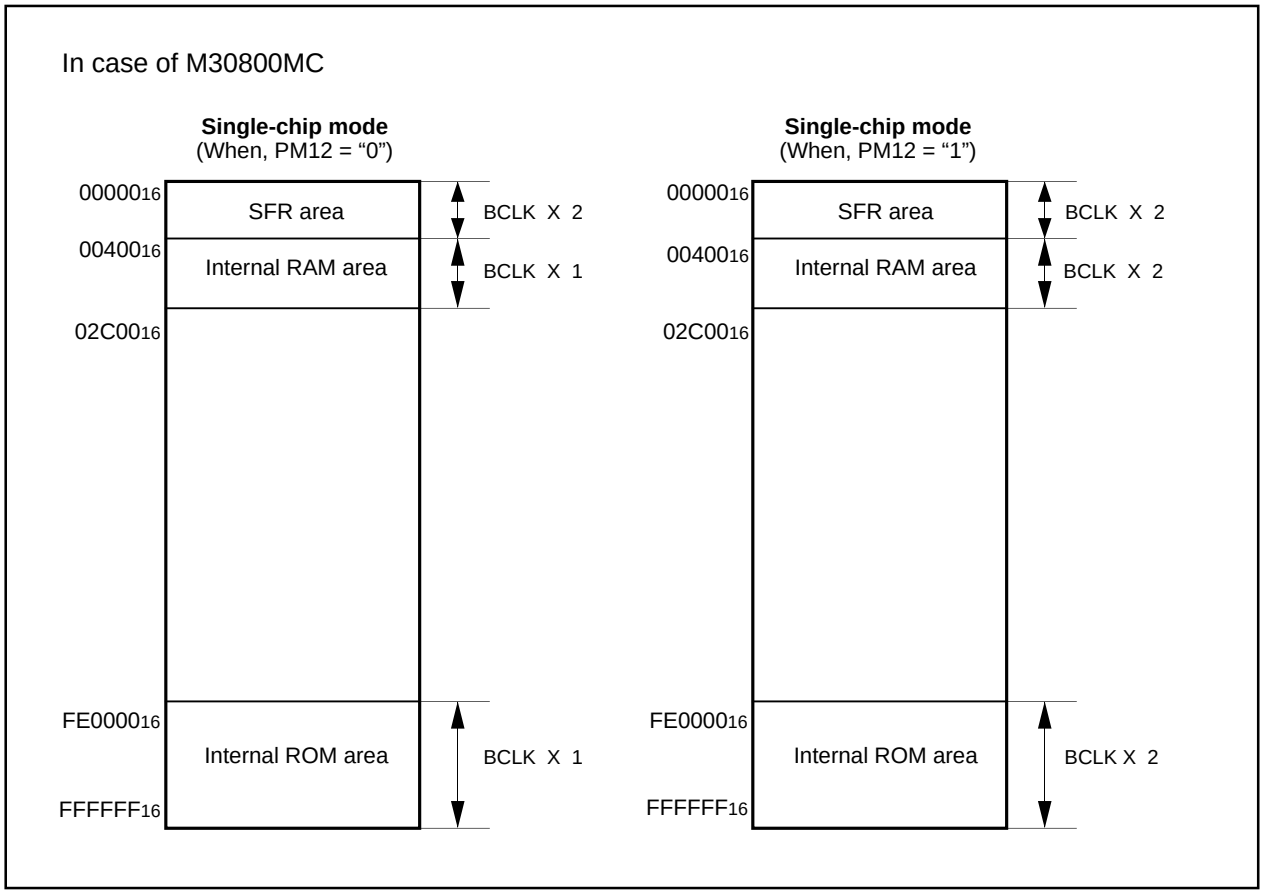
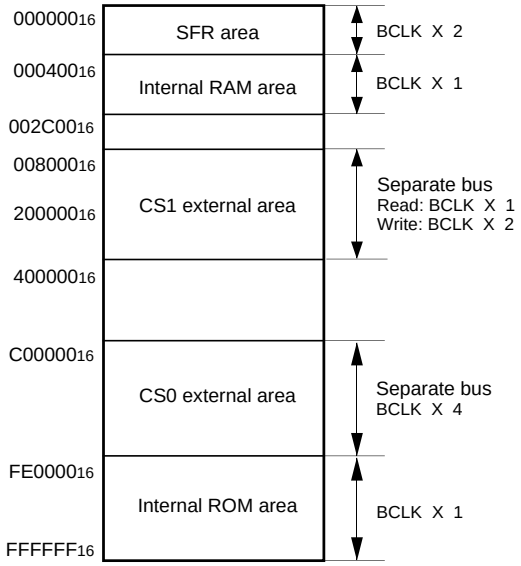



**Figure 3.5.5. Relation of processor mode and the wait bit (PM12, WCRi) (1)**

In case of M30800MC

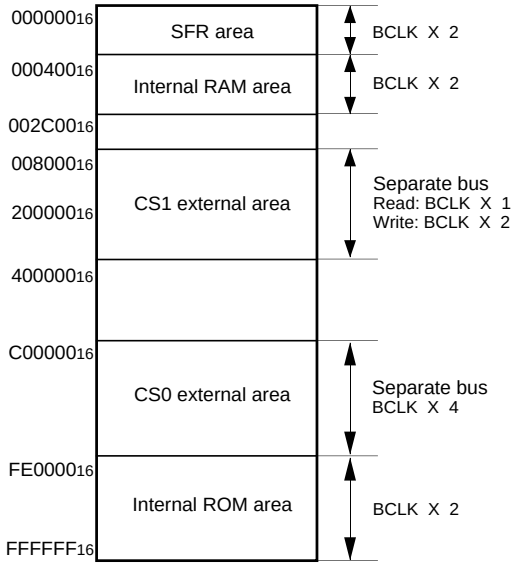
**Memory expansion mode (Mode 2)**

When,
PM12="0"
PM04, PM05="00"
WCR0, WCR1="00"
WCR6, WCR7="11"



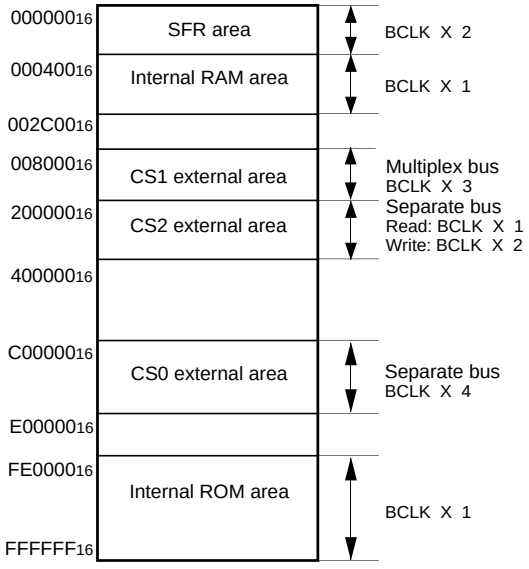

**Memory expansion mode (Mode 2)**

When,
PM12="1"
PM04, PM05="00"
WCR0, WCR1="00"
WCR6, WCR7="11"




**Memory expansion mode (Mode 1)**

When,
PM12="0"
PM04, PM05="10"
WCR0, WCR1="01"
WCR2, WCR3="00"
WCR6, WCR7="11"




**Memory expansion mode (Mode 3)**

When,
PM12="1"
PM04, PM05="01"
WCR0, WCR1="00"
WCR2, WCR3="10"
WCR4, WCR5="11"
WCR6, WCR7="10"

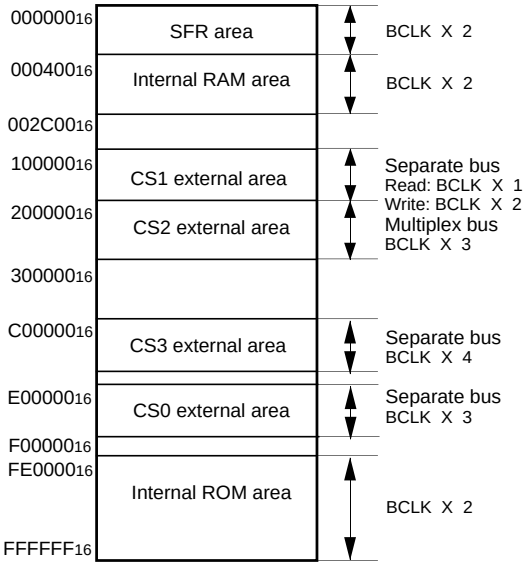



**Figure 3.5.6. Relation of processor mode and the wait bit (PM12, WCRi) (2)**

In case of M30800MA

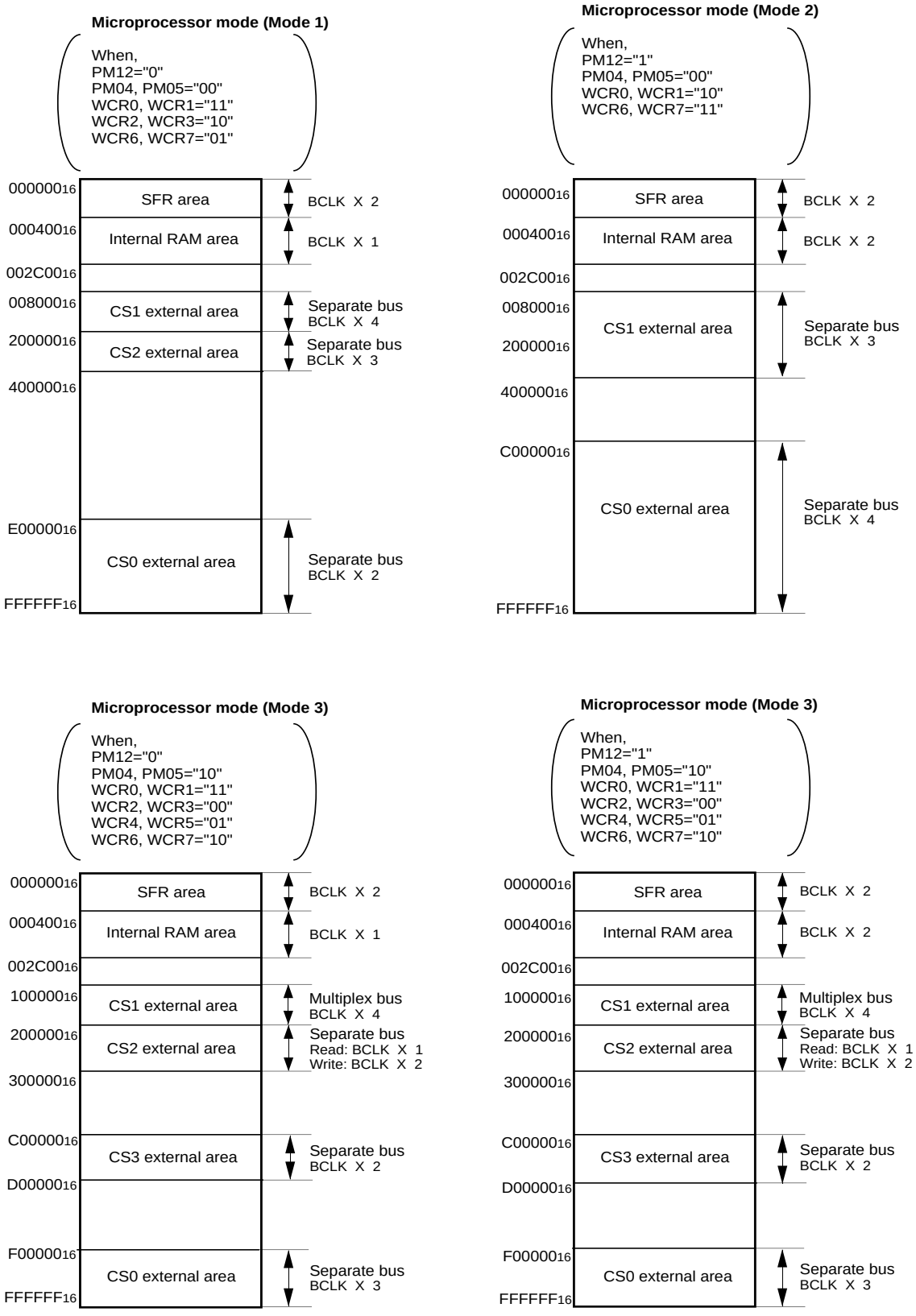


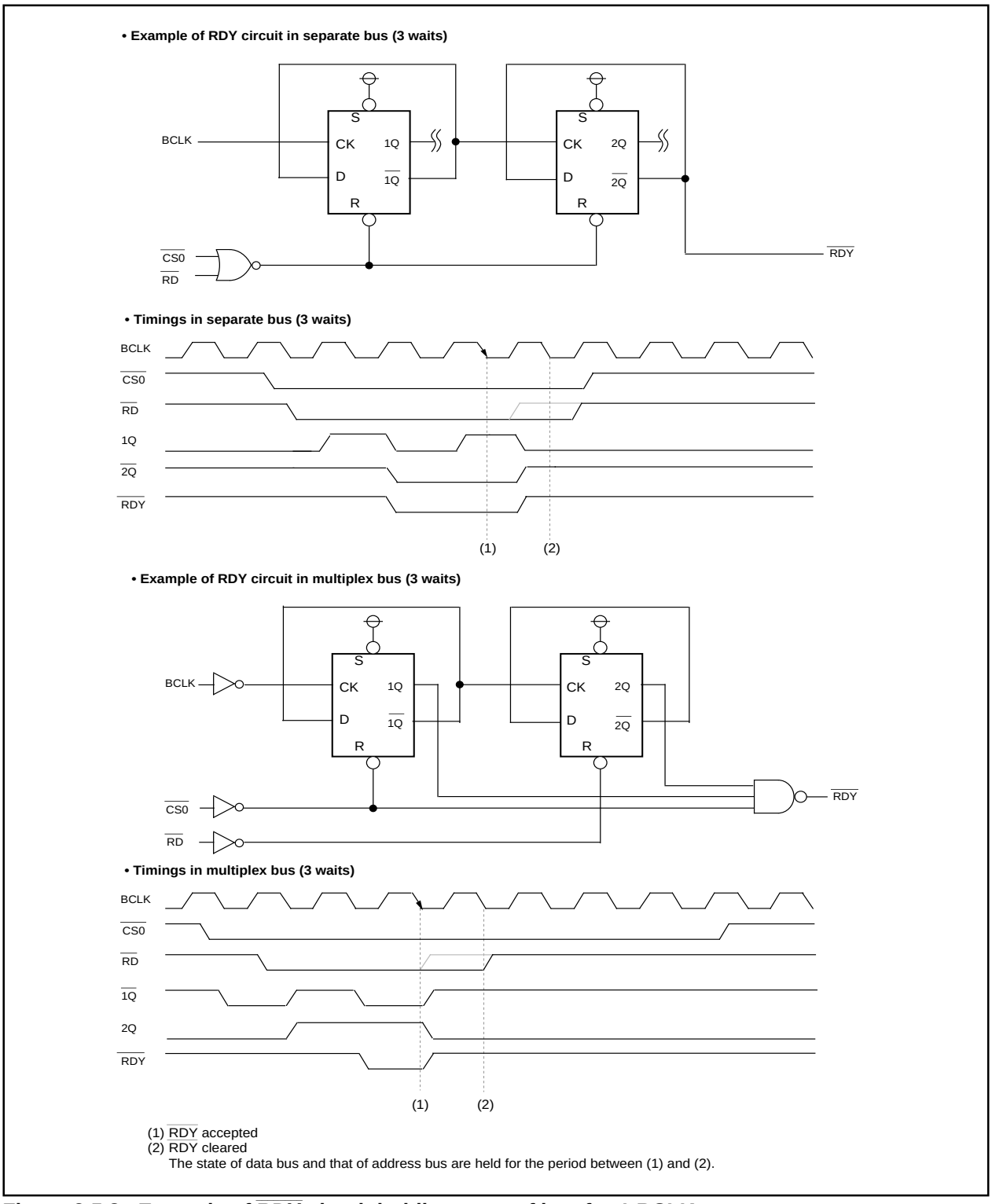

**Figure 3.5.7. Relation of processor mode and the wait bit (PM12, WCRi) (3)**

### (2) $\overline{\text{RDY}}$ function usage

To use the $\overline{\text{RDY}}$ function, set a software wait.

The $\overline{\text{RDY}}$ function operates when the BCLK signal falls with the $\overline{\text{RDY}}$ pin at “L”; the bus does not vary for 1 BCLK, and the state at that moment is held.

The $\overline{\text{RDY}}$ function holds the state of bus for the period in which the $\overline{\text{RDY}}$ pin is at “L”, and releases it when the BCLK signal falls with the $\overline{\text{RDY}}$ pin at “H”. Figure 3.5.8 shows an example of $\overline{\text{RDY}}$ circuit that holds the state of bus for 1 BCLK.




(1) $\overline{\text{RDY}}$ accepted
(2) RDY cleared
The state of data bus and that of address bus are held for the period between (1) and (2).

**Figure 3.5.8. Example of $\overline{\text{RDY}}$ circuit holding state of bus for 1 BCLK**

### 3.5.3 Connectable Memories

Connectable memories and their maximum frequencies are given here;
M16C/80 group maximum frequency is
20MHz(without the wait) for Vcc=5V,
10MHz(with the one wait) for Vcc=3V

**(1) Flash memories(Read only mode)**

(a) 3V without wait

| Maximum frequency (MHz)) | Model No. |
|---|---|
| 5.88 | M5M29GB/T160BVP-80 |

(b) 3V with 1 wait

| Maximum frequency (MHz)) | Model No. |
|---|---|
| 10.00 | M5M29GB/T160BVP-80 |

**(2) SRAM**

(a) 3V without wait

| Maximum frequency (MHz) | Model No. |
|---|---|
| 8.06 | M5M54R08AJ-15<br>M5M54R16AJ-15 |
| 8.19 | M5M54R08AJ-12<br>M5M54R16AJ-12 |
| 8.33 | M5M54R08AJ-10<br>M5M54R16AJ-150 |

(b) 3V with 1 wait

| Maximum frequency (MHz) | Model No. | |
|---|---|---|
| 10.00 | M5M54R08AJ-15<br>M5M54R08AJ-12<br>M5M54R08AJ-10 | M5M54R16AJ-15<br>M5M54R16AJ-12<br>M5M54R16AJ-150 |

**(3) DRAM**

(a) 3V with 1 wait

| Maximum frequency (MHz) | Model No. | |
|---|---|---|
| 7.14 | M5M465800DJ,DTP-6,6S<br>M5M467800DJ,DTP-6,6S<br>M5M465160DJ,DTP-6,6S | M5M465805DJ,DTP-6,6S<br>M5M467805DJ,DTP-6,6S<br>M5M465165DJ,DTP-6,6S |
| 7.35 | M5M465800DJ,DTP-5,5S<br>M5M467800DJ,DTP-5,5S<br>M5M465160DJ,DTP-5,5S | M5M465805DJ,DTP-5,5S<br>M5M467805DJ,DTP-5,5S<br>M5M465165DJ,DTP-5,5S |

(b) 3V with 2 waits

| Maximum frequency (MHz) | Model No. | |
|---|---|---|
| 10.00 | M5M465800DJ,DTP-6,6S<br>M5M467800DJ,DTP-6,6S<br>M5M465160DJ,DTP-6,6S<br>M5M465800DJ,DTP-5,5S<br>M5M467800DJ,DTP-5,5S<br>M5M465160DJ,DTP-5,5S | M5M465805DJ,DTP-6,6S<br>M5M467805DJ,DTP-6,6S<br>M5M465165DJ,DTP-6,6S<br>M5M465805DJ,DTP-5,5S<br>M5M467805DJ,DTP-5,5S<br>M5M465165DJ,DTP-5,5S |

## 3.6 Releasing an External Bus ($\overline{\text{HOLD}}$ input and $\overline{\text{HLDA}}$ output)

The Hold feature is to relinquish the address bus, the data bus, and the control bus on M16C/80 side in line with the Hold request from the bus master other than M16C/80 when the two or more bus masters share the address bus, the data bus, and the control bus. The Hold feature is effective only in memory expansion mode and microprocessor mode.

The sequence of using the Hold feature may be:

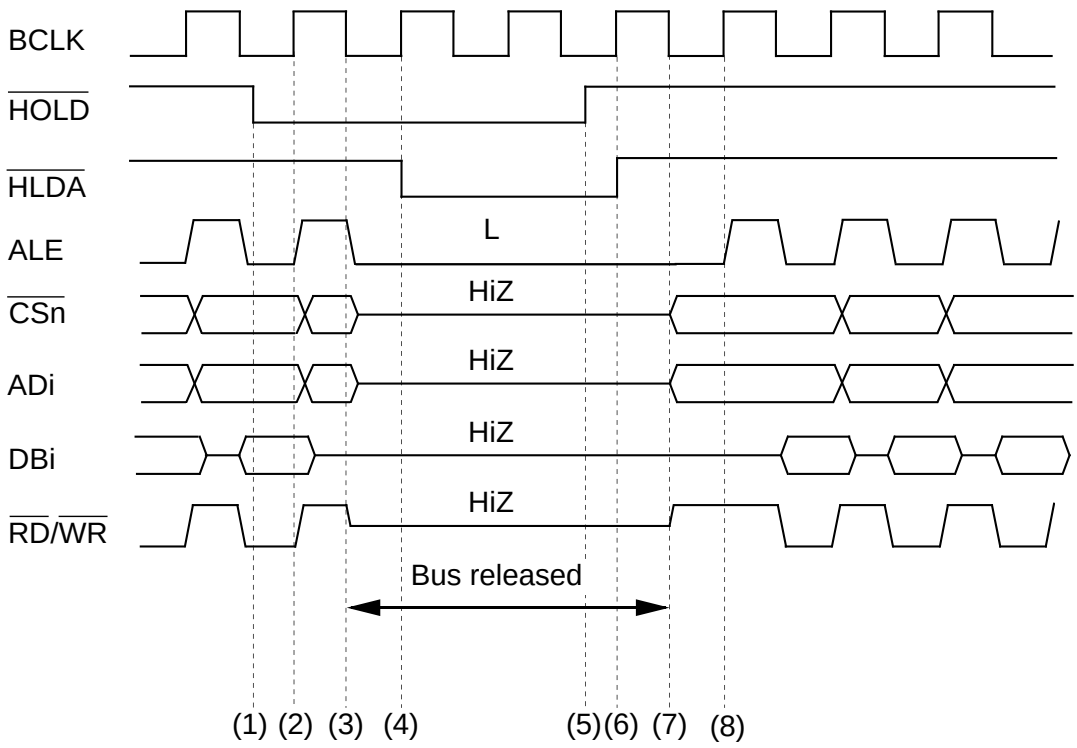
1. The external bus master turns the input level of the $\overline{\text{HOLD}}$ terminal to “L”.
2. When M16C/80 becomes ready to relinquish buses, each bus becomes high-impedance state at the falling edge of BCLK.
3. The output from $\overline{\text{HLDA}}$ terminal becomes “L” at the rising edge of the next BCLK.
4. The external bus master uses a bus.
5. When the external bus master finishes using a bus, the external bus master returns the input level of the $\overline{\text{HOLD}}$ terminal to “H”.
6. The output from $\overline{\text{HLDA}}$ terminal becomes “H” at the rising edge of the next BCLK.
7. Each bus returns from the high-impedance state to the former state at the falling edge of the next BCLK.

As given above, each bus invariably gets in the high-impedance state while the $\overline{\text{HLDA}}$ output is “L”. Also, M16C/80 doesn't relinquish buses during a bus cycle. That is, if a Hold request comes in during a bus cycle, the $\overline{\text{HLDA}}$ output become “L” after that bus cycle finishes.

In the Hold state, the state of each terminal becomes as follows.

- **Address bus $A_0$ to $A_{22}$, $\overline{A_{23}}$**
  High-impedance state. In the case $A_{16}$ to $A_{19}$ are used as ports $P4_0$ to $P4_3$ (multiplex for the whole area), the microcomputer maintains the status when hold signal is received.
- **Data bus $D_0$ to $D_{15}$**
  High-impedance state. In the case $D_8$ to $D_{15}$ are used as ports $P1_0$ to $P1_7$ (8-bit bus width for the whole external area) and $D_0$ to $D_{15}$ are used as ports $P0_0$ to $P0_7$ and $P1_0$ to $P1_7$ (multiplex for the whole area), the microcomputer maintains the status when hold signal is received.
- **$\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{WRL}}$, $\overline{\text{WRH}}$, $\overline{\text{BHE}}$**
  High-impedance state.
- **ALE**
  "L" level.
- **$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$**
  High-impedance state.

Figure. 3.6.1 shows an example of relinquishing external buses.




(1) An “L” level is input to the $\overline{\text{HOLD}}$ pin.
(2) $\overline{\text{HOLD}}$ is detected.
(3) The CPU releases the bus.
(4) An “L” is output to the $\overline{\text{HLDA}}$ pin.
(5) An “H” is input to the $\overline{\text{HOLD}}$ pin.
(6) An “H” is output to the $\overline{\text{HLDA}}$ pin.
(7) The CPU not releases the bus.
(8) The CPU resumes using the bus.

**Figure 3.6.1. Example of releasing the external bus**

## 4. Reference

Data Sheet
M16C/80 group data sheet Rev.E3
(Use the latest version on the Home page: http://www.renesas.com/)

User's Manual
M16C/80 group user's manual Rev.B
(Use the latest version on the Home page: http://www.renesas.com/)

## 5. Web-site and contact for support

Renesas Technology Corporation Semiconductor Home page
http://www.renesas.com/

E-mail Support
E-mail: support_apl@renesas.com

## REVISION HISTORY

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jan 16, 2004 | - | First edition issued |

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