Application Note

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture

AN-PM-079

Abstract

This applications note presents an example of a power architecture design for Ultrabook/Notebook applications operated from a dual cell (2S) stacked Li-ion or Li-polymer battery pack using Dialog Semiconductor's DA9313 converter and DA9063 power management IC.

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1 Terms and Definitions

BOM	Bill of Materials
DPWROK	Delayed Power OK
EC	Embedded Controller
HV	High Voltage
IC	Integrated Circuit
LV	Low Voltage
NVDC	Narrow Voltage DC/DC
MCP	Media Communication Processor
PCB	Printed Circuit Board
PCH	Platform Controller Hub
PFM	Pulse Frequency Modulation
PG	Power Good
PMIC	Power Management IC
PVC	Power Voltage Converter
ROP	Rest of Platform

2 References

[1] DA9313-Datasheet, Dialog Semiconductor

[2] DA9063-Datasheet, Dialog Semiconductor

3 Introduction

The purpose of this application note is to provide an example power architecture design for Ultrabook/Notebook (using Intel®'s Core™ and Xeon® (formerly Skylake (SKL)), Kaby Lake (KNL) or Cannonlake (CNL) processors) applications.

Dialog Semiconductor's DA9313 converter can be used to provide the system bus voltage from a dual cell (2S) stacked Li-ion or Li-polymer battery pack (5.4 V to 8.7 V). Additionally, Dialog Semiconductor's DA9063 LV PMIC can be used to power up the power rails of the rest of platform (ROP), see Figure 1.

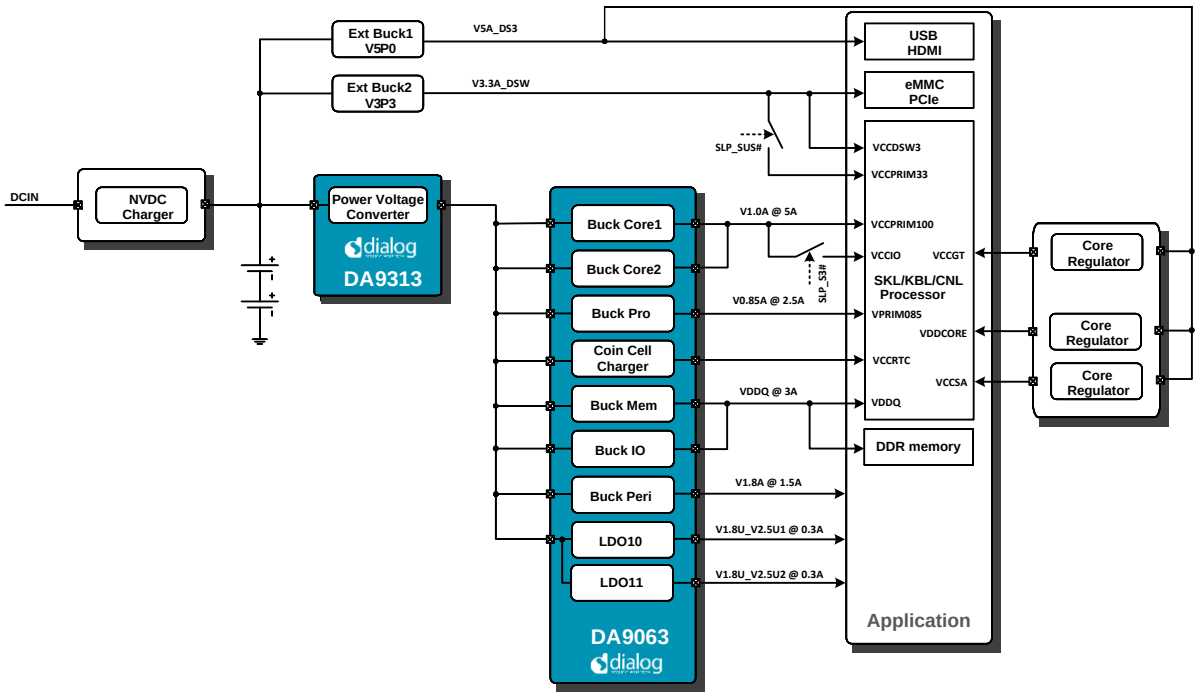


Figure 1: Power Architecture Block Diagram

NOTE
This example power architecture includes a narrow voltage DC/DC (NVDC) charger, two external buck regulators (Ext Buck1 and Ext Buck2) and some IMVP8™ core regulators available from third parties. Their operation is not described in this document.

4 ROP Support

This section describes how to combine and connect Dialog's DA9313 converter and DA9063 PMIC to support the Intel requirements for the ROP in a typical application.

Figure 2 shows how to connect some of the most relevant signals on the platform. The red arrows indicate power rails.

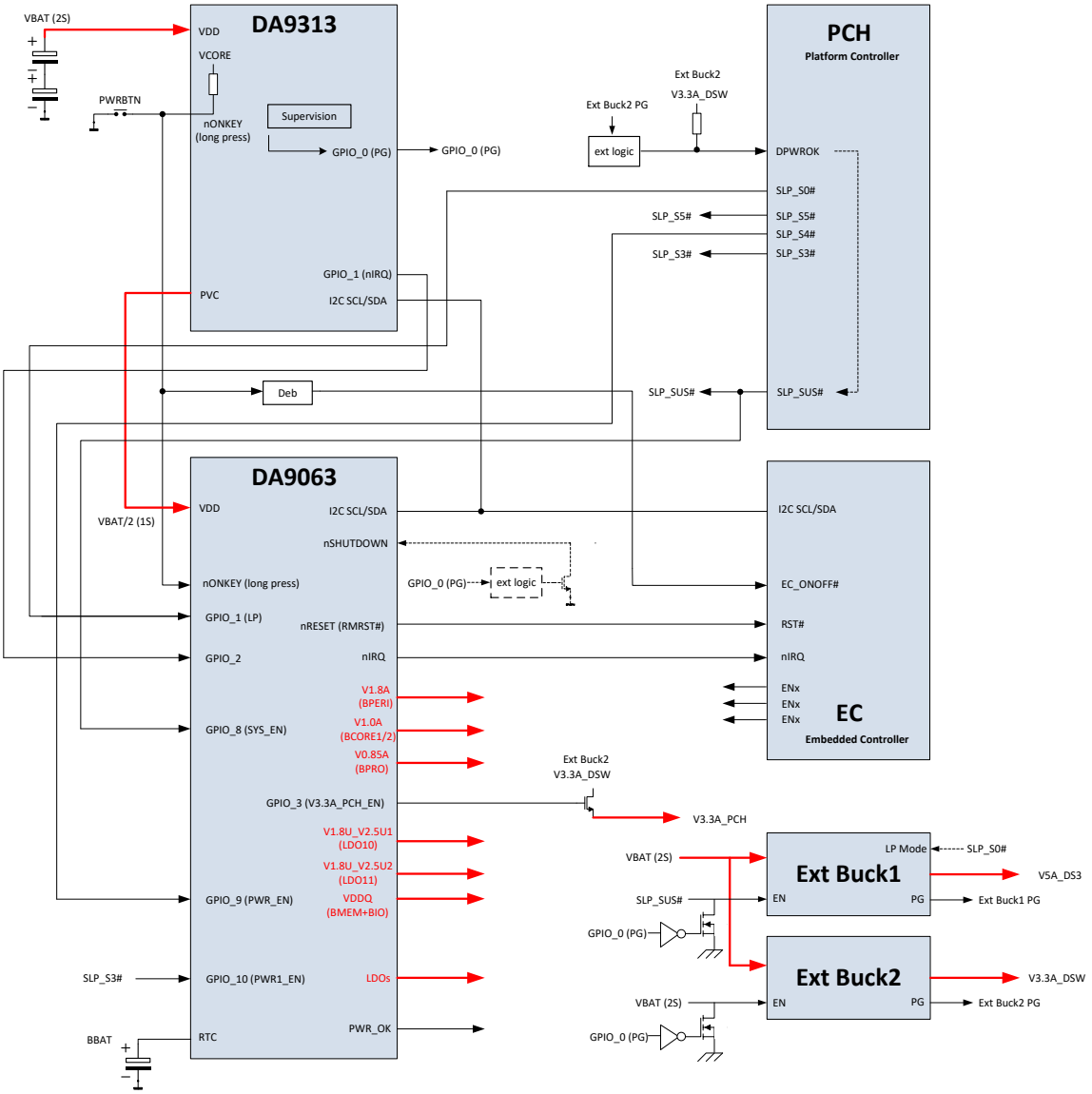


Figure 2: Main Signals Between DA9313, DA9063, PCH and EC

4.1 Power Distribution

A dual stacked Li-ion battery or an NVDC charger can fully power the system. Alternatively, the system can be powered using a combination of both. Therefore the actual input voltage of the system can vary between 6 V and 8.4 V.

To comply with the maximum supply voltage for the DA9063 (5.5 V), the system input voltage is halved by the DA9313 power voltage converter (PVC). The PVC rail is enabled in DA9313 by configuring PVC_EN = 1 and AUTOBOOT = 1. The PVC rail will remain enabled providing the input

voltage is higher than the configurable under-voltage lockout (UVLO) threshold ($V_{BAT\_UV\_CRIT}$ setting) of DA9313. To reduce the power dissipation, the automatic frequency mode of the DA9313 PVC should be configured by setting PVC_MODE = 1.

The DA9063 has AUTOBOOT = 1, therefore the DA9063 will initiate a power-up sequence as soon as the DA9313 PVC rail is up.

4.2 Rail Control

4.2.1 Platform Controller Supply

The platform controller hub (PCH) is supplied by the (always on) V3.3_DSW rail, except when fault conditions occur and a power cycle is needed. V3.3_DSW is enabled when the battery is present and disabled when the DA9313 power good (PG) is de-asserted. This rail is supported by an external buck regulator called Ext Buck2.

The output voltage is monitored and combined with the necessary signals, including the PG of the DA9313, to output the delayed power good signal (DPWROK) to the PCH.

4.2.2 S4/S5 Power States

After the assertion of SLP_SUS# from the PCH, the S4 (Suspend to Disk) or S5 (Soft Off) state is entered.

SLP_SUS# is connected to the enable pin of Ext Buck1, which is configured as V5A_DS3. The main purpose of Ext Buck1 is to supply the IMVP8 core regulators.As a result, V5A_DS3 is turned on as soon as the SLP_SUS# is asserted.

NOTE
Ext Buck1 can be disabled when the DA9313 PG is de-asserted. The SLP_SUS# port is also connected to GPIO_8 (SYS_EN) on DA9063. This starts a power-up sequence which ends on completion of domain SYSTEM (SYSTEM_END slot) in DA9063. Rails can be individually assigned to a dedicated slot of the sequencer, as shown in Figure 3.

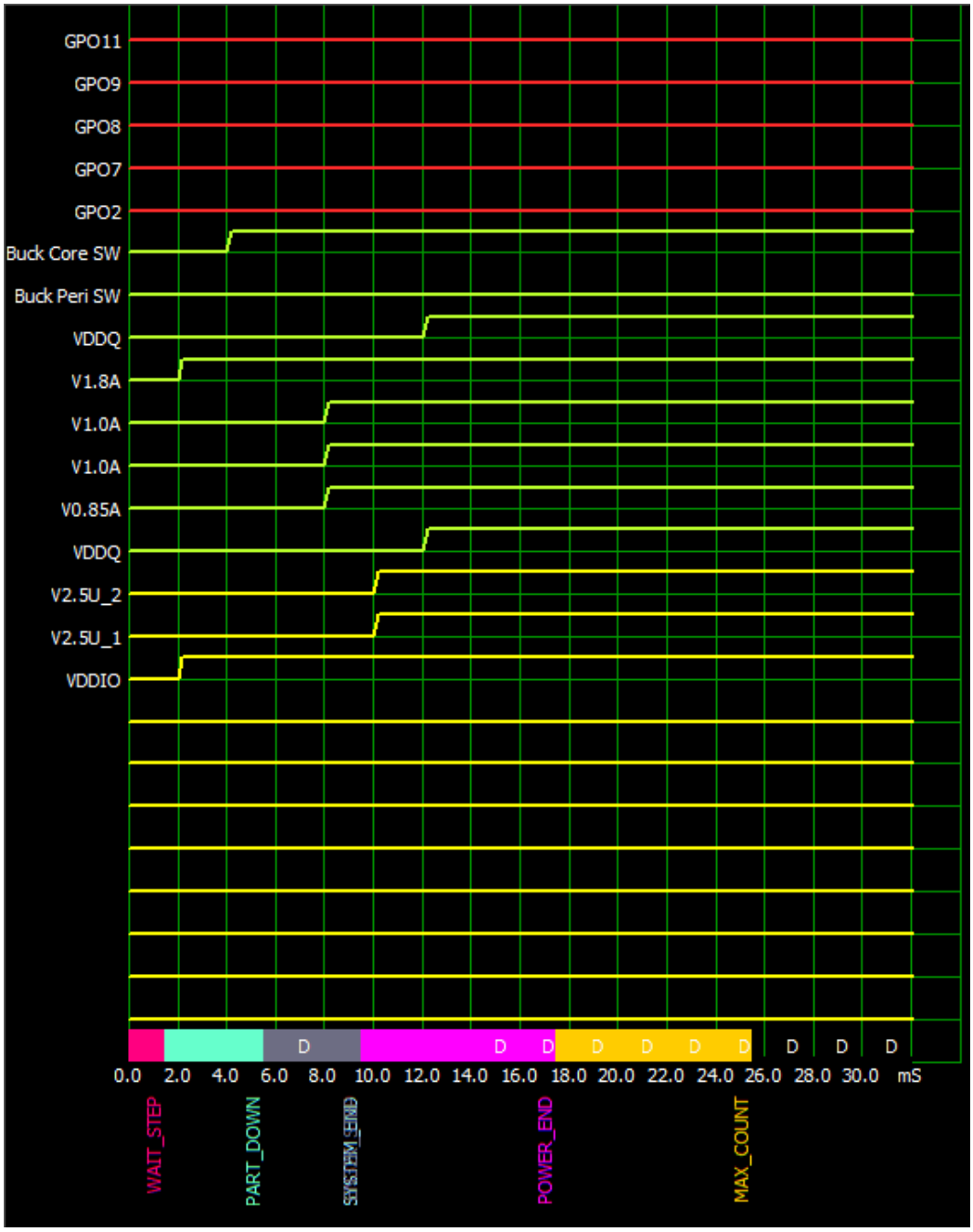


Figure 3: DA9063 Sequencer

To fulfil the start-up requirements for ROP, the V1.8A rail is assigned to slot 1, the V3.3A_PCH_EN is assigned to slot 2 (shown as Buck Core SW in Figure 3), a delay slot is assigned to slot 3 and the V1.0A rail is assigned to slot 4 (possibly together with V0.85V when the rail is present).

GPIO_3 of DA9063 is used as a sequence controlled output port (called CORE_SWG), to enable an external FET for the generation of the V3.3A_PCH rail. This is easily implemented via the rail switch implementation of DA9063.

At the end of the domain SYSTEM the nRESET port of DA9063 is released as needed for RSMRST#.

Table 1: RESET (0x99)

Bit	Type	Label	Default	Description
7:6	R/W	RESET_EVENT	01	RESET timer started by 00: EXT_WAKEUP 01: SYS_UP 10: PWR_UP 11: leaving PMIC RESET state (do not use in combination with nRES_MODE = 1)
5:0	R/W	RESET_TIMER	000101	000000: 0.000 ms 000001: 1.024 ms 000010: 2.048 ms 000011: 3.072 ms 000100: 4.096 ms 000101: 5.120 ms …. 011110: 30.720 ms 011111: 31.744 ms 100000: 32.768 ms 100001: 65.536 ms 100010: 98.304 ms ….. 111101: 983.040 ms 111110: 1015.808 ms 111111: 1048.576 ms

4.2.3 S0 Power State

The transition from S4/S5 to S0 (Working) state is driven by the PCH through SLP_S3#, SLP_S4# and SLP_S5#.

SLP_S4# is connected to GPIO_9 (PWR_EN) on DA9063. This continues the power-up sequencing up to POWER_END, as shown in Figure 3. V1.8U_V2.5U1 and V1.8U_V2.5U2 are assigned to slot 5; VDDQ is assigned to slot 6.

SLP_S3# is connected to GPIO_10 (PWR1_EN) on DA9063. This can be used to enable other LDOs on DA9063 after having assigned them to a sequencer slot.

SLP_S5# is generally used to shut power off to all non-critical systems when in the S5 (Soft Off) states. Though in this example power architecture, SLP_S5# is not used by the DA9313 or the DA9063.

4.3 Low Power Mode

SLP_S0# is a platform level low power mode indicator that is set low to send the system into connected standby mode.

To save power, connect SLP_S0# to Ext Buck1 (V5A) LP mode. This sets Ext Buck1 into pulse frequency modulation (PFM) mode. If this connection is not possible the operating mode should be configured by I^2C.

DA9063 GPIO_1 is also connected to SLP_S0# and controls the operation of V1.0A and VDDQ. The B-registers are selected depending on the GPIO_1 level (active high for normal operation and active low for standby).

The LP voltage of the regulators can be configured in VBCORE1_B and VBMEM_B, whilst the operation is set to PFM mode if BCORE1_SL_B = 1, BMEM_SL_B = 1 and BCORE1_MODE = 00, BMEM_MODE_ 00.

Table 2: BMEM_CONF (0xA1)

Bit	Type	Label	Default	Description
7:6	R/W	BMEM_ MODE	00	00: Sleep/Synchronous mode controlled via voltage A and B registers 01: BUCKMEM always operates in Sleep Mode 10: BUCKMEM always operates in Synchronous Mode 11: BUCKMEM operates in Automatic Mode

Table 3: VBMEM_B (0xB7)

Bit	Type	Label	Default	Description
7	R/W	BMEM_SL_B	1	0: Configures BUCKMEM to Synchronous mode, when selecting B voltage settings 1: Configures BUCKMEM to Sleep mode, when selecting B voltage settings

4.4 I²C Interface

The embedded controller (EC) can communicate via I²C with DA9313 and DA9063. The lines are pulled up to the 3.3 V rail generated from the always on V3.3A_DSW.

4.5 nIRQ

DA9313 GPIO_1 is configured as nIRQ and is connected to DA9063 GPIO_2, (configured as input). Therefore, any DA9313 interrupt is directly passed to the EC via the DA9063 nIRQ pin.

4.6 Power Button

The power button (PWRBTN) connects to DA9313 and DA9063 and has an internal pull-up to VCORE.

For both devices only the long press functionality for emergency reset is used. This is enabled when the press time is longer than KEY_DELAY + SHUT_DELAY. The system is power cycled and both devices are reset.

After a long nONKEY press, DA9313 and DA9063 will initially only assert control bit E_KEY_RESET in the fault register and signal a non-maskable interrupt allowing the host to clear the armed reset sequence within 1 s. If the host does not clear E_KEY_RESET a power cycle is initiated.

The short press detection is managed by the EC and the PCH. A debounced version of the signal is needed. This function must be implemented externally using an additional circuit.

NOTE
In SHELF mode (that is DA9313 POWER-DOWN state), the whole supply chain is unpowered therefore no nONKEY can be captured by the DA9063. In this case, a special feature is available in the DA9313 that automatically pulls down the nONKEY briefly to allow the DA9063 to wake up. The nONKEY is de-asserted after a small delay.

4.6.1 Short Press

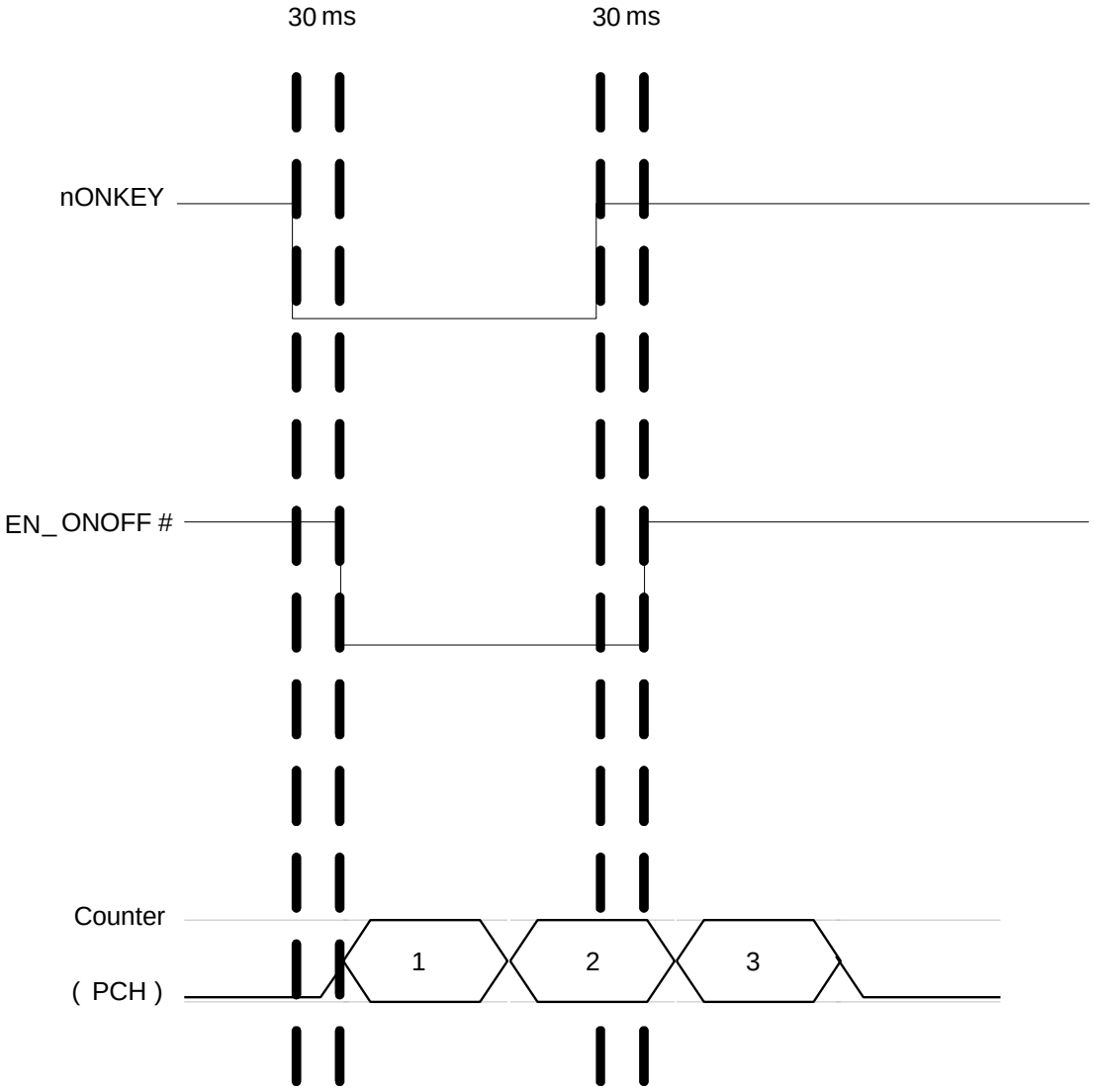


Figure 4: Short Press Timing

4.6.1.1 Short Press Operation Signal Description

- The nONKEY press is debounced by an external circuitry.
- The EC communicates to the PCH which initiates a counter.
- If the counter elapses before 5 s, the PCH knows it is a short press.

4.6.2 Long Press (Cold Off)

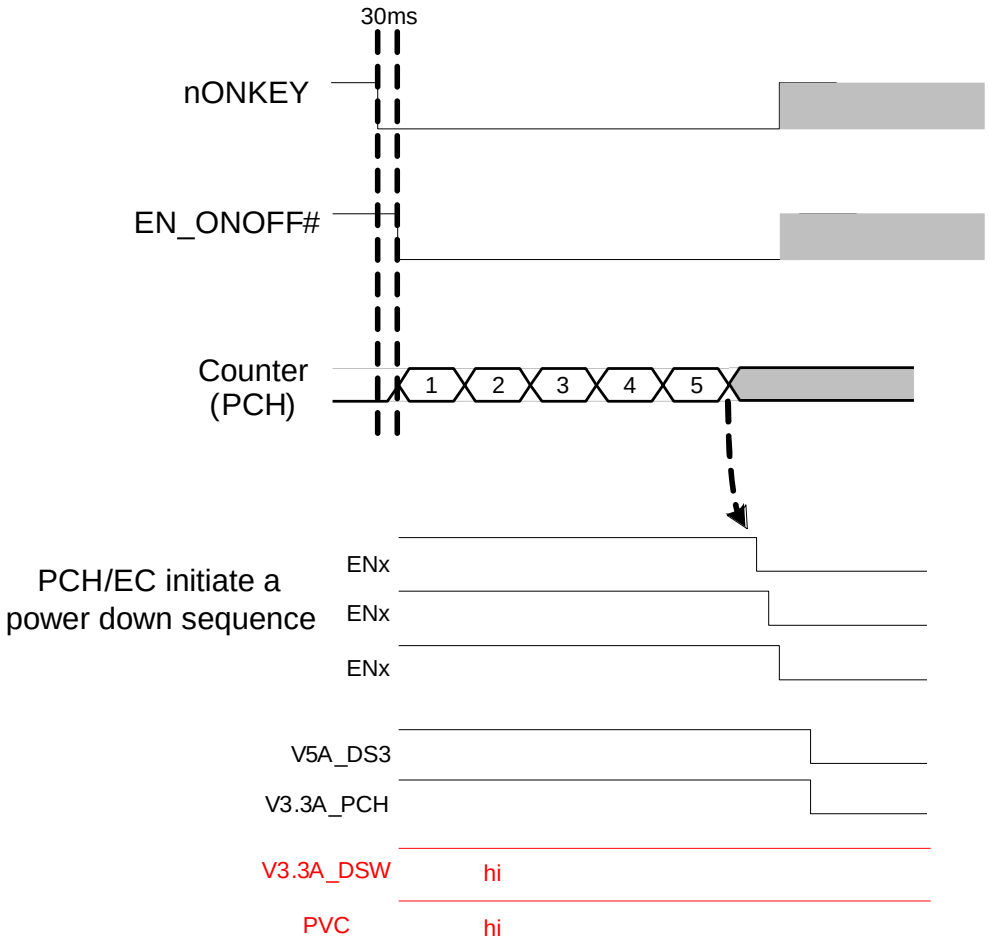


Figure 5: Long Press (Cold Off) Timing

4.6.2.1 Long Press (Cold Off) Operation Signal Sequence

- The nONKEY press is debounced by an external device.
- The EC communicates to the PCH which initiates a counter.
- The counter reaches 5 s so the PCH knows it is a long press.
- The PCH initiates a cold off sequence.
- All rails are shut down, except the V3.3A_DSW from Ext Buck2 and the PVC.
- The PVC must be kept on in order to supply the LV PMIC:
  - Allows the nONKEY detection to wake up.
  - Allows supplying the RTC from the main V_{BAT} instead of from the backup battery.

4.6.3 Long Press (Emergency Reset)

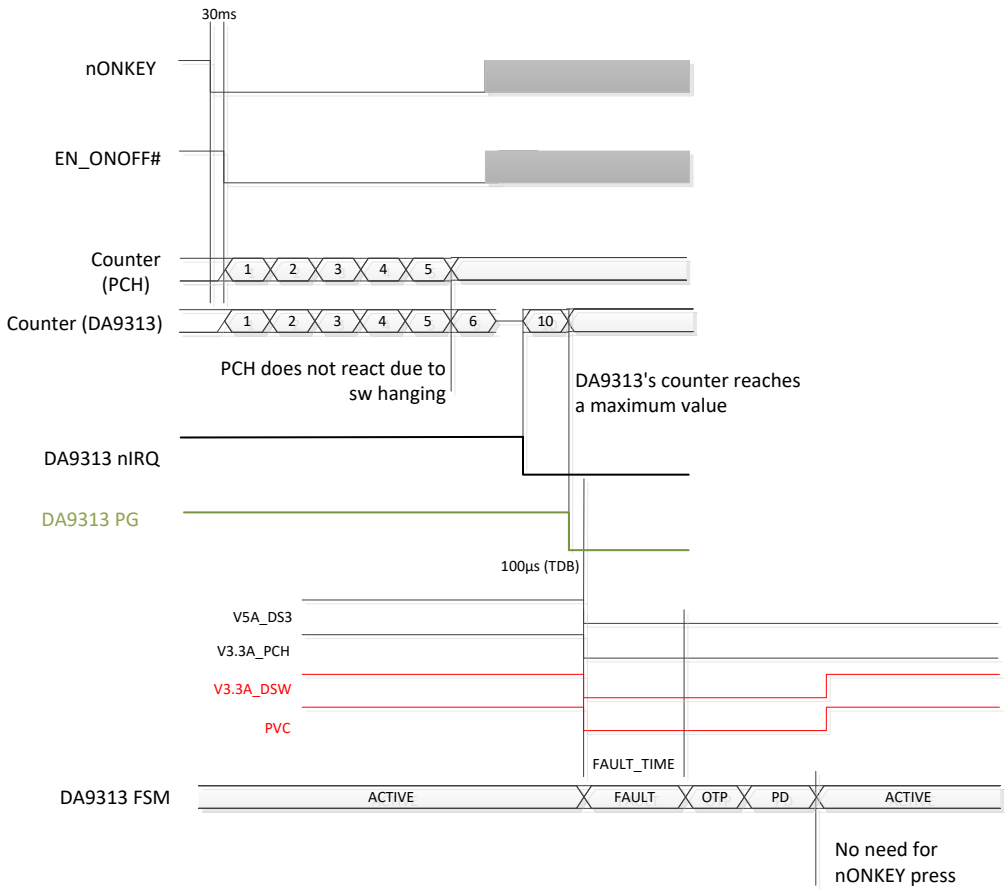


Figure 6: Long Press (Emergency Reset) Timing

4.6.3.1 Long Press (Emergency Reset) Operation Signal Description

- The nONKEY press is debounced by an external device.
- The EC communicates to the PCH which initiates a counter.
- The counter reaches 5 s but the PCH does not react, due to for example hanging software.
- DA9313 and DA9063 have an internal counter (long press). When reaching the long press time they generate an IRQ and wait 1 s for the host processor to clear the KEY_RESET event.
- If the event is not cleared, DA9313 de-asserts PG (power cycle indicator function) to signal the host, the DA9063 and Ext Buck1 / Ext Buck2 that it is shutting down 10 µs (configurable) after PG is de-asserted.
- DA9313 and DA9063 will wait a FAULT_TIME before powering up again, so that the external capacitors of the PVC / buck / LDO rails can be discharged in a clean way.

4.7 Shutdown Source

4.7.1 Firmware Shutdown

When a force shutdown is initiated by the processor, this is done via an I^2C write on DA9313 SOFTRESET bit. DA9313 is power cycled and consequently all devices connected to the PVC are power cycled as well.

The DA9313 PG signal is de-asserted at the beginning of the power cycle causing Ext Buck1 and Ext Buck2 to switch off and the system to shut down.

4.7.2 Surprise Shutdown

A surprise shutdown could be caused by an unexpected power loss, an over-temperature or a VR fault.

If an input under-voltage or a critical over-temperature condition happens to DA9313, it is power cycled and consequently all devices connected to the PVC are power cycled as well. DA9313 PG signal is de-asserted and after 10 µs (configurable) it begins a power cycle.

If the failure happens at DA9063, it initiates a power-down sequence. In this case the DPWROK signal is released during the power-down sequence.

4.7.3 Store the Reset Source

When the system recovers and powers up after a failure, both devices will have logged the reason for the failure. This is supported in the DA9313 even in the case of the main battery being removed because the information should be mirrored in a domain supplied by the backup battery. So an event will be generated after recovery and even after battery re-insertion.

NOTE
On DA9063 the backup battery does not supply the FAULT_LOG register, which contains information on the reason of the specific failure. So the main battery is needed to store this information.

4.7.4 Forced Cold Off

A forced cold off (FCO) can be actioned via the power button. In this case DA9313 must initiate the power-down sequence slightly ahead of DA9063. Before the DA9313 initiates a power-down sequence, it de-asserts the PG 1 s before bringing down the PVC rail so that the host can be warned of an imminent power-down event and act upon it.

The cause of the power-down event is stored in DA9313's FAULT_LOG register. The long press duration of the power button can be programmed on both DA9313 and DA9063.

4.7.4.1 Critical Temperature

The critical temperature (CRITTEMP) bit in the FAULT_LOG of both DA9313 and DA9063, indicates which device has generated a shutdown due to over-temperature.

4.7.4.2 Other Reset Sources

There are additional failure sources supported by DA9313 and DA9063; for example an under-voltage condition at V_{BAT} or a permanent short circuit at the PVC output. For these conditions, the DA9313 initiates a shutdown of the PVC rail. The related fault cause is stored in the FAULT_LOG register.

4.8 Rail Control

Figure 7 shows the power-up of the platform to S0. The green signals are internal rails; the blue signals are platform rails. Signals coming from the EC and PCH are red.

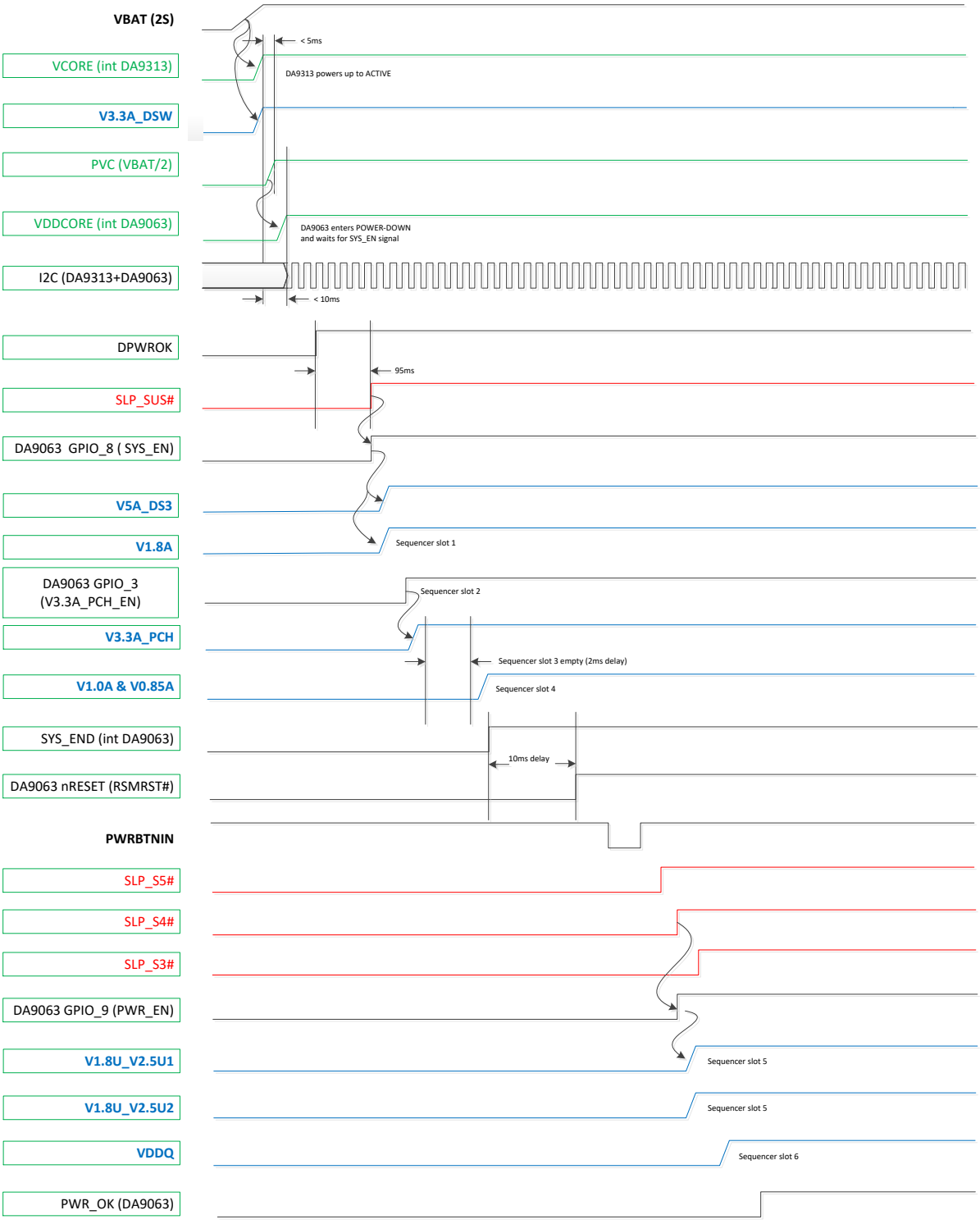


Figure 7: Power-Up from Cold Boot to S0

Table 4: Power Up from Cold Boot to S0 Signal Descriptions

Signal	Description
DPWROK	A delayed V3.3A_DSW_PG signal from the Ext Buck2.
SLP_SUS#	PCH sleep control signal output that allows for entering S4 or S5 state.
V5AEN/SYS_EN	An input signal from the host processor to the DA9063 that enables the regulators in domain SYSTEM. The feature is enabled using GPIO8.
V3.3V_PCH_EN	Enables the 3.3 V line switch, via DA9063 GPIO_3, that connects the Ext Buck2 output to the PCH.
SYS_END (SYSTEM_END)	Internal to DA9063,indicates that the last supply of domain SYSTEM has been reached.
RSMRST#	Connected to DA9063's nRESET pin to tell the host to enter the reset state.
PWRBTNIN	Power button input signal.
SLP_S3#, SLP_S4# SLP_S5#	Used by the PCH to enable some voltage regulators to enter the S0 state.
PWR_EN	An input signal from the host processor to the DA9063. It is used to trigger a wake-up event from POWER-DOWN mode to continue the power-up sequence. The feature is enabled using GPIO9.
PWR_OK	A regulator status indicator from DA9063. It is asserted if none of the selected DA9063 regulators are out-of-range. The feature is outputted on GP_FB2.

4.9 Power Good Signals

The DA9313 and DA9063 with an external circuit fully meet the requirements for the PG generation.

4.9.1 Delayed Power Good

The delayed power good signal (DPWROK) of the Ext Buck2 regulator (that is V3.3V_DSW power domain) that can be generated using a few logic gates externally. DPWORK must be asserted no earlier than 10 ms after the V3.3A_DSW rail is valid, and it must immediately de-assert without any delay if $V_{BAT} \leq 5.4$ V.

4.9.2 RSMRST#_PWRGD Generation

This is supported by the nRESET signal of DA9063. The actual voltages are not actively monitored, but at the end of the power-up sequence the nRESET signal is released. It relies on sequencing information rather than on actual voltage power good. If active monitoring is needed, an external supervision and logic should be added.

A few logic gates are externally required, see Figure 8.

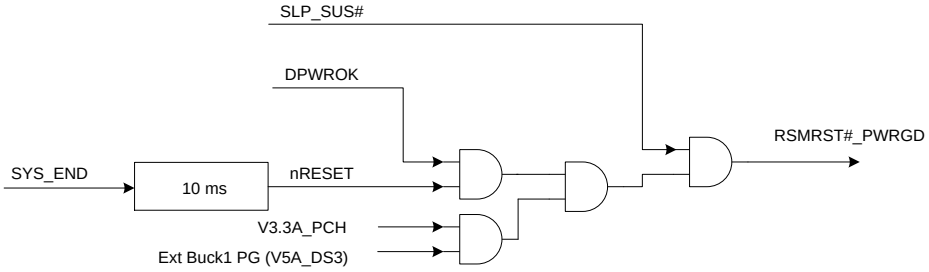


Figure 8: RSMRST#_PWRGD Signal Generation

4.9.3 VCCST_PWRGD, SYS_PWROK, ALL_SYS_PWRGD, PCH_PWROK Generation

The PWR_OK configurable output port on the DA9063 generates a subset of the signals. An additional external supervision is necessary along with a few external logic blocks, see Figure 9.

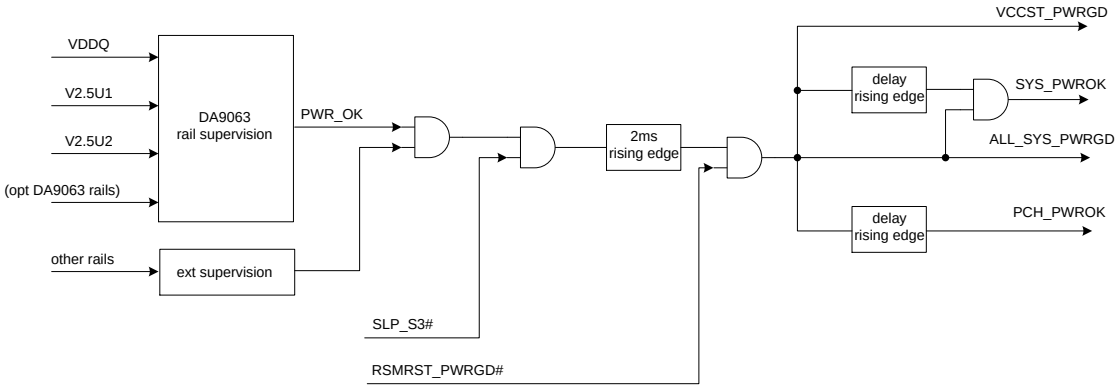


Figure 9: Power Good Signals Generation

An embedded ADC in the DA9063 monitors the VDDQ, V1.8U_V2.5U1 and V1.8U_V2.5U2 rails (and optionally DA9063 generated rails such as V1.8A and V1.00A) by using channels 8, 9, and 10 of the ADC scheduler. The monitoring can be enabled individually on each regulator resulting in the output signal PWR_OK, providing all rails are powered.

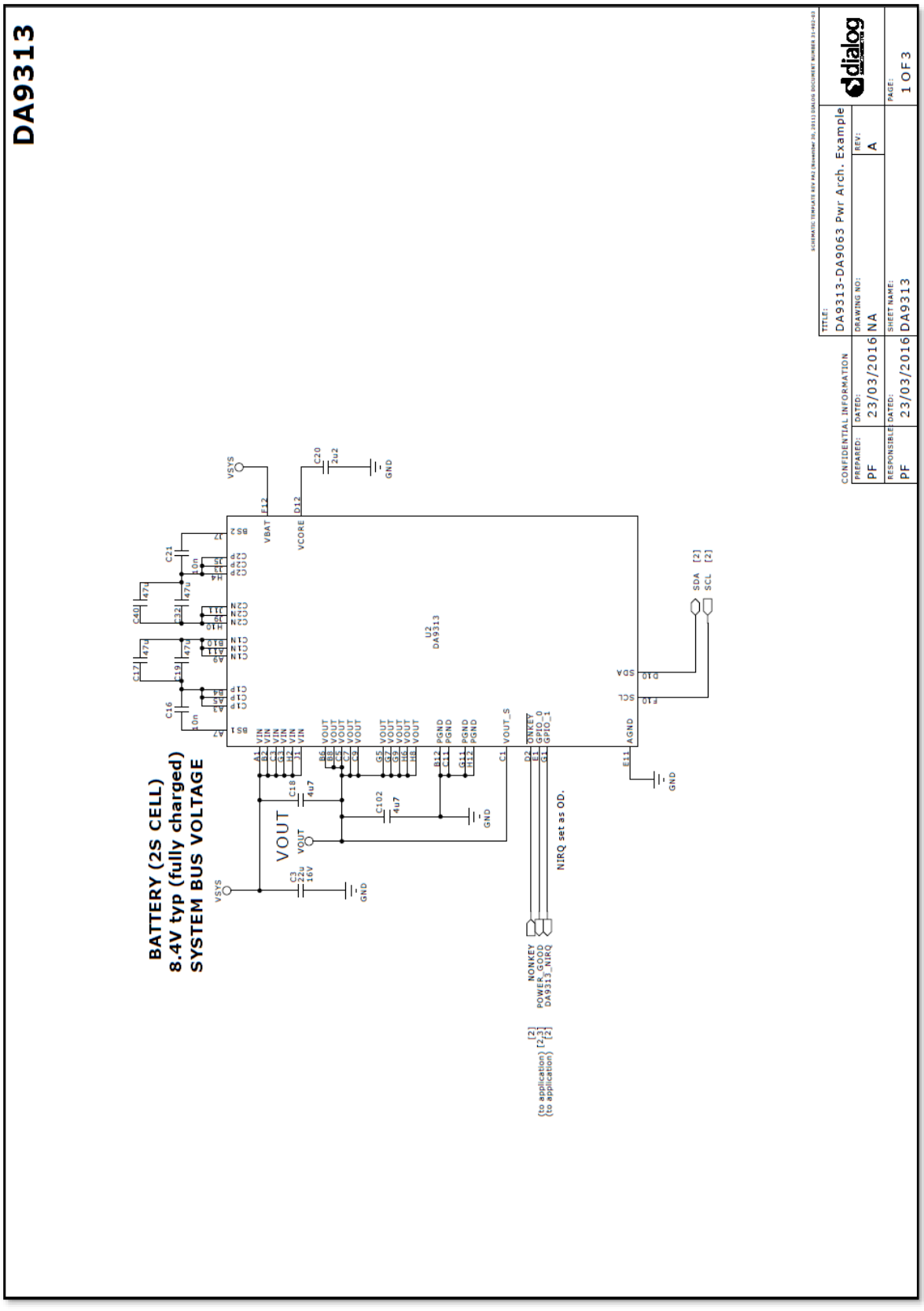
Table 5: ADC Channel Assignment

ADC Channel	Regulator	Enable
A8	BUCKCORE1 BUCKCORE2 BUCKPRO LDO3 LDO4 LDO11	BCORE1_MON_EN BCORE2_MON_EN BPRO_MON_EN LDO3_MON_EN LDO4_MON_EN LDO11_MON_EN
A9	BUCKIO BUCKMEM BUCKPERI LDO1 LDO2 LDO5	BIO_MON_EN BMEM_MON_EN BPERI_MON_EN LDO1_MON_EN LDO2_MON_EN LDO5_MON_EN
A10	LDO6 LDO7	LDO6_MON_EN LDO7_MON_EN

	LDO8 LDO9 LDO10	LDO8_MON_EN LDO9_MON_EN LDO10_MON_EN

5 Example Power Architecture Schematic

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture



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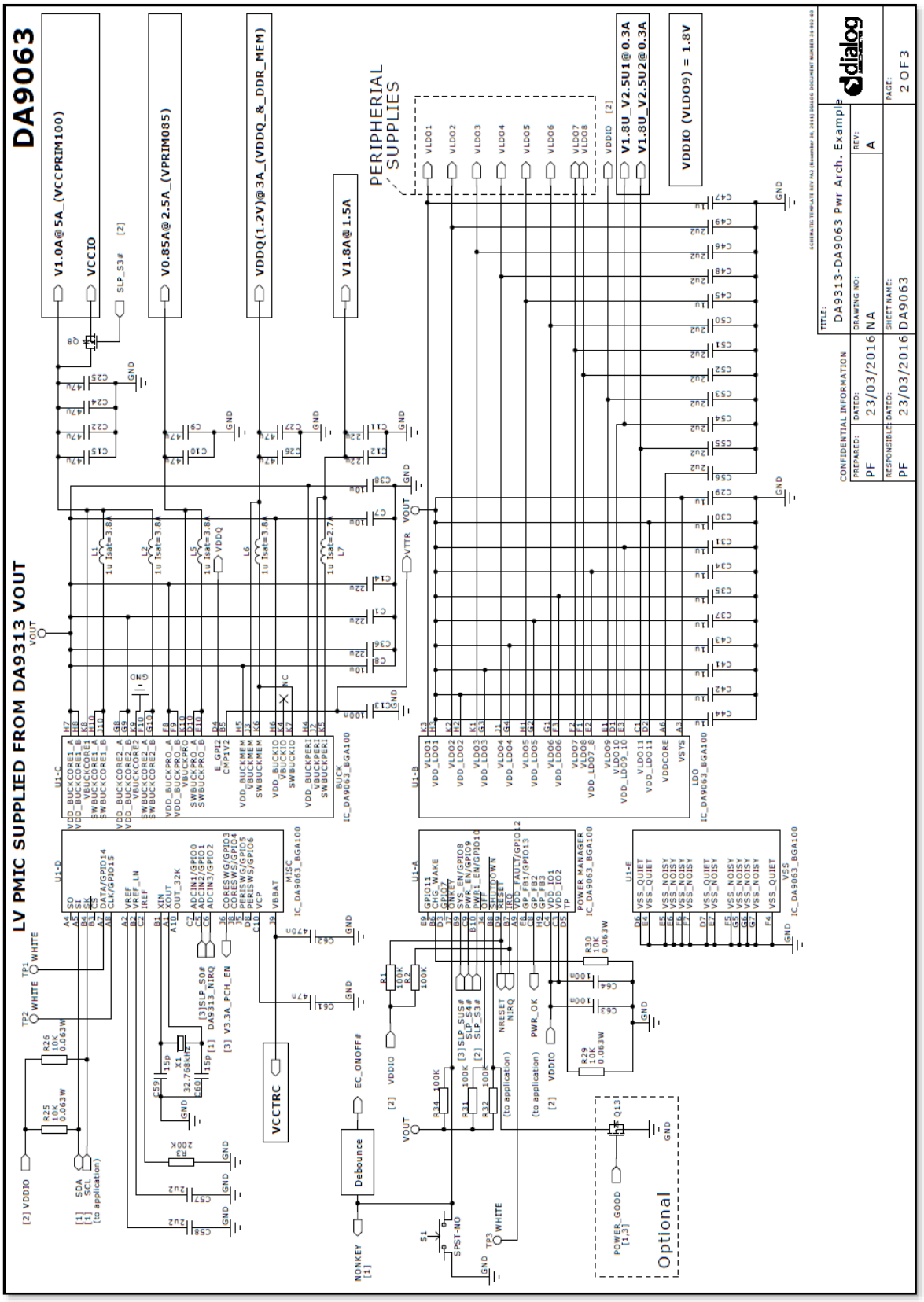

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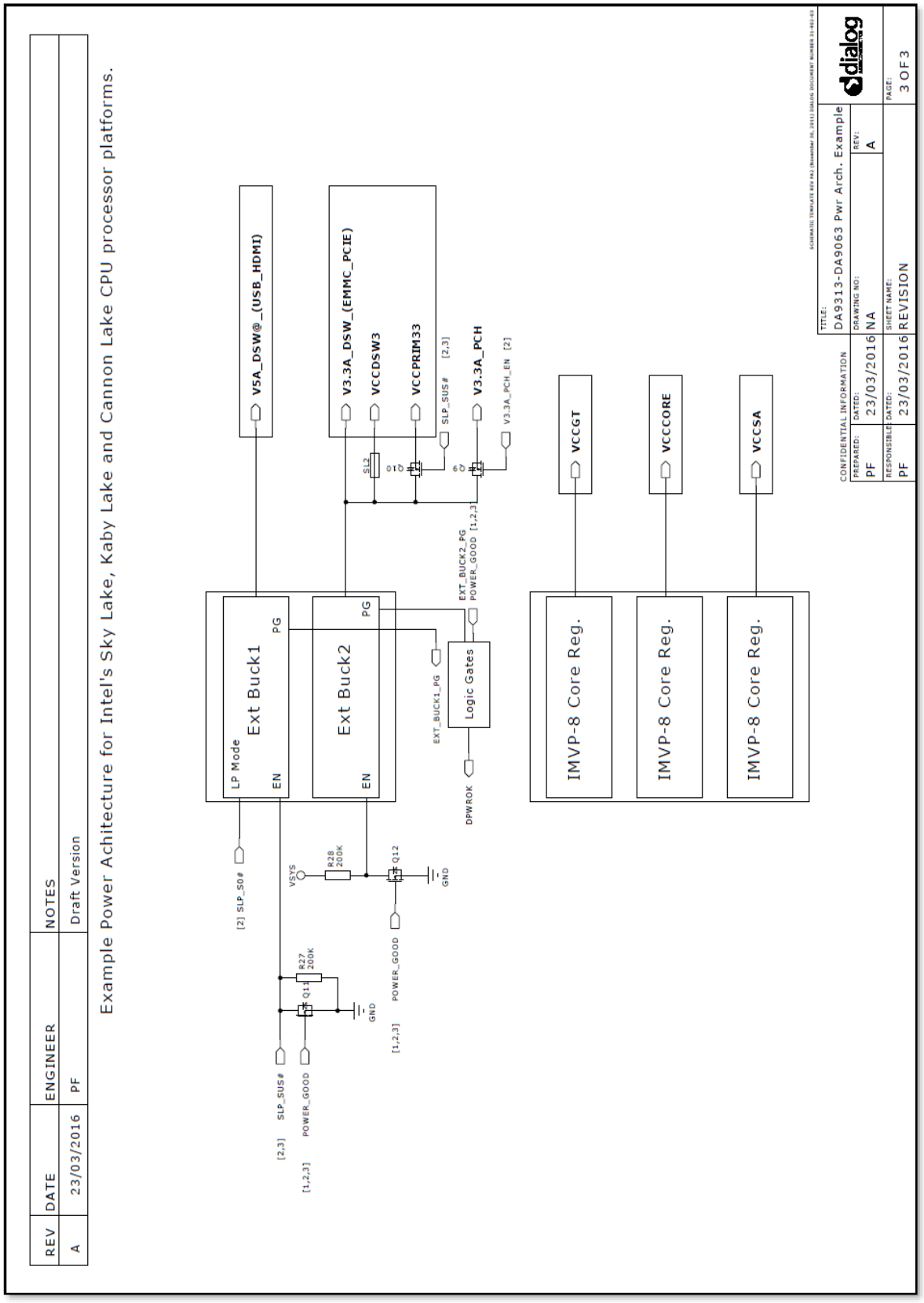


Figure 10: Example Power Architecture Schematic

6 Example Power Architecture BOM

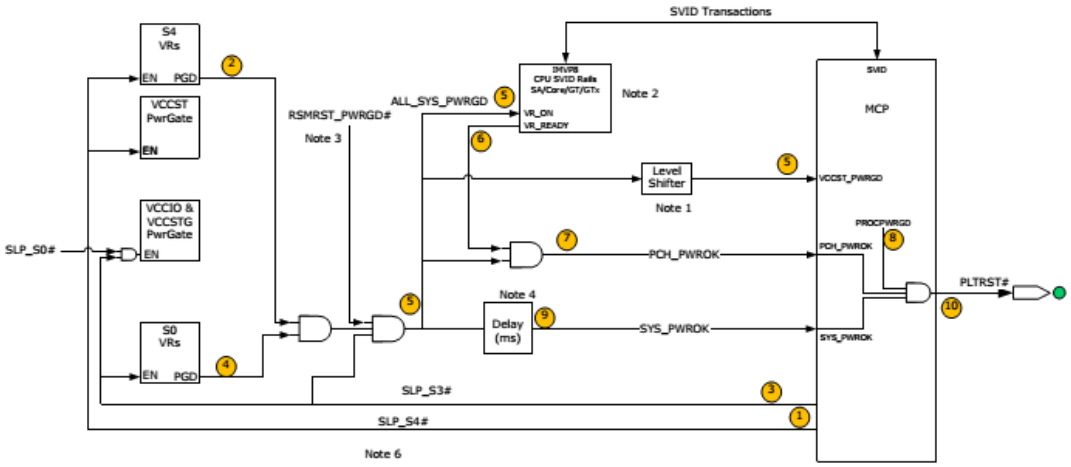
Table 6: DA9313 BOM

Ref Des	Value	Description	Mfr	Part Number	Qty
U2	DA9313		Dialog	DA9313	1
C3	22 µF	0805 16V JB capacitor	TDK	C2012JB1C226M085AC	1
C18, C102	4.7 µF	0402 10V X5R capacitor	Murata	GRM155R61A475MEAA	2
C20	2.2 µF	0402 16V X5R capacitor	Murata	GRM155R61C225KE11	1
C16, C21	10 nF	0201 10V X7R capacitor	Murata	GRM033R71A103KA01D	2
C17, C19, C32, C40	47 µF	0603 6.3V X5R capacitor	Murata	GRM188R60J476ME15	4

Table 7: DA9063 BOM

Ref Des	Value	Description	Mfr	Part Number	Qty
U1	DA9063		Dialog	DA9063	1
L1, L2, L5, L6	1 µH	DFE252012 series SMD inductor	Murata-Toko	1239AS-H-1R0M	4
L7	1 µH	DFE201610 series SMD inductor	Murata-Toko	1285AS-H-1R0N	1
C9, C10, C15, C22, C24, C25, C26, C27	47 µF	0805 6.3V X5R capacitor	Murata	GRM21BR60J476M#	8
C11, C12	22 µF	0603 6.3V X5R capacitor	TDK	C1608X5R0J226M080AC#	2
C1, C14, C36	22 µF	0805 10V X5R capacitor	Taiyo Yuden	LMK212BJ226MG-T#	3
C7, C8, C38	10 µF	0805 10V X7R capacitor	Murata	GRM21BR71A106KE51L#	3
C13, C63, C64	100 nF	0402 10V X5R capacitor	Murata	GRM155R61A104KA01D#	3
R25, R26, R29, R30	10 kΩ	0402 resistor	Yageo	RC0402FR-0710KL	4
C57, C58, C46, C48, C49, C50, C51, C52, C53, C54, C55, C56	2.2 µF	0402 6.3V X5R capacitor	Kemet	C0402C225M9PACTU#	12
R3	200 kΩ	0402 resistor	Yageo	RC0402FR-07200KL#	1
C59, C60	15 pF	0402 COG capacitor	Murata	GRM1555C1H150JZ01D#	2
X1	32.768 kHz	XTAL 32.768kHz 9.0pF SM FC-135	EPSON TOYOCOM	FC-135 32.768KHZ 20PPM,9.0PF#	1
C61	47 nF	0402 10V X5R capacitor	Murata	GRM155R61A473KA01D#	1
C62	470 nF	0402 10V X5R capacitor	Murata	GRM155R61A474KE15D#	1
R1, R2, R31, R32, R34	100 kΩ	0404 resistor	Yageo	RC0402FR-07100KL#	5
C29, C30, C31, C34, C35, C37, C41, C43, C42, C44, C45, C47	1 µF	0402 10V X5R capacitor	Murata	GRM155R61A105KE15D#	12

7 Platform Flow Diagrams



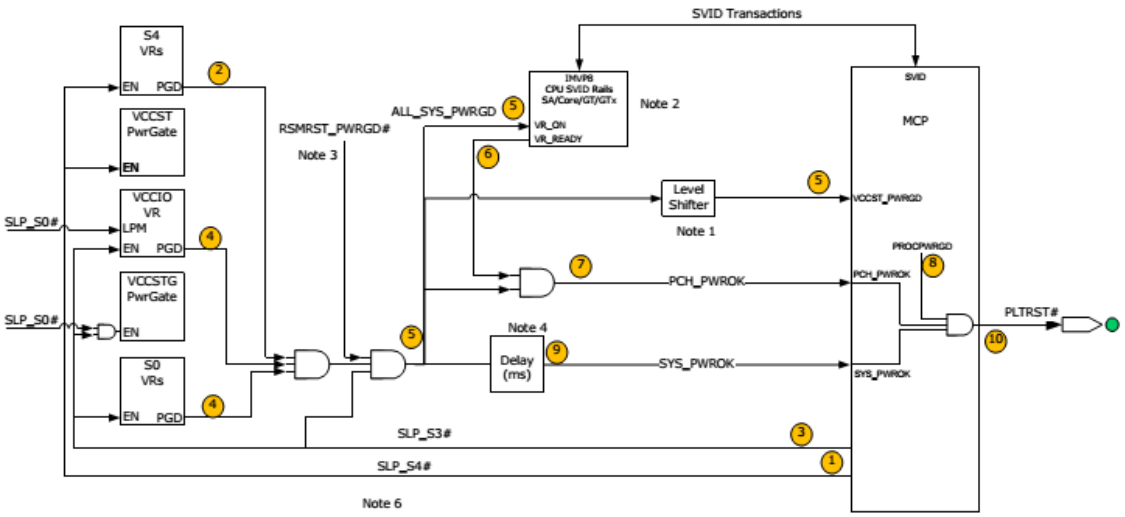
Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

Notes:

1. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
2. VCCSA SVID domain is expected to be a IMVP8 non-Zero voltage boot domain. VCC, VCCGT, and VCCGTx are zero volt boot domains
3. Optional, Added for addition system robustness
4. This delay is not explicitly required. For systems supporting traditional PCIe* add-in cards that require up to 100ms delay from power stable to PLTRST# de-assertion or simply require extra timing delay in the cold boot sequence to support other external devices, the PCH can guarantee a 99ms delay by enabling tPCH33 timing through soft straps. If more or less time is required, then a specific timing delay circuit may be required
5. Enable inputs may be qualified by other signals and factors not shown
6. DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown
7. CCOPC and VCCEOPIO with OPC support not shown in this diagram. See OPC Power Control Connections figure

Figure 11: SKL U/Y (Volume Segment) Flow Diagram

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture



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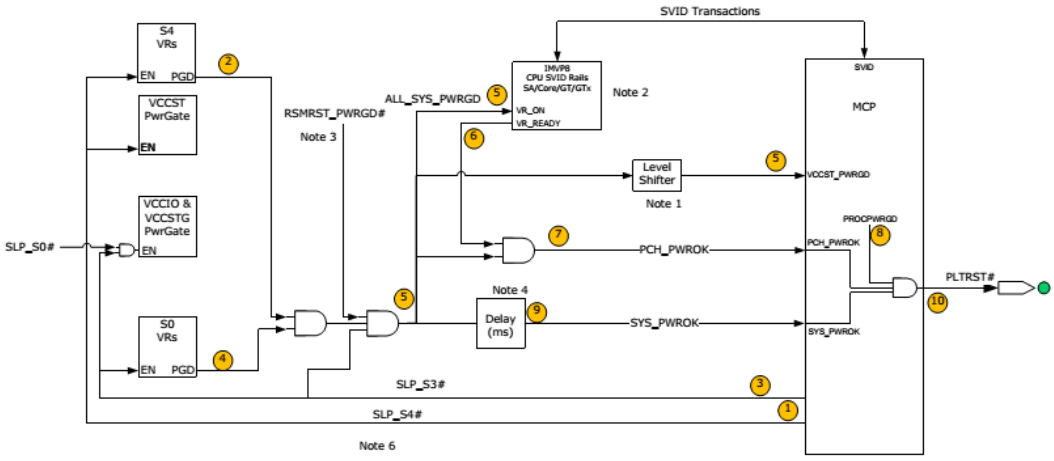
5. Enable inputs may be qualified by other signals and factors not shown
6. DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown
7. CCOPC and VCCEOPIO with OPC support not shown in this diagram. See OPC Power Control Connections figure

Figure 12: SKL U/Y (Premium Segment) Flow Diagram

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture



Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

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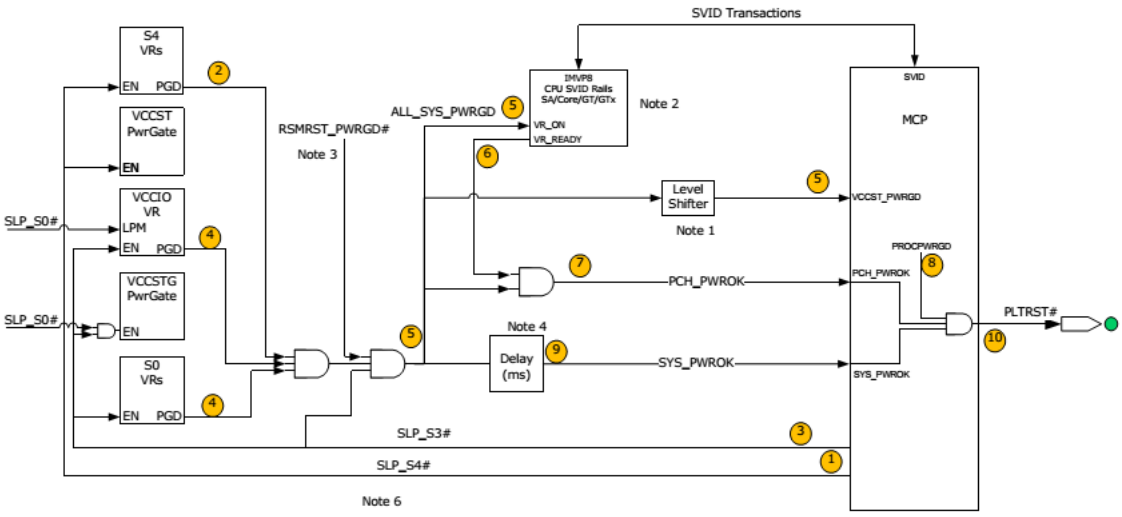
5. Enable inputs may be qualified by other signals and factors not shown
6. DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown
7. CCOPC and VCCEOPIO with OPC support not shown in this diagram. See OPC Power Control Connections figure

Figure 13: KBL U/Y (Volume Segment) Flow Diagram

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture



Many variations exist on how the various PWRGD signals can be generated on a MB platform to balance system robustness with platform costs constraints and area constraints. This is just one example of possible logic connections. A baseline configuration is shown in the diagram.

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5. Enable inputs may be qualified by other signals and factors not shown
6. DSW/PRIM VRs and DSW_PWROK/RSMRST# logic not shown
7. CCOPC and VCCEOPIO with OPC support not shown in this diagram. See OPC Power Control Connections figure

Figure 14: KBL (Premium Segment) Flow Diagram

Revision History

Revision	Date	Description
1.0	06-Apr-2016	Initial release
1.1	21-Feb-2107	Minor changes
1.2	23-Feb-2022	Document rebranded to Renesas.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

DA9313-DA9063: Example Ultrabook/Notebook Power Architecture

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