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SH7263/SH7203 Group

Example of Cache Memory Setting

Introduction

This application note describes an example of cache-function settings for the SH7263/SH7203.

Target Device

SH7263/SH7203

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1. Preface

1.1 Specifications

The instruction cache and the operand cache are enabled and placed in the write-back mode.

1.2 Modules Used

- Instruction cache and operand cache

1.3 Applicable Conditions

- MCU SH7263/SH7203
- Operating frequency Internal clock: 200 MHz
  Bus clock: 66.67 MHz
  Peripheral clock: 33.33 MHz
- Compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01 Release01
  (from Renesas Technology Corp.)
- Compiler options -cpu=sh2afpu -fpu=single -include="$(WORKSPDIR)\inc"
  -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath
  -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0
  -struct_alloc=1 -nologo

1.4 Related Application Note

The operation of the sample program in this application note was confirmed with the configuration specified in the application note "Example of SH7263/SH7203 *Initial Configuration*". Please refer to that note in combination with this one.

2. Description of the Sample Application

This sample application employs the instruction cache and operand cache.

2.1 Summary of MCU Functions Used

If the instruction cache and operand cache are enabled (respectively, when the ICE and the OCE bits in the register CCR1 are set to 1), whenever an instruction or data in a cacheable area is accessed, the cache is searched to see if it contains the desired instruction or data. The cache is searched according to the following procedure.

1. A single entry is selected by using bits 10 to 4 of the address used to access memory from CPU and the tag addresses at the corresponding entry number in all four ways are read out. At this time, the highest-order three bits of the tag addresses are always cleared to 0.
2. Bits 31 to 11 of the address used to access memory are compared with the tag addresses that have been read out. Address comparison is with the tag addresses read out from the entries in all four ways.
3. When the result of comparison is a match with a tag address and the selected entry is valid (V=1), a cache hit is said to have occurred. When the comparison does not show a match or the selected entry is not valid (V=0), a cache miss is said to have occurred.
4. In the case of a cache hit, the long-word (LW) of data at the position in the data array defined by bits 3 and 2 of the accessed address is read or written.

Table 1 Overview of Caches

Item	Description
Capacity	Instruction cache: 8 KB Operand cache: 8 KB
Structure	Instructions and data are separated; each cache is 4-way set associative
Cache lock function	Ways 2 and 3 can be locked (only in the operand cache)
Line size	16 bytes
Number of entries/ways	128
Write system	Write-back and write-through methods are selectable
Replacement method	Least-recently-used (LRU) algorithm

Note: For details on the caches, refer to the section on *Cache* in the *SH7263/SH7203 Group Hardware Manual*.

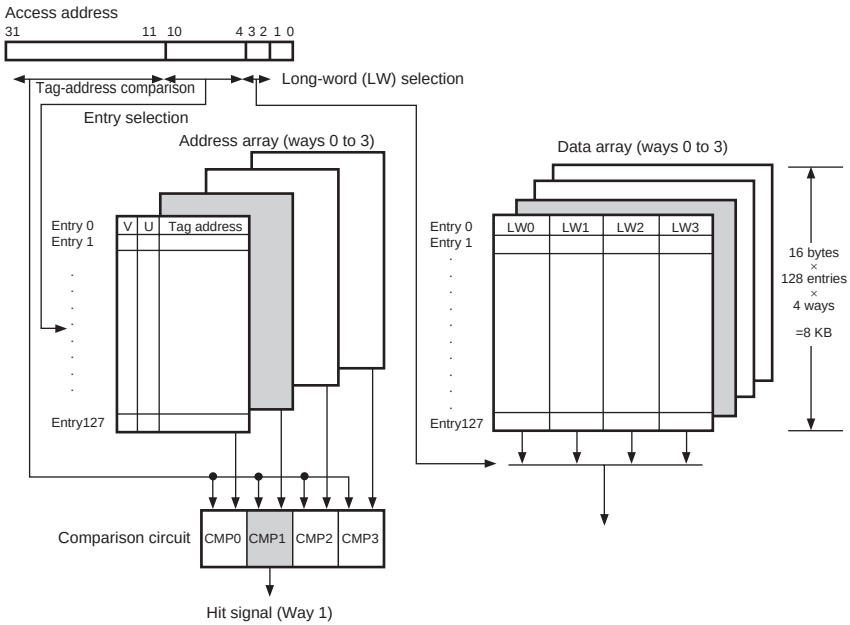


Figure 1 Overview of the Cache-Search Scheme

2.2 Procedure for Setting the Module Used

The procedure for setting up the caches is described below.

Cache control register 1 (CCR1) is used to select the cache mode. Once CCR1 has been set, access to areas for which caching has been enabled must only proceed after the CCR1 register has been read (this prevents access to such areas while the cache mode is being updated). Also, program code that manipulates the cache control registers must be executed from an area for which caching is disabled.

This sample application also changes the interrupt mask to prevent the acceptance of interrupt processing that might include access to the cache-enabled spaces while the cache mode is being updated.

Figure 2 is a flow chart showing an example of the procedure used to enable both the instruction cache and operand cache.

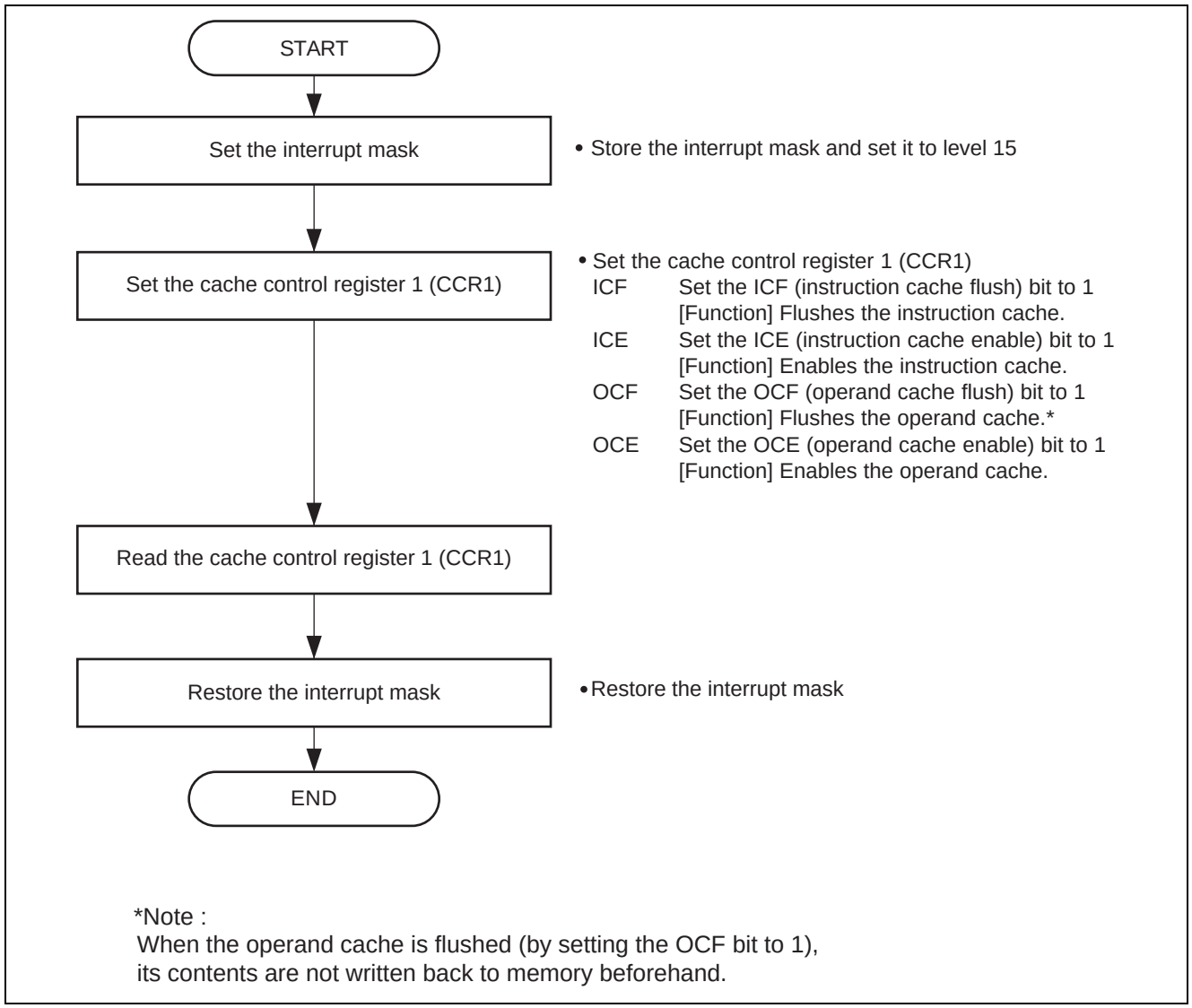


Figure 2 Example Flow for Settings Up the Cache

2.3 Description of the Sample Program

The sample program enables the instruction cache and the operand cache, and then writes data equivalent to a single cache entry (line) to external memory (SDRAM). Since the operand cache is enabled (in write-back mode) for the target region of memory, the data are actually written to the cache. That is, the data are not reflected in the external memory (SDRAM).

The section name for the cache manipulation function is adjusted so that the function is placed in a cache-disabled space.

2.4 Procedure for Processing by the Sample Program

Table 2 describes how the cache is set up by the sample program. Table 3 describes the macro definitions used in the sample program. Figure 3 shows a flow chart of processing by the sample program.

Table 2 Cache Settings

Register Name	Address	Setting	Description
Cache control register1 (CCR1)	H'FFFC 1000	H'0000 0909	ICF = 1; Flushes the instruction cache ICE = 1; Enables the instruction cache OCF = 1; Flushes the operand cache OCE = 1; Enables the operand cache Note: ICF and OCF are always read as 0.

Table 3 Cache-Related Macro Definitions in the Sample Program

Macro Definition	Setting	Function
CACHE_OFF	H'0000	Turns the cache off
CACHE_I_FLUSH	H'0080	Flushes the instruction cache
CACHE_I_ON	H'0100	Enables the instruction cache
CACHE_O_FLUSH	H'0001	Flushes the operand cache
CACHE_O_ON	H'0008	Enables the operand cache
CACHE_O_WT	H'0002	Places the operand cache in write-through mode

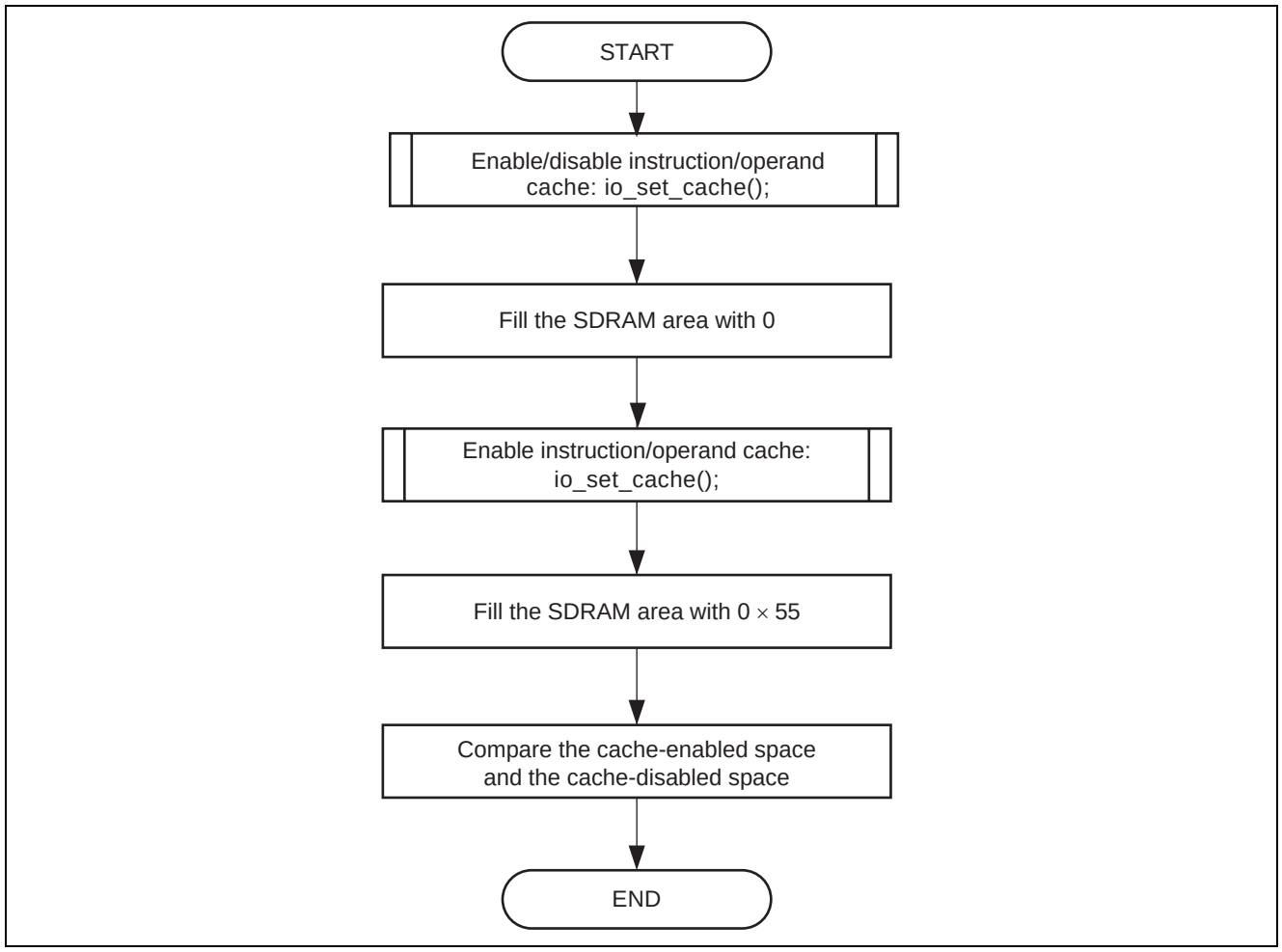


Figure 3 Flow of Processing by the Sample Program

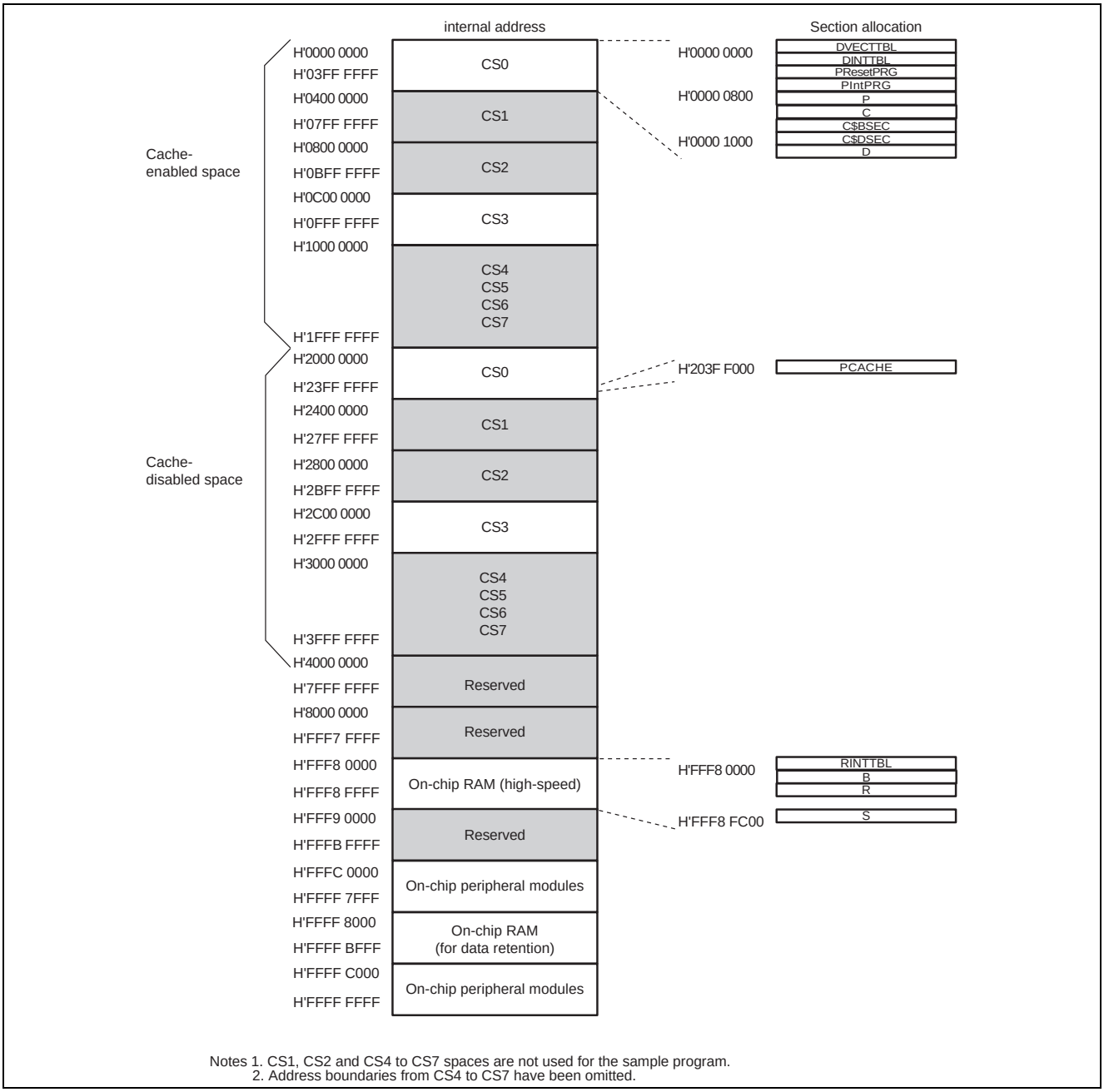
2.5 Allocation of Sections in the Sample Program

The #pragma section directive is used with the corresponding extended compiler function to set a section name for the function that actually manipulates the cache control registers.

In the sample program, the area for program code of the io_set_cache function is set to the PCACHE section. Only this part of the program is allocated to a cache-disabled space of the SH7263/SH7203. That is, the rest of the program is allocated to a space where caching is performed if it is enabled (the P section).

Section allocation (address specification) is specified by linkage editor options.

Figure 4 shows a memory map for the sample program.



Notes 1. CS1, CS2 and CS4 to CS7 spaces are not used for the sample program.
2. Address boundaries from CS4 to CS7 have been omitted.

Figure 4 Memory Map of the Sample Program

2.6 Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*********************************************************************
*
*   System Name: SH7203 Sample Program
*   File Name  : main.c
*   Contents   : sample of cache register
*   Version    : 1.00.00
*   Model      : M3A-HS30
*   CPU        : SH7203
*   Compiler   : SHC9.1.1.0
*   Note       : Sample program to confirm the cache operation.
*                <Caution>
*                This sample program is for reference
*                and its operation is not guaranteed.
*                Customers should use this sample program for technical reference
*                in software development.
*
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*
*  history      :2008.01.10  ver.1.00.00
*""FILE COMMENT END""*****************************************************************/
#include <machine.h>
#include “iodefine.h”       / *iodefine.h is a file automatically generated by the
                              High-performance Embedded Workshop. */

/* ==== Macro definition ==== */
/* ----Cache settings ---- */
#define CACHE_OFF       0x0000u
#define CACHE_I_FLUSH   0x0800u
#define CACHE_I_ON      0x0100u
#define CACHE_O_FLUSH   0x0008u
#define CACHE_O_ON      0x0001u
#define CACHE_IO_ON     (CACHE_I_ON  | CACHE_O_ON)
#define CACHE_O_WT      0x0002u

/* ----SDRAM area address ---- */
#define SDRAM_ADDR1   (unsigned char *)(0x0c000000)   /*Cache-enabled area */
#define SDRAM_ADDR2   (unsigned char *)(0x2c000000)   /*Cache-disabled area */

/* ==== Prototype declaration ==== */
void main(void);
int io_set_cache(unsigned int mode);

```

2. Sample Program Listing: main.c (2)

```
/*""FUNC COMMENT""*****************************************************************************
* Outline       : Sample Program main (example of using cache memory)
*-----------------------------------------------------------------------------------------------
* Include       :
*-----------------------------------------------------------------------------------------------
* Declaration   : void main(void);
*-----------------------------------------------------------------------------------------------
* Function      : Example of enabling / disabling cache memory.
                : After the SDRAM area has been initialized with the operand cache OFF,
                : a fill operation is performed with the operand cache ON,
                : and the cached area is compared with its shadow in the cache-disabled space.
*-----------------------------------------------------------------------------------------------
* Argument      : void
*-----------------------------------------------------------------------------------------------
* Return Value  : void
*-----------------------------------------------------------------------------------------------
* Notice        : In this sample program, the cache is flushed. Therefore,
                : a program for initialization that enables the cache will invalidate
                : the contents of the cache.
*""FUNC COMMENT END""*************************************************************************/
void main(void)
{
   int i;
   unsigned char *ptr1, *ptr2;

   /*==== Disabling instruction and operand caches ==== */
   io_set_cache(CACHE_OFF | CACHE_I_FLUSH | CACHE_O_FLUSH);

   /*==== Filling SDRAM area with 0 ==== */
   ptr1 = SDRAM_ADDR1;
   for(i=0; i < 16; i++){
            *ptr1++ =0;
   }

   /*==== Enabling instruction and operand caches ==== */
   io_set_cache(CACHE_I_ON | CACHE_O_ON | CACHE_I_FLUSH | CACHE_O_FLUSH);

   /*==== Filling SDRAM area with 0x55 ==== */
   ptr1 = SDRAM_ADDR1;
   for(i=0; i < 16; i++){
            *ptr1++ = 0x55;
   }

   /*==== Comparing cache-enabled and cache-disabled spaces ==== */
   ptr1 = SDRAM_ADDR1;         /* cache-enabled space */
   ptr2 = SDRAM_ADDR2;         /* cache-disabled space */

   for(i=0; i < 16; i++){
            if(*ptr1++ == *ptr2++ ){
                 while(1){
                     /* Error in operand-cache setting */
                 }
```

3. Sample Program Listing: main.c (3)

```
101         }
102     }
103
104     while(1){
105             /* Program end */
106     }
107
108 }
109
110 #pragma section CACHE                /* Allocated in the CSO cache-disabled space*/
111 /*""FUNC COMMENT""*****************************************************************************
112 * Outline       : Cache setting
113 *-----------------------------------------------------------------------------------------------
114 * Include       : #Include “iodefine.h”
115 *-----------------------------------------------------------------------------------------------
116 * Declaration   : int io_set_cache(unsigned int mode);
117 *-----------------------------------------------------------------------------------------------
118 * Function      : Cache is placed in the mode specified by the argument “mode”.
119 *-----------------------------------------------------------------------------------------------
120 * Argument      : unsigned int mode : Combos of the following modes are obtained by logical OR
121                 :               : CACHE_I_FLUSH : Instruction cache flush
122 *               :               : CACHE_I_ON    : Instruction cache enable
123 *               :               : CACHE_O_FLUSH : Operand cache flush
124 *               :               : CACHE_O_ON    : Operand cache enable
125 *               :               : CACHE_IO_ON   : Instruction/operand cache ON
126 *               :               : CACHE_O_WT    : Write-through mode
127 *               :               : CACHE_OFF     : Instruction/operand cache disable
128 *-----------------------------------------------------------------------------------------------
129 * Return Value                  : 0             : Normally finished
130 *-----------------------------------------------------------------------------------------------
131 * Notice        :non
132 *""FUNC COMMENT END""*************************************************************************/
133 int io_set_cache(unsigned int mode)
134 {
135         volatile unsigned long reg;
136         int mask;
137
138         /*==== Setting interrupt mask ==== */
139         mask = get_imask();
140         set_imask(15);               /* Set to level 15*/
141
142         /*==== Setting cache register ==== */
143         CCNT.CCR1.LONG = mode;
144
145         /*==== Reading cache register ==== */
146         reg = CCNT.CCR1.LONG;
147
148         /*==== Canceling interrupt mask ==== */
149         set_imask(mask);               /* Set to the original level*/
150
151         return 0;
152 }
153
154 /* End of File */
```

3. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7203 Group Hardware Manual
  SH7263 Group Hardware Manual
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