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SH7730 Group

Example of BSC SDRAM Interface Connection (32-Bit Data Bus)

Introduction

This application note introduces the synchronous DRAM (SDRAM) interface of the bus state controller (BSC) and includes a sample application.

Target Device

SH7730

Contents

1. Preface

1.1 Specifications

- Two 128-Mbit (2 M × 16 bits × 4 banks) SDRAM modules are connected to the SH7730 with a 32-bit data bus width. SDRAM is initialized by using the SDRAM interface function of the SH7730.

1.2 Module Used

- Bus state controller (BSC)

1.3 Applicable Conditions

- Evaluation board: The AP-SH4A-1A board incorporates the SH7730 with SH-4A CPU core and is available from AlphaProject Co., Ltd.
  - External memory (area 0): 4-MB NOR-type flash memory: S29AL032D70TFI04 from Spansion
  - External memory (area 3): 32-MB SDR-SDRAM (16 MB × 2): K4S281632F-UC75 from Samsung
- MCU: SH7730 (R8A77301)
- Operating frequency: CPU clock: 266.66 MHz
  SuperHyway bus clock: 133.33 MHz
  Bus clock: 66.66 MHz
  Peripheral clock: 33.33 MHz
- Bus width for area 0: 16-bit fixed (with the MD3 pin at the low level)
- Clock operating mode: Mode 2 (with the MD0 pin at the low level, and the MD1 pin at the high level)
- Endian: Big endian (with the MD5 pin at the low level)
- Toolchain: SuperH RISC engine Standard Toolchain Ver.9.1.1.0: Available from Renesas Technology
- Compiler options: Default settings of High-performance Embedded Workshop
  (-cpu = sh4a –debug –optimize = 0 -noinline
  -gbr = auto –macsave = 0 –save_cont_reg = 0 –chgincpath –errorpath
  -global_volatile = 0 -opt_range = all -infinite_loop = 0 -del_vacant_loop = 0
  -struct_alloc = 1 -nologo)

1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the *SH7730 Group Application Note: Example of Initialization* (REJ06B0848). Please refer to that document in combination with this one.

2. Description of Sample Application

2.1 Operational Overview of Module Used

The bus state controller (BSC) of the SH7730 supports an SDRAM interface that is connectable to SDRAM units that have 11, 12, or 13 bits of row address, 8, 9, or 10 bits of column address, 4 or fewer banks, and in which the A10 pin is used to set precharge mode in read and write command cycles. Burst reading/single writing (burst length 1) and burst reading/burst writing (burst length 1) are supported as SDRAM operating modes.

Table 1 provides the specifications of SDRAM used in this sample application.

Table 1 Specifications of SDRAM Used in this Sample Application

Item	Description
Type number	K4S281632F-UC75 from Samsung
Capacity (configuration)	128 Mbits (2 M × 16 bits × 4 banks)
Number of units used	2
CAS latency	2 or 3 (programmable)
Refresh cycles	4,096 refresh cycles per 64 ms
Burst length	1, 2, 4, or 8 full pages (programmable)
Row address	A0 to A11
Column address	A0 to A8
Precharge	Auto precharge/all bank precharge controlled via A10

Figure 1 shows a memory map.

Memory type and the data-bus width for connection are specifiable per CS space. SDRAM can be connected in the CS2 and CS3 spaces of the SH7730. In this application note, SDRAM is connected in the CS3 space.

In cases where the SDRAM is only connected in one area, make the SDRAM-connection settings for area 3, and make normal space settings or settings for the connection of SRAM with byte selection for area 2.

Bits of CS3WCR set the numbers of cycles between the various commands for SDRAM in both areas (areas 2 and 3). Therefore, SDRAM-connection settings that only apply to area 2 are not possible.

In the sample application, the SDRAM is at the locations from H'0C00 0000 to H'0DFF FFFF in the physical address space.

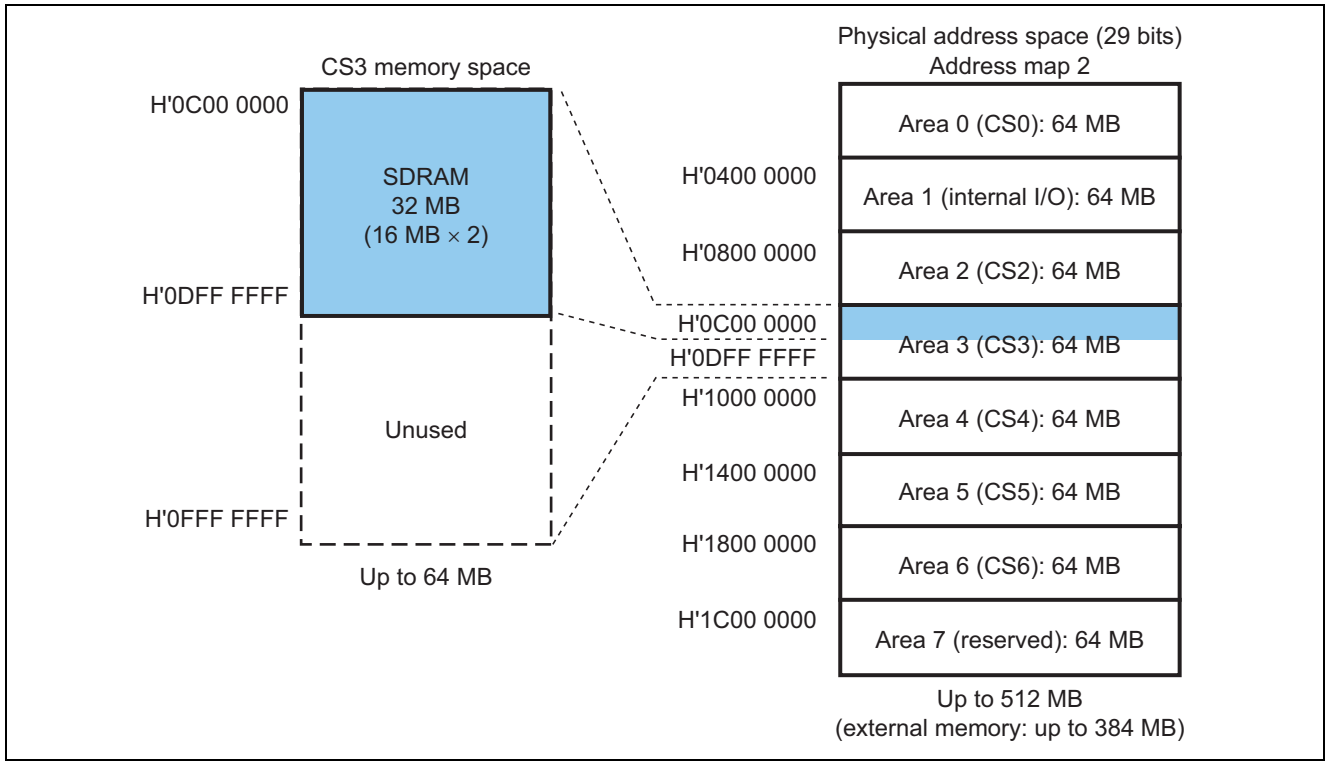


Figure 1 Memory Map

From the software point of view, the physical address space is further mapped onto the virtual address space. Address conversion from the virtual address space to the physical address space differs according to whether the memory management unit (MMU) is or is not in use.

For details, please refer to the section on the bus state controller (BSC) and the memory management unit (MMU) in the *SH7730 Group Hardware Manual* (REJ09B0359).

Figure 2 shows an example of circuitry for SDRAM connection.

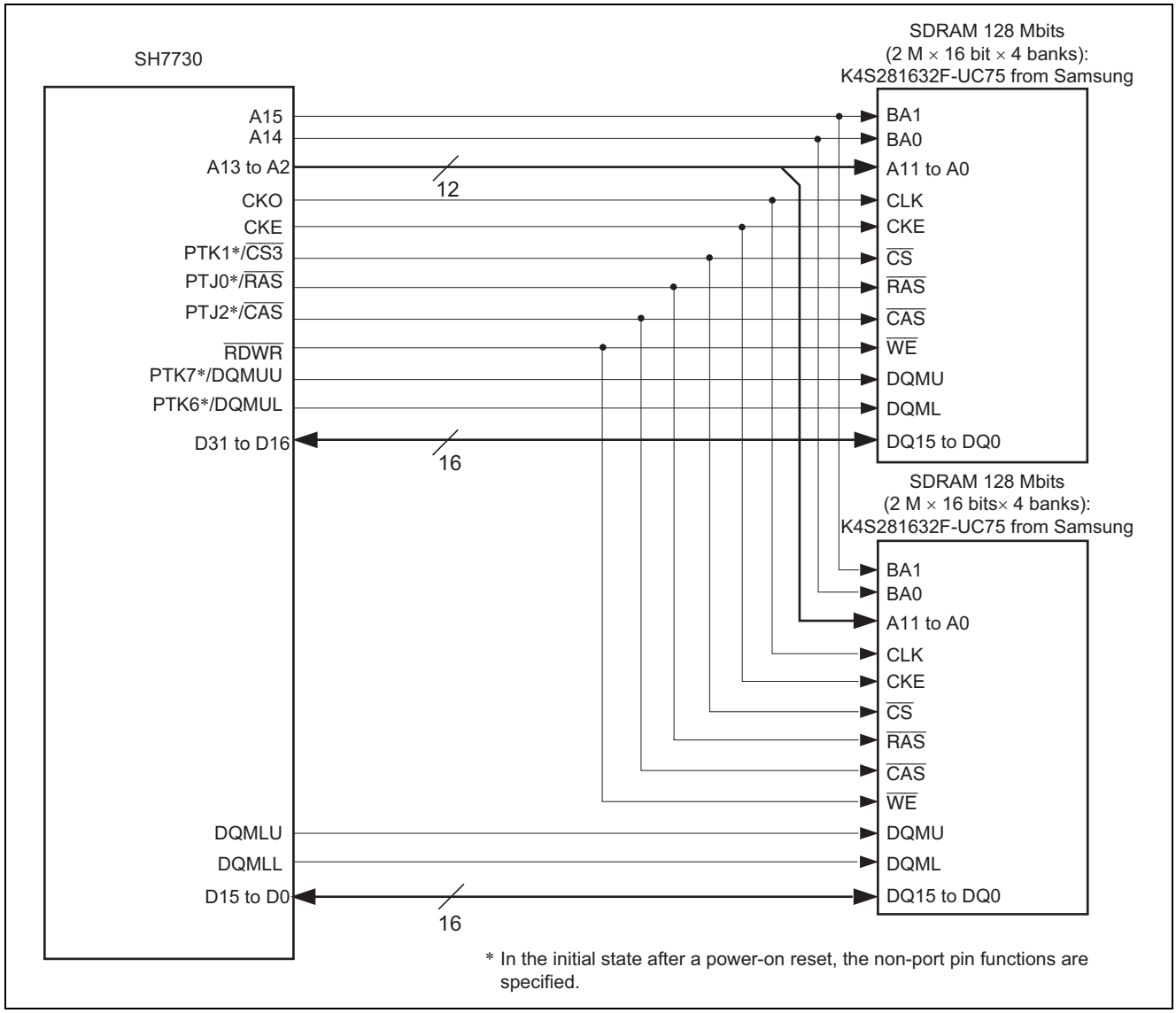


Figure 2 Example of Circuitry for SDRAM Connection (128-Mbit SDRAM × 2, 32-Bit Bus)

Table 2 gives a list of how address-output pins are multiplexed.

Table 2 Connections between SH7730 Pin Functions and SDRAM

SH7730	Row Address	Column Address	SDRAM Pin	Function
A15	A24*2	A24*2	A13 (BA1)	Specifies bank
A14	A23*2	A23*2	A12 (BA0)	Specifies bank
A13	A22	A13	A11	Address
A12	A21	L/H*1	A10/AP	Specifies address/precharge
A11	A20	A11	A9	Address
A10	A19	A10	A8	Address
A9	A18	A9	A7	Address
A8	A17	A8	A6	Address
A7	A16	A7	A5	Address
A6	A15	A6	A4	Address
A5	A14	A5	A3	Address
A4	A13	A4	A2	Address
A3	A12	A3	A1	Address
A2	A11	A2	A0	Address

Notes: 1. The L/H bit is used in command specification; it is fixed at low or high according to the access mode.
2. Bank address specification

2.2 Procedure for Setting Module Used

2.2.1 Example of the Initialization Procedure for SDRAM

Figure 3 gives an example of the initialization procedure to place SDRAM in the CS3 space.

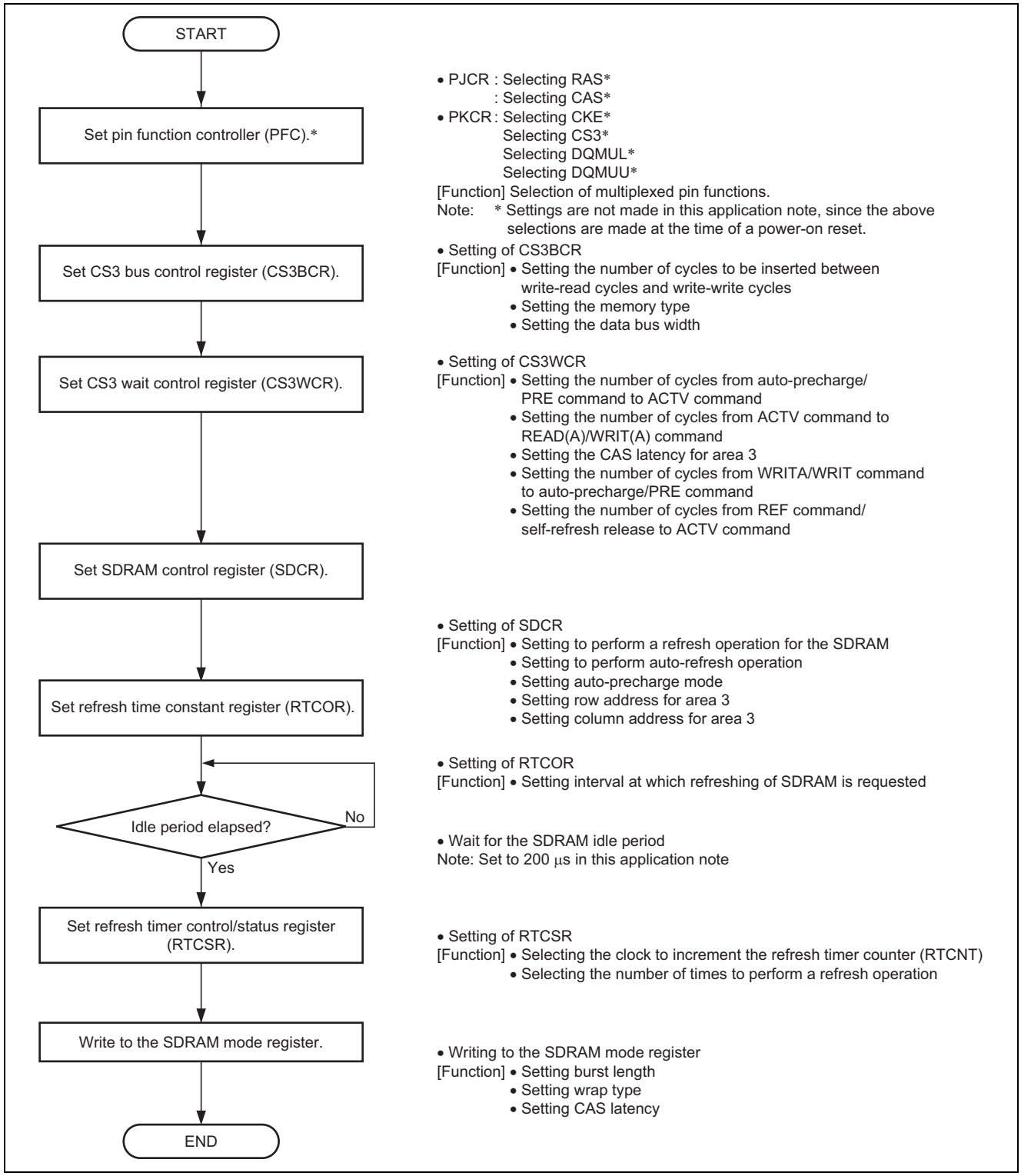


Figure 3 Example of Procedure for Initial Settings to Place SDRAM in the CS3 Space

2.3 Power-On Sequence

To perform SDRAM initialization, registers of the bus state controller must first be set, followed by a write to the SDRAM mode register.

Once power has been supplied, SDRAM needs a constant idle period. An idle period of at least 200 µs is set up by the software in this application note. The required period differs with the SDRAM specification. Please refer to the manual for the SDRAM you are using.

To write to the SDRAM mode register, a mode-register setting (MRS) command is issued in combination with $\overline{CS3}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{RDWR}$ pins. The address latched at that time is used as the data for input to SDRAM. Table 3 shows the addresses to be accessed in writing to the SDRAM mode register when SDRAM is allocated to the CS3 space.

Table 3 Addresses to be Accessed as Values Written to the SDRAM Mode Register (CS3 Space)

Data Bus Width	CAS Latency	Burst Read/Single Write (Burst Length 1)		Burst Read/Burst Write (Burst Length 1)	
		Access Address	External Address Pin	Access Address	External Address Pin
16 bits	2	H'FEC1 5440	H'0000 0440	H'FEC1 5040	H'0000 0040
	3	H'FEC1 5460	H'0000 0460	H'FEC1 5060	H'0000 0060
32 bits	2	H'FEC1 5880	H'0000 0880	H'FEC1 5080	H'0000 0080
	3	H'FEC1 58C0	H'0000 08C0	H'FEC1 50C0	H'0000 00C0

In this application note, the following settings are made in the SDRAM mode register.

- Burst length: burst read/single write (burst length 1)
- Wrap type: sequential
- CAS latency: 2 cycles

As shown in table 3, these settings are written to the SDRAM mode register by writing a word with any value to H'FEC1 5080 (the data are ignored). In detail, the following commands are consecutively issued to the SDRAM.

1. All bank precharge command (PALL)
   Idle cycles (Tpw) as specified by the TRP[1:0] bits in CS3WCR are inserted between the PALL and the first REF.
2. Auto-refresh command (REF; eight times)
   Idle cycles (Trc) as specified by the TRC[1:0] bits in CS3WCR are inserted after the REF command is issued.
3. Mode-register setting command (MRS)

Figure 4 shows an example of timing in writing to the SDRAM mode register.

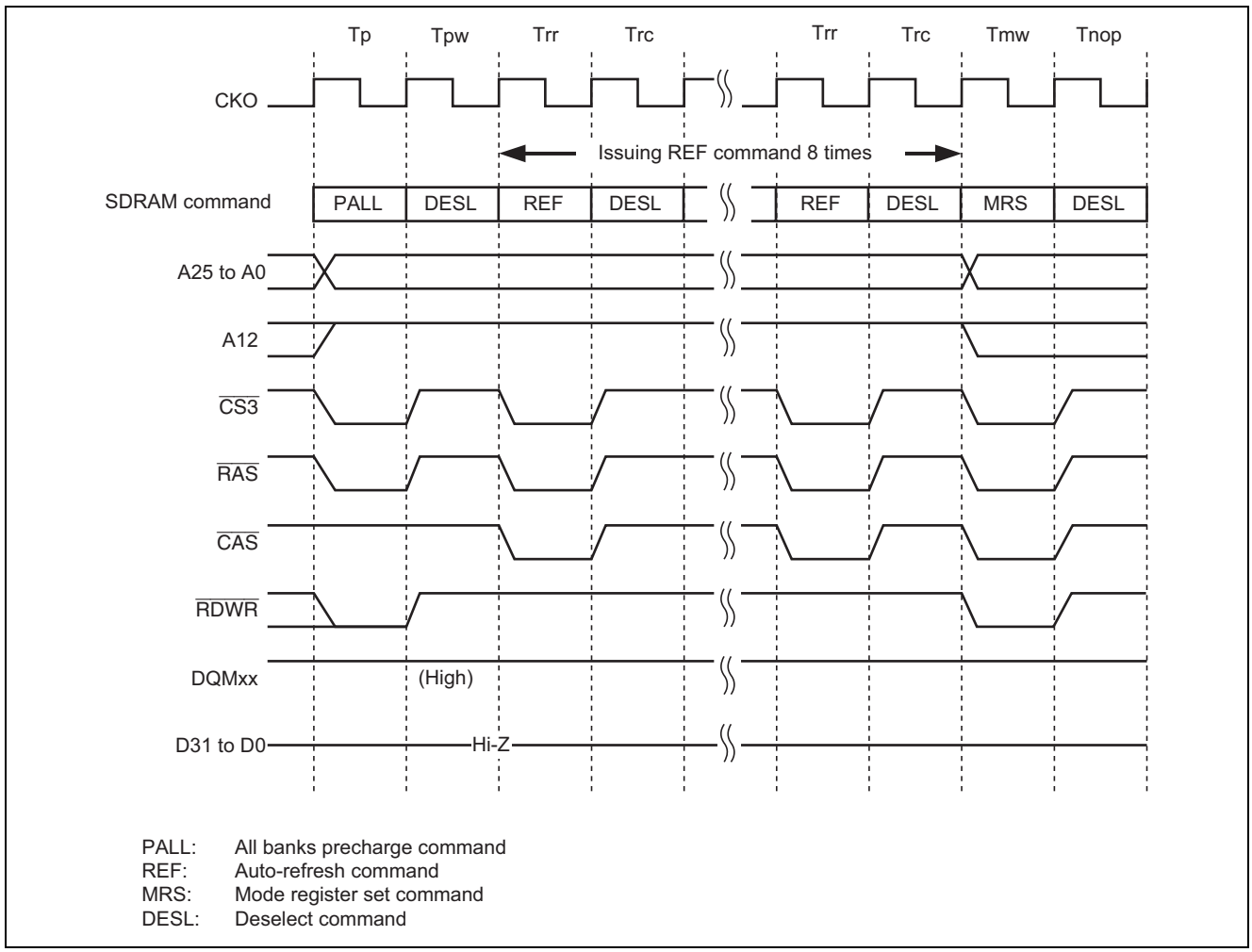


Figure 4 Example of Timing in Writing to the SDRAM Mode Register

2.4 Example of Bus State Controller Settings

Table 4 gives an example of bus state controller settings for bus-clock operation of the SH7730 at 66.66 MHz. For details on individual registers, please refer to the section on the bus state controller in the *SH7730 Group Hardware Manual*(REJ09B0359).

Table 4 Example of Bus State Controller Settings

Name of Register	Address	Setting	Function
CS2 space bus control register (CS2BCR)	H'FEC1 0008	H'36DB 0600	• Retains the initial value
CS2 space wait control register (CS2WCR)	H'FEC1 0028	H'0000 0540	• Retains the initial value
CS3 space bus control register (CS3BCR)	H'FEC1 000C	H'1000 4600	• Specifies the idle cycles between write-read cycles and write-write cycles. IWW[2:0] = B'001: 1 cycle • Specifies the memory type TYPE[3:0] = B'0100: SDRAM • Specifies the data bus width BSZ[1:0] = B'11: 32-bit data bus width
CS3 space wait control register (CS3WCR)	H'FEC1 002C	H'0000 248A	• Number of cycles from auto precharge /PRE command to ACTV command TRP[1:0] = B'01: 2 cycles • Number of cycles from ACTV command to READ(A)/WRITE(A) command TRCD[1:0] = B'01: 2 cycles • CAS latency of area 3 A3CL[1:0] = B'01: 2 cycles • Number of cycles from WRITA/WRIT command to auto precharge/PRE command TRWL[1:0] = B'10: 2 cycles • Number of cycles from REF command /self-refresh release to ACTV command TRC[1:0] = B'10: 6 cycles
SDRAM control register (SDCR)	H'FEC1 0044	H'0000 0809	• Refresh control RFSH = 1: Refresh RMODE = 0: Auto-refresh • Power-down mode PDOWN = 0: Does not place the SDRAM in power-down mode after access completion • Bank active mode BACTV = 0: Auto precharge mode • Number of row address bits for area 3 A3ROW[1:0] = B'01: 12 bits • Number of column address bits for area 3 A3COL[1:0] = B'01: 9 bits

Name of Register	Address	Setting	Function
Refresh timer control/status register (RTCSR)	H'FEC1 0048	H'A55A 0010*	• Compare match interrupt enable CMIE = 0: Disables the CMF interrupt request • Clock select CKS[2:0] = B'010: Selects Bϕ/16 as the clock • Refresh count RRC[2:0] = B'000: Once
Refresh time constant register (RTCOR)	H'FEC1 0050	H'A55A 003E*	• 1 cycle = 1/(Bϕ (66.66 MHz)/16) ≈ 240 ns • Interval between SDRAM-refresh requests: 64ms/4,096 cycles= 15.625 µs • Setting value of RTCOR = 15.625 µs ÷ 240 ns ≈ 65 = H'41 Note: The setting in this application note is H'3E, since this leads to a reasonable margin for the issuing of refresh requests (refer to section 2.5.3).

Note*: When writing, set the higher-order 16 bits of write data to H'A55A so that the write protection is canceled.

2.5 Settings of SDRAM Timing in the Application Note

To connect SDRAM, the number of wait cycles corresponding to the access speed (CAS latency) and other AC characteristics of the SDRAM in use must be set. The interval for refreshing must also be set. This section describes the main points regarding the settings in this application note for the cycles of waiting and refreshing.

In this application note, the bus clock for the SH7730 is set to 66.66 MHz (tcyc = 15 ns).

For AC characteristics of the SH7730 and SDRAM, refer to the datasheets for the individual devices. The SDRAM starts operating on a rising edge of CKO.

2.5.1 Description of Individual Cycles

1. The operation of SDRAM reading in this application note for the SH7730 is as follows.

   — Tr : An ACTV command is issued.
   — Trw : Wait cycles are inserted between the ACTV command and READ(A) or WRIT(A) command. The wait cycles are equivalent to the number set by the TRCD[1:0] bits in CS3WCR – 1.
   — Tc : A READ(A) command is issued.
   — Tcw : Wait cycles are inserted between the Tc and Td cycles. The wait cycles are equivalent to the number set for the CAS latency; the number of wait cycles for insertion is set by the A3CL[1:0] bits in CS3WCR.
   — Td : Read data are retrieved.
   — Tde : This is an idle cycle that is necessary for transfer of the read data within this LSI. One cycle must be allowed without fail for both burst-read and single-read operations.
   — Tap : This is a cycle of waiting for completion of auto-precharge. The wait cycles for insertion are equivalent to the number set by the TRP[1:0] bits in CS3WCR – 1.

2. The operation of SDRAM writing in this application note for the SH7730 is as follows.

   — Tr : An ACTV command is issued.
   — Trw : Wait cycles are inserted between the ACTV command and READ(A) or WRIT(A) command. The wait cycles are equivalent to the number set by the TRCD[1:0] bits in CS3WCR – 1.
   — Tc : A WRIT(A) command is issued.
   — Trwl : This is a cycle of waiting for activation of auto-precharge. The number of wait cycles for insertion is set by the TRWL[1:0] bits in CS3WCR.
   — Tap : This is a cycle of waiting for completion of auto-precharge. The wait cycles for insertion are equivalent to the number set by the TRP[1:0] bits in CS3WCR – 1.

2.5.2 Cycles of Waiting for Access

1. Set the cycle of waiting (Trw) between the Tr and Tc cycles.
2. Set the cycle of waiting (Tcw) between the Tc and Td cycles.
3. Set the cycle of waiting (Tap) between the Tde and Tr cycles.
4. Set the cycle of waiting (Trwl) until auto precharging is activated.

With this setting, it is confirmed that bus timings of the SH7730 and SDRAM are satisfied. (In this application note, the following settings are made; Trw = 1, Tcw = 1, Tap = 1, Trwl = 2, tcyc = 15 ns, and CL = 2.)

Furthermore, Tr, Tc, Td, and Tde used in the following formulae are tcyc.

- tRC of the SDRAM (for read cycles)

  $tRC\ (min) \leq (tcyc \times Trw) + (Tc) + (tcyc \times (CL - 1)) + (Td) + (Tde) + (tcyc \times Tap) + (Tr)$..... (figure 5)

Note: Tr = Tc = Td = Tde = tcyc

- tRAS of the SDRAM (row activation time)

  $tRAS\ (min) \leq (tcyc \times Trw) + (Tc) + (tcyc \times BL)$ ..... (figure 6)

Note: BC means the number of rounds of burst access (count of repetition of access with burst length 1).

- tRCD of the SDRAM (delay time from RAS to CAS)

  $tRCD\ (min) \leq (tcyc \times Trw) + (Tc)$ ..... (figure 5)

- tRP of the SDRAM (row precharge time for read cycles)

  $tRP\ (min) \leq (tcyc \times (CL - 2)) + (Td) + (Tde) + (tcyc \times Tap) + (Tr)$ ..... (figure 5)

- tRC of the SDRAM (for write cycles)

  $tRC\ (min) \leq (tcyc \times Trw) + (tcyc \times BC) + (tcyc \times Trwl) + (tcyc \times Tap) + (Tr)$..... (figure 7)

Note: BC means the number of rounds of burst access (count of repetition of access with burst length 1).

- tRP of the SDRAM (row precharge time for write cycles)

  $tRP\ (min) \leq (tcyc \times Tap) + (Tr)$ ..... (figure 7)

- tRDL of the SDRAM (write recovery time)

  $tRDL\ (min) \leq (tcyc \times Trwl)$ ..... (figure 7)

- tDAL of the SDRAM (delay time from end of data input to Act)

  $tDAL\ (min) \leq (tcyc \times Trwl) + (tcyc \times Tap) + (Tr)$..... (figure 7)

- tRRD of the SDRAM (delay time from Act to Act)

  $tRRD\ (min) \leq (tcyc \times Tpw) + (Trr)$..... (figure 9)

Note: Tpw = Tap

2.5.3 Refresh Cycle

1. Set the interval (tREF) for refreshing of the SDRAM.
2. Set cycle of waiting (Trc) between auto-refresh cycles.

Confirm that these settings satisfy the bus-timing requirements of the SH7730 and SDRAM.

- tREF of the SDRAM (refresh intervals)

  $tREF\ (max) \geq tcyc \times CKS \times RTCOR \times Ref\_Cyc$

Note *: According to the SDRAM specification, refresh operations must be performed 4,096 times (Ref_Cyc) within the period of 64 ms (tREF). The value in the above formula must therefore satisfy this condition. The result under "Reference" below indicates that tREF (64 ms) ≥ 60.9 ms will meet the condition.

Reference

When Tcyc = 15 ns, CKS = 16, RTCOR = 62, and Ref_Cyc = 4,096,

- Period corresponding to number of clock cycles for the refresh counter: tcyc × CKS = 240 (ns)
- Interval between refreshing: tcyc × CKS × RTCOR = 14.9 (µs)*
- Intervals corresponding to refreshing 4,096 times: tcyc × CKS × RTCOR × Ref_Cyc = 60.9 (ms)

  Please note that when a refresh request is generated during a bus cycle, the refresh operation is halted until the end of the bus cycle. In consideration of such delays in the timing of refresh operations, the setting for RTCOR in this application note allows a reasonable margin.

- tRC of the SDRAM (for the refresh cycle)

  $tRC\ (min) \leq (tcyc \times Trc) + (Tr)$ ..... (figure 9)

Note: Tr = Trc = tcyc

2.6 Timing Charts

Figure 5 shows the timing for single reading of the SDRAM with bus-clock operation at 66.66 MHz.

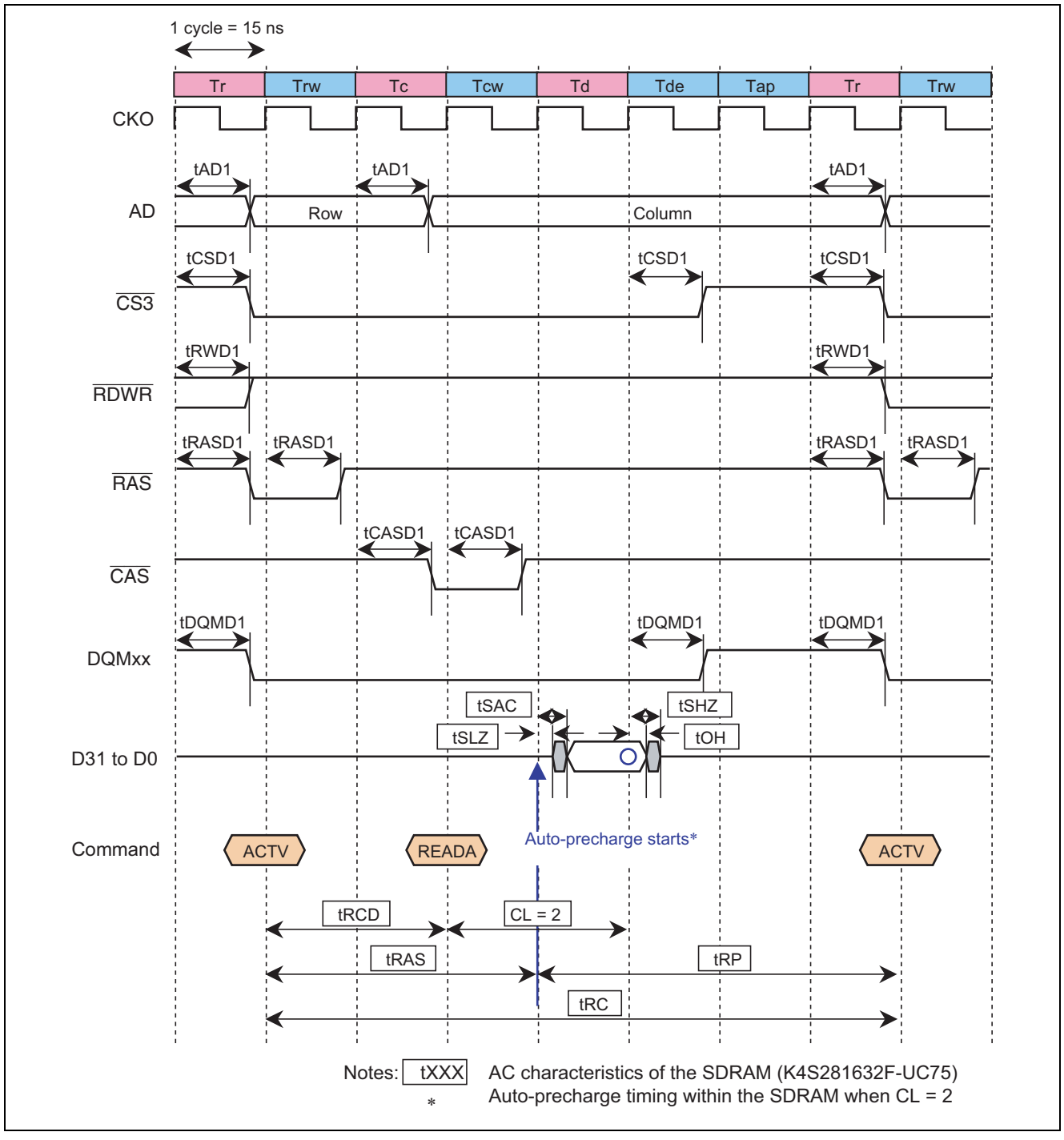


Figure 5 Timing for Single Reading of the SDRAM

Figure 6 shows the timing for burst reading of the SDRAM (CL = 2).

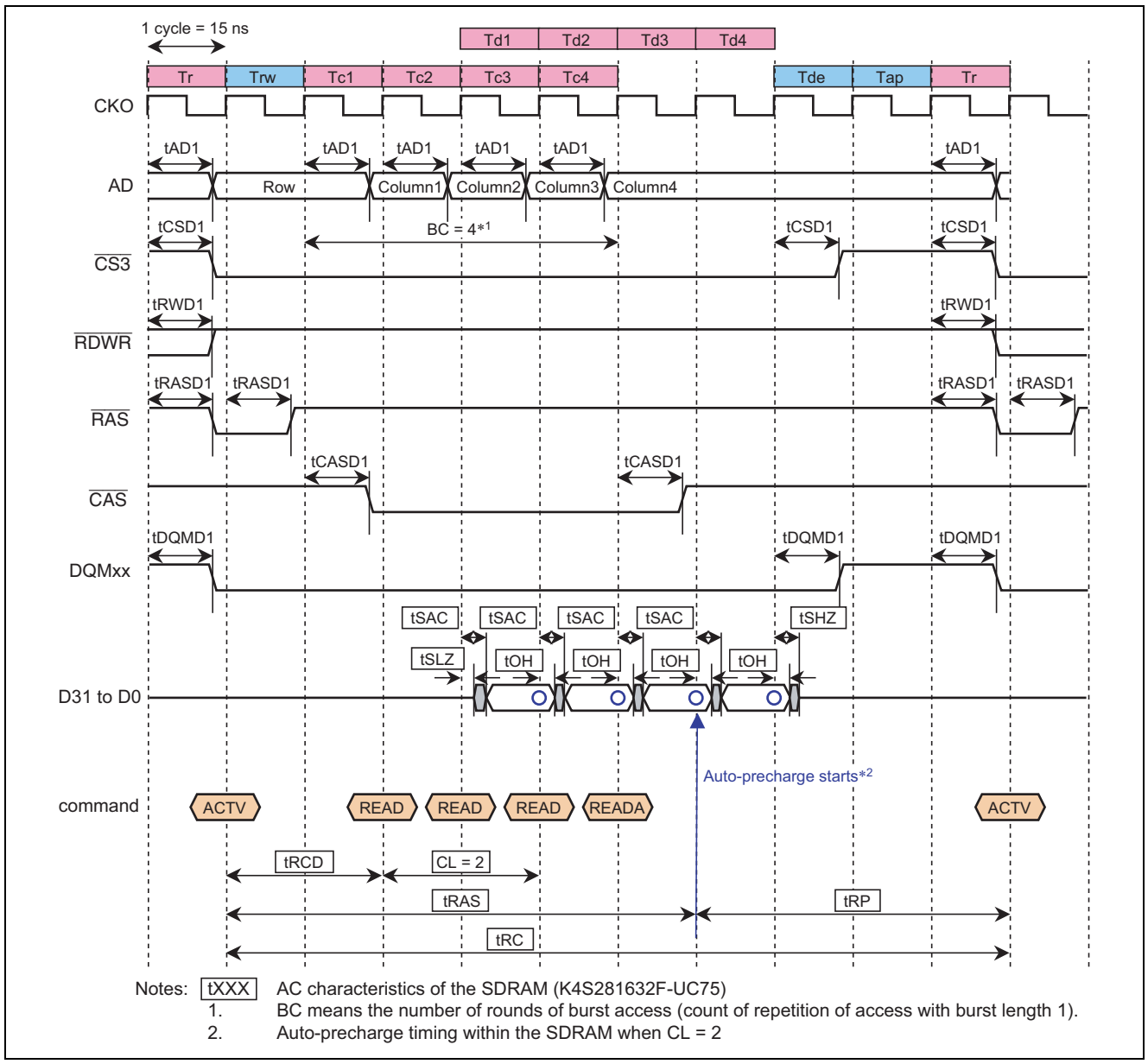


Figure 6 Timing for Burst Reading of the SDRAM

Figure 7 shows the timing for single writing of the SDRAM.

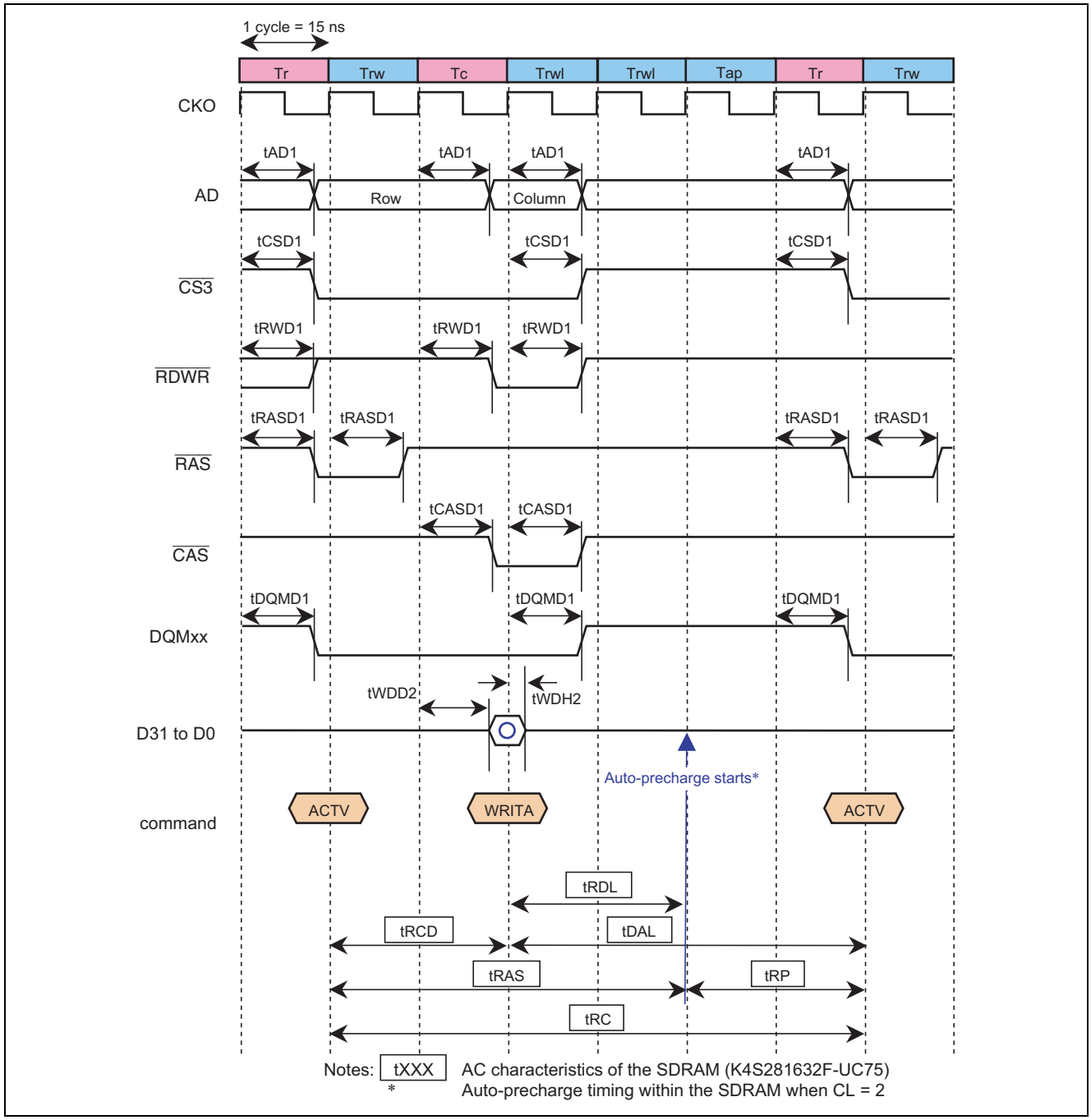
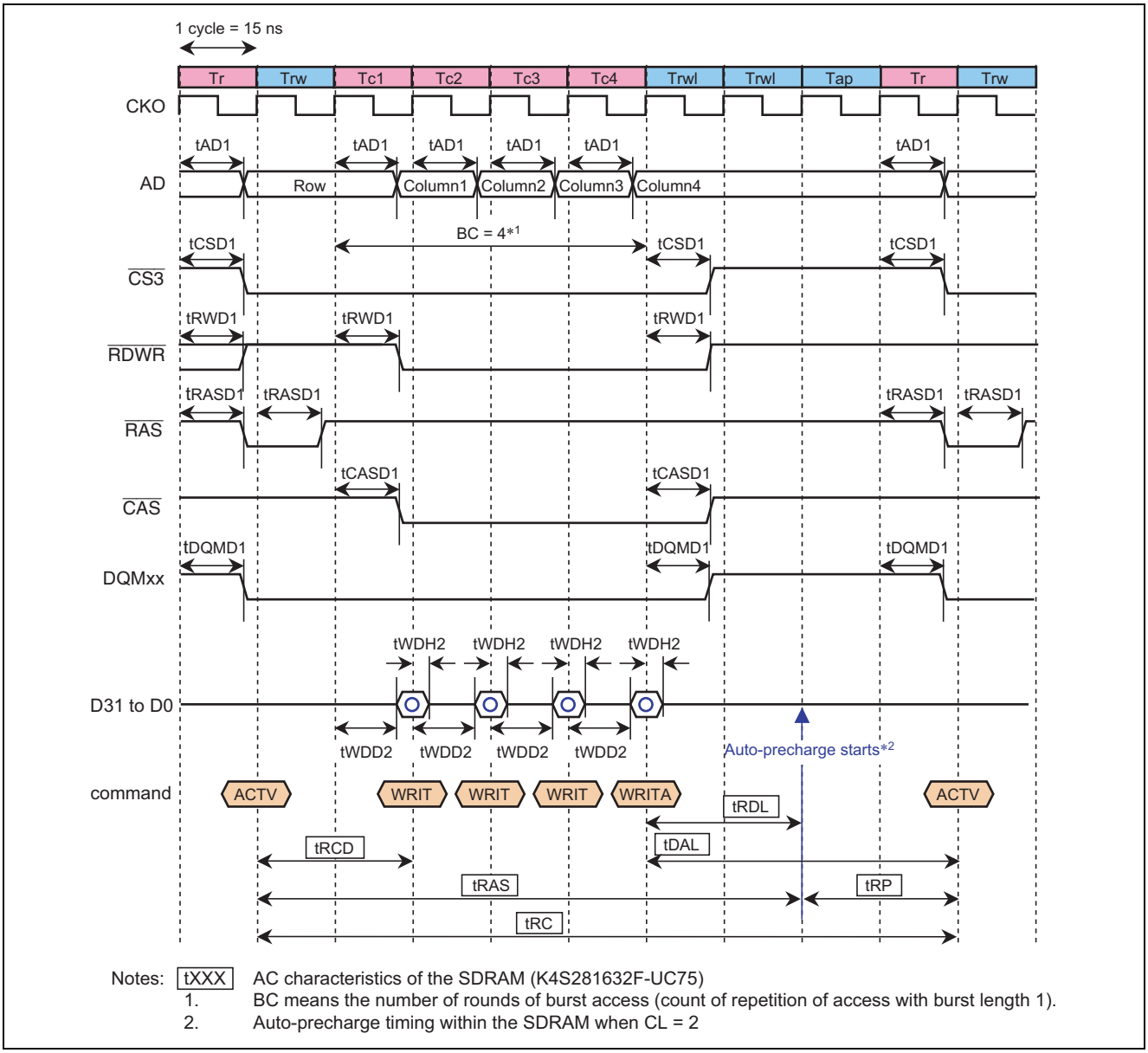


Figure 7 Timing for Single Writing of the SDRAM

Figure 8 shows the timing for burst writing of the SDRAM.



Notes: tXXX AC characteristics of the SDRAM (K4S281632F-UC75)
1. BC means the number of rounds of burst access (count of repetition of access with burst length 1).
2. Auto-precharge timing within the SDRAM when CL = 2

Figure 8 Timing for Burst Writing of the SDRAM

Figure 9 shows the timing for refreshing of the SDRAM.

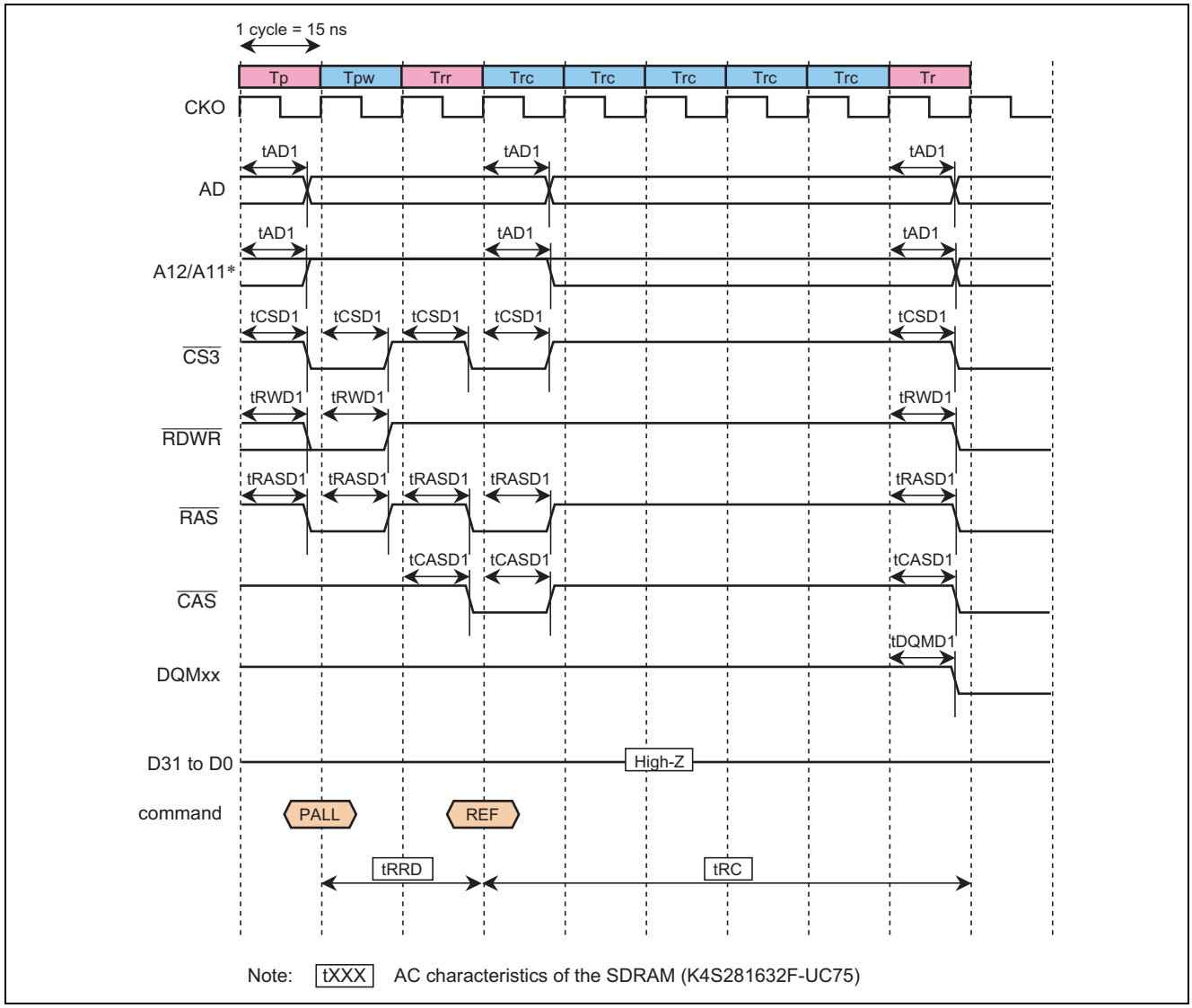


Figure 9 Timing for Refreshing of the SDRAM

3. Documents for Reference

- Software Manual
  SH-4A Software Manual (REJ09B0003)
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7730 Group Hardware Manual (REJ09B0359)
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