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Renesas Electronics Corporation

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H8/300H Tiny Series

Entering Subactive Mode

Introduction

Subactive mode is entered.

Target Device

H8/3664

Contents

1. Specifications

- Subactive mode is entered.
- To switch to sleep mode from active mode, a SLEEP instruction is executed.
- When the switch that is connected to the $\overline{\text{IRQ0}}$ pin is turned on in sleep mode, an IRQ0 interrupt occurs, sleep mode is cleared, and a transition is made to subactive mode.
- In subactive mode, a timer A interrupt is requested every 0.5 s. The timer A interrupt handling turns on and off the LED every 0.5 s.
- When the switch that is connected to the $\overline{\text{IRQ1}}$ pin is turned on in subactive mode, an IRQ1 interrupt occurs. Then after the IRQ1 interrupt handling ends, executing a SLEEP instruction enables a direct transition to active mode.
- The LED is connected to the P74 output pin of port 7.

Figure 1 shows an example of connecting switches to the $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ input pins.

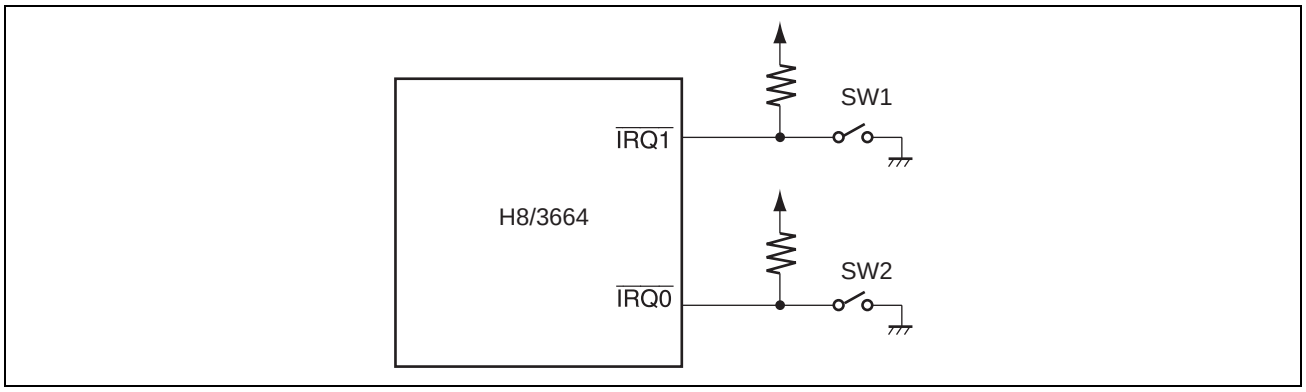


Figure 1 Example of Switch Connection for Entering Subactive Mode

2. Description of Functions Used

In this sample task, this LSI enters subactive mode, a power-down mode. Figure 2 shows a diagram of transition to subactive mode. The subactive mode functions are described below.

- If an interrupt (timer A, timer V, timer W, IRQ3 to IRQ0, WKP5 to WKP0, watchdog timer, SCI3, I^2C, or A/D converter) occurs while the LSON bit in SYSCR2 is set to 1 in sleep mode, a transition is made to subactive mode. If an interrupt (timer A, timer W, IRQ3 to IRQ0, WKP5 to WKP0, watchdog timer, or I^2C) occurs in subsleep mode, a transition is made to subactive mode.
- No transition is made to subactive mode if the I bit in the condition code register (CCR) is set to 1 or the requested interrupt is disabled in the corresponding interrupt enable register.
- Subactive mode is cleared by execution of a SLEEP instruction or by input at the $\overline{\text{RES}}$ pin.
- In the case of clearing subactive mode by executing a SLEEP instruction, when a SLEEP instruction is executed while the SSBY bit is set to X (either 1 or 0) in SYSCR1, the DTON bit is set to 1, the SMSEL bit is set to X (either 1 or 0), and the LSON bit is cleared to 0 in SYSCR2, this LSI makes a direct transition from subactive mode to active mode.
- In using the $\overline{\text{RES}}$ pin to initiate the transition from subactive mode, the IC enters the reset state and cancels subactive mode when a low level is placed on the $\overline{\text{RES}}$ pin. Once the pulse generator output has become stable, the $\overline{\text{RES}}$ pin is driven high, after which the CPU starts reset exception handling. Since system clock signals are supplied to the entire LSI as soon as the system clock pulse generator starts functioning, the $\overline{\text{RES}}$ pin must be kept low until the pulse generator output is stable.
- The oscillation stabilization waiting time after exit from subactive mode is set by the STS2 to STS0 bits in SYSCR1.
- In this sample task, the operating frequency is 16 MHz, and the waiting time is 131,072 states (oscillation stabilization waiting time: 8.2 ms).
- The CPU can execute programs in two modes: active mode and subactive mode. A direct transition is a transition between these two modes without stopping program execution. A direct transition can be made by executing a SLEEP instruction while the DTON bit in SYSCR2 is set to 1. The direct transition also enables modification of the operating frequency in active mode or subactive mode. After the mode transition, direct transition interrupt handling starts. If the direct transition interrupt is disabled in interrupt enable register 1 (IENR1), a transition is made instead to sleep mode or subsleep mode. Note that if a direct transition is attempted while the I bit in CCR is set to 1, sleep mode or subsleep mode will be entered, and the resulting mode cannot be cleared by means of an interrupt.
- If a SLEEP instruction is executed while the SSBY bit is set to X (either 1 or 0) in SYSCR1, and the SMSEL bit is set to X (either 1 or 0), the LSON bit is cleared to 0, and the DTON bit is set to 1 in SYSCR2 in subactive mode, a direct transition is made to active mode after the waiting time set in the STS2 to STS0 bits in SYSCR1 has elapsed.

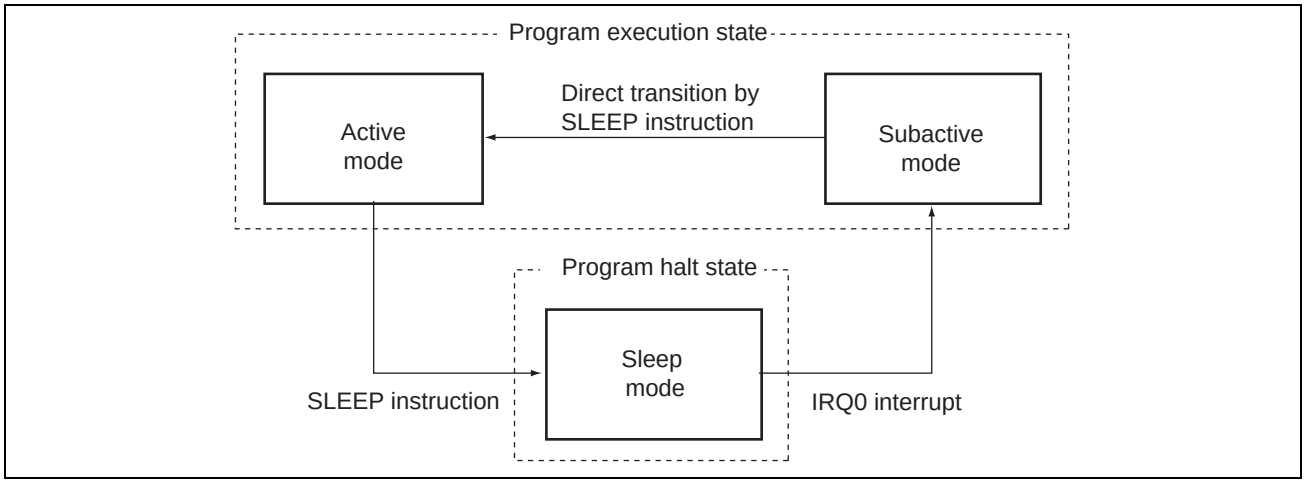


Figure 2 Transitions to and from Subactive Mode

Table 1 lists the function allocation for this sample task. The functions listed in table 1 are allocated for a transition to subactive mode.

Table 1 Function Allocation

Function	Description
SYSCR1	Controls power-down mode
SYSCR2	Controls power-down mode
PCR7	Sets P74 output pin function
PDR7	Stores P74 output pin data
P74	LED output pin
$\overline{\text{IRQ0}}$	Input pin for switch 1
IRRI0	Indicates whether or not an IRQ0 interrupt is requested
IEN0	Enables $\overline{\text{IRQ0}}$ pin interrupt requests
$\overline{\text{IRQ1}}$	Input pin for switch 2

3. Description of Operations

Figure 3 shows this sample task's principle of operation. The hardware and software processing shown in figure 3 performs a transition to subactive mode.

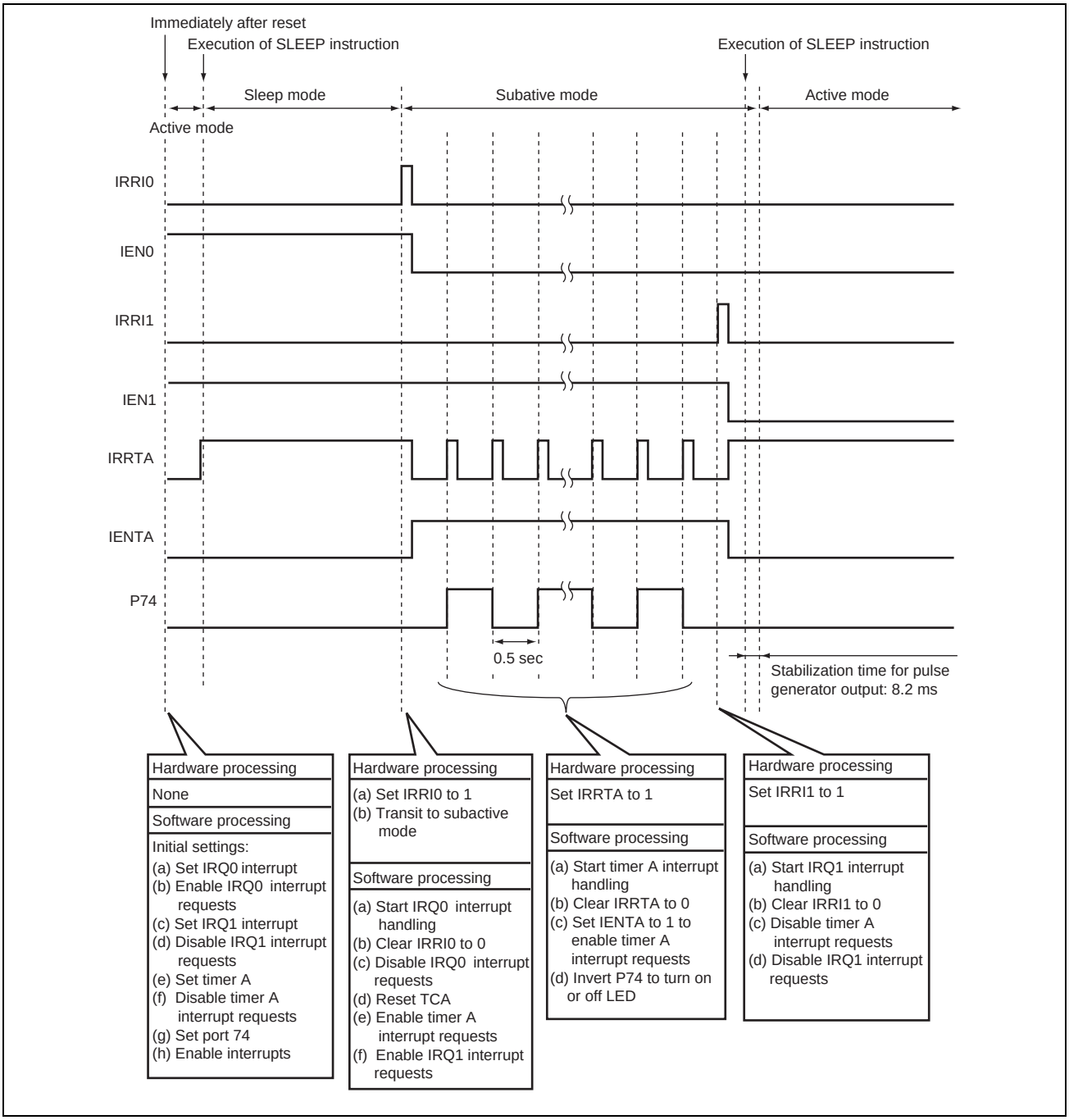


Figure 3 Operation Principle: Transition to Subactive Mode

4. Description of Software

4.1 Description of Modules

Table 2 describes the software used in this sample task.

Table 2 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets IRQ0, IRQ1, and timer A interrupts and port 7, enables interrupts, and transits to sleep mode and active mode.
Switch 1 on	IRQ0	During the IRQ0 interrupt handling routine, disables IRQ0 interrupts.
Switch 2 on	IRQ1	During the IRQ1 interrupt handling routine, sets SWONF, and disables timer A and IRQ1 interrupts.
LED control	taint	During the timer A interrupt handling routine, enables interrupts and controls the LED.
Direct transition	dtint	During the direct transition interrupt handling routine, clears the direct transition interrupt request flag.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 3 describes the internal registers used in this sample task.

Table 3 Description of Internal Registers

Register Name		Function	Address	Setting
TMA		Timer mode register A: When TMA is set to H'19, timer A is set to clock time-base, and the TCA overflow cycle to 0.5 s.	H'FFA6	H'19
TCA		Timer counter A: 8-bit counter that overflows every 0.5 s by clock time-base and has clock input of PSW output clock	H'FFA7	H'00
PDR7	P74	Port data register 7 (port data register 74): When P74 is cleared to 0, the P74 pin output level is low. When P74 is set to 1, the P74 pin output level is high.	H'FFDA Bit 4	 1
PCR7	PCR74	Port control register 7 (port control register 74): When PCR74 is set to 1, the P74 pin functions as an output pin.	H'FFEA Bit 4	 1

Table 3 Description of Internal Registers (cont)

Register	Name	Function	Address	Setting
SYSCR1	SSBY	System control register 1 (software standby): When SSBY is cleared to 0, after execution of a SLEEP instruction in active mode, a transition is made to sleep mode or subsleep mode. After execution of a SLEEP instruction in subactive mode, a direct transition is made to active mode.	H'FFF0 Bit 7	 0
	STS2 STS1 STS0	System control register 1 (standby timer select 2 to 0): When STS2 is set to 1 and STS1 and STS0 are both cleared to 0, the wait time is set to 131.072 states.	H'FFF0 Bit 6 Bit 5 Bit 4	 STS2 = 1 STS1 = 0 STS0 = 0
SYSCR2	SMSEL	System control register 2 (sleep mode selection): When SMSEL is cleared to 0, after execution of a SLEEP instruction, a transition is made to sleep mode.	H'FFF1 Bit 7	 0
	LSON	System control register 2 (low speed on flag): When LSON is set to 1, sleep mode, subsleep mode, or subactive mode (direct transition) is selected as the mode to transit to after execution of a SLEEP instruction.	H'FFF1 Bit 6	 1
	DTON	System control register 2 (direct transfer on flag): When DTON is cleared to 0, sleep mode, subsleep mode, standby mode is selected as the mode to transit to after execution of a SLEEP instruction.	H'FFF1 Bit 5	 0
	MA2 MA1 MA0	System control register 2 (active mode clock select 2 to 0:) When MA2 is cleared to 0, and MA1 and MA0 are both set to 1, ϕOSC is selected as the clock in active mode.	H'FFF1 Bit 4 Bit 3 Bit 2	 MA2 = 0 MA1 = 1 MA0 = 1
	SA1 SA0	System control register 2 (subactive mode clock select 1 and 0:) When SA1 and SA0 are both cleared to 0, ϕw/8 is selected as the CPU operating clock in subactive mode.	H'FFF1 Bit 1 Bit 0	 SA1 = 0 SA0 = 0
PMR1	IRQ1	Port mode register 1 ($\overline{\text{IRQ1}}$ pin function switch): When IRQ1 is cleared to 0, the $\overline{\text{IRQ1}}$ pin functions as the I/O port. When IRQ1 is set to 1, the $\overline{\text{IRQ1}}$ pin functions as the $\overline{\text{IRQ1}}$ input pin.	H'FFE0 Bit 1	 1
	IRQ0	Port mode register 1 ($\overline{\text{IRQ0}}$ pin function switch): When IRQ0 is cleared to 0, the $\overline{\text{IRQ0}}$ pin functions as the I/O port. When IRQ0 is set to 1, the $\overline{\text{IRQ0}}$ pin functions as the $\overline{\text{IRQ0}}$ input pin.	H'FFE0 Bit 0	 1

Table 3 Description of Internal Registers (cont)

Register	Name	Function	Address	Setting
IEGR1	IEG1	Interrupt edge select register 1 (IRQ1 edge select): When IEG1 is cleared to 0, the falling edge of the $\overline{\text{IRQ1}}$ pin input is detected. When IEG1 is set to 1, the rising edge of the $\overline{\text{IRQ1}}$ pin input is detected.	H'FFF2 Bit 1	1
	IEG0	Interrupt edge select register 1 (IRQ0 edge select): When IEG0 is cleared to 0, the falling edge of the $\overline{\text{IRQ0}}$ pin input is detected. When IEG0 is set to 1, the rising edge of the $\overline{\text{IRQ0}}$ pin input is detected.	H'FFF2 Bit 0	1
IENR1	IENDT	Interrupt enable register 1 (direct transition interrupt enable): When IENDT is cleared to 0, direct transition interrupt requests are disabled. When IENDT is set to 1, direct transition interrupt requests are enabled.	H'FFF4 Bit 7	1
	IENTA	Interrupt enable register 1 (timer A interrupt enable): When IENTA is cleared to 0, timer A interrupt requests are disabled. When IENTA is set to 1, timer A interrupt requests are enabled.	H'FFF4 Bit 6	1
	IEN1	Interrupt enable register 1 (IRQ1 interrupt enable): When IEN1 is cleared to 0, interrupt requests from the $\overline{\text{IRQ1}}$ pin are disabled. When IEN1 is set to 1, interrupt requests from the $\overline{\text{IRQ1}}$ pin are enabled.	H'FFF4 Bit 1	1
	IEN0	Interrupt enable register 1 (IRQ0 interrupt enable): When IEN0 is cleared to 0, interrupt requests from the $\overline{\text{IRQ0}}$ pin are disabled. When IEN0 is set to 1, interrupt requests from the $\overline{\text{IRQ0}}$ pin are enabled.	H'FFF4 Bit 0	1

Table 3 Description of Internal Registers (cont)

Register	Name	Function	Address	Setting
IRR1	IRRDT	Interrupt request register 1 (direct transition interrupt request flag): When IRRDT is cleared to 0, no direct transition interrupt is requested. When IRRDT is set to 1, a direct transition interrupt is requested.	H'FFF6 Bit 7	0
	IRRTA	Interrupt request register 1 (timer A interrupt request flag): When IRRTA is cleared to 0, no timer A interrupt is requested. When IRRTA is set to 1, a timer A interrupt is requested.	H'FFF6 Bit 6	0
	IRRI1	Interrupt flag register 1 (IRQ1 interrupt request flag): When IRRI1 is cleared to 0, no IRQ1 interrupt is requested. When IRRI1 is set to 1, an IRQ1 interrupt is requested.	H'FFF6 Bit 1	0
	IRRI0	Interrupt flag register 1 (IRQ0 interrupt request flag): When IRRI0 is cleared to 0, no IRQ0 interrupt is requested. When IRRI0 is set to 1, an IRQ0 interrupt is requested.	H'FFF6 Bit 0	0

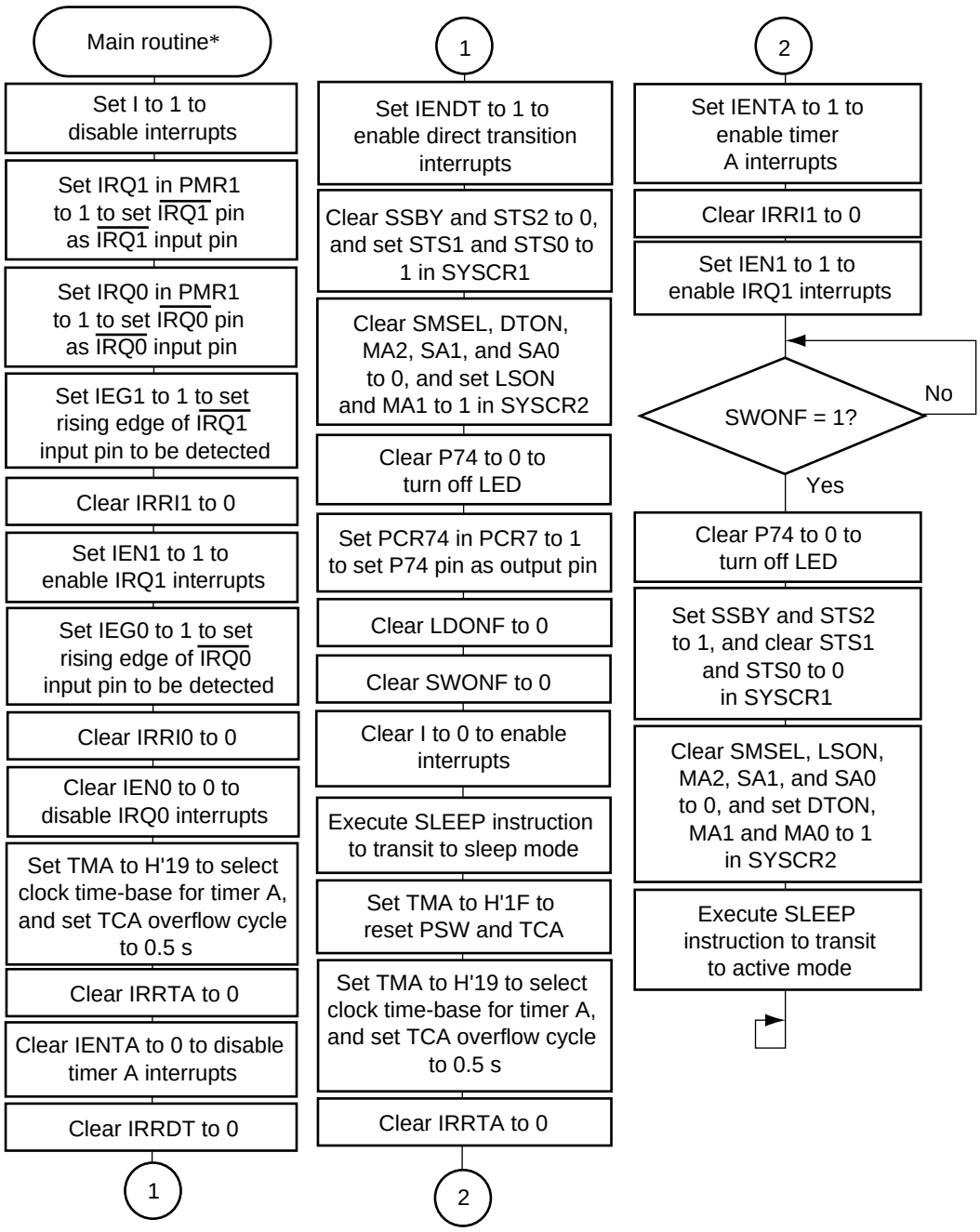
4.4 Description of RAM

Table 4 describes the RAM used in this sample task.

Table 4 Description of RAM

Label	Name	Function	Address	Used in
USRF	SWONF	Flag for judging on/off switch 2	H'FB80 Bit 1	Main routine Switch 2 on
	LDONF	Flag for judging on/off of the LED	H'FB80 Bit 0	LED control

5. Flowcharts



Note: * In this sample task, the stack pointer is set in INIT.SRC (assembly).

Figure 4 Flowchart for Main Routine

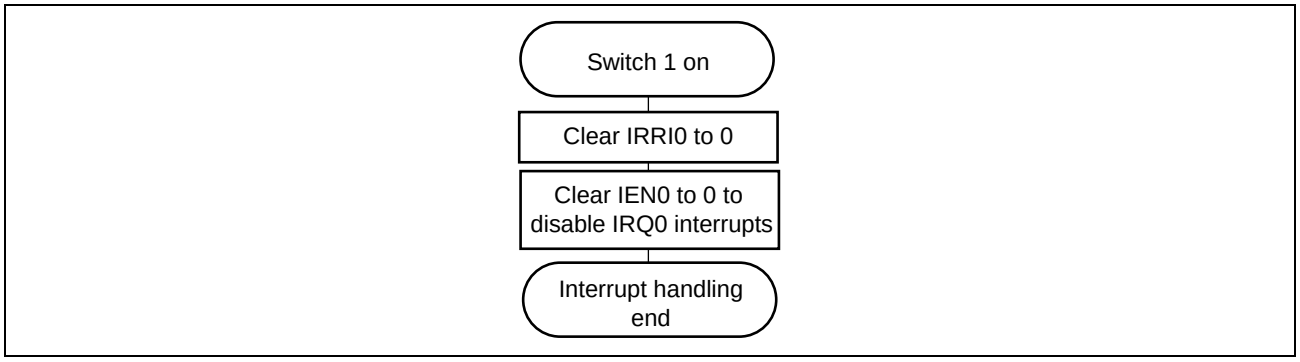


Figure 5 Flowchart for IRQ0 Interrupt Handling Routine

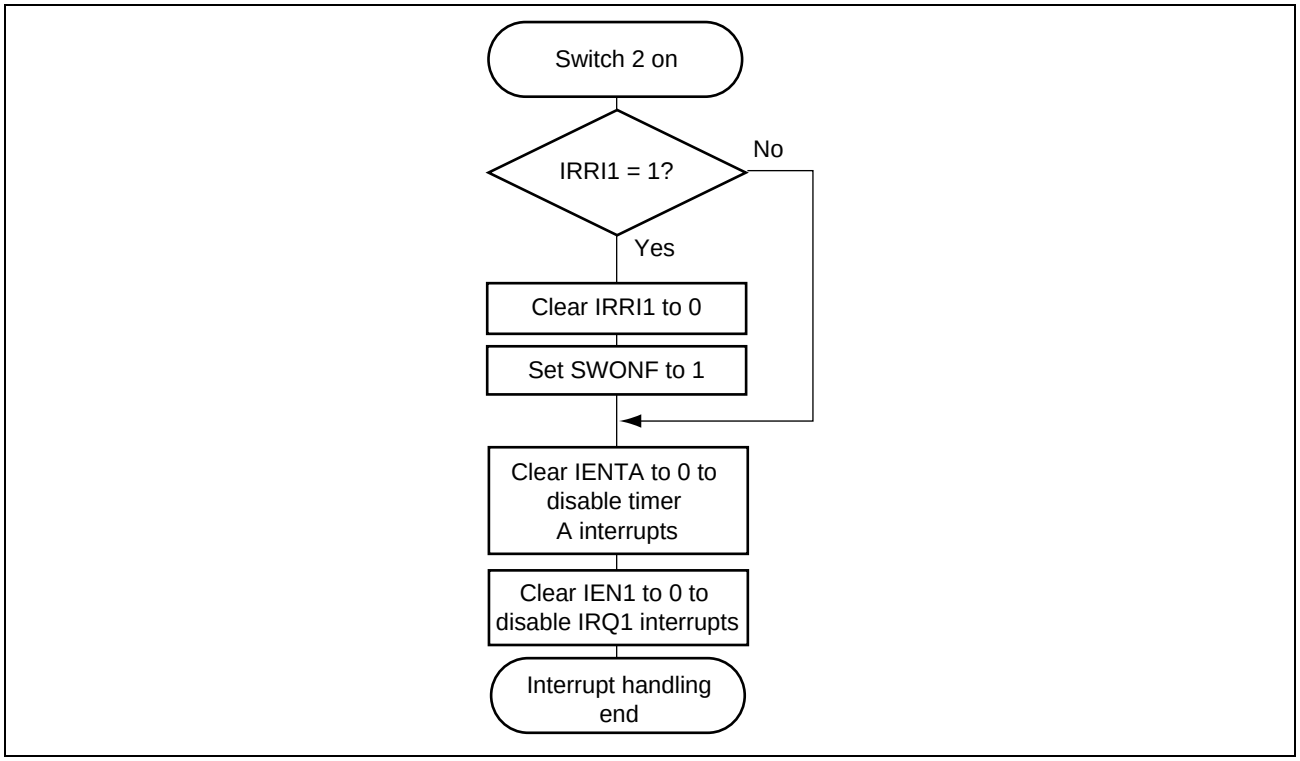


Figure 6 Flowchart for IRQ1 Interrupt Handling Routine

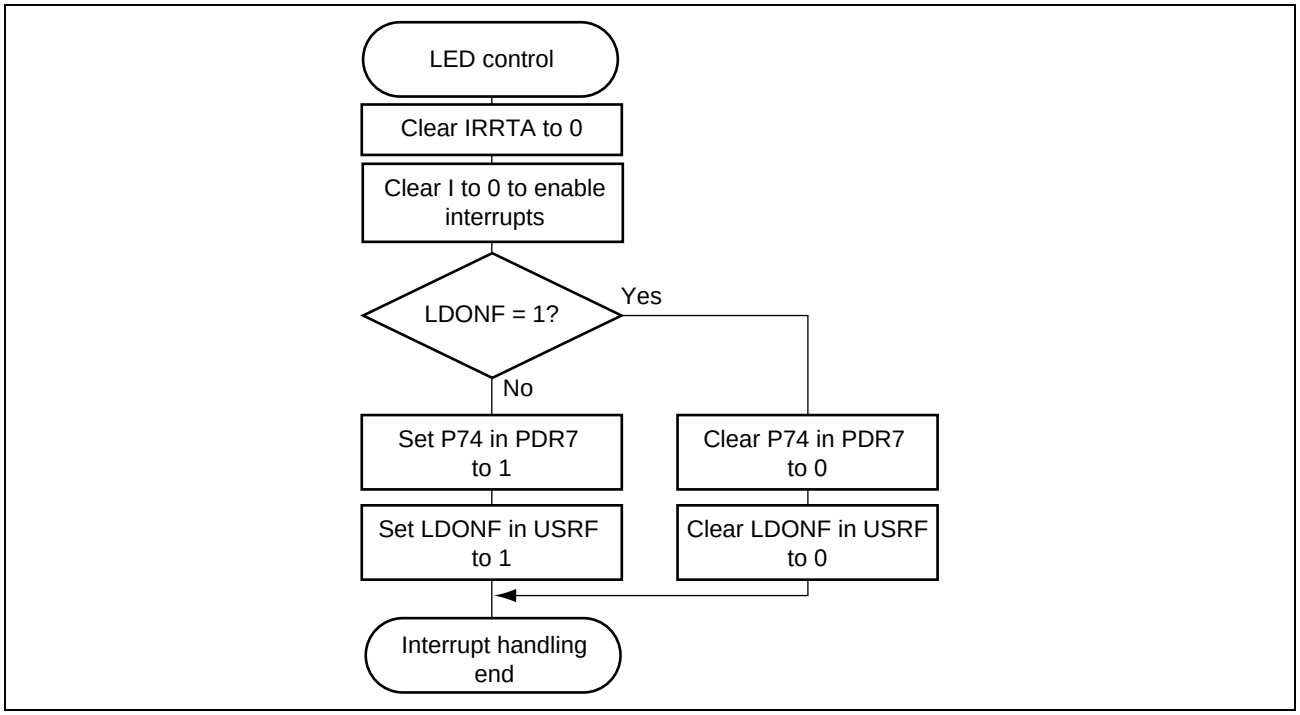


Figure 7 Flowchart for Timer A Interrupt Handling Routine

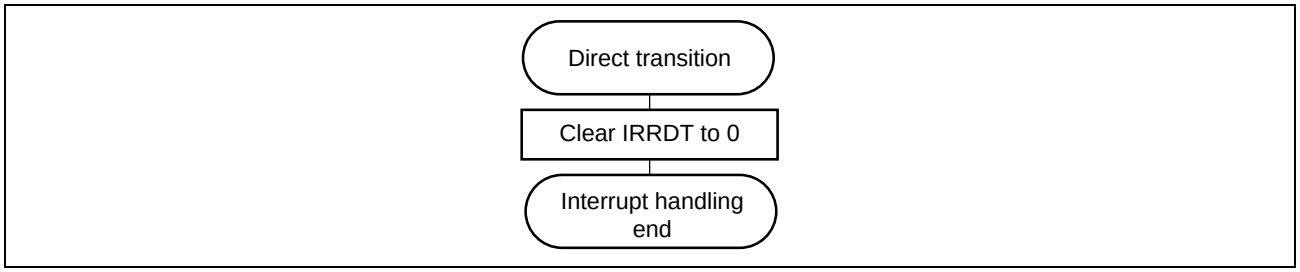


Figure 8 Flowchart for Direct Transition Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
      .EXPORT  _INIT
      .IMPORT  _main
 ;
      .SECTION    P,CODE
 _INIT:
      MOV.W    #H'FF80,R7
      LDC.B    #B'10000000,CCR
      JMP      @_main
 ;
      .END
```

```
/*******************************************************/
/*                                                     */
/*    H8/300H Tiny Series -H8/3664-                    */
/*    Application Note                                 */
/*                                                     */
/*    'Transition to Subactive Mode'                   */
/*                                                     */
/*    Function                                         */
/*    : Power-Down Mode                                */
/*       Subactive Mode                                */
/*                                                     */
/*    External Clock : 16MHz                           */
/*    Internal Clock : 16MHz                           */
/*    Sub Clock      : 32.768kHz                       */
/*                                                     */
/*******************************************************/

#include    <machine.h>
```

```
/*******************************************************/
/*    Symbol Definition                                */
/*******************************************************/
struct BIT {
    unsigned char    b7:1;      /* bit7 */
    unsigned char    b6:1;      /* bit6 */
    unsigned char    b5:1;      /* bit5 */
    unsigned char    b4:1;      /* bit4 */
    unsigned char    b3:1;      /* bit3 */
    unsigned char    b2:1;      /* bit2 */
    unsigned char    b1:1;      /* bit1 */
    unsigned char    b0:1;      /* bit0 */
};

#define   TMA        *(volatile unsigned char *)0xFFA6 /* Timer Mode Register A                        */
#define   TCA        *(volatile unsigned char *)0xFFA7 /* Timer Counter A                              */
#define   PDR7_BIT   (*(struct BIT *)0xFFDA)           /* Port Data Register 7                         */
#define   P74        PDR7_BIT.b4                       /* Port Data Register 7 bit4                    */
#define   PMR1_BIT   (*(struct BIT *)0xFFE0)           /* Port Mode Register 1                         */
#define   IRQ1_SET   PMR1_BIT.b5                       /* Port Mode Register 1 bit5                    */
#define   IRQ0_SET   PMR1_BIT.b4                       /* Port Mode Register 1 bit4                    */
#define   PCR7_BIT   (*(struct BIT *)0xFFEA)           /* Port Control Register 7                      */
#define   PCR74      PCR7_BIT.b4                       /* Port Control Register 7 bit4                 */
#define   SYSCR1     *(volatile unsigned char *)0xFFF0 /* System Control Register 1                    */
#define   SYSCR1_BIT (*(struct BIT *)0xFFF0)           /* System Control Register 1                    */
#define   SSBY       SYSCR1_BIT.b7                     /* Software Standby                             */
#define   STS2       SYSCR1_BIT.b6                     /* Standby Timer Select 2                       */
#define   STS1       SYSCR1_BIT.b5                     /* Standby Timer Select 1                       */
#define   STS0       SYSCR1_BIT.b4                     /* Standby Timer Select 0                       */
#define   NESEL      SYSCR1_BIT.b3                     /* Noise Elimination Sampling Frequency Select */
#define   SYSCR2     *(volatile unsigned char *)0xFFF1 /* System Control Register 2                    */
#define   SYSCR2_BIT (*(struct BIT *)0xFFF1)           /* System Control Register 2                    */
#define   LSON       SYSCR2_BIT.b6                     /* Low Speed On Flag                            */
#define   DTON       SYSCR2_BIT.b5                     /* Direct Transfer On Flag                      */
#define   MA1        SYSCR2_BIT.b3                     /* Active Mode Clock Select 1                   */
#define   MA0        SYSCR2_BIT.b2                     /* Active Mode Clock Select 0                   */
#define   SA1        SYSCR2_BIT.b1                     /* Subactive Mode Clock Select 1                */
#define   SA0        SYSCR2_BIT.b0                     /* Subactive Mode Clock Select 0                */
#define   IEGR1_BIT  (*(struct BIT *)0xFFF2)           /* Interrupt Edge Select Register 1             */
```

```
#define   IEG1       IEGR1_BIT.b1                    /* IRQ1 Edge Select                          */
#define   IEG0       IEGR1_BIT.b0                    /* IRQ0 Edge Select                          */
#define   IENR1_BIT  (*(struct BIT *)0xFFF4)         /* Interrupt Enable Register 1               */
#define   IENDT      IENR1_BIT.b7                    /* Direct Transfer Interrupt Enable          */
#define   IENTA      IENR1_BIT.b6                    /* Timer A Interrupt Enable                  */
#define   IEN1       IENR1_BIT.b1                    /* IRQ1 Interrupt Request Enable             */
#define   IEN0       IENR1_BIT.b0                    /* IRQ0 Interrupt Request Enable             */
#define   IRR1_BIT   (*(struct BIT *)0xFFF6)         /* Interrupt Request Register 1              */
#define   IRRDT      IRR1_BIT.b7                     /* Direct Transfer Interrupt Request Flag    */
#define   IRRTA      IRR1_BIT.b6                     /* Timer A Interrupt Request Flag            */
#define   IRRI1      IRR1_BIT.b1                     /* IRQ1 Interrupt Request Flag               */
#define   IRRI0      IRR1_BIT.b0                     /* IRQ0 Interrupt Request Flag               */

#pragma        interrupt    (dtint)
#pragma        interrupt    (IRQ0)
#pragma        interrupt    (IRQ1)
#pragma        interrupt    (taint)

/*******************************************************/
/*     Function Definition                             */
/*******************************************************/
extern    void    INIT ( void );                        /* SP Set           */
void    main     ( void );
void    dtint    ( void );
void    IRQ0     ( void );
void    IRQ1     ( void );
void    taint    ( void );
void    wait     ( void );
void    sleep    ( void );

/*******************************************************/
/*    RAM define                                       */
/*******************************************************/
    unsigned char    USRF;                              /* User Flag Erea    */

#define        USRF_BIT    (*(struct BIT *)&USRF)
#define        SWONF        USRF_BIT.b1                /* Switch On  Flag   */
#define        LDONF        USRF_BIT.b0                /* LED On Flag       */
```

```
/*******************************************************/
/*    Vector Address                                   */
/*******************************************************/
#pragma    section        V1                           /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = {
    INIT                                               /* 00 Reset           */
};
#pragma    section        V2                           /* VECTOR SECTOIN SET */
void (*const VEC_TBL2[])(void) = {
    dtint                                              /* Sleep Interrupt    */
};
#pragma    section        V3                           /* VECTOR SECTOIN SET */
void (*const VEC_TBL3[])(void) = {
    IRQ0                                               /* IRQ0  Interrupt    */
};
#pragma    section        V4                           /* VECTOR SECTOIN SET */
void (*const VEC_TBL4[])(void) = {
    IRQ1                                               /* IRQ1  Interrupt    */
};
#pragma    section        V5                           /* VECTOR SECTOIN SET */
void (*const VEC_TBL5[])(void) = {
    taint                                              /* timer A  Interrupt */
};
#pragma    section                                     /* P                  */

/*******************************************************/
/*    Main Program                                     */
/*******************************************************/
void    main ( void )
{

    set_imask_ccr(1);                                  /* Interrupt Disable  */

    IRQ1_SET = 1;                                       /* Initialize IRQ1 Terminal Input         */
    IRQ0_SET = 1;                                       /* Initialize IRQ0 Terminal Input         */

    IEG0 = 1;                                           /* Set Rising Edge of IRQ0 Terminal Input */
    IRRI0 = 0;                                          /* Clear IRRI0                            */
    IEN0 = 1;                                           /* IRQ0 Interruput Enable                 */
```

```
    IEG1 = 1;                           /* Set Rising Edge of IRQ1 Terminal Input */
    IRRI1 = 0;                          /* Clear IRRI1                            */
    IEN1 = 0;                           /* IRQ1 Interruput Disable                */

    TMA = 0x19;                         /* Set TMA3                               */

    IRRTA = 0;                          /* Clear IRRTA                            */
    IENTA = 0;                          /* Timer A Interrupt Disable              */

    IRRDT = 0;                          /* Clear IRRDT                            */
    IENDT = 1;                          /* Direct Transfer Interrupt Enable       */

    SYSCR1 = 0x30;                      /* Initialize Function of Sleep Mode 1    */
    SYSCR2 = 0x4C;                      /* Initiakize Function of Sleep Mode 2    */

    P74 = 0;                            /* Initialize P74                         */
    PCR74 = 1;                          /* Initialize P74 Output Port             */

    LDONF = 0;                          /* Initialize LDONF                       */
    SWONF = 0;                          /* Initialize SWONF                       */

    set_imask_ccr(0);                   /* Interrupt Enable                       */

    sleep();                            /* Transition to Sleep Mode               */

    TMA = 0x1F;                         /* Reset PSW & TCA                        */
    TMA = 0x19;                         /* Initialize Timer A Function            */

    IRRTA = 0;                          /* Clear IRRTA                            */
    IENTA = 1;                          /* Timer A Interrupt Enable               */

    IRRI1 = 0;                          /* Clear IRRI1                            */
    IEN1 = 1;                           /* IRQ1 Interrupt Enable                  */

    while(SWONF != 1){                  /* SWONF = "1" ?                          */
        ;
    }

    P74 = 0;                            /* Turn off LED                           */

    SYSCR1 = 0xC0;                      /* Initialize Fubction of Active Mode 1   */
    SYSCR2 = 0x2C;                      /* Initialize Function of Active Mode 2   */
    sleep();                            /* Transition to Active Mode              */

    while(1)    {
       ;
    }
}
```

```
/*********************************************************/
/*    IRQ0 Interrupt                                     */
/*********************************************************/
void    IRQ0 ( void )
{

    IRRI0 = 0;                                          /* Clear IRRI0                          */

    IEN0 = 0;                                           /* IRQ0 Interrupt Disable               */

}

/*********************************************************/
/*    IRQ1 Interrupt                                     */
/*********************************************************/
void    IRQ1 ( void )
{

    if(IRRI1 == 1){                                     /* IRRI1 = "1" ?                        */
        IRRI1 = 0;                                      /* Clear IRRI1                          */
        SWONF = 1;                                      /* Set SWONF                            */
        IENTA = 0;                                      /* Timer A Interrupt Disable            */
        IEN1 = 0;                                       /* IEN1 Interrupt Disable               */
    }
}
```

```
/*******************************************************/
/*    Timer A Interrupt                                */
/*******************************************************/
void    taint ( void )
{

    IRRTA = 0;                                  /* Clear IRRTA                  */

    set_imask_ccr(0);                           /* Interrupt Enable             */

    if(LDONF == 1){                             /* LDONF = "1" ?                */
        P74 = 0;                                /* Turn off LED                 */
        LDONF = 0;                              /* Clear LDONF                  */
    }
        else{
            P74 = 1;                            /* Turn on LED                  */
            LDONF = 1;                          /* Set LDONF                    */
        }
}

/*******************************************************/
/*    Direct Transfer Interrupt                        */
/*******************************************************/
void    dtint ( void )
{

    IRRDT = 0;                                  /* Clear IRRDT                  */

}
```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'001A
CV3	H'001C
CV4	H'001E
CV5	H'0026
P	H'0100
B	H'FB80

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
2.00	Sep.01.06	All pages	Format has been changed from Hitachi version to Renesas version.

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