Application Note

DVFS and LDO Bypass Operation on i.MX6 Based Platform with DA9063

AN-PM-053

Abstract

This application note describes the functionality of the DVFS and LDO bypass features of the i.MX6 Freescale SoC, and explains how it can be used in a system in conjunction with the DA9063 PMIC.

Finally, it analyses the implementation on a Dialog Semiconductor PEBIX platform and the performance improvement achieved in terms of power saving.

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1 Terms and Definitions

BSP	Board Support Package
CPU	Central Processing Unit
DVFS	Dynamic Voltage Frequency Scaling
FET	Field Effect Transistor
LDO	Low DropOut Voltage Regulator
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuits
SoC	System on (a) Chip

2 References

[1] DA9063, Datasheet, Dialog Semiconductor.

[2] AN-PM-024 DA9063 Voltage Monitoring, Application Note, Dialog Semiconductor.

3 Introduction

The Board Support Package (BSP) used in the PEBIX[1] board features the bypass mode and Dynamic Voltage Frequency Scaling (DVFS) software functions which improve power saving efficiency on a system equipped with a PMIC. DVFS is applied on the ARM core voltage domain.

The bypass mode implements a mechanism where the internal LDOs of the i.MX6 are bypassed by fully switching on their respective pass device (FET), with the consequence that no regulation is performed.

The DVFS technique is implemented in the kernel, by using an interrupt generated by the DVFS block (internal to i.MX6) which tracks the CPU load. Within the kernel it is possible to define two CPU load thresholds, above which the DVFS block generates two interrupts to the ARM core, according to the CPU load. In turn the ARM core programs the external PMIC according to a Table (look-up Table) implemented in the kernel, which relates voltage rail levels (VDDSOC, VDDCORE) and ARM cores clock frequencies. A high CPU load would increase both VDDSOC, VDDCORE power rails and also the clock frequency and vice versa. The result is a power saving which is a paramount requirement for mobile applications, where normally a battery is the power source of the system.

4 Bypass Mode Implemented in the PEBIX Platform

The bypass mode functionality has been tested on a PEBIX platform with an i.MX6Q processor and a DA9063 PMIC. For other platforms with the same hardware architecture as PEBIX, the results can vary due to the dependency on PCB layout.

Figure 1 shows a simplified block diagram of the i.MX6 SoC with its internal LDOs. Since, in bypass mode, the i.MX6Q LDOs simply pass through the input voltages to the outputs (the LDO MOSFETs are permanently on with no regulation), the host CPU must program the external PMIC to generate the required VDDCORE and VDDSOC according to the look-up Table (Table 1) and applied by Android application in run time.

Without bypass mode, the internal LDOs will regulate the applied voltages at the input. With this configuration the required input voltage level must of course be higher.

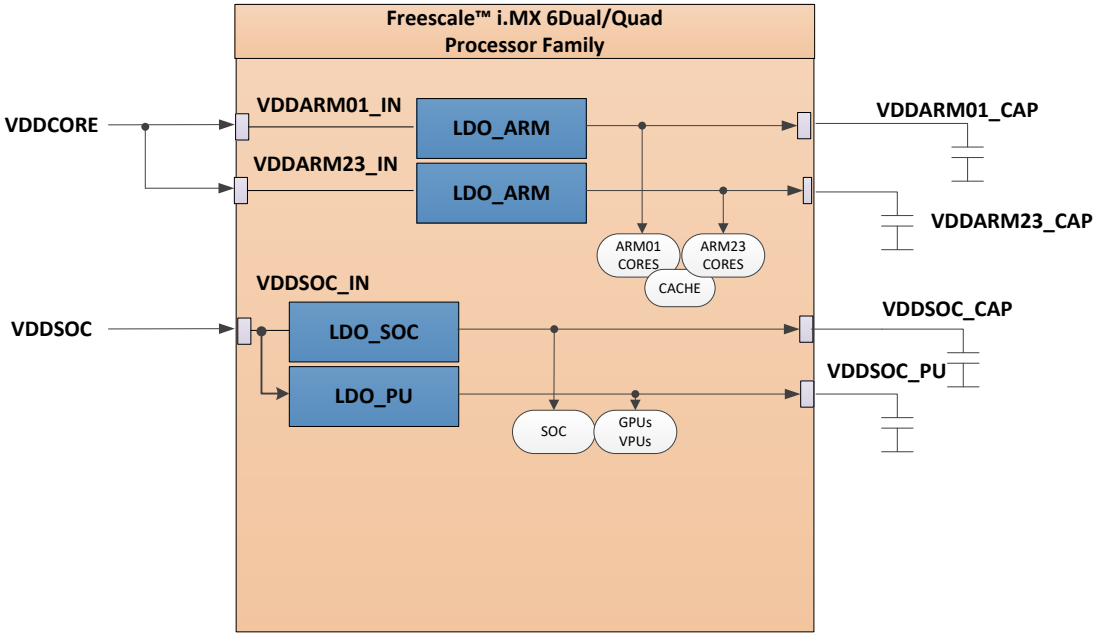

Figure 1: i.MX6 Internal LDOs

[1] PEBIX = PMIC Evaluation Board for i.MX6 Q/D process. It is an i.MX6 Q/D based platform with a DA9063 PMIC.

5 Measurement Method and Results

Tests were carried out on a PEBIX board which was designed with specific jumper links on all supply rails to allow current measurements. For the tests, only VDDSOC and VDDCORE rails were monitored. A video clip was running to exercise the SoC power demand on these rails.

Both currents I_ARM and I_SOC have a complex profile due to the continuous load transient, such as whilst streaming a video clip, as shown in Figure 2. The average current (RMS value measured in a long time slot) was measured by using a scope and a current probe on these rails, for both conditions: bypass and no bypass mode.

For the tests, the ARM core clock frequency was set in the software to 1 GHz or 800 MHz.

Clock frequencies higher than 1 GHz cannot be implemented as the i.MX6 device is rated only up to this frequency.

In this report the following definitions will be used:

Pb = Power in bypass mode

Pr = power in no-bypass mode (regulated)

Vb = voltage rail in bypass mode

Vr = voltage rail in no bypass mode (regulated)

Table 1: Best Combinations of Clock Frequency and Voltage Rails

Clock frequency = 1GHz	Rail	Rail input
.pu_voltage	VDDSOC	1250
.soc_voltage		1250
.cpu_voltage	VDDCORE	1300
Clock frequency = 800MHz		
.pu_voltage	VDDSOC	1250
.soc_voltage		1250
.cpu_voltage	VDDCORE	1200
Clock frequency = 400MHz		
.pu_voltage	VDDSOC	1250
.soc_voltage		1250
.cpu_voltage	VDDCORE	1100

Normally, the DVFS mechanism can be applied to both VDDSOC and VDDCORE rails. However, after experimenting with different frequencies and voltage levels, the best combinations of clock frequency and voltage rails were found and gathered in

Note that VDDSOC is kept constant due to a hardware limitation. A large voltage drop on the main rail VDDSOC does not allow further reduction of the voltage levels without causing a software crash.

5.1 Results

The Appendix includes scope screenshots which show the complex profile of both I_ARM and I_SOC currents. The complexity is due to the continuous load transients while streaming the video clip. Figure 3 shows the VDDCORE (core voltage) dynamically switched mainly between two values, according to Table 1. For example, if the clock frequency is set to 1 GHz, the VDDCORE voltage is mainly switched between the values 1.3 V and 1.25 V. For an 800 MHz clock frequency, these values will be between 1.25 V and 1.1 V.

5.2 Approximate Power Saving in Bypass Mode

The DVFS mechanism is also active during bypass mode. When DVFS become active, VDDCORE and VDDSOC voltages are adjusted according to the CPU load as per Table 1.

Table 2 presents a summary of the current measurements while running the video clip. The power input demand can be estimated with the formulae:

Pr = VDDCORE x (I_ARM + I_SOC)

Pb = VDDCORE x I_ARM + VDDSOC x I_SOC

Table 2: Current Measurements Whilst Running Video (1 GHz)

Clock Frequency	LDO Mode	VDDCORE (V)	I_ARM (mA)	VDDSOC (V)	I_SOC (mA)	P (mW)
1 GHz	No bypass	1.38	110	1.38	450	773
1 GHz	bypass	1.30	125	1.25	406	670 max
1 GHz	bypass	1.10	125	1.25	406	509 min

From the values shown it is possible to estimate the power saving, assuming the system is always working in one of the following two conditions:

- Worst case, where it is assumed the voltage rails are always set to the highest level by the DVFS mechanism
  - ΔP min = 773 - 670 =103 mW → 13.3 %
- Best case, where it is assumed the voltage rails are always set to the lowest level by the DVFS mechanism
  - ΔP max = 773 - 509 =264 mW → 34.2 %

When bypass mode is not active (no-bypass) a portion of the input power is lost in the internal LDOs due to voltage drop across the MOSFET pass devices. This is an unavoidable limitation of an LDO and requires Vin - Vout 1.1 V. However, when bypass mode is active, it is possible to lower the applied input voltage as there will be no voltage drop across the internal LDOs.

The above results show that the implementation of both bypass mode and DVFS mechanisms can lead to a significant power saving of at least 13.3 % if the input voltage is maintained at 1.3 V. As the input voltage is also toggled to a lower level of 1.1 V, then the actual figure will be between 13.3 % and 34.2 %.

Clock Frequency	LDO Mode	VDDCORE (V)	I_ARM (mA)	VDDSOC (V)	I_SOC (mA)	P (mW)
800MHz	No bypass	1.38	93	1.38	450	749
800MHz	bypass	1.25	86	1.25	418	625 max
800MHz	bypass	1.10	86	1.25	418	617 min

Table 3: Current Measurements Whilst Running Video (800 MHz)

Similarly, if the max clock frequency is set to 800 MHz, the power saving is as below:

- Worst case: ΔP min = 749 - 670 = 79 mW → 10.5 %
- Best case: ΔP max = 749 - 617 = 132 mW →17.6 %

6 Conclusions

Implementing the DVFS and bypass modes has been demonstrated to improve power saving. The power saving can be further improved if the mechanism is also applied to the VDDSOC rail. (This was not possible in the PEBIX platform due to a hardware limitation, as explained above.)

Lastly, as the DVFS modifies the rail voltages only in the range of tens of millivolts, the voltage drops, due to PCB track resistance, can also have an impact on the power saving. Therefore, designers may need to tune the rail voltages for each clock frequency (by modifying the kernel look-up, see Table 1) to achieve the best power saving whilst also remaining within the maximum rail voltages specified by the i.MX6 datasheet. Consequently, results may differ from those above due to the high dependency upon PCB layout and rail voltage settings in the kernel.

Appendix A Scope Screenshots

The following scope screenshots show the complex profile of both I_ARM and I_SOC currents.

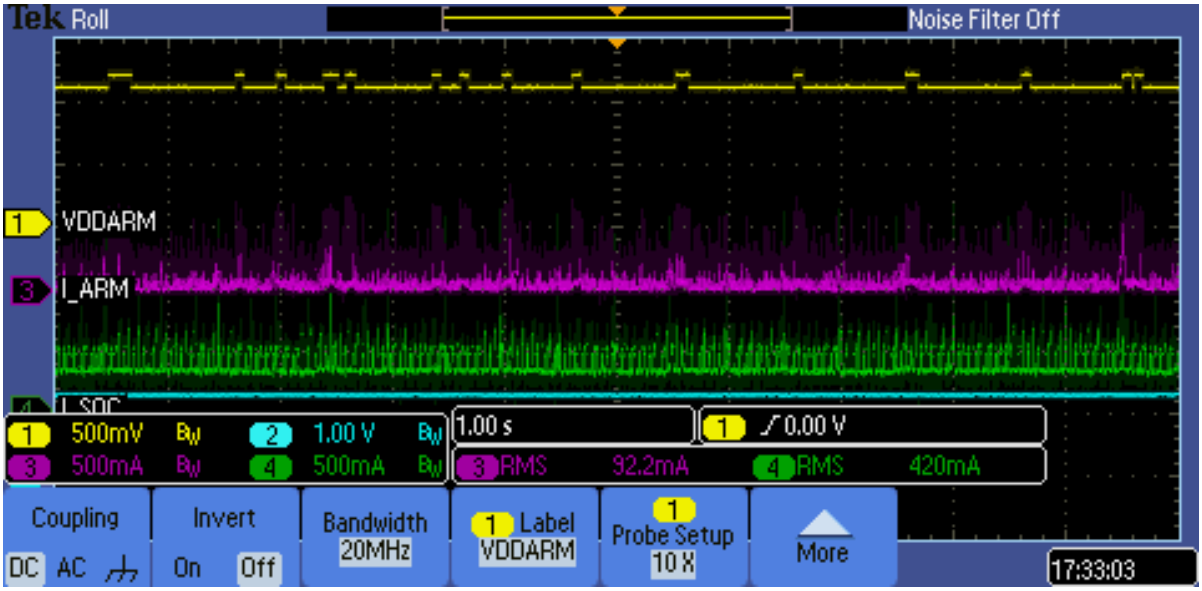

Figure 2: BYPASS MODE (ldo_active=OFF) at 800 MHz

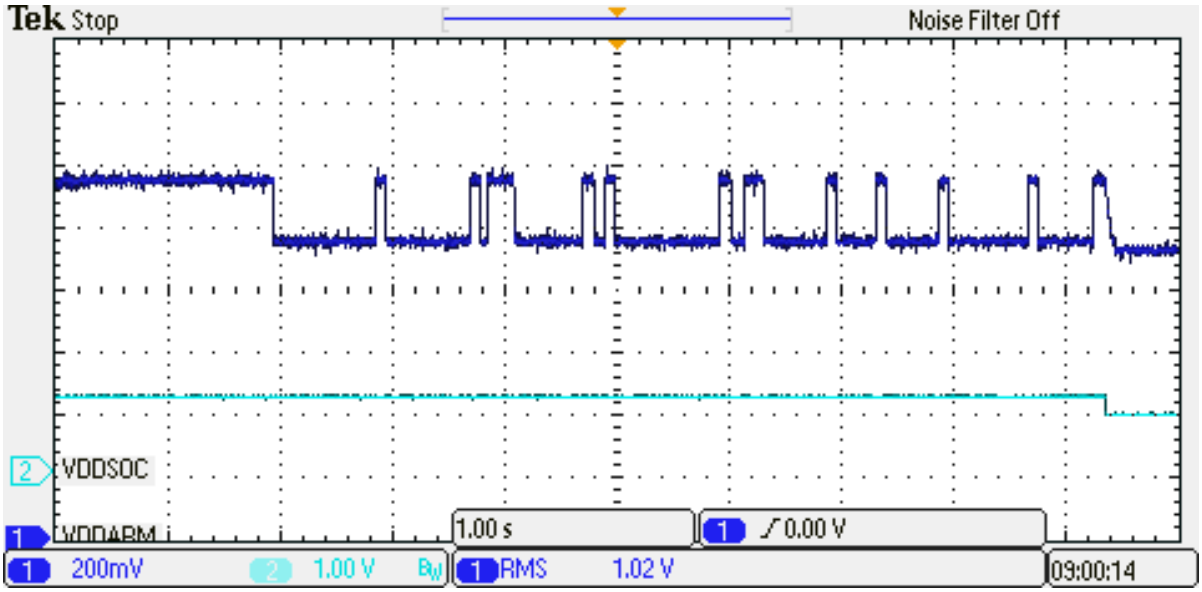

Figure 3: BYPASS MODE (ldo_active=OFF) at 800 MHz – Details of DVFS Performed on VDDCORE Supply

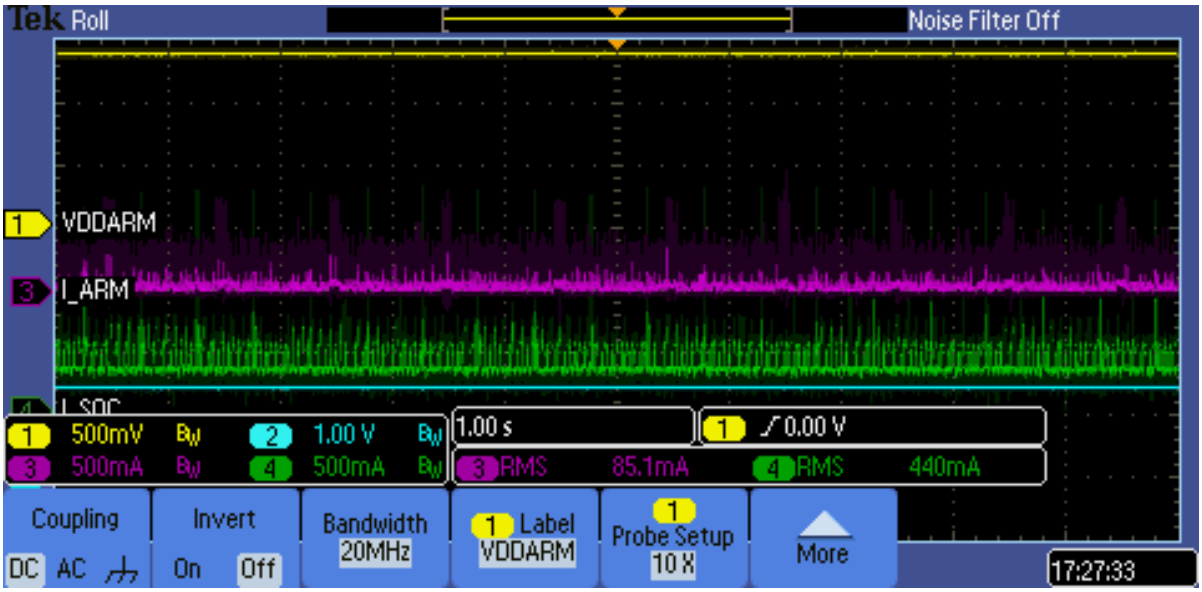

Figure 4: NO BYPASS MODE (ldo_active=ON) at 800 MHz – Voltage Rails and System Current

Figure 5: BYPASS MODE (ldo_active=OFF) at 1 GHz

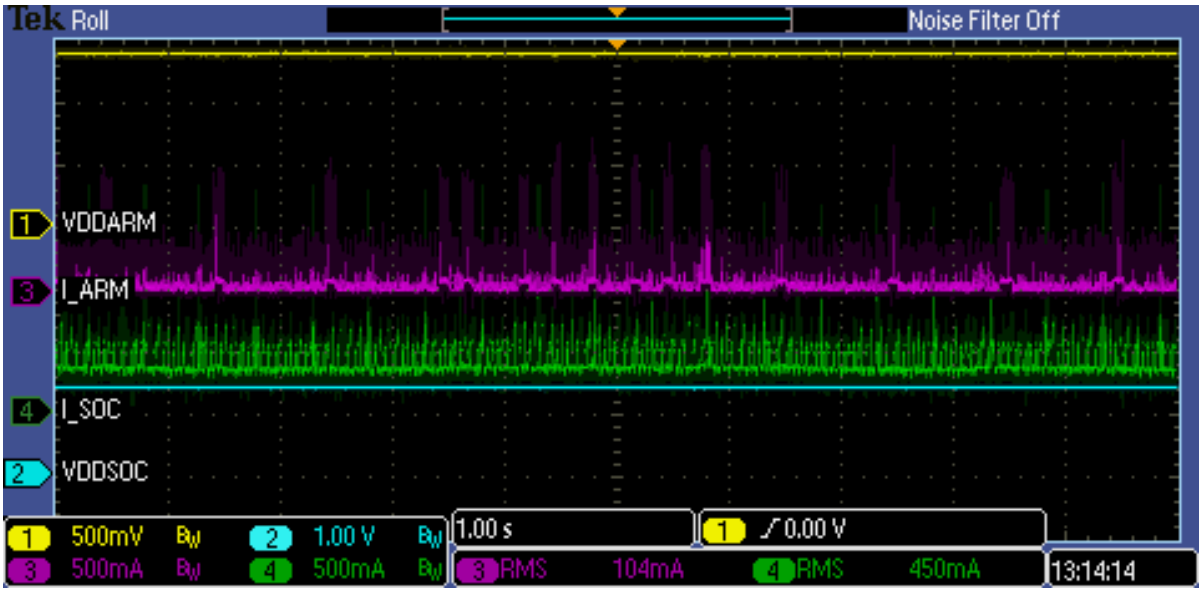

Figure 6: BYPASS MODE (ldo_active=OFF) at 1GHz – Voltage Rails and System Current

Revision History

Revision	Date	Description
1.0	17-Dec 2016	Initial version.
1.1	23-Sep-2016	Updated to latest publishing standards
1.2	16-Feb-2022	File was rebranded with new logo, copyright and disclaimer

Status Definitions

Status	Definition
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