Drain Voltage and Avalanche Ratings for GaN FETs

This application note compares a silicon MOSFET's avalanche rating and Renesas's GaN FET transient drain-to-source ("V_{TDS}") rating.

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Introduction

Many customers have asked if Renesas's GaN FETs have an avalanche rating. This note explains that, unlike traditional vertical silicon MOSFETs, Renesas's lateral GaN FETs do not have a body diode and therefore no physical avalanche mechanism. GaN FETs do have a dielectric breakdown voltage, similar to that of capacitors, which is often as much as three times higher than their datasheet maximum voltage rating. To confirm reliability, one of the several tests Renesas performs on its 650V-rated GaN FETs is the High Voltage Off State (HVOS), which applies as high as 1150V[1] for extended periods. One of the major advantages of GaN FETs is that they do not have this lossy high capacitance body diode. The absence of this parasitic body diode allows GaN FETs to be used in new topologies and to attain higher levels of efficiency in power conversion applications than is possible with silicon FETs. Instead of an avalanche voltage rating, which should never be exceeded in traditional high-voltage silicon MOSFETs due to reliability concerns, Renesas's GaN devices are rated for a transient peak voltage that is ~25% higher (e.g. 800V for a 650V part) than the continuous rating. This peak transient rating is significantly below voltage levels that could result in device failures.

Drain Voltage Stress and Avalanche

In many power conversion circuits the main switching power device will see a momentary voltage "spike" or overshoot at the turn-off edge due to stray inductances in series with the device.

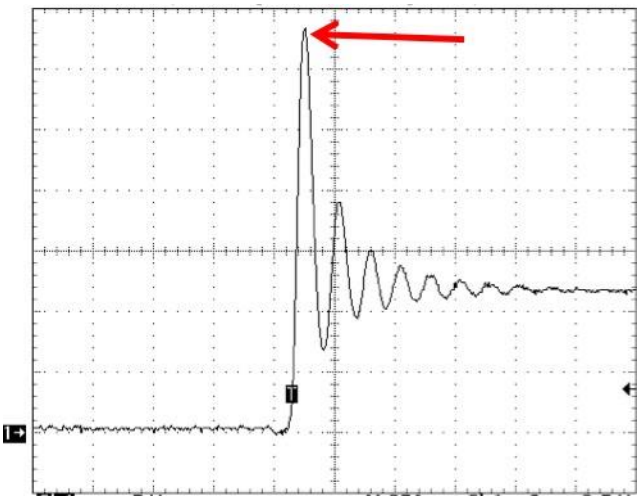

Figure 1. Severe drain voltage overshoot and ringing. Arrow points to peak voltage. In this example, the FET did not avalanche

The peak voltage in Figure 1 should not exceed the max voltage rating of a FET with no avalanche rating; or if a FET with avalanche capability is being used, that the avalanche current and energy ratings are not exceeded.

Figure 2 shows a waveform where the peak voltage exceeded the FET's rated voltage. MOSFETs that have an avalanche rating, exhibit a drain-source off characteristic that resembles a reverse-biased Zener diode (see Figure 3). The drain voltage will be clamped at the avalanche voltage.

[1] HVOS (voltage acceleration) – 82°C at 1150V, 1100V, 1050V (50% fail): High voltages can be a significant reliability concern but Renesas device design has limited the electric field strength to levels similar to those seen in RF GaN high electron mobility transistor (HEMT) devices.

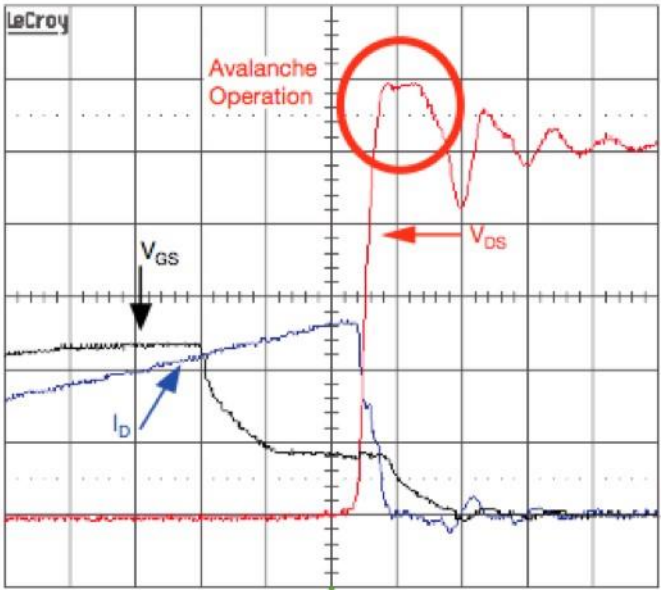

Figure 2. Silicon MOSFET drain turn-off voltage with avalanche event
(image from eeweb.com)

The designer should validate the drain current during avalanche and compare the waveforms to the MOSFET datasheet:

Table 1. Typical silicon MOSFET avalanche rating

Symbol	Parameter	Min	Typ	Max	Unit
E_{AS}	Avalanche energy, single pulse	—	—	249	mJ
E_{AR}	Avalanche energy, repetitive	—	—	1.24	mJ
I_{AS}	Avalanche current, single pulse	—	—	7.4	A

During the avalanche event, the drain conducts current, which dissipates energy in the channel. This energy cannot be allowed to exceed the data sheet maximum. If the avalanche is a repetitive event, i.e. occurs at every switching cycle, the average current cannot be greater than a value such that the power dissipation overheats the die.

Moreover, if avalanche occurs repetitively during normal operation, it dissipates heat and reduces system efficiency and, for high voltage MOSFETs, reduces reliability.

In contrast, Renesas GaN devices do not avalanche. Their V-I characteristic does not exhibit the clamping voltage of a silicon MOSFET undergoing avalanche:

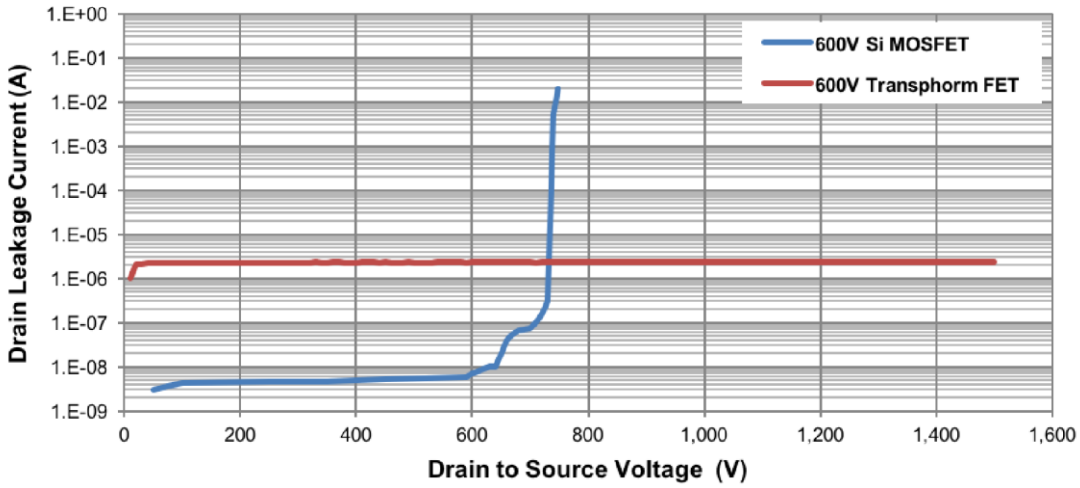

Figure 3. Off-state drain V-I characteristic - Si MOSFET vs Renesas FET

This behavior begs the question: “If the device does not avalanche even at 1.5kV, why is the device not rated at 1.5kV?” The answer is that when the device is exposed to a continuous high voltage for long periods of time, the operational life can be reduced. JEDEC standards include “HTRB” (high temperature reverse bias) testing, which in a FET actually means “high temperature with high voltage applied to the drain” (even though there is no parasitic body diode in the GaN FET structure; the term “reverse bias” comes from the reverse body diode voltage testing of silicon MOSFETs). The testing involves statistical predictions using a specified sample size, at different voltages. A device will have a specified voltage rating if it meets certain reliability standards, such as JEDEC, for that specific voltage.

Renesas’s 650V-rated devices have passed JEDEC standard HTRB tests. Using voltage accelerated testing results as a basis

(Figure 4), under both the 650V “rated value” and 480V “nominal use” voltages, Renesas has predicted an MTTF (Mean Time to Failure) well in excess of 108 hours or > 10,000 years of expected life for its devices.

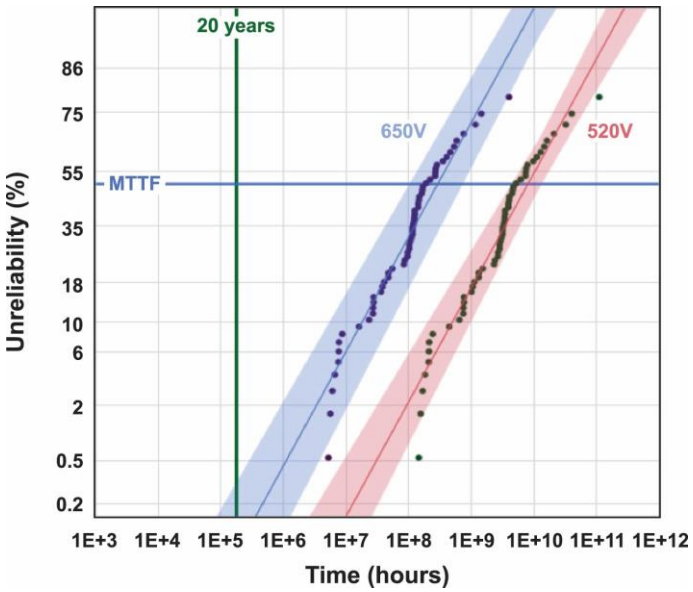

Figure 4. “Use-plots” based on voltage-accelerated testing showing all failed devices during HVOS testing at 82°C for the reciprocal field TDDB model. 99% confidence limits shown, Tj = 82°C, TDDB inverse voltage model (Smith, 2015)

Figure 4 shows the results of highly accelerated voltage stress testing. The time dependent dielectric breakdown (TDDB) model is shown to apply as the lifetime predictive mechanism. Additionally, Renesas also specifies a momentary repetitive peak voltage (transient) rating that is substantially higher than the DC max voltage rating, called "V_{TDS}". V_{TDS} is tested in production and guaranteed in the datasheets.

The "V_{TDS} = 800V" specification means V_{DS} can reach up to 800V for up to 1µs, and up to a duty cycle of 10%. This 23% allowable voltage overshoot gives the Renesas GaN FET considerably more flexibility than an avalanche rating. The test fixture and waveforms are shown in Figures 5 and 6. The test is performed with a pulse width of 1µs to allow Renesas the ability to guarantee operation for voltage spikes up to 1µs in duration.

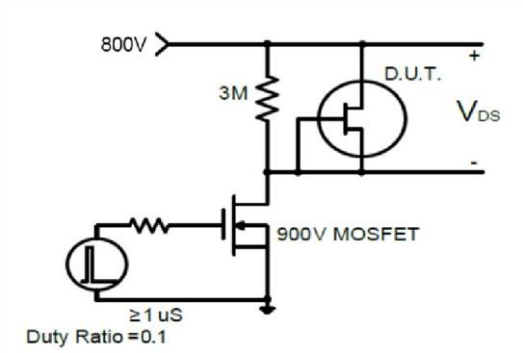

Figure 5. Spike voltage test circuit

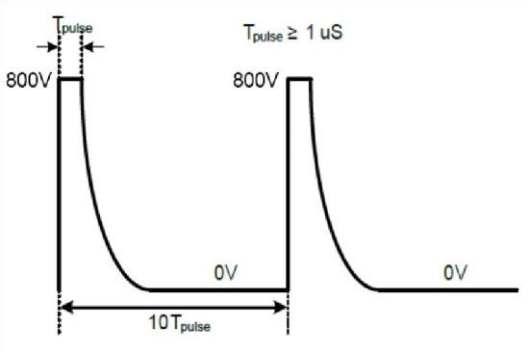

Figure 6. Spike voltage waveform

Testing GaN FET Max V_{DS}

If confirmation of the maximum voltage rating of a Renesas FET is required, do not use an unclamped inductive load test that will force an unclamped high voltage on the drain. Instead, apply the rated V_{DS} and measure the leakage current to determine if it is within the specification:

Table 2. Example of drain leakage current spec (TPH3207WS)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{DSS}	Drain-to-source leakage current, T_J=25°C	—	5	50	µA	V_{DS}=650V, V_{GS}=0V, T_J=25°C
	Drain-to-source leakage current, T_J=150°C	—	10	—	µA	V_{DS}=650V, V_{GS}=0V, T_J=150°C

Conclusion

The transient V_{DS} rating (V_{TDS}) of Renesas's GaN FET devices lends flexibility and additional reliability over that of an avalanche-rated high-voltage silicon MOSFET.

Bibliography

Smith, K. (2015). Lifetime Tests of 600-V GaN-on-Si Power Switches and HEMTs. *Special Issue on Reliability Issues in Power Electronics*.