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Renesas Electronics Corporation

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H8/300L Super Low Power Series

Division of 32-Bit Binary Numbers (DIV)

Introduction

The software DIV divides a 32-bit binary number by another 32-bit binary number and places the result (a 32-bit binary number) in general-purpose registers.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Dividend	R0, R1	4
	Divisor	R2, R3	4
Output	Result of division (Quotient)	R0, R1	4
	Result of division (Remainder)	R4, R5	4
	Errors	Z flag (CCR)	

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
○	○	×	×	○	○	—	—

I	U	H	U	N	Z	V	C
—	×	—	×	○	○	×	×

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
58
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
1374
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Description

4.1 Details of functions

1. The following arguments are used with the software DIV:
   - R0: Sets the upper 2 bytes of a 32-bit binary dividend. The upper 2 bytes of the result of division (quotient) are placed in this register after execution of the software DIV.
   - R1: Sets the lower 2 bytes of the 32-bit binary dividend. The lower 2 bytes of the result of division (quotient) are placed in this register after execution of the software DIV.
   - R2: Sets the upper 2 bytes of a 32-bit binary divisor as an input argument.
   - R3: Sets the lower 2 bytes of the 32-bit binary divisor as an input argument.
   - R4: The upper 2 bytes of the result of division (remainder) are placed in this register as an output argument.
   - R5: The lower 2 bytes of the result of division (remainder) are placed in this register as an output argument.
   - Z flag (CCR): Indicates the presence or absence of an error (division by 0) with the software DIV as an output argument.
     - Z flag = 1: The divisor was 0.
     - Z flag = 0: The divisor was not 0.

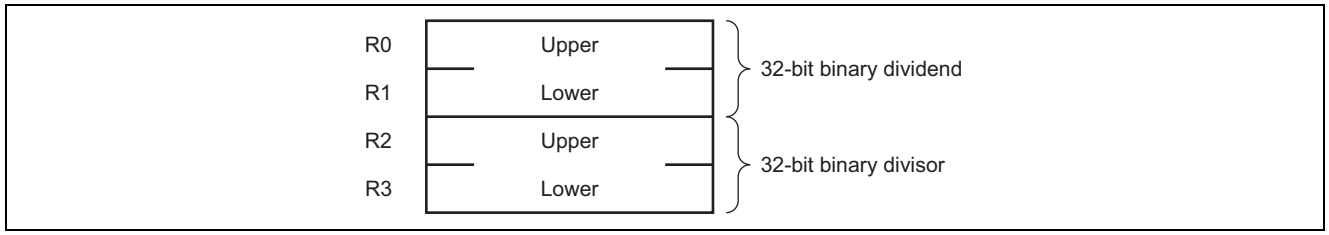


Figure 1 Input Argument Setting

2. The following figure illustrates the execution of the software DIV. When the input arguments are set as shown in (1), the result of division is placed as shown in (2).

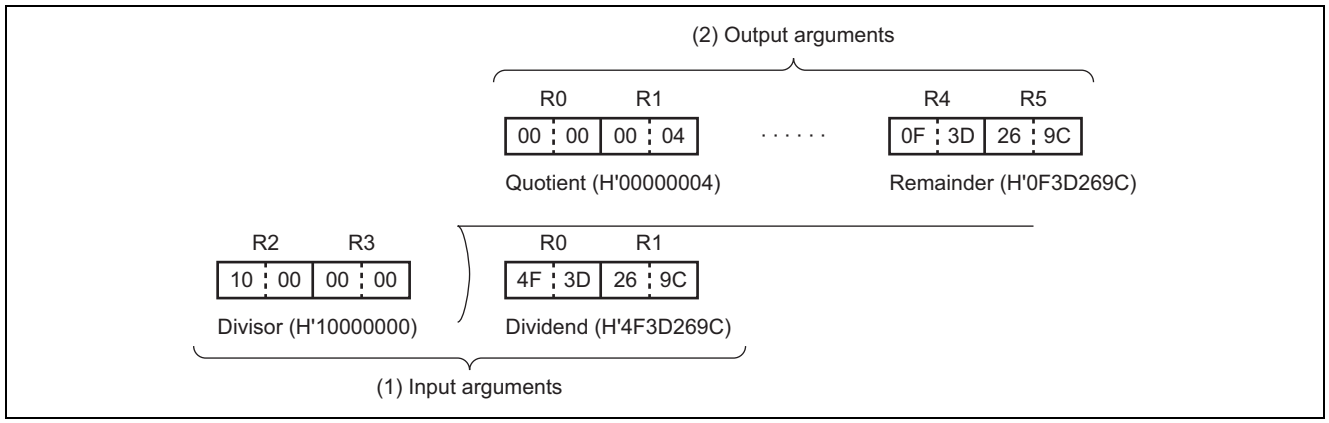


Figure 2 Example of Software DIV Execution

3. Table 1 lists the results of division with 0 placed in the input arguments.

Table 1 Results of Division with 0 Placed in Input Arguments

Input argument		Output argument		
Dividend (R0, R1)	**Divisor (R2, R3)**	**Quotient (R0, R1)**	**Remainder (R4, R5)**	**Error (Z)**
H'**** ****	H'0000 0000	H'**** ****	H'0000 0000	1
H'0000 0000	H'**** ****	H'0000 0000	H'0000 0000	0
H'0000 0000	H'0000 0000	H'0000 0000	H'0000 0000	1

Note: H'**** **** is a hexadecimal number.

4.2 Notes on usage

1. When the upper bits are not used (see figure 3), set them to 0; otherwise, a correct result cannot be obtained because division is done on the numbers including indeterminate data.

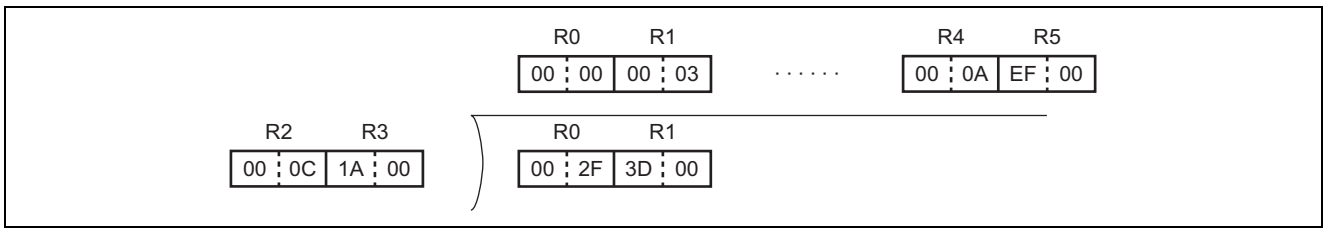


Figure 3 Example of Division with Upper Bits Unused

2. After execution of the software DIV, the dividend will be lost because the quotient is placed in R0 and R1. When the dividend is still needed after software DIV execution, save it in memory.

4.3 Data memory

The software DIV uses no data memory.

4.4 Example of usage

Set a dividend and a divisor in the input arguments and call the software DIV as a subroutine.

```
WORK1    . RES. W    2    ---------- Reserve a data memory area in which the user program places
                                     a 32-bit binary dividend.

WORK2    . RES. W    2    ---------- Reserve a data memory area in which the user program places
                                     a 16-bit binary divisor.

WORK3    . RES. W    2    ---------- Reserve a data memory area in which the user program places
                                     a 32-bit binary quotient.

WORK4    . RES. W    2    ---------- Reserve a data memory area in which the user program places
                                     a 32-bit binary remainder.
           .
           .
           .
         MOV. W        @WORK1, R0   -------
         MOV. W        @WORK1+2, R1 -------  Contain the 32-bit binary dividend set by
                                            the user program.
         MOV. W        @WORK2, R2   -------
         MOV. W        @WORK2+2, R3 -------  Contain the 32-bit binary divisor set by
                                            the user program.

         JSR           @DIV         -------  Call the software DIV as a subroutine.

         BEQ           ERROR        -------  Branch to the error processing routine
                                            when an error has occurred as the result of division.

         MOV. W R0,    @WORK3
         MOV. W R1,    @WORK3+2     -------  Place the result of division set in the output
         MOV. W R4,    @WORK4                arguments in the data memory of the user program.
         MOV. W R5,    @WORK4+2
           .
           .
           .
ERROR    Error processing routine
```

4.5 Operation

1. A binary division can be done by performing a series of subtractions. Figure 4 shows an example of division (H'0D ÷ H'03).

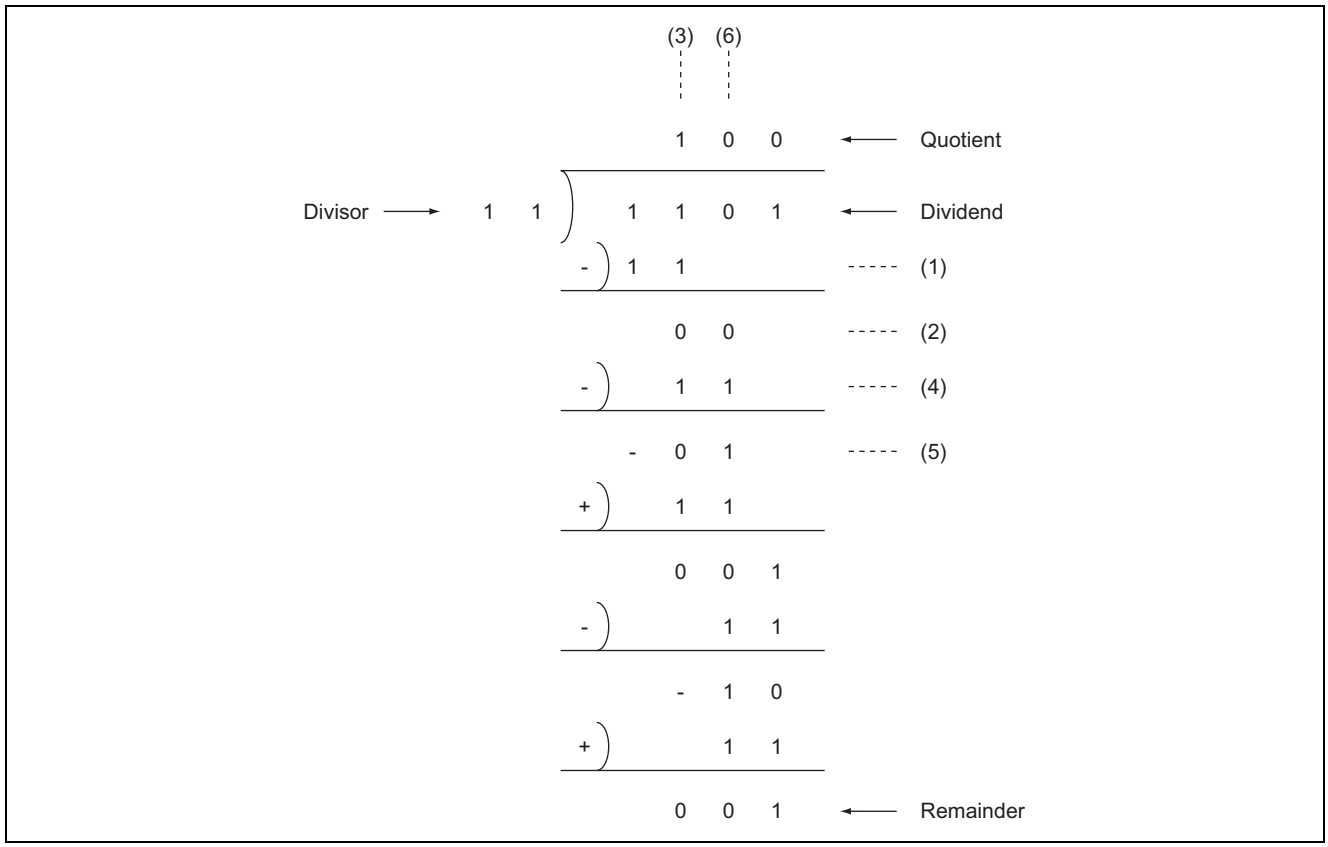
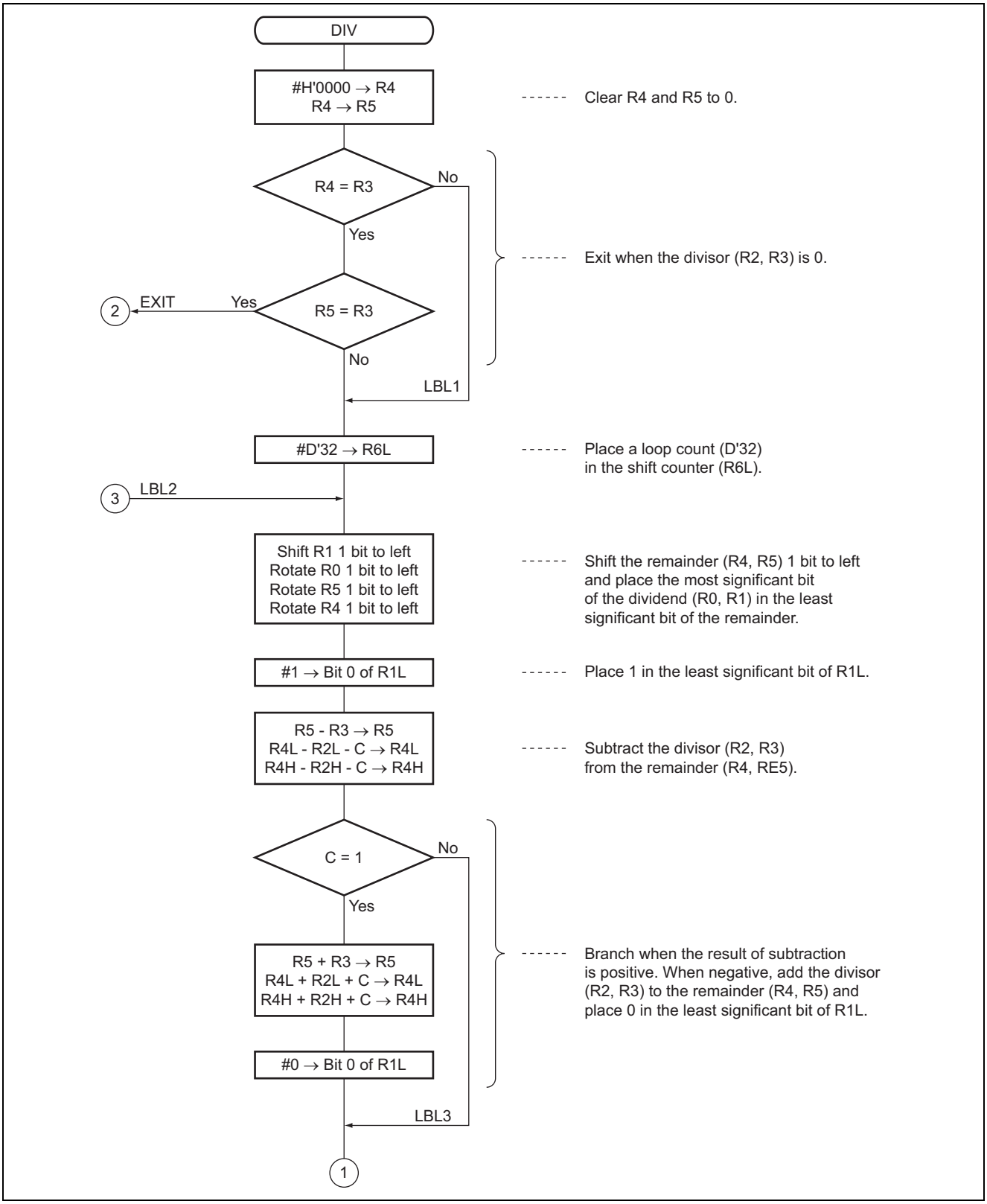


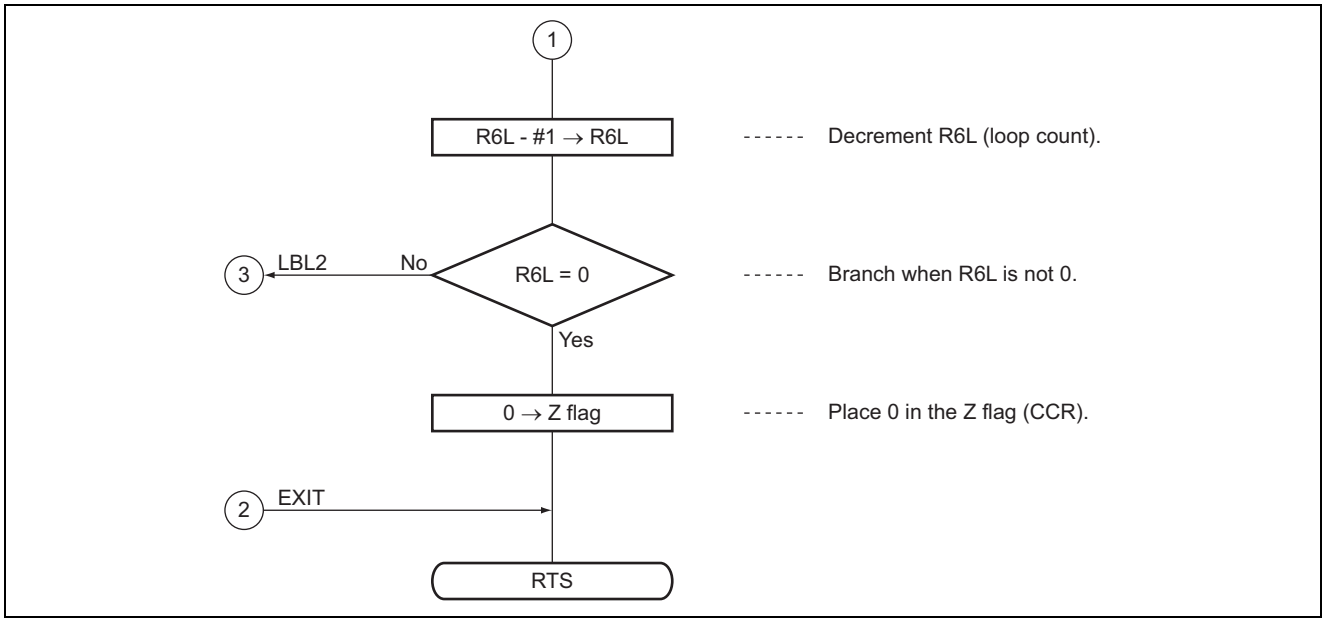
Figure 4 Example of Software DIV Execution (H'0D ÷ H'03)

This example indicates that the quotient and remainder are obtained by repeating a process of subtracting the dividend from the divisor. More specifically, the dividend is taken out bit by bit from the upper bits and the divisor is subtracted from the sum of the data extracted and the result of the previous subtraction.

2. The program runs in the following steps:
   a. A shift count (D'32) is set.
   b. The dividend is shifted 1 bit to the left and the MSB thus loaded to the C bit is set as the LSB of the remainder.
   c. The divisor is subtracted from the remainder.
      When the result is positive, the least significant bit of the dividend is set to 1 ((1) → (2) → (3) in figure 4).
      When the result is negative, the least significant bit of the dividend is set to 0, and the divisor is added to the result, returning it to the state before the subtraction ((4) → (5) → (6) in figure 4).
   d. The shift count (set in step a) is decremented.
   e. Steps b to d are repeated until the shift count reaches H'00.

5. Flowchart


DIV
#H'0000 → R4
R4 → R5
Clear R4 and R5 to 0.
R4 = R3
No
Yes
Exit when the divisor (R2, R3) is 0.
2
EXIT
Yes
R5 = R3
No
LBL1
#D'32 → R6L
Place a loop count (D'32)
in the shift counter (R6L).
3
LBL2
Shift R1 1 bit to left
Rotate R0 1 bit to left
Rotate R5 1 bit to left
Rotate R4 1 bit to left
Shift the remainder (R4, R5) 1 bit to left
and place the most significant bit
of the dividend (R0, R1) in the least
significant bit of the remainder.
#1 → Bit 0 of R1L
Place 1 in the least significant bit of R1L.
R5 - R3 → R5
R4L - R2L - C → R4L
R4H - R2H - C → R4H
Subtract the divisor (R2, R3)
from the remainder (R4, RE5).
C = 1
No
Yes
R5 + R3 → R5
R4L + R2L + C → R4L
R4H + R2H + C → R4H
Branch when the result of subtraction
is positive. When negative, add the divisor
(R2, R3) to the remainder (R4, R5) and
place 0 in the least significant bit of R1L.
#0 → Bit 0 of R1L
LBL3
1


1
R6L - #1 → R6L
------ Decrement R6L (loop count).
3
LBL2
No
R6L = 0
------ Branch when R6L is not 0.
Yes
0 → Z flag
------ Place 0 in the Z flag (CCR).
2
EXIT
RTS

6. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 09:58:57
PROGRAM NAME =
 1                              ;*************************************************************
 2                              ;*
 3                              ;*      00 - NAME   :32 BIT DIVISION (DIV)
 4                              ;*
 5                              ;*************************************************************
 6                              ;*
 7                              ;*      ENTRY       :R0 (UPPER WORD DIVIDEND)
 8                              ;*                   R1 (LOWER WORD DIVIDEND)
 9                              ;*                   R2 (UPPER WORD DIVISOR)
10                              ;*                   R3 (LOWER WORD DIVISOR)
11                              ;*
12                              ;*      RETURNS     :R0 (UPPER WORD QUOTIENT)
13                              ;*                   R1 (LOWER WORD QUOTIENT)
14                              ;*                   R2 (UPPER WORD RESIDUE)
15                              ;*                   R3 (LOWER WORD RESIDUE)
16                              ;*                   Z flag OF CCR (Z=0;TRUE , Z=1;FALSE)
17                              ;*
18                              ;*************************************************************
19                              ;
20  DIV_code C    0000                      .SECTION                  DIV_code,CODE,ALIGN=2
21                                          .EXPORT  DIV
22                              ;
23  DIV_code C          00000000  DIV       .EQU $                    ;Entry point
24  DIV_code C    0000  79040000            MOV.W    #H'0000,R4       ;Clear R4
25  DIV_code C    0004  0D45                MOV.W    R4,R5            ;Clear R5
26  DIV_code C    0006  1D42                CMP.W    R4,R2
27  DIV_code C    0008  4604                BNE      LBL1             ;Branch if Z flag = 0
28  DIV_code C    000A  1D43                CMP.W    R4,R3
29  DIV_code C    000C  472A                BEQ      EXIT             ;Branch if Z flag = 1 then exit
30  DIV_code C    000E              LBL1
31  DIV_code C    000E  FE20                MOV.B    #D'32,R6L        ;Set byte counter
32  DIV_code C    0010              LBL2
33  DIV_code C    0010  1009                SHLL     R1L              ;Shift dividend 1 bit left
34  DIV_code C    0012  1201                ROTXL    R1H
35  DIV_code C    0014  1208                ROTXL    R0L
36  DIV_code C    0016  1200                ROTXL    R0H
37                              ;
38  DIV_code C    0018  120D                ROTXL    R5L
39  DIV_code C    001A  1205                ROTXL    R5H
40  DIV_code C    001C  120C                ROTXL    R4L
41  DIV_code C    001E  1204                ROTXL    R4H
42                              ;
43  DIV_code C    0020  7009                BSET     #0,R1L           ;Bit set bit 0 of R1L
44                              ;
45  DIV_code C    0022  1935                SUB.W    R3,R5            ;R5 - R3 -> R5
46  DIV_code C    0024  1EAC                SUBX.B   R2L,R4L          ;R4L - R2L - C -> R4L
47  DIV_code C    0026  1E24                SUBX.B   R2H,R4H          ;R4H - R2H - C -> R4H
```

```
48                                  ;
49  DIV_code C    0028  4408              BCC     LBL3              ;Branch if C = 0
50  DIV_code C    002A  0935              ADD.W   R3,R5             ;R3 + R5 -> R3
51  DIV_code C    002C  0EAC              ADDX.B  R2L,R4L           ;R2L + R4L + C -> R4L
52  DIV_code C    002E  0E24              ADDX.B  R2H,R4H           ;R2H + R4H + C -> R4H
53                                  ;
54  DIV_code C    0030  7209              BCLR    #0,R1L            ;Bit clear bit 0 of R1L
55  DIV_code C    0032              LBL3
56  DIV_code C    0032  1A0E              DEC.B   R6L               ;Decrement R6L
57  DIV_code C    0034  46DA              BNE     LBL2              ;Branch if Z=0
58  DIV_code C    0036  06FB              ANDC    #B'11111011,CCR   ;Clear Z flag
59  DIV_code C    0038              EXIT
60  DIV_code C    0038  5470              RTS
61                                  ;
62                                          .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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