RX26T Group, RX24T/RX24U Group

Differences Between the RX26T Group and the RX24T/RX24U Group

Introduction

This application note is intended as a reference to points of difference in the peripheral functions, I/O registers, and pin functions between the RX26T Group and RX24T/RX24U Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX26T Group, the 100-pin package version of the RX24T Group, and the 144-pin package version of the RX24U Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware for the products in question.

Target Device

RX26T Group, RX24T Group, and RX24U Group

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1. Comparison of Built-In Functions of RX26T Group and RX24T/RX24U Group

A comparison of the built-in functions of the RX26T Group and RX24T/RX24U Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is Comparison of Built-In Functions of RX24T Group, RX24U Group, and RX26T Group.

Table 1.1 Comparison of Built-In Functions of RX24T Group, RX24U Group, and RX26T Group

Function	RX24T		RX24U	RX26T
	Chip Version A	Chip Version B		
CPU	●/▲/■			
Operating modes	●/▲			
Address space	▲			
Resets	●			
Option-setting memory	●/▲/■			
Voltage detection circuit (LVDAb for RX24T/RX24U, and LVDA for RX26T)	●/▲/■			
Clock generation circuit	●/▲/■			
Clock frequency accuracy measurement circuit (CAC)	○			
Low power consumption	●/▲/■			
Register write protection function	●/■			
Exception handling	○			
Interrupt controller (ICUb for RX24T/RX24U, and ICUG for RX26T)	●			
Buses	●/■			
Memory-protection unit (MPU)	○			
DMA controller (DMACAa)	×			○
Data transfer controller (DTCa for RX24T/RX24U, and DTCb for RX26T)	●			
Event link controller (ELC)	×			○
I/O ports	●/▲/■			
Multi-function pin controller (MPC)	●/▲			
Multi-function timer pulse unit 3 (MTU3d)	●/▲			
Port output enable 3 (POE3b and POE3A for RX24T, POE3A for RX24U, and POE3D for RX26T)	●/▲/■*1			
General purpose PWM timer (GPTB for RX24T/RX24U, and GPTWa for RX26T)	●/▲/■			
High resolution PWM waveform generation circuit (HRPWM)	×			○
Port output enable for GPTW (POEG)	×			○
8-bit timer (TMR for RX24T/RX24U, and TMRb for RX26T)	●			
Compare match timer (CMT)	●			
Compare match timer W (CMTW)	×			○
Watchdog timer (WDTA)	×			○
Independent watchdog timer (IWDTa)	●/■			
Serial communications interface (SCIg for RX24T/RX24U, and SCIk and SCIh for RX26T)	●/▲/■			
Serial communications interface (RSCI)	×			○
I^2C bus interface (RIICa)	●			
I^3C bus interface (RI3C)	×			○

Function	RX24T		RX24U	RX26T
	Chip Version A	Chip Version B		
CAN module (RSCAN for RX24T/RX24U), CAN FD module (CANFD-Lite for RX26T)	●/▲/■			
Serial peripheral interface (RSPIb for RX24T/RX24U, and RSPId for RX26T)	●/▲/■			
Serial peripheral interface (RSPIA)	×			○
CRC calculator (CRC for RX24T/RX24U, and CRCA for RX26T)	●/▲			
Trigonometric function calculator (TFUv2)	×			○
Trusted Secure IP (TSIP-Lite)	×			○
12-bit A/D converter (S12ADF for RX24T/RX24U, and S12ADHa for RX26T)	●/▲/■			
D/A converter (DA, DAa for RX24T, and DAa for RX24U) 12-bit D/A converter (R12DAb for RX26T)	●/▲/■*2			
Temperature sensor (TEMPS)	×			○
Comparator C (CMPC) (CMPCa for RX26T)	●/▲/■			
Data operation circuit (DOC) (DOCA for RX26T)	●/▲/■			
RAM	●/▲			
Flash memory	●/▲/■			
Packages	●/■			

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Notes: 1. On the RX24T Group, the POE3b is implemented on chip version A and the POE3A is implemented on chip version B.
2. On the RX24T Group, the DA is implemented on chip version A and the DAa is implemented on chip version B.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX24T/RX24U	RX26T
CPU	• Maximum operating frequency: 80 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • ROM cache: 2 KB (disabled by default)	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions (For products with a RAM capacity of 64 KB) • 111 instructions (For products with a RAM capacity of 48 KB) — Basic instructions: 77 — Single-precision floating point instructions: 11 — DSP instructions: 23 — Instructions for register bank save function: 2 (Only for products with a RAM capacity of 64 KB) • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits

Item	RX24T/RX24U	RX26T
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparison of Operating Mode Registers.

Table 2.2 Comparison of Operating Mode Registers

Register	Bit	RX24T/RX24U	RX26T
SYSCR1	—	System control register 1	System control register 1
		Initial value after a reset differs.	
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is Comparative Memory Map in Single-Chip Mode.

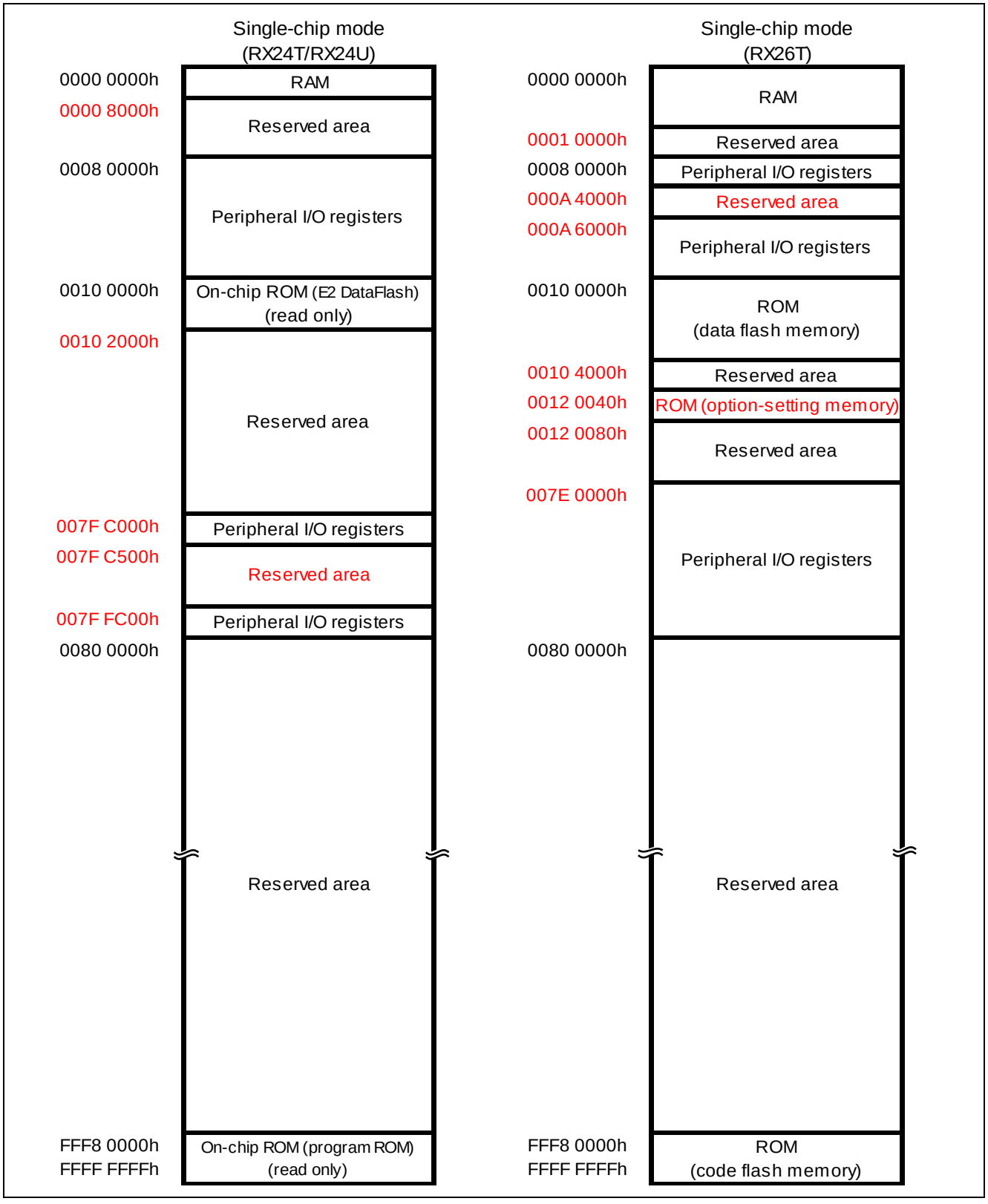

Figure 2.1 Comparative Memory Map in Single-Chip Mode

2.4 Resets

Table 2.3 is Comparative Overview of Resets, and Table 2.4 is Comparison of Reset-Related Registers.

Table 2.3 Comparative Overview of Resets

Item	RX24T/RX24U	RX26T
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Independent watchdog timer reset	Independent watchdog timer underflow, or refresh error	Independent watchdog timer underflow or refresh error
Watchdog timer reset	—	Watchdog timer underflow or refresh error
Software reset	Register setting	Register setting

Table 2.4 Comparison of Reset-Related Registers

Register	Bit	RX24T/RX24U	RX26T
RSTSR2	WDTRF	—	Watchdog timer reset detect flag

2.5 Option-Setting Memory

Figure 2.2 is Comparison of Option-Setting Memory Areas, and Table 2.5 is Comparison of Option-Setting Memory Registers.

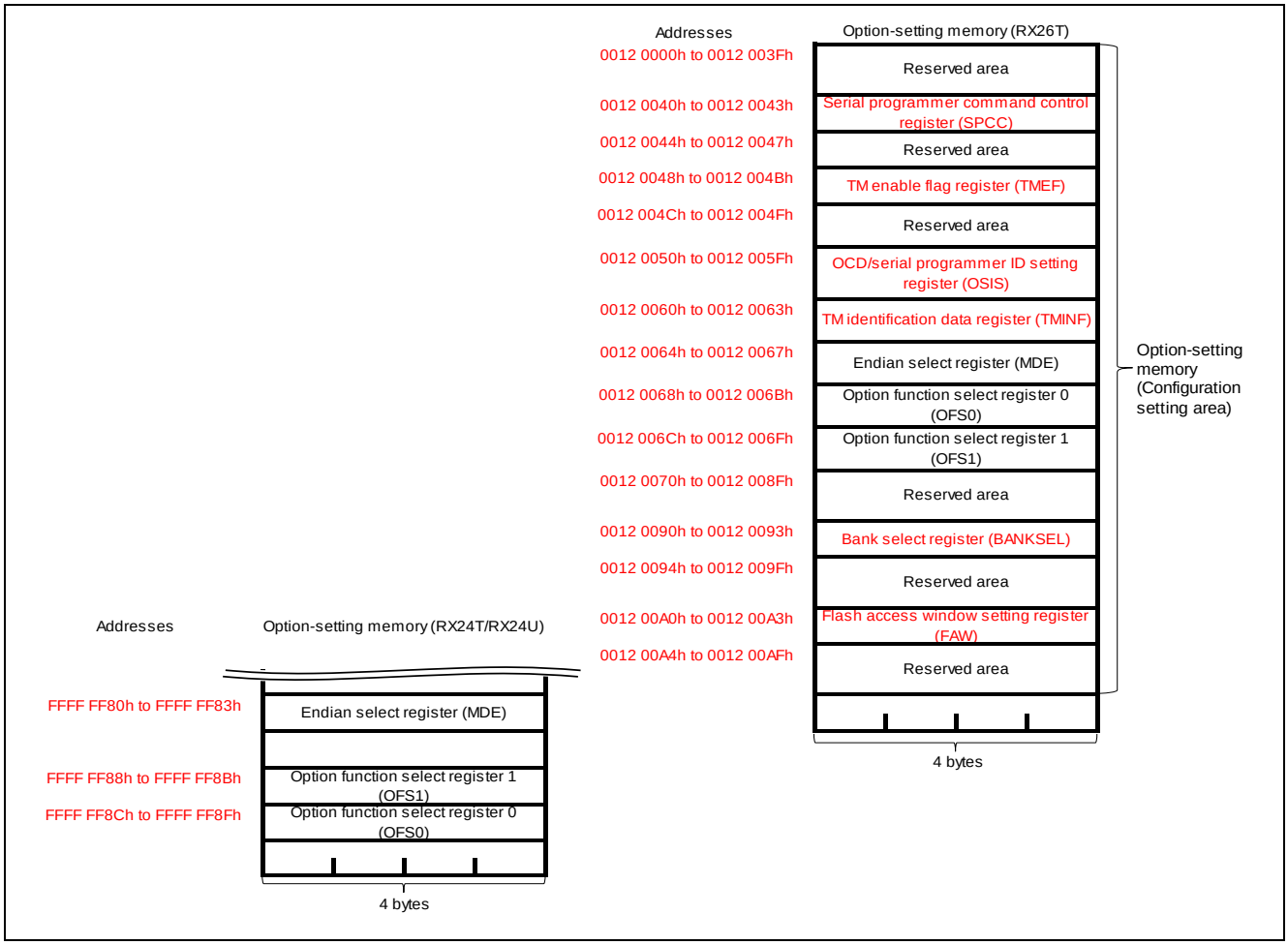

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.5 Comparison of Option-Setting Memory Registers

Register	Bit	RX24T/RX24U	RX26T (OFSM)
SPCC	—	—	Serial programmer command control register
OSIS	—	—	OCD/serial programmer ID setting register
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.
	WDTSTRT	—	WDT start mode select bit
	WDTTOPS[1:0]	—	WDT timeout period select bits
	WDTCKS[3:0]	—	WDT clock frequency division ratio select bits
	WDTRPES[1:0]	—	WDT window end position select bits
	WDTRPSS[1:0]	—	WDT window start position select bits
	WDTRSTIRQS	—	WDT reset interrupt request select bit
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Settings other than above are prohibited when the voltage detection 0 circuit is used.	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected 1 1: 4.22 V is selected
MDE	BANKMD[2:0]	—	Bank mode select bits
TMEF	—	—	TM enable flag register
TMINF	—	—	TM identification data register
BANKSEL	—	—	Bank select register
FAW	—	—	Flash access window setting register

2.6 Voltage Detection Circuit

Table 2.6 is Comparative Overview of Voltage Detection Circuits, and Table 2.7 is Comparison of Voltage Detection Circuit Registers.

In addition, Table 2.8 is Comparison of Setting Procedures for Monitoring Vdet1, Table 2.9 is Comparison of Setting Procedures for Monitoring Vdet2, and Table 2.10 to Table 2.13 are comparative listings of the setting procedures for bits related to the voltage monitoring 1 and 2 interrupts and the voltage monitoring 1 and 2 resets.

Table 2.6 Comparative Overview of Voltage Detection Circuits

Item		RX24T (LVDAb)/RX24U (LVDAb)			RX26T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
	Detection voltage	Selectable from 3 levels using the OFS1 register	Selectable from 9 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 4 levels using LVDLVLR. LVD2LVL[1:0] bits	Selectable from 2 levels using OFS1. VDSEL[1:0] bits	Selectable from 5 levels using LVDLVLR. LVD1LVL[3:0] bits	Selectable from 5 levels using LVDLVLR. LVD2LVL[3:0] bits
	Monitoring flag	Not available	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2	Not available	LVD1SR.LVD1 MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2 MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection		LVD1SR.LVD1 DET flag: Vdet1 passage detection	LVD2SR.LVD2 DET flag: Vdet2 passage detection
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage Monitoring 1 reset	Voltage Monitoring 2 reset	Voltage monitoring 0 reset	Voltage Monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupt	Not available	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt	Not available	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either

Item		RX24T (LVDAb)/RX24U (LVDAb)			RX26T (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Digital filter	Enable/ disable switching	—	—	—	Digital filter function not available	Available	Available
	Sampling time	—	—	—	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	—	—	Not available	Available Output of event signals on detection of Vdet crossings	Available Output of event signals on detection of Vdet crossings

Table 2.7 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
LVDLVLR	—	Voltage detection level select register	Voltage detection level select register
		Initial value after a reset differs.	
	LVD1LVL [3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL [1:0] (RX24T/ RX24U) LVD2LVL [3:0] (RX26T)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.
LVD1CR0	—	Voltage monitoring 1 circuit control register 0	Voltage monitoring 1 circuit control register 0
		Initial value after a reset differs.	
	LVD1DFDIS	—	Voltage monitoring 1 digital filter disable mode select bit
	LVD1FSAMP [1:0]	—	Sampling clock select bits
LVD2CR0	—	Voltage monitoring 2 circuit control register 0	Voltage monitoring 2 circuit control register 0
		Initial value after a reset differs.	
	LVD2DFDIS	—	Voltage monitoring 2 digital filter disable mode select bit
	LVD2FSAMP [1:0]	—	Sampling clock select bits

Table 2.8 Comparison of Setting Procedures for Monitoring Vdet1

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Setting procedure for monitoring Vdet1	1	Specify the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 level select).	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.9 Comparison of Setting Procedures for Monitoring Vdet2

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Setting procedure for monitoring Vdet2	1	Specify the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 level select).	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Wait for at least td(E-A).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 2).	LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2)

Table 2.10 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Set the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	Set LVD1CR0.LVD1RI = 0 (voltage monitoring 1 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	9	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	—
	10	Set the LVD1SR.LVD1DET bit to 0.	Set LVD1SR.LVD1DET = 0.
	11	Set the LVD1CR0.LVD1RIE bit to 1 (enabling voltage monitoring 1 interrupts/resets).	Set LVD1CR0.LVD1RIE = 1 (enabling voltage monitoring 1 interrupts/resets).
	12	—	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 1 reset	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	• Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.	Set LVCMPCR.LVD1E = 1 (enabling the voltage detection 1 circuit).
	3	Set the LVD1CR0.LVD1RIE bit to 1 (enabling voltage monitoring 1 interrupts/resets).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD1E bit to 1 (enabling the voltage detection 1 circuit).	• Set the LVD1CR0.LVD1RI = 1 (voltage monitoring 1 reset). • Select the type of reset negation by setting the LVD1CR0.LVD1RN bit.
	8	Wait for at least td(E-A).	Set LVD1SR.LVD1DET = 0.
	9	—	Set LVD1CR0.LVD1RIE = 1 (enabling voltage monitoring 1 interrupts/resets).
	10	Set the LVD1CR0.LVD1CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1CMPE = 1 (enabling output of the results of comparison by voltage monitoring 1).

Table 2.11 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 1 interrupt	1	Set the LVD1CR0.LVD1RIE bit to 0 (disabling voltage monitoring 1 interrupts/resets).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD1CR0.LVD1CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1RIE = 0 (disabling voltage monitoring 1 interrupts/resets).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is in use — (No procedure)
	5	Set the LVCMPCR.LVD1E bit to 0 (disabling the voltage detection 1 circuit).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—
Operation-disable setting procedure for bits related to voltage monitoring 1 reset	1	Set the LVD1CR0.LVD1CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 1).	Set LVD1CR0.LVD1CMPE = 0 (disabling output of the results of comparison by voltage monitoring 1).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD1E bit to 0 (disabling the voltage detection 1 circuit).	Set LVD1CR0.LVD1RIE = 0 (disabling voltage monitoring 1 interrupts/resets).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD1CR0.LVD1DFDIS = 1 (disabling the digital filter). • When the digital filter is in use — (No procedure)
	5	Set the LVD1CR0.LVD1RIE bit to 0 (disabling voltage monitoring 1 interrupts/resets).	Set LVCMPCR.LVD1E = 0 (disabling the voltage detection 1 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD1E, LVD1CR0.LVD1RIE, and LVD1CR0.LVD1CMPE.	—

Table 2.12 Comparison of Operation-Enable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	Set the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	Set LVD2CR0.LVD2RI = 0 (voltage monitoring 2 interrupt).
	8	Wait for at least td(E-A).	• Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. • Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	9	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 2).	—
	10	Set the LVD2SR.LVD2DET bit to 0.	Set LVD2SR.LVD2DET = 0.
	11	Set the LVD2CR0.LVD2RIE bit to 1 (enabling voltage monitoring 2 interrupts/resets).	Set LVD2CR0.LVD2RIE = 1 (enabling voltage monitoring 2 interrupts/resets).
	12	—	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-enable setting procedure for bits related to voltage monitoring 2 reset	1	Set the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.
	2	• Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set LVCMPCR.LVD2E = 1 (enabling the voltage detection 2 circuit).
	3	Set the LVD2CR0.LVD2RIE bit to 1 (enabling voltage monitoring 2 interrupts/resets).	Wait for at least td(E-A) (LVD operation stabilization time after LVD is enabled).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • When the digital filter is not in use — (No procedure)
	5	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 0 (enabling the digital filter). • When the digital filter is not in use — (No procedure)
	6	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	7	Set the LVCMPCR.LVD2E bit to 1 (enabling the voltage detection 2 circuit).	• Set the LVD2CR0.LVD2RI = 1 (voltage monitoring 2 reset). • Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.
	8	Wait for at least td(E-A).	Set LVD2SR.LVD2DET = 0.
	9	—	Set LVD2CR0.LVD2RIE = 1 (enabling voltage monitoring 2 interrupts/resets).
	10	Set the LVD2CR0.LVD2CMPE bit to 1 (enabling output of the results of comparison by voltage monitoring 2).	Set LVD2CR0.LVD2CMPE = 1 (enabling output of the results of comparison by voltage monitoring 2).

Table 2.13 Comparison of Operation-Disable Setting Procedures for Bits Related to Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset

Item		RX24T (LVDAb)/RX24U (LVDAb)	RX26T (LVDA)
Operation-disable setting procedure for bits related to voltage monitoring 2 interrupt	1	Set the LVD2CR0.LVD2RIE bit to 0 (disabling voltage monitoring 2 interrupts/resets).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVD2CR0.LVD2CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 2).	Set LVD2CR0.LVD2RIE = 0 (disabling voltage monitoring 2 interrupts/resets).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is in use — (No procedure)
	5	Set the LVCMPCR.LVD2E bit to 0 (disabling the voltage detection 2 circuit).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—
Operation-disable setting procedure for bits related to voltage monitoring 2 reset	1	Set the LVD2CR0.LVD2CMPE bit to 0 (disabling output of the results of comparison by voltage monitoring 2).	Set LVD2CR0.LVD2CMPE = 0 (disabling output of the results of comparison by voltage monitoring 2).
	2	— (No procedure because there is no digital filter)	• When the digital filter is in use Wait for at least 2n + 3 cycles of LOCO (where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency divided by n). • When the digital filter is not in use — (No procedure)
	3	Set the LVCMPCR.LVD2E bit to 0 (disabling the voltage detection 2 circuit).	Set LVD2CR0.LVD2RIE = 0 (disabling voltage monitoring 2 interrupts/resets).
	4	— (No procedure because there is no digital filter)	• When the digital filter is in use Set LVD2CR0.LVD2DFDIS = 1 (disabling the digital filter). • When the digital filter is in use — (No procedure)
	5	Set the LVD2CR0.LVD2RIE bit to 0 (disabling voltage monitoring 2 interrupts/resets).	Set LVCMPCR.LVD2E = 0 (disabling the voltage detection 2 circuit).
	6	Modify settings of bits related to the voltage detection circuit registers other than LVCMPCR.LVD2E, LVD2CR0.LVD2RIE, and LVD2CR0.LVD2CMPE.	—

2.7 Clock Generation Circuit

Table 2.14 is Comparative Overview of Clock Generation Circuits, and Table 2.15 is Comparison of Clock Generation Circuit Registers.

Table 2.14 Comparative Overview of Clock Generation Circuits

Item	RX24T	RX24U	RX26T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM.
	• Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules: The peripheral module clock PCLKA is the operating clock for the MTU and GPT, the peripheral module clock PCLKD is for the S12AD, and peripheral module clock PCLKB is for other modules.	• Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules: The peripheral module clock PCLKA is the operating clock for the MTU, GPT, and SCI11, the peripheral module clock PCLKD is for the S12AD, and peripheral module clock PCLKB is for other modules.	• Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, RSPIA, RSCI, RI3C, CANFD, MTU (internal peripheral bus), GPTW (internal peripheral bus), and HRPWM (internal peripheral bus). • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the counter reference clock for peripheral modules and the HRPWM reference clock (PCLKC) to be supplied to the MTU and GPTW. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD.
	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC.	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC.	• Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD.
	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN.	• Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX24T	RX24U	RX26T
Operating frequency	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same as the clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 80 MHz (max.) • PCLKA: 80 MHz (max.) • PCLKB: 40 MHz (max.) • PCLKD: 40 MHz (max.) • FCLK: 1 MHz to 32 MHz (ROM) • CACCLK: Same as the clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.)	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKC: 120 MHz (max.) • PCLKD: 8 MHz to 60 MHz (for conversion with the 12-bit A/D converter) • FCLK: — 4 MHz to 60 MHz (for programming and erasing the code flash memory and data flash memory) — 60 MHz (max.) (for reading from the data flash memory) • CACCLK: Same as the clock from respective oscillators • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and MTU and GPT pin output stops. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and MTU and GPT pin output stops. • Drive capacity switching function	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU and GPTW pins are driven to high-impedance state.

Item	RX24T	RX24U	RX26T
PLL frequency synthesizer	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock and HOCO (32 MHz) clock divided by 4 • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 40 MHz to 80 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of the PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz, 64 MHz	Oscillation frequency: 32 MHz, 64 MHz	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz	Oscillation frequency: 120 kHz
Event link function (output)	—	—	Detection of stopping of the main clock oscillator
Event link function (input)	—	—	Switching of the clock source to the low-speed on-chip oscillator

Table 2.15 Comparison of Clock Generation Circuit Registers

Register	Bit	RX24T/RX24U	RX26T
SCKCR	—	System clock control register	System clock control register
		Initial value after a reset differs.	
	PCKC[3:0]	—	Peripheral module clock C (PCLKC) select bits
SCKCR2	—	—	System clock control register 2
PLLCR	—	PLL control register	PLL control register
		Initial value after a reset differs.	
	PLLSRCSEL	PLL clock source selection bit (b2)	PLL clock source selection bit (b4)
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 : : 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 : : 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.
HOCOCR2	HCFRQ[1:0]	HOCO frequency setting bits b1 b0 0 0: 32 MHz 1 1: 64 MHz Settings other than the above are prohibited.	HOCO frequency setting bits b1 b0 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz Settings other than the above are prohibited.
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—

Register	Bit	RX24T/RX24U	RX26T
OSCOVFSR	—	Oscillation stabilization flag register	Oscillation stabilization flag register
		Initial value after a reset differs.	
	MOOVF	Main clock oscillation stabilization flag 0: Main clock oscillator stopped. 1: Oscillation of the main clock is stable, so the clock is available for use as the system clock.	Main clock oscillation stabilization flag 0: MOSTP = 1 (main clock oscillator stopped), or oscillation of the main clock has not yet become stable. 1: Oscillation of the main clock is stable, so the clock is available for use as the system clock.
	ILCOVF	—	IWDT-dedicated clock oscillation stabilization flag
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE.	Oscillation stop detection interrupt enable bit 0: The oscillation stop detection interrupt is disabled, and oscillation stop detection is not reported to the POE or POEG. 1: The oscillation stop detection interrupt is enabled, and oscillation stop detection is reported to the POE or POEG.
MOSCWTCR	—	Main clock oscillator wait control register	Main clock oscillator wait control register
		Initial value after a reset differs.	
	MSTS[4:0] (RX24T/ RX24U) MSTS[7:0] (RX26T)	Main clock oscillator wait time setting bits (b4 to b0) b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	Waiting time until output from the main clock oscillator to the internal circuits starts (b7 to b0) MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 (tMAINOSC: main clock oscillation stabilization time; fLOCO_max: maximum fLOCO frequency)

Register	Bit	RX24T/RX24U	RX26T
MOFCR	MODRV21 (RX24T/ RX24U) MODRV2 [1:0] (RX26T)	Main clock oscillator drive capability switch bits 0: 1 MHz or higher and lower than 10 MHz 1: 10 MHz to 20 MHz	Main clock oscillator drive capability 2 switch bits b5 b4 0 0: 20.1 to 24 MHz 0 1: 16.1 to 20 MHz 1 0: 8.1 to 16 MHz 1 1: 8 MHz
HOCOPCR	—	—	High-speed on-chip oscillator power supply control register
MEMWAIT	—	Memory wait cycle setting register	—

2.8 Low Power Consumption

Table 2.16 is Comparative Overview of Low Power Consumption Functions, Table 2.17 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.18 is Comparison of Low Power Consumption Registers.

Table 2.16 Comparative Overview of Low Power Consumption Functions

Item	RX24T/RX24U	RX26T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, PCLKC, PCLKD), and flash interface clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available: High-speed operating mode Middle-speed operating mode	—

Table 2.17 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX24T/RX24U	RX26T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Watchdog timer	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	Comparator C	Operation possible	—
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer	—	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Port output enable (POE)	—	Stopped (retained)
	8-bit timer (unit 0, unit1) (TMR)	—	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX24T/RX24U	RX26T
Software standby mode	I/O ports	Retained	Retained
	Comparator C	Operation possible	—

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.18 Comparison of Low Power Consumption Registers

Register	Bit	RX24T	RX24U	RX26T
MSTPCRA	—	Module stop control register A	Module stop control register A	Module stop control register A
		Initial value after a reset differs.		
	MSTPA0	—	—	Compare match timer W (unit 1) module stop bit
	MSTPA1	—	—	Compare match timer W (unit 0) module stop bit
	MSTPA7	General purpose PWM timer module stop bit Target module: GPT 0: Release from module-stop state 1: Transition to module-stop state	General purpose PWM timer module stop bit Target module: GPT 0: Release from module-stop state 1: Transition to module-stop state	General purpose PWM timer/high resolution PWM/GPTW-dedicated port output enable module stop bit Target module: GPTW, HRPWM, POEG 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA19	8-bit D/A converter module stop bit Target module: DA 0: Release from module-stop state 1: Transition to module-stop state	8-bit D/A converter module stop bit Target module: DA 0: Release from module-stop state 1: Transition to module-stop state	12-bit D/A converter module stop bit Target module: 12-bit DA 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA24	—	—	Module stop A24 setting bit
	MSTPA27	—	—	Module stop A27 setting bit
	MSTPA28	Data transfer controller module stop bit Target module: DTC 0: Release from module-stop state 1: Transition to module-stop state	Data transfer controller module stop bit Target module: DTC 0: Release from module-stop state 1: Transition to module-stop state	DMA controller/data transfer controller module stop bit Target module: DMAC/DTC 0: Release from module-stop state 1: Transition to module-stop state
	MSTPA29	—	—	Module stop A29 setting bit
	ACSE	—	—	All-module clock stop mode enable bit
MSTPCRB	MSTPB0	RSCAN module stop bit*1	RSCAN module stop bit*1	—
	MSTPB4	—	—	Serial communications interface 12 module stop bit
	MSTPB9	—	—	Event link controller module stop bit

Register	Bit	RX24T	RX24U	RX26T
MSTPCRC	MSTPC24	—	Serial communications interface 11 module stop bit Target module: SCI11 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 11 module stop bit Target module: RSCI11 0: Release from module-stop state 1: Transition to module-stop state
	MSTPC26	—	Serial communications interface 9 module stop bit Target module: SCI9 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 9 module stop bit Target module: RSCI9 0: Release from module-stop state 1: Transition to module-stop state
	MSTPC27	—	Serial communications interface 8 module stop bit Target module: SCI8 0: Release from module-stop state 1: Transition to module-stop state	Serial communications interface 8 module stop bit Target module: RSCI8 0: Release from module-stop state 1: Transition to module-stop state
	DSLPE	Deep sleep mode enable bit	Deep sleep mode enable bit	—
MSTPCRD	—	—	—	Module stop control register D
RSTCKCR	—	—	—	Sleep mode return clock source switching register
OPCCR	—	Operating power control register	Operating power control register	—

Note: 1. When rewriting this bit, confirm that the clock oscillation controlled by this bit is stable. To enter the software standby mode after rewriting this bit, wait for 2 cycles of CANMCLK after the rewrite, and then execute the WAIT instruction.

2.9 Register Write Protection Function

Table 2.19 is Comparative Overview of Register Write Protection Functions, and Table 2.20 is Comparison of Register Write Protection Function Registers.

Table 2.19 Comparative Overview of Register Write Protection Functions

Item	RX24T/RX24U	RX26T
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR, MEMWAIT	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR,HOCOCR, HOCOCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR • Registers related to the clock generation circuit: MOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR
PRC2 bit	• Registers related to the clock generation circuit: HOCOWTCR	—
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.20 Comparison of Register Write Protection Function Registers

Register	Bit	RX24T/RX24U	RX26T
PRCR	PRC2	Protect bit 2	—

2.10 Interrupt Controller

Table 2.21 is Comparative Overview of Interrupt Controllers, and Table 2.22 is Comparison of Interrupt Controller Registers.

Table 2.21 Comparative Overview of Interrupt Controllers

Item		RX24T (ICUb)/RX24U (ICUb)	RX26T (ICUG)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • Digital filter function: Supported	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.

Item		RX24T (ICUb)/RX24U (ICUb)	RX26T (ICUG)
Interrupts	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	Specified by registers.	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	This interrupt occurs when the main clock oscillator stop is detected.
	WDT underflow/ refresh error interrupt	—	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection 1 circuit (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection 2 circuit (LVD2)
	RAM error interrupt	—	Interrupt occurs when a parity check error is detected in RAM.
Return from low power consumption state	Sleep mode	Exit sleep mode by a non-maskable interrupt or any other interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	—	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, IWDT, or TMR0 to TMR3).
	Software standby mode	Exit deep software standby mode by a non-maskable interrupt or IRQ0 to IRQ7 interrupt.	Exit deep software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, or IWDT).

Table 2.22 Comparison of Interrupt Controller Registers

Register	Bit	RX24T (ICUb)/RX24U (ICUb)	RX26T (ICUG)
IRn*1	—	Interrupt request register n (n = 016 to 249)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 249)	Interrupt source priority register r (r = 000 to 255)
SWINT2R	—	—	Software interrupt 2 generation register
DTCERn*1	—	DTC transfer request enable register n (n = 027 to 248)	DTC transfer request enable register n (DTCERn) (n = 026 to 255)
	DTCE	DTC transfer request enable bit 0: Set to an interrupt source to the CPU. 1: Set to the DTC activation source.	DTC transfer request enable bit 0: Set to an interrupt source to the CPU, or DMAC activation source. 1: Set to the DTC activation source.
DMRSRm	—	—	DMAC activation source select register m (m = 0 to 7)
IRQCRi	—	IRQ control register I (i = 0 to 7)	IRQ control register I (i = 0 to 15)
IRQFLTE1	—	—	IRQ pin digital filter enable register 1
IRQFLTC1	—	—	IRQ pin digital filter setting register 1
NMISR	WDTST	—	WDT underflow/refresh error status flag
	RAMST	—	RAM error interrupt status flag
NMIER	WDTEN	—	WDT underflow/refresh error enable bit
	RAMEN	—	RAM error interrupt enable bit
NMICLR	WDTCLR	—	WDT clear bit
GRPBL0/ GRPBL1/ GRPBL2	—	—	Group BL0/BL1/BL2 interrupt request register
GRPAL0/ GRPAL1	—	—	Group AL0/ AL1 interrupt request register
GENBL0/ GENBL1/ GENBL2	—	—	Group BL0/BL1/BL2 interrupt request enable register
GENAL0/ GENAL1	—	—	Group AL0/ AL1 interrupt request enable register
PIARk	—	—	Software configurable interrupt A request register k (k = 0h to Fh, 12h to 14)
SLIARn	—	—	Software configurable interrupt A source select register n (n = 208 to 255)
SLIPRCR	—	—	Software configurable interrupt source select register Write protection register

Note: 1. On the RX24T Group, n = 250 to 255, and on the RX24U Group, n = 254, and 255 corresponds to a reserved memory area.

2.11 Buses

Table 2.23 is Comparative Overview of Buses, and Table 2.24 is Comparison of Bus Registers.

Table 2.23 Comparative Overview of Buses

Item		RX24T	RX24U	RX26T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM	Connected to code flash memory
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)

Item		RX24T	RX24U	RX26T
Internal peripheral buses	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (RSCAN and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (RSCAN and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (DOC, RSCI, CANFD, and CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU and GPT) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, GPT, and SCI11) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, GPTW, HRPWM, and RSPI) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	—	—	• Connected to peripheral modules (RSCI, RSPIA, RI3C, and CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.24 Comparison of Bus Registers

Register	Bit	RX24T/RX24U	RX26T
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved	Bus master code bits b6 b4 0 0 0: CPU 0 0 1: Reserved 0 1 0: Reserved 0 1 1: DTC/DMAC 1 0 0: Reserved 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved
BUSPRI	BPHB[1:0]	Internal peripheral bus 4 priority control bits b9 b8 0 0: Fixed priority 0 1: Toggled priority 1 0: Setting prohibited 1 1: Setting prohibited	Priority control bits for internal peripheral buses 4 and 5 b9 b8 0 0: Fixed priority 0 1: Toggled priority 1 0: Setting prohibited 1 1: Setting prohibited

2.12 Data Transfer Controller

Table 2.25 is Comparative Overview of Data Transfer Controllers, and Table 2.26 is Comparison of Data Transfer Controller Registers.

Table 2.25 Comparative Overview of Data Transfer Controllers

Item	RX24T (DTCa)/RX24U (DTCa)	RX26T (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode A single activation leads to the transfer of a single block of data. The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple types of data transfer can be performed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX24T (DTCa)/RX24U (DTCa)	RX26T (DTCb)
Transfer space	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (from 0000 0000h to 007F FFFFh or from FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	—	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.26 Comparison of Data Transfer Controller Registers

Register	Bit	RX24T (DTCa)/RX24U (DTCa)	RX26T (DTCb)
MRA	WBDIS	—	Write-back disable bit
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

2.13 I/O Ports

Table 2.27 is Comparative Overview of I/O Ports on 100-Pin Products, Table 2.29 is Comparative Overview of I/O Ports on 64-Pin Products, Table 2.30 is Comparison of I/O Port Functions, and Table 2.32 is Comparison of I/O Port Registers.

Table 2.27 Comparative Overview of I/O Ports on 100-Pin Products

Item	RX24T (100-Pin) Common to Chip Versions A and B	RX24U (100-Pin)	RX26T (100-Pin)
PORT0	P00 to P02	P00 to P02	P00, P01
PORT1	P10, P11	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P24, P27	P20 to P24, P27
PORT3	P30 to P33, P36, P37	P30 to P33, P36, P37	P30 to P33, P36, P37
PORT4	P40 to P47	P40 to P47	P40 to P47
PORT5	P50 to P55	P52 to P55	P50 to P55
PORT6	P60 to P65	P60 to P65	P60 to P65
PORT7	P70 to P76	P70 to P76	P70 to P76
PORT8	P80 to P82	P80 to P82	P80 to P82
PORT9	P90 to P96	P90 to P96	P90 to P96
PORTA	PA0 to PA5	PA0 to PA5	PA0 to PA5
PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE5	PE0 to PE5	PE0 to PE5
PORTN	—	—	PN6, PN7

Table 2.28 Comparative Overview of I/O Ports on 80-Pin Products

Item	RX24T (80-Pin)	RX26T (80-Pin)
PORT0	P00 to P02	P00, P01
PORT1	P10, P11	P10, P11
PORT2	P20 to P24	P20 to P22, P27
PORT3	P30, P31, P36, P37	P30, P31, P36, P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORT6	P62	P60, P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P90 to P96	P90 to P96
PORTA	PA3, PA5	PA3, PA5
PORTB	PB0 to PB6	PB0 to PB6
PORTD	PD2 to PD7	PD2 to PD7
PORTE	PE2 to PE4	PE2 to PE4
PORTN	—	PN6, PN7

Table 2.29 Comparative Overview of I/O Ports on 64-Pin Products

Item	RX24T (64-Pin)	RX26T (64-Pin)
PORT0	P00 to P02	P00, P01
PORT1	P11	P11
PORT2	P21 to P24	P20 to P22
PORT3	P30, P31, P36, P37	P36, P37
PORT4	P40 to P42, P44 to P46	P40 to P47
PORT5	P50 to P54	P52 to P54
PORT6	—	P64, P65
PORT7	P70 to P76	P70 to P76
PORT9	P90 to P96	P90 to P96
PORTB	PB1 to PB6	PB0 to PB6
PORTD	PD3 to PD7	PD3 to PD7
PORTE	PE2	PE2
PORTN	—	PN6, PN7

Table 2.30 Comparison of I/O Port Functions

Item	Port Symbol	RX24T	RX24U	RX26T
Input pull-up function	PORT0	P00 to P02	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17	P10, P11
	PORT2	P20 to P24	P20 to P27	P20 to P24, P27
	PORT3	P30 to P33, P36, P37	P30 to P37	P30 to P33, P36, P37
	PORT4	P40 to P47	P40 to P47	P40 to P47
	PORT5	P50 to P55	P50 to P55	P50 to P55
	PORT6	P60 to P65	P60 to P65	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P84	P80 to P82
	PORT9	P90 to P96	P90 to P96	P90 to P96
	PORTA	PA0 to PA5	PA0 to PA7	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6	—
	PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
	PORTF	—	PF0 to PF3	—
	PORTG	—	PG0 to PG2	—
	PORTN	—	—	PN6, PN7
Open-drain output function	PORT0	P00 to P02	P00 to P02	P00, P01
	PORT1	P10, P11	P10 to P17	P10, P11
	PORT2	P20 to P24	P20 to P27	P20 to P24, P27
	PORT3	P30 to P33, P36, P37	P30 to P37	P30 to P33, P36, P37
	PORT4	—	—	P40 to P47
	PORT5	—	—	P50 to P55
	PORT6	—	—	P60 to P65
	PORT7	P70 to P76	P70 to P76	P70 to P76
	PORT8	P80 to P82	P80 to P84	P80 to P82
	PORT9	P90 to P96	P90 to P96	P90 to P96
	PORTA	PA0 to PA5	PA0 to PA7	PA0 to PA5
	PORTB	PB0 to PB7	PB0 to PB7	PB0 to PB7
	PORTC	—	PC0 to PC6	—
	PORTD	PD0 to PD7	PD0 to PD7	PD0 to PD7
	PORTE	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
	PORTF	—	PF0 to PF3	—
	PORTG	—	PG0 to PG2	—
	PORTN	—	—	PN6
5 V tolerant	PORTB	PB1, PB2	PB1, PB2	PB1, PB2

Table 2.31 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX24T	RX24U	RX26T
PORT0	Fixed to normal output	—	—	—
	Normal/high	P00 to P02	P00 to P02	P00, P01
PORT1	Fixed to normal output	—	—	—
	Normal/high	P10, P11	P10 to P17	P10, P11
PORT2	Fixed to normal output	—	—	—
	Normal/high	P20 to P24	P20 to P27	P20 to P24, P27
PORT3	Fixed to normal output	P36, P37	P36, P37	P36, P37
	Normal/high	P30 to P33	P30 to P35	P30 to P33
PORT4	Fixed to normal output	P40 to P47	P40 to P47	P40 to P47
	Normal/high	—	—	—
PORT5	Fixed to normal output	P50 to P55	P50 to P55	P50 to P55
	Normal/high	—	—	—
PORT6	Fixed to normal output	P60 to P65	P60 to P65	P60 to P65
	Normal/high	—	—	—
PORT7	Fixed to normal output	—	—	—
	Fixed to high drive output	P71 to P76	P71 to P76	—
	Normal/high	P70	P70	P70
	Normal/high/large current output	—	—	P71 to P76
PORT8	Fixed to normal output	—	—	—
	Fixed to high drive output	P81	P81	—
	Normal/high	P80, P82	P80, P82 to P84	P80, P82
	Normal/high/large current output	—	—	P81
PORT9	Fixed to normal output	—	—	—
	Fixed to high drive output	P90 to P95	P90 to P95	—
	Normal/high	P96	P96	P96
	Normal/high/large current output	—	—	P90 to P95
PORTA	Fixed to normal output	—	—	—
	Normal/high	PA0 to PA5	PA0 to PA7	PA0 to PA5
PORTB	Fixed to normal output	—	—	PB1, PB2
	Fixed to high drive output	PB1, PB2, PB5	PB1, PB2, PB5	—
	Normal/high	PB0, PB3, PB4, PB6, PB7	PB0, PB3, PB4, PB6, PB7	PB0, PB3, PB4, PB6, PB7
	Normal/high/large current output	—	—	PB5
PORTC	Fixed to normal output	—	—	—
	Normal/high	—	PC0 to PC6	—
PORTD	Fixed to normal output	—	—	—
	Fixed to high drive output	PD3	PD3	—
	Normal/high	PD0 to PD2, PD4 to PD7	PD0 to PD2, PD4 to PD7	PD0 to PD2, PD4 to PD7
	Normal/high/large current output	—	—	PD3
PORTE	Fixed to normal output	—	—	—
	Normal/high	PE0, PE1, PE3 to PE5	PE0, PE1, PE3 to PE6	PE0, PE1, PE3 to PE5
PORTF	Fixed to normal output	—	—	—
	Normal/high	—	PF0 to PF3	—
PORTG	Fixed to normal output	—	—	—
	Normal/high	—	PG0 to PG2	—
PORTN	Normal/high	—	—	PN6, PN7

Table 2.32 Comparison of I/O Port Registers

Register	Bit	RX24T	RX24U	RX26T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to G)	Pm0 to Pm7 I/O select bits (m = 0 to 9, A, B, D, E, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G)	Pm0 to Pm7 output data store bits (m = 0 to 9, A, B, D, E, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 bits (m = 0 to 9, A to G)	Pm0 to Pm7 bits (m = 0 to 9, A, B, D, E, N)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 pin mode control bits (m = 0 to 3, 7 to 9, A to G)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A, B, D, E, N)
ODR0	B0, B2, B4, B6	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 3, 7 to 9, A to G)	Pm0, Pm1, Pm2, and Pm3 output type select bits (m = 0 to 9, A, B, D, E)
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2, 7, 9, A, B, D, E)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 7 to 9, A to E)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2 to 7, 9, A, B, D, E, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A, B, D, E, N)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A, B, D, E)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A to G)	Pm0 to Pm7 drive capacity control bits (m = 0 to 3, 7 to 9, A, B, D, E, N)
DSCR2	—	—	—	Drive capacity control register 2
POHSR1	—	—	—	Port output retention setting register 1
POHSR2	—	—	—	Port output retention setting register 2
POHCR	—	—	—	Port output retention control register
GPSEXT	—	—	—	General I/O pin select extended register

2.14 Multi-Function Pin Controller

Table 2.33 and Table 2.34 compare the assignments of multiplexed pins, and Table 2.35 to Table 2.52 show a comparison of the multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX26T Group only, **orange text** pins that exist on the RX24T and RX24U Groups only, **light green text** pins that exist on the RX24U Group only, and **purple text** pins that exist on the RX26T and RX24T Groups only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.33 Comparison of Multiplexed Pin Assignments (100-Pin)

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX26T (MPC) 100-Pin
Interrupts	IRQ0 (input)	P10	○	○	○	○
		P52	○	○	○	○
		PE2	×	×	×	○
		PE5	○	○	○	○
	IRQ1 (input)	P11	○	○	○	○
		P53	○	○	○	○
		P95	×	×	×	○
		PA5	○	○	○	○
		PE4	○	○	○	○
	IRQ2 (input)	P00	○	○	○	○
		P54	○	○	○	○
		PB6	×	×	×	○
		PD4	○	○	○	○
		PE3	○	○	○	○
	IRQ3 (input)	P55	○	○	○	○
		P82	×	×	×	○
		PB4	○	○	○	○
		PD5	○	○	○	×
	IRQ4 (input)	P01	○	○	○	○
		P24	×	×	×	○
		P60	○	○	○	○
		P96	○	○	○	○
		PB1	×	×	×	○
	IRQ5 (input)	P02	○	○	○	×
		P61	○	○	○	○
		P70	○	○	○	○
		P80	×	×	×	○
		PB6	○	○	○	×
		PD6	○	○	○	○
		PN7	×	×	×	○
	IRQ6 (input)	P21	○	○	○	○
		P31	○	○	○	○
		P62	○	○	○	○
		PD5	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Interrupts	IRQ7 (input)	P20	○	○	○	○
		P30	○	○	○	○
		P63	○	○	○	○
		PE0	×	×	×	○
	IRQ8 (input)	P64				○
		PB0				○
		PD7				○
	IRQ9 (input)	P65				○
		PB3				○
	IRQ10 (input)	P22				○
	IRQ11 (input)	P23				○
	IRQ12 (input)	P32				○
	IRQ13 (input)	P33				○
	IRQ14 (input)	P93				○
		PA1				○
	IRQ15 (input)	P27				○
		PE1				○
	NMI (input)	PE2	○	○	○	○
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	○	○	○
		P70	×	×	×	○
		PB3	○	○	○	○
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	○	○	○
		PB2	○	○	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	P27	×	×	×	○
		PB1	○	○	○	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	○	○	○
	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P27	×	×	○	○
		P95	×	×	×	○
		PA5	○	○	○	○
	MTIOC1B (input/output)/ MTIOC1B# (input/output)	PA4	○	○	○	○
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	P94	×	×	×	○
		PA3	○	○	○	○
	MTIOC2B (input/output)/ MTIOC2B# (input/output)	PA2	○	○	○	○
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○	○
		P33	○	○	○	○
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○	○
	MTIOC3C (input/output)/ MTIOC3C# (input/output)	P32	○	○	○	○
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Multi-function timer unit 3	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○	○	○
		P82	○	○	○	○
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○	○	○
		P81	○	○	○	○
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○	○	○
		P80	○	○	○	○
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	P93	×	×	×	○
		PA1	○	○	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○	○	○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	P92	×	×	×	○
		PA0	○	○	○	○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○	○	○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○	○	○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○	○	○	○
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○	○	○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○	○	○	○
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P00	×	×	×	○
		P21	○	○	○	○
		PD7	○	○	○	○
	MTIOC9B (input/output)	P22				○
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10	○	○	○	○
		PE0	○	○	○	○
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P01	×	×	×	○
		P20	○	○	○	○
		PD6	○	○	○	○
	MTIOC9D (input/output)	P11				○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	P02	○	○	○	×
		PE1	○	○	○	○
		PE5	×	×	×	○
		PN7	×	×	×	○
	MTCLKA (input)/ MTCLKA# (input)	P21	○	○	○	○
		P33	○	○	○	○
	MTCLKB (input)/ MTCLKB# (input)	P20	○	○	○	○
		P32	○	○	○	○
	MTCLKC (input)/ MTCLKC# (input)	P11	○	○	○	○
		P31	○	○	○	○
		P70	×	×	×	○
		PE4	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Multi-function timer unit 3	MTCLKD (input)/ MTCLKD# (input)	P10	○	○	○	○
		P22	×	×	×	○
		P30	○	○	○	○
		PE3	○	○	○	○
	ADSM0 (output)	PB2	○	○	○	○
	ADSM1 (output)	PB1	○	○	○	○
General purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71	×	○	○	○
		PD2	×	○	○	○
		PD7	×	×	×	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74	×	○	○	○
		PD1	×	○	○	○
		PD6	×	×	×	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72	×	○	○	○
		PD0	×	○	○	○
		PD5	×	×	×	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75	×	○	○	○
		PB7	×	○	○	○
		PD4	×	×	×	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P73	×	○	○	○
		PB6	×	○	○	○
		PD3	×	×	×	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P76	×	○	○	○
		PB5	×	○	○	○
		PD2	×	×	×	○
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P10	×	×	×	○
		P32	×	×	×	○
		PB6	×	×	×	○
		PD1	×	×	×	○
		PD7	×	○	○	○
		PE5	×	×	×	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P11	×	×	×	○
		P33	×	×	×	○
		PB5	×	×	×	○
		PD0	×	×	×	○
		PD6	×	○	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71				○
		P95				○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74				○
		P92				○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72				○
		P94				○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75				○
		P91				○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73				○
		P93				○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76				○
		P90				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
General purpose PWM timer	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P32				○
		P95				○
		PB2				○
	GTIOC7A (input/output)	PD5				○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P33				○
		P92				○
		PB1				○
	GTIOC7B (input/output)	PD3				○
	GTECLKA (input)	PD5	×	○	○	
	GTECLKB (input)	PD4	×	○	○	
	GTECLKC (input)	PD3	×	○	○	
	GTECLKD (input)	PB4	×	○	○	
	GTETRG (input)	PB4	×	○	○	
	GTETRGA (input)	P01				○
		P11				○
		P70				○
		P96				○
		PB4				○
		PD5				○
		PE3				○
		PE4				○
	GTETRGB (input)	P01				○
		P10				○
		P70				○
		P96				○
		PB4				○
		PD4				○
		PE3				○
		PE4				○
		PE5				○
	GTETRGC (input)	P01				○
		P11				○
		P70				○
		P96				○
		PB4				○
		PD3				○
		PE3				○
		PE4				○
	GTETRGD (input)	P01				○
		P10				○
		P70				○
		P96				○
		PB4				○
		PE3				○
		PE4				○
		PE5				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
General purpose PWM timer	GTADSM0 (output)	P94	×	×	×	○
		PA3	×	○	○	○
		PB2	×	×	×	○
	GTADSM1 (output)	PA2	×	○	○	○
		PB1	×	×	×	○
	GTCPPO0 (output)	P11				○
		P33				○
		P70				○
		PB4				○
	GTCPPO4 (output)	P96				○
		PA1				○
	GTIU (input)	P00				○
		P21				○
		P31				○
		PB3				○
		PD7				○
	GTIV (input)	P10				○
		P22				○
		P30				○
		PB2				○
		PE0				○
	GTIW (input)	P01				○
		P20				○
		PB1				○
		PD6				○
	GTOULO (output)	P74				○
		P92				○
	GTOUUP (output)	P71				○
		P95				○
	GTOVLO (output)	P75				○
		P91				○
	GTOVUP (output)	P72				○
		P94				○
	GTOWLO (output)	P76				○
		P90				○
	GTOWUP (output)	P73				○
		P93				○
8-bit timer	TMO0 (output)	P33	○	○	○	○
		PB0	○	○	○	○
		PD3	○	○	○	○
	TMCI0 (input)	PB1	○	○	○	○
		PD4	○	○	○	○
	TMRI0 (input)	PB2	○	○	○	○
		PD5	○	○	○	○
	TMO1 (output)	PD6	○	○	○	○
	TMCI1 (input)	PD2	○	○	○	○
		PE0	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC) 100-Pin Chip Version A	RX24T (MPC) 100-Pin Chip Version B	RX24U (MPC) 100-Pin	RX26T (MPC) 100-Pin
8-bit timer	TMRI1 (input)	PD7	○	○	○	○
	TMO2 (output)	P20	×	×	×	○
		P23	○	○	○	○
		P27	×	×	×	○
		P92	×	×	×	○
		PA0	○	○	○	○
		PD1	○	○	○	○
	TMCI2 (input)	P24	○	○	○	○
	TMRI2 (input)	P22	○	○	○	○
	TMO3 (output)	P11	○	○	○	○
	TMCI3 (input)	P95	×	×	×	○
		PA5	○	○	○	○
	TMRI3 (input)	P10	○	○	○	○
	TMO4 (output)	P22	○	○	○	○
		P82	○	○	○	○
		P93	×	×	×	○
		PA1	○	○	○	○
		PD2	○	○	○	○
	TMCI4 (input)	P21	○	○	○	○
		P81	○	○	○	○
	TMRI4 (input)	P20	○	○	○	○
		P80	○	○	○	○
	TMO5 (output)	PE1	○	○	○	○
	TMCI5 (input)	PE0	○	○	○	○
	TMRI5 (input)	PD7	○	○	○	○
	TMO6 (output)	P21	×	×	×	○
		P24	○	○	○	○
		P27	×	×	×	○
		P32	○	○	○	○
		PD0	○	○	○	○
	TMCI6 (input)	P30	○	○	○	○
		PD4	○	○	○	○
	TMRI6 (input)	P31	○	○	○	○
		P70	×	×	×	○
		PD5	○	○	○	○
	TMO7 (output)	PA2	○	○	○	○
	TMCI7 (input)	PA4	○	○	○	○
	TMRI7 (input)	P94	×	×	×	○
		PA3	○	○	○	○
CAN module	CTXD0 (output)	PA0	×	○	○	
	CRXD0 (input)	PA1	×	○	○	
Port output enable 3	POE0# (input)	P70	○	○	○	○
	POE4# (input)	P96	○	○	○	○
	POE8# (input)	PB4	○	○	○	○
	POE9# (input)	P11				○
		P27				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Port output enable 3	POE10# (input)	PE2	○	○	○	○
		PE4	○	○	○	○
	POE11# (input)	PE3	○	○	○	○
	POE12# (input)	P01	○	○	○	○
		P10	○	○	○	○
Serial communications interface	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	PD5	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	○	○
	SCK1 (input/output)	PD4	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	○	○	×
		PD6	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	P37	×	×	×	○
		P91	×	×	×	○
		PB6	○	○	○	○
		PE0	×	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	P36	×	×	×	○
		P90	×	×	×	○
		PB5	○	○	○	○
		PD7	×	○	○	○
	SCK5 (input/output)	P70	×	×	×	○
		PB7	○	○	○	○
		PD2	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PB4	○	○	○	○
		PE1	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P80	○	○	○	○
		P95	×	×	×	○
		PA5	○	○	○	○
		PB1	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P81	○	○	○	○
		PB0	○	○	○	○
		PB2	○	○	○	○
	SCK6 (input/output)	P82	○	○	○	○
		PA4	○	○	○	○
		PB3	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10	○	○	○	○
		PA2	○	○	○	○
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PD5			○	
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PD3			○	
	SCK11 (input/output)	PD4			○	

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Serial communications interface	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PD6			○	
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00				○
		P22				○
		P80				○
		PB6				○
		PB4				○
		PD6				○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01				○
		P21				○
		P23				○
		P81				○
		PB5				○
		PB3				○
		PD4				○
	SCK12 (input/output)	P82				○
		PB7				○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE1				○
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	P20				○
		P22				○
		P95				○
		PA5				○
		PD1				○
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	P21				○
		P23				○
		PA4				○
		PB0				○
		PD0				○
		PD7				○
	SCK008 (input/output)	P11				○
		P22				○
		P24				○
		P30				○
		P94				○
		PA3				○
		PD2				○
	TXDB008 (output)	P22				○
		P94				○
		PA3				○
		PD2				○
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	P20				○
		P24				○
		P30				○
		P96				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Serial communications interface	DE008 (output)	P20				○
		P24				○
		P30				○
		P96				○
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	P00				○
		PA2				○
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	P01				○
		P10				○
		P93				○
		P94				○
		PA1				○
		PA3				○
	SCK009 (input/output)	P11				○
		P92				○
		PA0				○
		PD7				○
		PE4				○
		PE5				○
	TXDB009 (output)	P11				○
		P92				○
		PA0				○
		PD7				○
		PE4				○
		PE5				○
	CTS009# (input)/ RTS009# (output)/ SS009# (input)	P70				○
		PB3				○
		PE3				○
		PE5				○
	DE009 (output)	P70				○
		PB3				○
		PE3				○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P93				○
		PA1				○
		PB6				○
		PD5				○
	TXD011 (output)/ TXDA011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P92				○
		PA0				○
		PB5				○
		PD3				○
	SCK011 (input/output)	PB4				○
		PB7				○
		PD4				○
	TXDB011 (output)	PB4				○
		PB7				○
		PD4				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Serial communications interface	CTS011# (input)/ RTS011# (output)/ SS011# (input)	PB0				○
		PB4				○
		PD6				○
	DE011 (output)	PB0				○
		PD6				○
I²C bus interface	SCL0 (input/output)	PB1	○	○	○	○
	SDA0 (input/output)	PB2	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P20	×	×	×	○
		P24	○	○	○	○
		P27	×	×	×	○
		PA4	○	○	○	○
		PB3	○	○	○	○
		PD0	○	○	○	○
	MOSIA (input/output)	P21	×	×	×	○
		P23	○	○	○	○
		PB0	○	○	○	○
		PD2	○	○	○	○
	MISOA (input/output)	P22	○	○	○	○
		P95	×	×	×	○
		PA5	○	○	○	○
		PB4	×	×	×	○
		PD1	○	○	○	○
	SSLA0 (input/output)	P30	○	○	○	○
		P70	×	×	×	○
		P94	×	×	×	○
		PA3	○	○	○	○
		PD6	○	○	○	○
	SSLA1 (output)	P31	○	○	○	○
		PA2	○	○	○	○
		PD7	○	○	○	○
	SSLA2 (output)	P32	○	○	○	○
		P93	×	×	×	○
		PA1	○	○	○	○
		PE0	○	○	○	○
	SSLA3 (output)	P33	○	○	○	○
		P92	×	×	×	○
		PA0	○	○	○	○
		PE1	○	○	○	○
	RSPCK0 (input/output)	P20				○
		P24				○
		P27				○
		P70				○
		P91				○
		P96				○
		PA4				○
		PB5				○
		PD0				○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Serial peripheral interface	MOSI0 (input/output)	P21				○
		P23				○
		P72				○
		P93				○
		PB0				○
		PD2				○
		PD3				○
	MISO0 (input/output)	P22				○
		P71				○
		P92				○
		P95				○
		PA5				○
		PB6				○
		PD1				○
	SSL00 (input/output)	P30				○
		P73				○
		P94				○
		PA3				○
		PD5				○
		PD6				○
	SSL01 (output)	P31				○
		P74				○
		P90				○
		PA2				○
		PB4				○
		PD7				○
	SSL02 (output)	P32				○
		P75				○
		P93				○
		P95				○
		PA1				○
		PD4				○
		PE0				○
	SSL03 (output)	P33				○
		P76				○
		P92				○
		P96				○
		PA0				○
		PB7				○
		PE1				○
12-bit A/D converter	AN000 (input)	P40	○	○	○	○
	AN001 (input)	P41	○	○	○	○
	AN002 (input)	P42	○	○	○	○
	AN003 (input)	P43	○	○	○	○
	AN016 (input)	P20	○	○	○	
	AN100 (input)	P44	○	○	○	○
	AN101 (input)	P45	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
12-bit A/D converter	AN102 (input)	P46	○	○	○	○
	AN103 (input)	P47	○	○	○	○
	AN116 (input)	P21	○	○	○	
	AN200 (input)	P52	×	×	×	○
		P60	○	○	○	×
	AN201 (input)	P53	×	×	×	○
		P61	○	○	○	×
	AN202 (input)	P54	×	×	×	○
		P62	○	○	○	×
	AN203 (input)	P55	×	×	×	○
		P63	○	○	○	×
	AN204 (input)	P50	×	×	×	○
		P64	○	○	○	×
	AN205 (input)	P51	×	×	×	○
		P65	○	○	○	×
	AN206 (input)	P50	○	○	×*1	×
		P60	×	×	×*1	○
	AN207 (input)	P51	○	○	×*1	×
		P61	×	×	×*1	○
	AN208 (input)	P52	○	○	○	×
		P62	×	×	×	○
	AN209 (input)	P53	○	○	○	×
		P63	×	×	×	○
	AN210 (input)	P54	○	○	○	×
		P64	×	×	×	○
	AN211 (input)	P55	○	○	○	×
		P65	×	×	×	○
	AN216 (input)	P20				○
	AN217 (input)	P21				○
	ADTRG0# (input)	P20	○	○	○	○
		P93	×	×	×	○
		PA1	○	○	○	○
		PA4	○	○	○	○
	ADTRG1# (input)	P21	○	○	○	○
		P95	×	×	×	○
		PA5	○	○	○	○
	ADTRG2# (input)	P22	○	○	○	○
		PB0	○	○	○	○
	ADST0 (output)	P02	○	○	○	×
		PD6	○	○	○	○
		PE5	×	×	×	○
		PN7	×	×	×	○
	ADST1 (output)	P00	○	○	○	○
	ADST2 (output)	P01	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
8-bit D/A converter/ 12-bit D/A converter	DA0 (output)	P24	×	○	○	×
		P64	×	×	×	○
	DA1 (output)	P23	×	○	○	×
		P65	×	×	×	○
Clock frequency accuracy measurement circuit	CACREF (input)	P00	×	×	×	○
		P23	○	○	○	○
		PB3	○	○	○	○
Comparator	COMP0 (output)	P00	×	×	×	○
		P24	○	○	○	○
	COMP1 (output)	P01	×	×	×	○
		P23	○	○	○	○
	COMP2 (output)	P22	○	○	○	○
	COMP3 (output)	P30	○	○	○	○
		P80	×	×	×	○
	COMP4 (output)	P20				○
		P81				○
	COMP5 (output)	P21				○
		P82				○
	CMPC00 (input)	P40	○	○	○	○
	CMPC01 (input)	P40	○	○	○	○
	CMPC02 (input)	P45	○	○	○	×
		P52	×	×	×	○
	CMPC03 (input)	P45	○	○	○	×
		P60	×	×	×	○
	CMPC10 (input)	P41	×	×	×	○
		P44	○	○	○	×
	CMPC11 (input)	P41	×	×	×	○
		P44	○	○	○	×
	CMPC12 (input)	P46	○	○	○	×
		P53	×	×	×	○
	CMPC13 (input)	P46	○	○	○	×
		P61	×	×	×	○
	CMPC20 (input)	P42	×	×	×	○
		P45	○	○	○	×
	CMPC21 (input)	P42	×	×	×	○
		P45	○	○	○	×
	CMPC22 (input)	P40	○	○	○	×
		P54	×	×	×	○
	CMPC23 (input)	P40	○	○	○	×
		P63	×	×	×	○
	CMPC30 (input)	P44	×	×	×	○
		P46	○	○	○	×
	CMPC31 (input)	P44	×	×	×	○
		P46	○	○	○	×
	CMPC32 (input)	P44	○	○	○	×
		P55	×	×	×	○

Module/ Function	Pin Function	Port Allocation	RX24T (MPC)		RX24U (MPC)	RX26T (MPC)
			100-Pin			
			Chip Version A	Chip Version B	100-Pin	100-Pin
Comparator	CMPC33 (input)	P44	○	○	○	×
		P64	×	×	×	○
	CMPC40 (input)	P45				○
	CMPC41 (input)	P45				○
	CMPC42 (input)	P50				○
	CMPC43 (input)	P62				○
	CMPC50 (input)	P46				○
	CMPC51 (input)	P46				○
	CMPC52 (input)	P51				○
	CMPC53 (input)	P65				○
	CVREFC0 (input)	P20	○	×		×
		P53	×	×		○
	CVREFC1 (input)	P21	○	×		×
		P54	×	×		○
CAN FD module	CTX0 (output)	P23				○
		P92				○
		PA0				○
		PB3				○
		PB5				○
		PD7				○
	CRX0 (input)	P22				○
		P93				○
		PA1				○
		PB4				○
		PB6				○
		PE0				○
Compare match timer W	TOC0 (output)	PB6				○
	TIC0 (input)	PB5				○
	TOC1 (output)	PB3				○
	TIC1 (input)	PB2				○
	TOC2 (output)	PB1				○
	TIC2 (input)	PB0				○
	TOC3 (output)	P11				○
	TIC3 (input)	P00				○
		P10				○
I^3C bus interface	SCL00 (input/output)	PB1				○
	SDA00 (input/output)	PB2				○

Note: 1. 100-pin packages of the RX24U Group do not have this function.

Table 2.34 Comparison of Multiplexed Pin Assignments (80-Pin/64-Pin)

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Interrupts	IRQ0 (input)	P10	○	×	○	×
		P52	○	○	○	○
		PE2	×	×	○	○
	IRQ1 (input)	P11	○	○	○	○
		P53	○	○	○	○
		P95	×	×	○	○
		PA5	○	×	○	×
		PE4	○	×	○	×
	IRQ2 (input)	P00	○	○	○	○
		P54	○	○	○	○
		PB6	×	×	○	○
		PD4	○	○	○	○
		PE3	○	×	○	×
	IRQ3 (input)	P55	○	×	○	×
		PB4	○	○	○	○
		PD5	○	○	×	×
	IRQ4 (input)	P01	○	○	○	○
		P60	×	×	○	×
		P96	○	○	○	○
		PB1	×	×	○	○
	IRQ5 (input)	P02	○	○	×	×
		P70	○	○	○	○
		PB6	○	○	×	×
		PD6	○	○	○	○
		PN7	×	×	○	○
	IRQ6 (input)	P21	○	○	○	○
		P31	○	○	○	×
		P62	○	×	×	×
		PD5	×	×	○	○
	IRQ7 (input)	P20	○	×	○	○
		P30	○	○	○	×
	NMI (input)	PE2	○	○	○	○
	IRQ8 (input)	P64			○	○
		PB0			○	○
		PD7			○	○
	IRQ9 (input)	P65			○	○
		PB3			○	○
	IRQ10 (input)	P22			○	○
	IRQ14 (input)	P93			○	○
	IRQ15 (input)	P27			○	×
Multi-function timer unit 3	MTIOC0A (input/output)/ MTIOC0A# (input/output)	P31	○	○	○	×
		P70	×	×	○	○
		PB3	○	○	○	○
	MTIOC0B (input/output)/ MTIOC0B# (input/output)	P30	○	○	○	×
		PB2	○	○	○	○
	MTIOC0C (input/output)/ MTIOC0C# (input/output)	P27	×	×	○	×
		PB1	○	○	○	○
	MTIOC0D (input/output)/ MTIOC0D# (input/output)	PB0	○	×	○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Multi-function timer unit 3	MTIOC1A (input/output)/ MTIOC1A# (input/output)	P27	×	×	○	×
		P95	×	×	○	○
		PA5	○	×	○	×
	MTIOC2A (input/output)/ MTIOC2A# (input/output)	P94	×	×	○	○
		PA3	○	×	○	×
	MTIOC3A (input/output)/ MTIOC3A# (input/output)	P11	○	○	○	○
	MTIOC3B (input/output)/ MTIOC3B# (input/output)	P71	○	○	○	○
	MTIOC3D (input/output)/ MTIOC3D# (input/output)	P74	○	○	○	○
	MTIOC4A (input/output)/ MTIOC4A# (input/output)	P72	○	○	○	○
	MTIOC4B (input/output)/ MTIOC4B# (input/output)	P73	○	○	○	○
	MTIOC4C (input/output)/ MTIOC4C# (input/output)	P75	○	○	○	○
	MTIOC4D (input/output)/ MTIOC4D# (input/output)	P76	○	○	○	○
	MTIC5U (input)/ MTIC5U# (input)	P24	○	○	×	×
	MTIC5V (input)/ MTIC5V# (input)	P23	○	○	×	×
	MTIC5W (input)/ MTIC5W# (input)	P22	○	○	○	○
	MTIOC6A (input/output)/ MTIOC6A# (input/output)	P93	×	×	○	○
	MTIOC6B (input/output)/ MTIOC6B# (input/output)	P95	○	○	○	○
	MTIOC6C (input/output)/ MTIOC6C# (input/output)	P92	×	×	○	○
	MTIOC6D (input/output)/ MTIOC6D# (input/output)	P92	○	○	○	○
	MTIOC7A (input/output)/ MTIOC7A# (input/output)	P94	○	○	○	○
	MTIOC7B (input/output)/ MTIOC7B# (input/output)	P93	○	○	○	○
	MTIOC7C (input/output)/ MTIOC7C# (input/output)	P91	○	○	○	○
	MTIOC7D (input/output)/ MTIOC7D# (input/output)	P90	○	○	○	○
	MTIOC9A (input/output)/ MTIOC9A# (input/output)	P00	×	×	○	○
		P21	○	○	○	○
		PD7	○	○	○	○
	MTIOC9B (input/output)/ MTIOC9B# (input/output)	P10	○	×	○	×
	MTIOC9C (input/output)/ MTIOC9C# (input/output)	P01	×	×	○	○
		P20	○	×	○	○
		PD6	○	○	○	○
	MTIOC9D (input/output)/ MTIOC9D# (input/output)	P02	○	○	×	×
		PN7	×	×	○	○
	MTCLKA (input)/ MTCLKA# (input)	P21	○	○	○	○
	MTCLKB (input)/ MTCLKB# (input)	P20	○	×	○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Multi-function timer unit 3	MTCLKC (input)/ MTCLKC# (input)	P11	○	○	○	○
		P31	○	○	○	×
		P70	×	×	○	○
		PE4	○	×	○	×
	MTCLKD (input)/ MTCLKD# (input)	P10	○	×	○	×
		P22	×	×	○	○
		P30	○	○	○	×
		PE3	○	×	○	×
	ADSM0 (output)	PB2	○	○	○	○
	ADSM1 (output)	PB1	○	○	○	○
	MTIOC9B (input/output)	P22			○	○
	MTIOC9D (input/output)	P11			○	○
General purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P71	×	×	○	○
		PD2	×	×	○	×
		PD7	×	×	○	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P74	×	×	○	○
		PD6	×	×	○	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P72	×	×	○	○
		PD5	×	×	○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P75	×	×	○	○
		PD4	×	×	○	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P73	×	×	○	○
		PB6	×	×	○	○
		PD3	×	×	○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P76	×	×	○	○
		PB5	×	×	○	○
		PD2	×	×	○	×
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P10	×	×	○	×
		PB6	×	×	○	○
		PD7	×	×	○	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P11	×	×	○	○
		PB5	×	×	○	○
		PD6	×	×	○	○
	GTADSM0 (output)	P94	×	×	○	○
		PA3	×	×	○	×
		PB2	×	×	○	○
	GTADSM1 (output)	PB1	×	×	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P71			○	○
		P95			○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P74			○	○
		P92			○	○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P72			○	○
		P94			○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P75			○	○
		P91			○	○
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P73			○	○
		P93			○	○
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P76			○	○
		P90			○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
General purpose PWM timer	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P95			○	○
		PB2			○	○
	GTIOC7A (input/output)	PD5			○	○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P92			○	○
		PB1			○	○
	GTIOC7B (input/output)	PD3			○	○
	GTETRGA (input)	P01			○	○
		P11			○	○
		P70			○	○
		P96			○	○
		PB4			○	○
		PD5			○	○
		PE3			○	×
		PE4			○	×
	GTETRGB (input)	P01			○	○
		P10			○	×
		P70			○	○
		P96			○	○
		PB4			○	○
		PD4			○	○
		PE3			○	×
		PE4			○	×
	GTETRGC (input)	P01			○	○
		P11			○	○
		P70			○	○
		P96			○	○
		PB4			○	○
		PD3			○	○
		PE3			○	×
		PE4			○	×
	GTETRGD (input)	P01			○	○
		P10			○	×
		P70			○	○
		P96			○	○
		PB4			○	○
		PE3			○	×
		PE4			○	×
	GTCPPO0 (output)	P11			○	○
		P70			○	○
		PB4			○	○
	GTCPPO4 (output)	P96			○	○
	GTIU (input)	P00			○	○
		P21			○	○
		P31			○	×
		PB3			○	○
		PD7			○	○
	GTIV (input)	P10			○	×
		P22			○	○
		P30			○	×
		PB2			○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
General purpose PWM timer	GTIW (input)	P01			○	○
		P20			○	○
		PB1			○	○
		PD6			○	○
	GTOULO (output)	P74			○	○
		P92			○	○
	GTOUUP (output)	P71			○	○
		P95			○	○
	GTOVLO (output)	P75			○	○
		P91			○	○
	GTOVUP (output)	P72			○	○
		P94			○	○
	GTOWLO (output)	P76			○	○
		P90			○	○
	GTOWUP (output)	P73			○	○
		P93			○	○
8-bit timer	TMO0 (output)	PB0	○	×	○	○
		PD3	○	○	○	○
	TMCI0 (input)	PB1	○	○	○	○
		PD4	○	○	○	○
	TMRI0 (input)	PB2	○	○	○	○
		PD5	○	○	○	○
	TMO1 (output)	PD6	○	○	○	○
	TMCI1 (input)	PD2	○	×	○	×
	TMRI1 (input)	PD7	○	○	○	○
	TMO2 (output)	P23	○	○	×	×
		P20	×	×	○	○
		P27	×	×	○	×
		P92	×	×	○	○
	TMCI2 (input)	P24	○	○	×	×
	TMRI2 (input)	P22	○	○	○	○
	TMO3 (output)	P11	○	○	○	○
	TMCI3 (input)	P95	×	×	○	○
		PA5	○	×	○	×
	TMRI3 (input)	P10	○	×	○	×
	TMO4 (output)	P22	○	○	○	○
		P93	×	×	○	○
		PD2	○	×	○	×
	TMCI4 (input)	P21	○	○	○	○
	TMRI4 (input)	P20	○	×	○	○
	TMRI5 (input)	PD7	○	○	○	○
	TMO6 (output)	P21	×	×	○	○
		P24	○	○	×	×
		P27	×	×	○	×
	TMCI6 (input)	P30	○	○	○	×
		PD4	○	○	○	○
	TMRI6 (input)	P31	○	○	○	×
		P70	×	×	○	○
		PD5	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
8-bit timer	TMRI7 (input)	P94	×	×	○	○
		PA3	○	×	○	×
Port output enable 3	POE0# (input)	P70	○	○	○	○
	POE4# (input)	P96	○	○	○	○
	POE8# (input)	PB4	○	○	○	○
	POE10# (input)	PE2	○	○	○	○
		PE4	○	×	○	×
	POE11# (input)	PE3	○	×	○	×
	POE12# (input)	P01	○	○	○	○
		P10	○	×	○	×
	POE9# (input)	P11			○	○
		P27			○	×
Serial communications interface	RXD1 (input)/ SMISO1(input/output)/ SSCL1 (input/output)	PD5	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	PD3	○	○	○	○
	SCK1 (input/output)	PD4	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P02	○	○	×	×
		PD6	○	○	○	○
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	P37	×	×	○	○
		P91	×	×	○	○
		PB6	○	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	P36	×	×	○	○
		P90	×	×	○	○
		PB5	○	○	○	○
		PD7	×	×	○	○
	SCK5 (input/output)	P70	×	×	○	○
		PD2	○	×	○	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PB4	○	○	○	○
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P95	×	×	○	○
		PA5	○	×	○	×
		PB1	○	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	PB0	○	×	○	○
		PB2	○	○	○	○
	SCK6 (input/output)	PB3	○	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P10	○	×	○	×
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	P00			○	○
		P22			○	○
		PB4			○	○
		PB6			○	○
		PD6			○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Serial communications interface	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	P01			○	○
		P21			○	○
		PB3			○	○
		PB5			○	○
		PD4			○	○
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	P20			○	○
		P22			○	○
		P95			○	○
		PA5			○	×
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	P21			○	○
		PB0			○	○
		PD7			○	○
	SCK008 (input/output)	P11			○	○
		P22			○	○
		P30			○	×
		P94			○	○
		PA3			○	×
		PD2			○	×
	TXDB008 (output)	P22			○	○
		P94			○	○
		PA3			○	×
		PD2			○	×
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	P20			○	○
		P30			○	×
		P96			○	○
	DE008 (output)	P20			○	○
		P30			○	×
		P96			○	○
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	P00			○	○
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	P01			○	○
		P10			○	×
		P93			○	○
		P94			○	○
		PA3			○	×
	SCK009 (input/output)	P11			○	○
		P92			○	○
		PD7			○	○
		PE4			○	×
	TXDB009 (output)	P11			○	○
		P92			○	○
		PD7			○	○
		PE4			○	×
	CTS009# (input)/ RTS009# (output)/ SS009# (input)	P70			○	○
		PB3			○	○
		PE3			○	×
	DE009 (output)	P70			○	○
		PB3			○	○
		PE3			○	×

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Serial communications interface	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P93			○	○
		PB6			○	○
		PD5			○	○
	TXD011 (output)/ TXDA011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P92			○	○
		PB5			○	○
		PD3			○	○
	SCK011 (input/output)	PB4			○	○
		PD4			○	○
	TXDB011 (output)	PB4			○	○
		PD4			○	○
	CTS011# (input)/ RTS011# (output)/ SS011# (input)	PB0			○	○
		PB4			○	○
		PD6			○	○
	DE011 (output)	PB0			○	○
		PD6			○	○
I^2C bus interface	SCL0 (input/output)	PB1	○	○	○	○
	SDA0 (input/output)	PB2	○	○	○	○
Serial peripheral interface	RSPCKA (input/output)	P20	×	×	○	○
		P24	○	○	×	×
		P27	×	×	○	×
		PB3	○	○	○	○
	MOSIA (input/output)	P21	×	×	○	○
		P23	○	○	×	×
		PB0	○	×	○	○
		PD2	○	×	○	×
	MISOA (input/output)	P22	○	○	○	○
		P95	×	×	○	○
		PA5	○	×	○	×
		PB4	×	×	○	○
	SSLA0 (input/output)	P30	○	○	○	×
		P70	×	×	○	○
		P94	×	×	○	○
		PA3	○	×	○	×
		PD6	○	○	○	○
	SSLA1 (output)	P31	○	○	○	×
		PD7	○	○	○	○
	SSLA2 (output)	P93	×	×	○	○
	SSLA3 (output)	P92	×	×	○	○
	RSPCK0 (input/output)	P20			○	○
		P27			○	×
		P70			○	○
		P91			○	○
		P96			○	○
		PB5			○	○

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Serial peripheral interface	MOSI0 (input/output)	P21			○	○
		P72			○	○
		P93			○	○
		PB0			○	○
		PD2			○	×
		PD3			○	○
	MISO0 (input/output)	P22			○	○
		P71			○	○
		P92			○	○
		P95			○	○
		PA5			○	×
		PB6			○	○
	SSL00 (input/output)	P30			○	×
		P73			○	○
		P94			○	○
		PA3			○	×
		PD5			○	○
		PD6			○	○
	SSL01 (output)	P31			○	×
		P74			○	○
		P90			○	○
		PB4			○	○
		PD7			○	○
	SSL02 (output)	P75			○	○
		P93			○	○
		P95			○	○
		PD4			○	○
	SSL03 (output)	P76			○	○
		P92			○	○
		P96			○	○
12-bit A/D converter	AN000 (input)	P40	○	○	○	○
	AN001 (input)	P41	○	○	○	○
	AN002 (input)	P42	○	○	○	○
	AN003 (input)	P43	○	×	○	○
	AN016 (input)	P20	○	×		
	AN100 (input)	P44	○	○	○	○
	AN101 (input)	P45	○	○	○	○
	AN102 (input)	P46	○	○	○	○
	AN103 (input)	P47	○	×	○	○
	AN116 (input)	P21	○	○		
	AN200 (input)	P52	×	×	○	○
	AN201 (input)	P53	×	×	○	○
	AN202 (input)	P54	×	×	○	○
		P62	○	×	×	×
	AN203 (input)	P55	×	×	○	×
	AN204 (input)	P50	×	×	○	×
	AN205 (input)	P51	×	×	○	×
	AN206 (input)	P50	○	○	×	×
		P60	×	×	○	×
	AN207 (input)	P51	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
12-bit A/D converter	AN208 (input)	P52	○	○	×	×
	AN209 (input)	P53	○	○	×	×
	AN210 (input)	P54	○	○	×	×
		P64	×	×	○	○
	AN211 (input)	P55	○	×	×	×
		P65	×	×	○	○
	ADTRG0# (input)	P20	○	×	○	○
		P93	×	×	○	○
	ADTRG1# (input)	P21	○	○	○	○
		P95	×	×	○	○
		PA5	○	×	○	×
	ADTRG2# (input)	P22	○	○	○	○
		PB0	○	×	○	○
	ADST0 (output)	P02	○	○	×	×
		PD6	○	○	○	○
		PN7	×	×	○	○
	ADST1 (output)	P00	○	○	○	○
	ADST2 (output)	P01	○	○	○	○
	AN216 (input)	P20			○	○
	AN217 (input)	P21			○	○
	DA0 (output)	P64			○	○
	DA1 (output)	P65			○	○
Clock frequency accuracy measurement circuit	CACREF (input)	P00	×	×	○	○
		P23	○	○	×	×
		PB3	○	○	○	○
Comparator	COMP0 (output)	P00	×	×	○	○
		P24	○	○	×	×
	COMP1 (output)	P01	×	×	○	○
		P23	○	○	×	×
	COMP2 (output)	P22	○	○	○	○
	COMP3 (output)	P30	○	○	○	×
	CVREFC0 (input)	P20	○	×	×	×
		P53	×	×	○	○
	CVREFC1 (input)	P21	○	○	×	×
		P54	×	×	○	○
	CMPC00 (input)	P40	○	○	○	○
	CMPC01 (input)	P40	○	○	○	○
	CMPC02 (input)	P45	○	○	×	×
		P52	×	×	○	○
	CMPC03 (input)	P45	○	○	×	×
		P60	×	×	○	×
	CMPC10 (input)	P41	×	×	○	○
		P44	○	○	×	×
	CMPC11 (input)	P41	×	×	○	○
		P44	○	○	×	×
	CMPC12 (input)	P46	○	○	×	×
		P53	×	×	○	○
	CMPC13 (input)	P46	○	○	×	×

Module/ Function	Pin Function	Port Allocation	RX24T(MPC)		RX26T(MPC)	
			80-Pin	64-Pin	80-Pin	64-Pin
Comparator	CMPC20 (input)	P42	×	×	○	○
		P45	○	○	×	×
	CMPC21 (input)	P42	×	×	○	○
		P45	○	○	×	×
	CMPC22 (input)	P40	○	○	×	×
		P54	×	×	○	○
	CMPC23 (input)	P40	○	○	×	×
	CMPC30 (input)	P44	×	×	○	○
		P46	○	○	×	×
	CMPC31 (input)	P44	×	×	○	○
		P46	○	○	×	×
	CMPC32 (input)	P44	○	○	×	×
		P55	×	×	○	×
	CMPC33 (input)	P44	○	○	×	×
		P64	×	×	○	○
	COMP4 (output)	P20			○	○
	COMP5 (output)	P21			○	○
	CMPC40 (input)	P45			○	○
	CMPC41 (input)	P45			○	○
	CMPC42 (input)	P50			○	×
	CMPC50 (input)	P46			○	○
	CMPC51 (input)	P46			○	○
	CMPC52 (input)	P51			○	×
	CMPC53 (input)	P65			○	○
Compare match timer W	TOC0 (output)	PB6			○	○
	TIC0 (input)	PB5			○	○
	TOC1 (output)	PB3			○	○
	TIC1 (input)	PB2			○	○
	TOC2 (output)	PB1			○	○
	TIC2 (input)	PB0			○	○
	TOC3 (output)	P11			○	○
	TIC3 (input)	P00			○	○
		P10			○	×
I^3C bus interface	SCL00 (input/output)	PB1			○	○
	SDA00 (input/output)	PB2			○	○
CAN FD module	CRX0 (input)	P22			○	○
		P93			○	○
		PB4			○	○
		PB6			○	○
	CTX0 (output)	P92			○	○
		PB3			○	○
		PB5			○	○
		PD7			○	○

Table 2.35 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX24T (n = 0 to 2)	RX24U (n = 0 to 2)	RX26T(n = 0, 1)
P00PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADST1	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADST1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000111b: CACREF 001001b: ADST1 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011000b: GTIU 011101b: TIC3 011110b: COMP0 101100b: RXD009/ SMISO009/ SSCL009
P01PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE12# 01001b: ADST2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000111b: POE12# 001001b: ADST2 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTIW 011110b: COMP1 101100b: XD009/TXDA009/ SMOSI009/ SSDA009
P02PFS	—	P02 pin function control register	P02 pin function control register	—

Table 2.36 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX24T (n = 0, 1)	RX24U (n = 0 to 7)	RX26T(n = 0, 1)
P10PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B#*1 00100b: MTCLKD#*1 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00010b: MTCLKD 00011b: MTIOC9B# 00100b: MTCLKD# 00101b: TMRI3 00111b: POE12# 01010b: CTS6#/RTS6#/SS6#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000010b: MTCLKD 000011b: MTIOC9B# 000100b: MTCLKD# 000101b: TMRI3 000111b: POE12# 001010b: CTS6#/RTS6#/ SS6# 010100b: GTIOC3A 010101b: GTETRGB 010110b: GTIOC3A# 010111b: GTETRGD 011000b: GTIV 011101b: TIC3 101100b: TXD009/TXDA009/ SMOSI009/ SSDA009
P11PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A#*1 00100b: MTCLKC#*1 00101b: TMO3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKC 00011b: MTIOC3A# 00100b: MTCLKC# 00101b: TMO3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKC 000011b: MTIOC3A# 000100b: MTCLKC# 000101b: TMO3 000111b: POE9# 001000b: MTIOC9D 010100b: GTIOC3B 010101b: GTETRGA 010110b: GTIOC3B# 010111b: GTETRGC 011000b: GTCPPO0 011101b: TOC3 101100b: SCK009 101101b: SCK008 101110b: TXDB009
P12PFS	—	—	P12 pin function control register	—
P13PFS	—	—	P13 pin function control register	—
P14PFS	—	—	P14 pin function control register	—
P15PFS	—	—	P15 pin function control register	—
P16PFS	—	—	P16 pin function control register	—
P17PFS	—	—	P17 pin function control register	—

Note: 1. Only on chip version B in the RX24T Group

Table 2.37 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P20PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00010b: MTCLKB 00011b: MTIOC9C#*1 00100b: MTCLKB#*1 00101b: TMRI4 01001b: ADTRG0#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00010b: MTCLKB 00011b: MTIOC9C# 00100b: MTCLKB# 00101b: TMRI4 01001b: ADTRG0#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000010b: MTCLKB 000011b: MTIOC9C# 000100b: MTCLKB# 000101b: TMRI4 000110b: TMO2 001001b: ADTRG0# 001101b: RSPCKA 001110b: RSPCK0 011000b: GTIW 011110b: COMP4 101100b: CTS008#/ RTS008#/SS008# 101101b: RXD008/ SMISO008/ SSCL008 101110b: DE008
P21PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00010b: MTCLKA 00011b: MTIOC9A#*1 00100b: MTCLKA#*1 00101b: TMCI4 01001b: ADTRG1#	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00010b: MTCLKA 00011b: MTIOC9A# 00100b: MTCLKA# 00101b: TMCI4 01001b: ADTRG1#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000010b: MTCLKA 000011b: MTIOC9A# 000100b: MTCLKA# 000101b: TMCI4 000110b: TMO6 001001b: ADTRG1# 001100b: TXD12/SMISO12/ SSDA12/TXDX12/ SIOX12 001101b: MOSIA 001110b: MOSI0 011000b: GTIU 011110b: COMP5 101100b: TXD008/TXDA008/ SMOSI008/ SSDA008

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P22PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W#*1 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 11110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI2 00110b: TMO4 01001b: ADTRG2# 01101b: MISOA 10110b: COMP2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTCLKD 000011b: MTIC5W# 000100b: MTCLKD# 000101b: TMRI2 000110b: TMO4 001000b: MTIOC9B 001001b: ADTRG2# 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: MISOA 001110b: MISO0 010000b: CRX0 011000b: GTIV 011110b: COMP2 101100b: RXD008/ SMISO008/ SSCL008 101101b: SCK008 101110b: TXDB008
P23PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V#*1 00101b: TMO2 00111b: CACREF 01101b: MOSIA 11110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMO2 00111b: CACREF 01101b: MOSIA 10110b: COMP1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMO2 000111b: CACREF 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001101b: MOSIA 001110b: MOSI0 010000b: CTX0 011110b: COMP1 101100b: TXD008/TXDA008/ SMOSI008/ SSDA008

Register	Bit	RX24T (n = 0 to 4)	RX24U (n = 0 to 7)	RX26T (n = 0 to 4, 7)
P24PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U#*1 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 11110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMCI2 00110b: TMO6 01101b: RSPCKA 10110b: COMP0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000011b: MTIC5U# 000101b: TMCI2 000110b: TMO6 001101b: RSPCKA 001110b: RSPCK0 011110b: COMP0 101100b: CTS008#/ RTS008#/SS008# 101101b: SCK008 101110b: DE008
P25PFS	—	—	P25 pin function control register	—
P26PFS	—	—	P26 pin function control register	—
P27PFS	—	—	P27 pin function control register	P27 pin function control register
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (100/80-pin) P21: IRQ6 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (144/100-pin) P21: IRQ6 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ7 (48/64/80/100-pin) P21: IRQ6 (48/64/80/100-pin) P22: IRQ10 (64/80/100-pin) P23: IRQ11 (100-pin) P24: IRQ4 (100-pin) P27: IRQ15 (80/100-pin)
	ASEL	Analog pin function select bit 0: Used as other than as analog pin 1: Used as analog pin [In case of chip version A] P20: AN016, CVREFC0 (100/80-pin) P21: AN116, CVREFC1 (100/80/64-pin) [In case of chip version B] P20: AN016, CVREFC0 (100-pin) P21: AN116, CVREFC1 (100-pin) P23: DA1 (100-pin) P24: DA0 (100-pin)	Analog pin function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN016 (144/100-pin) P21: AN116 (144/100-pin) P23: DA1 (144/100-pin) P24: DA0 (144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P20: AN216 (48/64/80/100-pin) P21: AN217 (48/64/80/100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.38 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX24T (n = 0 to 3)	RX24U (n = 0 to 5)	RX26T (n = 0 to 3, 6, 7)
P30PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B#*1 00100b: MTCLKD#*1 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKD 00011b: MTIOC0B# 00100b: MTCLKD# 00101b: TMCI6 01101b: SSLA0 11110b: COMP3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKD 000011b: MTIOC0B# 000100b: MTCLKD# 000101b: TMCI6 001101b: SSLA0 001110b: SSL00 011000b: GTIV 011110b: COMP3 101100b: SCK008 101101b: CTS008#/ RTS008#/SS008# 101110b: DE008
P31PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A#*1 00100b: MTCLKC#*1 00101b: TMRI6 01101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTCLKC 00011b: MTIOC0A# 00100b: MTCLKC# 00101b: TMRI6 01101b: SSLA1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 001101b: SSLA1 001110b: SSL01 011000b: GTIU
P32PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C#*1 00100b: MTCLKB#*1 00101b: TMO6 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKB 00011b: MTIOC3C# 00100b: MTCLKB# 00101b: TMO6 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKB 000011b: MTIOC3C# 000100b: MTCLKB# 000101b: TMO6 001101b: SSLA2 001110b: SSL02 010100b: GTIOC3A 010101b: GTIOC7A 010110b: GTIOC3A# 010111b: GTIOC7A#

Register	Bit	RX24T (n = 0 to 3)	RX24U (n = 0 to 5)	RX26T (n = 0 to 3, 6, 7)
P33PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A#*1 00100b: MTCLKA#*1 00101b: TMO0 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: MTIOC3A# 00100b: MTCLKA# 00101b: TMO0 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: MTIOC3A# 000100b: MTCLKA# 000101b: TMO0 001101b: SSLA3 001110b: SSL03 010100b: GTIOC3B 010101b: GTIOC7B 010110b: GTIOC3B# 010111b: GTIOC7B# 011000b: GTCPPO0
P34PFS	—	—	P34 pin function control register	—
P35PFS	—	—	P35 pin function control register	—
P36PFS	—	—	—	P36 pin function control register
P37PFS	—	—	—	P37 pin function control register
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (100/80/64-pin) P31: IRQ6 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (144/100-pin) P31: IRQ6 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ7 (80/100-pin) P31: IRQ6 (80/100-pin) P32: IRQ12 (100-pin) P33: IRQ13 (100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.39 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
P4nPFS	ASEL	Analog pin function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (100/80/64-pin) P41: AN001 (100/80/64-pin) P42: AN002 (100/80/64-pin) P43: AN003 (100/80-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (100/80/64-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (100/80/64-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (100/80/64-pin) P47: AN103 (100/80-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01, CMPC22, CMPC23 (144/100-pin) P41: AN001 (144/100-pin) P42: AN002 (144/100-pin) P43: AN003 (144/100-pin) P44: AN100, CMPC10, CMPC11, CMPC32, CMPC33 (144/100-pin) P45: AN101, CMPC02, CMPC03, CMPC20, CMPC21 (144/100-pin) P46: AN102, CMPC12, CMPC13, CMPC30, CMPC31 (144/100-pin) P47: AN103 (144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000, CMPC00, CMPC01 (48/64/80/100-pin) P41: AN001, CMPC10, CMPC11 (48/64/80/100-pin) P42: AN002, CMPC20, CMPC21 (48/64/80/100-pin) P43: AN003 (48/64/80/100-pin) P44: AN100, CMPC30, CMPC31 (48/64/80/100-pin) P45: AN101, CMPC40, CMPC41 (64/80/100-pin) P46: AN102, CMPC50, CMPC51 (64/80/100-pin) P47: AN103 (64/80/100-pin)

Table 2.40 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 5)	RX26T (n = 0 to 5)
P5nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN206 (100/80/64-pin) P51: AN207 (100/80/64-pin) P52: AN208 (100/80/64-pin) P53: AN209 (100/80/64-pin) P54: AN210 (100/80/64-pin) P55: AN211 (100/80-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN206 (144-pin) P51: AN207 (144-pin) P52: AN208 (144/100-pin) P53: AN209 (144/100-pin) P54: AN210 (144/100-pin) P55: AN211 (144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P50: AN204, CMPC42 (80/100-pin) P51: AN205, CMPC52 (80/100-pin) P52: AN200, CMPC02 (48/64/80/100-pin) P53: AN201, CMPC12 (48/64/80/100-pin) P54: AN202, CMPC22 (64/80/100-pin) P55: AN203, CMPC32 (80/100-pin)

Table 2.41 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 5)	RX26T (n = 0 to 5)
P6nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (100-pin) P61: IRQ5 (100-pin) P62: IRQ6 (100/80-pin) P63: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (144/100-pin) P61: IRQ5 (144/100-pin) P62: IRQ6 (144/100-pin) P63: IRQ7 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ4 (80/100-pin) P61: IRQ5 (100-pin) P62: IRQ6 (48/100-pin) P63: IRQ7 (100-pin) P64: IRQ8 (64/80/100-pin) P65: IRQ9 (64/80/100-pin)
	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN200 (144/100-pin) P61: AN201 (144/100-pin) P62: AN202 (144/100-pin) P63: AN203 (144/100-pin) P64: AN204 (144/100-pin) P65: AN205 (144/100-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN200 (100-pin) P61: AN201 (100-pin) P62: AN202 (100/80-pin) P63: AN203 (100-pin) P64: AN204 (100-pin) P65: AN205 (100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P60: AN206, CMPC03 (80/100-pin) P61: AN207, CMPC13 (100-pin) P62: AN208, CMPC43 (48/100-pin) P63: AN209, CMPC23 (100-pin) P64: AN210, CMPC33, DA0 (64/80/100-pin) P65: AN211, CMPC53, DA1 (64/80/100-pin)

Table 2.42 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX26T (n = 0 to 6)
P70PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0#	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE0# 01010b: CTS9#/RTS9#/SS9#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTCLKC 000011b: MTIOC0A# 000100b: MTCLKC# 000101b: TMRI6 000111b: POE0# 001010b: SCK5 001101b: SSLA0 001110b: RSPCK0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS009#/ RTS009#/SS009# 101110b: DE009
P71PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B#*1 10100b: GTIOC0A*1 10110b: GTIOC0A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00011b: MTIOC3B# 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000011b: MTIOC3B# 001110b: MISO0 010100b: GTIOC0A 010101b: GTIOC4A 010110b: GTIOC0A# 010111b: GTIOC4A# 011000b: GTOUUP
P72PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A#*1 10100b: GTIOC1A*1 10110b: GTIOC1A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4A 00011b: MTIOC4A# 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000011b: MTIOC4A# 001110b: MOSI0 010100b: GTIOC1A 010101b: GTIOC5A 010110b: GTIOC1A# 010111b: GTIOC5A# 011000b: GTOVUP

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX26T (n = 0 to 6)
P73PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B#*1 10100b: GTIOC2A*1 10110b: GTIOC2A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00011b: MTIOC4B# 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000011b: MTIOC4B# 001110b: SSL00 010100b: GTIOC2A 010101b: GTIOC6A 010110b: GTIOC2A# 010111b: GTIOC6A# 011000b: GTOWUP
P74PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D#*1 10100b: GTIOC0B*1 10110b: GTIOC0B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00011b: MTIOC3D# 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000011b: MTIOC3D# 001110b: SSL01 010100b: GTIOC0B 010101b: GTIOC4B 010110b: GTIOC0B# 010111b: GTIOC4B# 011000b: GTOULO
P75PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C#*1 10100b: GTIOC1B*1 10110b: GTIOC1B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4C 00011b: MTIOC4C# 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000011b: MTIOC4C# 001110b: SSL02 010100b: GTIOC1B 010101b: GTIOC5B 010110b: GTIOC1B# 010111b: GTIOC5B# 011000b: GTOVLO
P76PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D#*1 10100b: GTIOC2B*1 10110b: GTIOC2B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00011b: MTIOC4D# 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000011b: MTIOC4D# 001110b: SSL03 010100b: GTIOC2B 010101b: GTIOC6B 010110b: GTIOC2B# 010111b: GTIOC6B# 011000b: GTOWLO

Note: 1. Only on chip version B in the RX24T Group

Table 2.43 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX24T (n = 0 to 2)	RX24U (n = 0 to 2)	RX26T (n = 0 to 2)
P80PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W#*1 00101b: TMRI4 01010b: RXD6/SMISO6/ SSCL6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5W 00011b: MTIC5W# 00101b: TMRI4 01010b: RXD6/SMISO6/ SSCL6	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000011b: MTIC5W# 000101b: TMRI4 001010b: RXD6/SMISO6/ SSCL6 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011110b: COMP3
P81PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V#*1 00101b: TMCI4 01010b: TXD6/SMOSI6/ SSDA6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5V 00011b: MTIC5V# 00101b: TMCI4 01010b: TXD6/SMOSI6/ SSDA6	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000011b: MTIC5V# 000101b: TMCI4 001010b: TXD6/SMOSI6/ SSDA6 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 011110b: COMP4
P82PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U#*1 00101b: TMO4 01010b: SCK6	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIC5U 00011b: MTIC5U# 00101b: TMO4 01010b: SCK6	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000011b: MTIC5W# 000101b: TMRI4 001010b: SCK6 001100b: SCK12 011110b: COMP5
P83PFS	—	—	P83 pin function control register	—
P84PFS	—	—	P84 pin function control register	—
P8nPFS	ISEL	—	—	Interrupt input function select bit

Note: 1. Only on chip version B in the RX24T Group

Table 2.44 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX26T (n = 0 to 6)
P90PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7D 00011b: MTIOC7D#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7D 00011b: MTIOC7D#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7D 000011b: MTIOC7D# 001010b: TXD5/SMOSI5/ SSDA5 001110b: SSL01 010100b: GTIOC6B 010110b: GTIOC6B# 011000b: GTOWLO
P91PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7C 00011b: MTIOC7C#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7C 000011b: MTIOC7C# 001010b: RXD5/SMISO5/ SSCL5 001110b: RSPCK0 010100b: GTIOC5B 010110b: GTIOC5B# 011000b: GTOVLO
P92PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6D 00011b: MTIOC6D#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6D 000010b: MTIOC6C 000011b: MTIOC6D# 000100b: MTIOC6C# 000101b: TMO2 001101b: SSLA3 001110b: MISO0 010000b: CTX0 010100b: GTIOC4B 010101b: GTIOC7B 010110b: GTIOC4B# 010111b: GTIOC7B# 011000b: GTOULO 101100b: SCK009 101101b: TXD011/TXDA011/ SMOSI011/ SSDA011 101110b: TXDB009 110011b: SSL03

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX26T (n = 0 to 6)
P93PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7B 00011b: MTIOC7B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7B 000010b: MTIOC6A 000011b: MTIOC7B# 000100b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001101b: SSLA2 001110b: MOSI0 010000b: CRX0 010100b: GTIOC6A 010110b: GTIOC6A# 011000b: GTOWUP 101100b: TXD009/TXDA009/ SMOSI009/ SSDA009 101101b: RXD011/ SMISO011/ SSCL011 110011b: SSL02
P94PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC7A 00011b: MTIOC7A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC7A 000010b: MTIOC2A 000011b: MTIOC7A# 000100b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTIOC5A 010101b: GTADSM0 010110b: GTIOC5A# 011000b: GTOVUP 101100b: TXD009/TXDA009/ SMOSI009/ SSDA009 101101b: SCK008 101110b: TXDB008 110011b: SSL00

Register	Bit	RX24T (n = 0 to 6)	RX24U (n = 0 to 6)	RX26T (n = 0 to 6)
P95PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6B 00011b: MTIOC6B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6B 00011b: MTIOC6B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6B 000010b: MTIOC1A 000011b: MTIOC6B# 000100b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/ SSCL6 001101b: MISOA 001110b: SSL02 010100b: GTIOC4A 010101b: GTIOC7A 010110b: GTIOC4A# 010111b: GTIOC7A# 011000b: GTOUUP 101101b: RXD008/ SMISO008/ SSCL008 110011b: MISO0
P96PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 000000b: Hi-Z 000111b: POE4#	Pin function select bits b4 b0 000000b: Hi-Z 000111b: POE4#	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE4# 001110b: SSL03 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO4 101100b: CTS008#/ RTS008#/SS008# 101110b: DE008 110011b: RSPCK0
P9nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P96: IRQ4 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P93: IRQ14 (48/64/80/100-pin) P95: IRQ1 (48/64/80/100-pin) P96: IRQ4 (64/80/100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.45 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 7)	RX26T (n = 0 to 5)
PA0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6C 00010b: MTIOC6C#*1 00101b: TMO2 01101b: SSLA3 10000b: CTXD0*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6C 00010b: MTIOC6C# 00101b: TMO2 01101b: SSLA3 10000b: CTXD0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6C 000011b: MTIOC6C# 000101b: TMO2 001101b: SSLA3 001110b: SSL03 010000b: CTX0 101100b: SCK009 101101b: TXD011/TXDA011/ SMOSI011/ SSDA011 101110b: TXDB009
PA1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6A 00010b: MTIOC6A#*1 00101b: TMO4 01001b: ADTRG0# 01101b: SSLA2 10000b: CRXD0*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC6A 00010b: MTIOC6A# 00101b: TMO4 01001b: ADTRG0# 01101b: SSLA2 10000b: CRXD0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC6A 000011b: MTIOC6A# 000101b: TMO4 001001b: ADTRG0# 001101b: SSLA2 001110b: SSL02 010000b: CRX0 011000b: GTCPPO4 101100b: TXD009/TXDA009/ SMOSI009/ SSDA009 101101b: RXD011/ SMISO011/ SSCL011
PA2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTIOC2B#*1 00101b: TMO7 01010b: CTS6#/RTS6#/SS6# 01101b: SSLA1 10100b: GTADSM1*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00011b: MTIOC2B# 00101b: TMO7 01010b: CTS6#/RTS6#/SS6# 01101b: SSLA1 10100b: GTADSM1	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000011b: MTIOC2B# 000101b: TMO7 001010b: CTS6#/RTS6#/ SS6# 001101b: SSLA1 001110b: SSL01 010100b: GTADSM1 101101b: RXD009/ SMISO009/ SSCL009

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 7)	RX26T (n = 0 to 5)
PA3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC2A#*1 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00011b: MTIOC2A# 00101b: TMRI7 01101b: SSLA0 10100b: GTADSM0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000011b: MTIOC2A# 000101b: TMRI7 001101b: SSLA0 001110b: SSL00 010100b: GTADSM0 101100b: TXD009/TXDA009/ SMOSI009/ SSDA009 101101b: SCK008 101110b: TXDB008
PA4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00010b: MTIOC1B#*1 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC1B# 00101b: TMCI7 01001b: ADTRG0# 01010b: SCK6 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000011b: MTIOC1B# 000101b: TMCI7 001001b: ADTRG0# 001010b: SCK6 001101b: RSPCKA 001110b: RSPCK0 101101b: TXD008/TXDA008/ SMOSI008/ SSDA008
PA5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00010b: MTIOC1A#*1 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/SMISO6/ SSCL6 01101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC1A# 00101b: TMCI3 01001b: ADTRG1# 01010b: RXD6/SMISO6/ SSCL6 01101b: MISOA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000011b: MTIOC1A# 000101b: TMCI3 001001b: ADTRG1# 001010b: RXD6/SMISO6/ SSCL6 001101b: MISOA 001110b: MISO0 101101b: RXD008/ SMISO008/ SSCL008
PA6PFS	—	—	PA6 pin function control register	—
PA7PFS	—	—	PA7 pin function control register	—
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA5: IRQ1 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ14 (100-pin) PA5: IRQ1 (80/100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.46 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PB0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D#*1 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00011b: MTIOC0D# 00101b: TMO0 01001b: ADTRG2# 01010b: TXD6/SMOSI6/ SSDA6 01101b: MOSIA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000011b: MTIOC0D# 000101b: TMO0 001001b: ADTRG2# 001010b: TXD6/SMOSI6/ SSDA6 001101b: MOSIA 001110b: MOSI0 011101b: TIC2 101100b: TXD008/TXDA008/ SMOSI008/ SSDA008 101101b: CTS011#/ RTS011#/SS011# 101110b: DE011
PB1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C#*1 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00011b: MTIOC0C# 00101b: TMCI0 01001b: ADSM1 01010b: RXD6/SMISO6/ SSCL6 01111b: SCL0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000011b: MTIOC0C# 000101b: TMCI0 001001b: ADSM1 001010b: RXD6/SMISO6/ SSCL6 001111b: SCL0 010100b: GTADSM1 010101b: GTIOC7B 010111b: GTIOC7B# 011000b: GTIW 011101b: TOC2 110010b: SCL00
PB2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B#*1 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00011b: MTIOC0B# 00101b: TMRI0 01001b: ADSM0 01010b: TXD6/SMOSI6/ SSDA6 01111b: SDA0	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000011b: MTIOC0B# 000101b: TMRI0 001001b: ADSM0 001010b: TXD6/SMOSI6/ SSDA6 001111b: SDA0 010100b: GTADSM0 010101b: GTIOC7A 010111b: GTIOC7A# 011000b: GTIV 011101b: TIC1 110010b: SDA00

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PB3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A#*1 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC0A 00011b: MTIOC0A# 00111b: CACREF 01010b: SCK6 01101b: RSPCKA	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000011b: MTIOC0A# 000111b: CACREF 001010b: SCK6 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001101b: RSPCKA 010000b: CTX0 011000b: GTIU 011101b: TOC1 101100b: CTS009#/ RTS009#/SS009# 101110b: DE009
PB4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/RTS5#/SS5# 10100b: GTETRG*1 10101b: GTECLKD*1	Pin function select bits b4 b0 00000b: Hi-Z 00111b: POE8# 01010b: CTS5#/RTS5#/SS5# 10100b: GTETRG 10101b: GTECLKD	Pin function select bits b5 b0 000000b: Hi-Z 000111b: POE8# 001010b: CTS5#/RTS5#/ SS5# 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: MISOA 001110b: SSL01 010000b: CRX0 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 011000b: GTCPPO0 101100b: CTS011#/ RTS011#/SS011# 101101b: SCK011 101110b: TXDB011
PB5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/ SSDA5 10100b: GTIOC2B*1 10110b: GTIOC2B#*1	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/ SSDA5 10100b: GTIOC2B 10110b: GTIOC2B#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: TXD5/SMOSI5/ SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001110b: RSPCK0 010000b: CTX0 010100b: GTIOC2B 010101b: GTIOC3B 010110b: GTIOC2B# 010111b: GTIOC3B# 011101b: TIC0 101101b: TXD011/TXDA011/ SMOSI011/ SSDA011

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PB6PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/ SSCL5 10100b: GTIOC2A*1 10110b: GTIOC2A#*1	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/ SSCL5 10100b: GTIOC2A 10110b: GTIOC2A#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: RXD5/SMISO5/ SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001110b: MISO0 010000b: CRX0 010100b: GTIOC2A 010101b: GTIOC3A 010110b: GTIOC2A# 010111b: GTIOC3A# 011101b: TOC0 101101b: RXD011/ SMISO011/ SSCL011
PB7PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B*1 10110b: GTIOC1B#*1	Pin function select bits b4 b0 00000b: Hi-Z 01010b: SCK5 10100b: GTIOC1B 10110b: GTIOC1B#	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK5 001100b: SCK12 001110b: SSL03 010100b: GTIOC1B 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (100/80/64-pin) PB6: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB4: IRQ3 (144/100-pin) PB6: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ8 (48/64/80/100-pin) PB1: IRQ4 (48/64/80/100-pin) PB3: IRQ9 (48/64/80/100-pin) PB4: IRQ3 (48/64/80/100-pin) PB6: IRQ2 (48/64/80/100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.47 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX24T	RX24U	RX26T
PCnPFS	—	—	PCn pin function control register (n = 0 to 6)	—

Table 2.48 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PD0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO6 01101b: RSPCKA 10100b: GTIOC1A*1 10110b: GTIOC1A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO6 01101b: RSPCKA 10100b: GTIOC1A 10110b: GTIOC1A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO6 001101b: RSPCKA 001110b: RSPCK0 010100b: GTIOC3B 010101b: GTIOC1A 010110b: GTIOC3B# 010111b: GTIOC1A# 101101b: TXD008/TXDA008/ SMOSI008/ SSDA008
PD1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO2 01101b: MISOA 10100b: GTIOC0B*1 10110b: GTIOC0B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO2 01101b: MISOA 10100b: GTIOC0B 10110b: GTIOC0B#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO2 001101b: MISOA 001110b: MISO0 010100b: GTIOC3A 010101b: GTIOC0B 010110b: GTIOC3A# 010111b: GTIOC0B# 101101b: RXD008/ SMISO008/ SSCL008
PD2PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 00110b: TMO4 01010b: SCK5 01101b: MOSIA 10100b: GTIOC0A*1 10110b: GTIOC0A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 00110b: TMO4 01010b: SCK5 01101b: MOSIA 10100b: GTIOC0A 10110b: GTIOC0A#	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI1 000110b: TMO4 001010b: SCK5 001101b: MOSIA 001110b: MOSI0 010100b: GTIOC2B 010101b: GTIOC0A 010110b: GTIOC2B# 010111b: GTIOC0A# 101101b: SCK008 101110b: TXDB008

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PD3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/ SSDA1 10101b: GTECLKC*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: TXD1/SMOSI1/ SSDA1 01011b: TXD11/SMOSI11/ SSDA11 10101b: GTECLKC	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMO0 001010b: TXD1/SMOSI1/ SSDA1 001110b: MOSI0 010100b: GTIOC2A 010101b: GTETRGC 010110b: GTIOC2A# 010111b: GTIOC7B 101101b: TXD011/TXDA011/ SMOSI011/ SSDA011
PD4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 10101b: GTECLKB*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 00110b: TMCI6 01010b: SCK1 01011b: SCK11 10101b: GTECLKB	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMCI0 000110b: TMCI6 001010b: SCK1 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001110b: SSL02 010100b: GTIOC1B 010101b: GTETRGB 010110b: GTIOC1B# 101101b: SCK011 101110b: TXDB011
PD5PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/SMISO1/ SSCL1 10101b: GTECLKA*1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 00110b: TMRI6 01010b: RXD1/SMISO1/ SSCL1 01011b: RXD11/SMISO11/ SSCL11 10101b: GTECLKA	Pin function select bits b5 b0 000000b: Hi-Z 000101b: TMRI0 000110b: TMRI6 001010b: RXD1/SMISO1/ SSCL1 001110b: SSL00 010100b: GTIOC1A 010101b: GTETRGA 010110b: GTIOC1A# 010111b: GTIOC7A 101101b: RXD011/ SMISO011/ SSCL011

Register	Bit	RX24T (n = 0 to 7)	RX24U (n = 0 to 7)	RX26T (n = 0 to 7)
PD6PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C#*1 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/SS1# 01101b: SSLA0 10100b: GTIOC3B*1 10110b: GTIOC3B#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9C 00011b: MTIOC9C# 00101b: TMO1 01001b: ADST0 01010b: CTS1#/RTS1#/SS1# 01011b: CTS11#/RTS11#/ SS11# 01101b: SSLA0 10100b: GTIOC3B 10110b: GTIOC3B#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9C 000011b: MTIOC9C# 000101b: TMO1 001001b: ADST0 001010b: CTS1#/RTS1#/ SS1# 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA0 001110b: SSL00 010100b: GTIOC0B 010101b: GTIOC3B 010110b: GTIOC0B# 010111b: GTIOC3B# 011000b: GTIW 101101b: CTS011#/ RTS011#/SS011# 101110b: DE011
PD7PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A#*1 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/SMOSI5/ SSDA5*1 01101b: SSLA1 10100b: GTIOC3A*1 10110b: GTIOC3A#*1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9A 00011b: MTIOC9A# 00101b: TMRI1 00110b: TMRI5 01010b: TXD5/SMOSI5/ SSDA5 01101b: SSLA1 10100b: GTIOC3A 10110b: GTIOC3A#	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9A 000011b: MTIOC9A# 000101b: TMRI1 000110b: TMRI5 001010b: TXD5/SMOSI5/ SSDA5 001101b: SSLA1 001110b: SSL01 010000b: CTX0 010100b: GTIOC0A 010101b: GTIOC3A 010110b: GTIOC0A# 010111b: GTIOC3A# 011000b: GTIU 101100b: SCK009 101101b: TXD008/TXDA008/ SMOSI008/ SSDA008 101110b: TXDB009
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (100/80/64-pin) PD5: IRQ3 (100/80/64-pin) PD6: IRQ5 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (144/100-pin) PD5: IRQ3 (144/100-pin) PD6: IRQ5 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (64/80/100-pin) PD5: IRQ6 (48/64/80/100-pin) PD6: IRQ5 (64/80/100-pin) PD7: IRQ8 (48/64/80/100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.49 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 6)	RX26T (n = 0 to 5)
PE0PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00011b: MTIOC9B#*1 00101b: TMCI1 00110b: TMCI5 01010b: RXD5/SMISO5/ SSCL5*1 01101b: SSLA2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9B 00011b: MTIOC9B# 00101b: TMCI1 00110b: TMCI5 01010b: RXD5/SMISO5/ SSCL5 01101b: SSLA2	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9B 000011b: MTIOC9B# 000101b: TMCI1 000110b: TMCI5 001010b: RXD5/SMISO5/ SSCL5 001101b: SSLA2 001110b: SSL02 010000b: CRX0 011000b: GTIV
PE1PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D#*1 00101b: TMO5 01010b: CTS5#/RTS5#/SS5# 01101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 00001b: MTIOC9D 00011b: MTIOC9D# 00101b: TMO5 01010b: CTS5#/RTS5#/SS5# 01101b: SSLA3	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC9D 000011b: MTIOC9D# 000101b: TMO5 001010b: CTS5#/RTS5# SS5# 001100b: CTS12#/RTS12#/ SS12# 001101b: SSLA3 001110b: SSL03
PE3PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKD 00100b: MTCLKD#*1 00111b: POE11#	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKD 00100b: MTCLKD# 00111b: POE11#	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKD 000100b: MTCLKD# 000111b: POE11# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 101100b: CTS009#/ RTS009#/SS009# 101110b: DE009
PE4PFS	PSEL[4:0] (RX24T/ RX24U) PSEL[5:0] (RX26T)	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKC 00100b: MTCLKC#*1 00111b: POE10#	Pin function select bits b4 b0 00000b: Hi-Z 00010b: MTCLKC 00100b: MTCLKC# 00111b: POE10#	Pin function select bits b5 b0 000000b: Hi-Z 000010b: MTCLKC 000100b: MTCLKC# 000111b: POE10# 010100b: GTETRGA 010101b: GTETRGB 010110b: GTETRGC 010111b: GTETRGD 101100b: SCK009 101110b: TXDB009
PE5PFS	—	—	—	PE5 pin function control register

Register	Bit	RX24T (n = 0 to 5)	RX24U (n = 0 to 6)	RX26T (n = 0 to 5)
PE6PFS	—	—	PE6 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (100/80-pin) PE4: IRQ1 (100/80-pin) PE5: IRQ0 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE3: IRQ2 (144/100-pin) PE4: IRQ1 (144/100-pin) PE5: IRQ0 (144/100-pin) PE6: IRQ3 (144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ7 (100-pin) PE1: IRQ15 (100-pin) PE2: IRQ0 (48/64/80/100) PE3: IRQ2 (80/100-pin) PE4: IRQ1 (80/100-pin) PE5: IRQ0 (100-pin)

Note: 1. Only on chip version B in the RX24T Group

Table 2.50 Comparison of PFn Pin Function Control Register (PFnPFS)

Register	Bit	RX24T	RX24U	RX26T
PFnPFS	—	—	PFn pin function control register (n = 0 to 3)	—

Table 2.51 Comparison of PGn Pin Function Control Register (PGnPFS)

Register	Bit	RX24T	RX24U	RX26T
PGnPFS	—	—	PGn pin function control register (n = 0 to 2)	—

Table 2.52 Comparison of PN7 Pin Function Control Registers (PN7PFS)

Register	Bit	RX24T	RX24U	RX26T
PN7PFS	—	—	—	PN7 pin function control register

2.15 Multi-Function Timer Pulse Unit 3

Table 2.53 is Comparative Overview of Multi-Function Timer Pulse Unit 3, and Table 2.54 is Comparison of Multi-Function Timer Pulse Unit 3 Registers.

Table 2.53 Comparative Overview of Multi-Function Timer Pulse Unit 3

Item	RX24T (MTU3d)/RX24U (MTU3d)	RX26T (MTU3d)
Pulse input/output	Max. 28 lines	Max. 28 lines
Pulse input	3 lines	3 lines
Count clocks	11 clocks for each channel (14 for MTU0 and MTU9, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))	11 clocks for each channel (14 for MTU0 and MTU9, 12 for MTU2, 10 for MTU5, and 4 for MTU1 and MTU2 (when LWA = 1))
Operating frequency	Up to 80 MHz	Up to 120 MHz
Available operations	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation	[MTU0 to MTU4, MTU6, MTU7, MTU9] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 14-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation	[MTU0, MTU3, MTU4, MTU6, MTU7, MTU9] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode linked to MTU1 or MTU2 (when TMDR3.LWA = 1) • Cascade connection operation

Item	RX24T (MTU3d)/RX24U (MTU3d)	RX26T (MTU3d)
Available operations	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode	[MTU3, MTU4, MTU6, MTU7] • Ability to produce 12-phase waveform output, comprising six phases each of positive and negative output, in complementary PWM or reset PWM mode, through linked operation of MTU3 or MTU4 and MTU6 or MTU7 • In complementary PWM mode, ability to transfer data from the buffer register to a temporary register at peaks or troughs of the timer counter or when writes to the buffer register (MTU4.TGRD or MTU7.TGRD) occur • Ability to specify double buffer function in complementary PWM mode
	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU3, MTU4] • Through linked operation with MTU0, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
	[MTU5] • Can be used as a dead time compensation counter.	[MTU5] • Can be used as a dead time compensation counter.
	[MTU6, MTU7] • Through linked operation with MTU9, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output	[MTU6, MTU7] • Through linked operation with MTU9, ability to specify the AC synchronous motor (brushless DC motor) drive mode using complementary PWM or reset PWM and to select two types (chopping or level) of waveform output
Interrupt skipping function	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode	Ability to skip interrupts at counter peak or trough and A/D converter conversion start triggers in complementary PWM mode
Interrupt sources	45 sources	45 sources
Buffer operation	Automatic transfer of register data (transfer from buffer register to timer register)	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D converter start request delay function Ability to synchronize operation with PWM output	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at user-specified timing using A/D converter start request delay function Ability to synchronize operation with PWM output
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.54 Comparison of Multi-Function Timer Pulse Unit 3 Registers

Register	Bit	RX24T (MTU3d)/RX24U (MTU3d)	RX26T (MTU3d)
TADSTRGR0	TADSMEN0	—	ADSM0 pin output enable bit
TADSTRGR1	TADSMEN1	—	ADSM1 pin output enable bit

2.16 Port Output Enable 3

Table 2.55 is Comparative Overview of Port Output Enable 3, and Table 2.56 is Comparison of Port Output Enable 3 Registers.

Table 2.55 Comparative Overview of Port Output Enable 3

Item	RX24T (POE3b, POE3A)/RX24U (POE3A)	RX26T (POE3D)
Pin status while output is disabled	• High-impedance • General I/O port*1	• High-impedance • General I/O port
Output stop control target pins	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPT output pins*1 — GPT0 pins (GTIOC0A, GTIOC0B) — GPT1 pins (GTIOC1A, GTIOC1B) — GPT2 pins (GTIOC2A, GTIOC2B) — GPT3 pins (GTIOC3A, GTIOC3B)	• MTU output pins — MTU0 pins (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) — MTU3 pins (MTIOC3B, MTIOC3D) — MTU4 pins (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D) — MTU6 pins (MTIOC6B, MTIOC6D) — MTU7 pins (MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D) — MTU9 pins (MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D) • GPTW output pins — GPTW0 pins (GTIOC0A, GTIOC0B) — GPTW1 pins (GTIOC1A, GTIOC1B) — GPTW2 pins (GTIOC2A, GTIOC2B) — GPTW3 pins (GTIOC3A, GTIOC3B) — GPTW4 pins (GTIOC4A, GTIOC4B) — GPTW5 pins (GTIOC5A, GTIOC5B) — GPTW6 pins (GTIOC6A, GTIOC6B) — GPTW7 pins (GTIOC7A, GTIOC7B)
Conditions for generating an output stop request	• Input pin changes: When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, POE11#, or POE12# • Register settings are specified. • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output	• Input pin changes: When signal input occurs on pin POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# • SPOER register settings are specified. • Detection of stopped oscillation on main clock oscillator • Detection of comparator C (CMPC) output
Conditions for generating an output stop request	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPT output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B	• Short circuit of output pins: A match (short circuit) of output signal levels (active level) lasting one or more cycles on one of the combinations of pins listed below [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D — MTIOC6B and MTIOC6D — MTIOC7A and MTIOC7C — MTIOC7B and MTIOC7D [GPTW output pins] — GTIOC0A and GTIOC0B — GTIOC1A and GTIOC1B — GTIOC2A and GTIOC2B — GTIOC4A and GTIOC4B — GTIOC5A and GTIOC5B — GTIOC6A and GTIOC6B — GTIOC7A and GTIOC7B

Item	RX24T (POE3b, POE3A)/RX24U (POE3A)	RX26T (POE3D)
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 can be set for each of the POE0#, POE4#, POE8#, POE10#, POE11# and POE12# input pins.	• Falling-edge detection or low level detection can be set for each of the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, and POE9# pins. For low level detection, the sampling clock can be selected from PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, and PCLK/128, and the sampling count can be selected from 4 times, 8 times, and 16 times.
	• Output on all control target pins can be stopped on detection of falling edges or sampling of the low level on the POE0#, POE4#, POE8#, POE10#, POE11# and POE12# pins.	• Output on all control target pins can be stopped on detection of the falling edge of input or low level on the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, or POE9# pin.
	• Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.	• Output on all control target pins can be stopped when oscillation stop is detected in the clock generation circuit.
	• It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be stopped.	• It is possible to compare levels output on pins for complementary PWM output from the MTU, and when simultaneous output of the active level continues for one or more cycles, output on the pins can be stopped.
	• It is possible to compare levels output on GPT output pins (GPT0, GPT1, and GPT2), and when simultaneous output of the active level continues for at least one cycle, output on the pins can be stopped.	• It is possible to compare levels output on GPTW output pins (GPTW0 to GPTW2, GPTW4 to GPTW6, and GPTW7 pins), and when simultaneous output of the active level continues for at least one cycle, output on the pins can be stopped.
	• Output on all control target pins can be stopped on detection of output of Comparator C (CMPC).	• Output on all control target pins can be stopped on detection of output of Comparator C (CMPC).
	• Output on all control target pins can be stopped by modifying settings of POE registers.	• Output on all control target pins can be stopped by modifying settings of POE registers.
	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.	• Interrupts can be generated in response to the results of input level sampling or output-level comparison.
		• Signals output from the MTU output pins (MTU0 to MTU4, MTU6, MTU7, MTU9) and GPTW output pins (GPTW0 to GPTW7) can be used to mask output stop requests by the POE0#, POE4#, POE8#, POE10#, POE11#, POE12#, POE9# pins and COMP0 to COMP5 level detection signal.

Note: 1. Only on chip version B in the RX24T Group

Table 2.56 Comparison of Port Output Enable 3 Registers

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR1	POE0M[1:0] (RX24T/RX24U) POE0M[3:0] (RX26T)	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Samples the low level of the POE0# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE0# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE0# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE0 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE0# pin input. 0 1: Samples the low level of the POE0# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE0# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE0# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE0 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE0# pin input. 0 0 0 1: Samples the input from the POE0# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE0# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE0# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE0# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE0# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE0# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE0M2[3:0]	—	—	POE0 sampling count select bit
	INV	—	—	POE0# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR2	POE4M[1:0] (RX24T/RX24U) POE4M[3:0] (RX26T)	POE4 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Samples the low level of the POE4# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE4# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE4# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE4 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE4# pin input. 0 1: Samples the low level of the POE4# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE4# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE4# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE4 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE4# pin input. 0 0 0 1: Samples the input from the POE4# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE4# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE4# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE4# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE4# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE4# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE4M2[3:0]	—	—	POE4 sampling count select bit
	INV	—	—	POE4# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR3	POE8M[1:0] (RX24T/RX24U) POE8M[3:0] (RX26T)	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Samples the low level of the POE8# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE8# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE8# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE8 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE8# pin input. 0 1: Samples the low level of the POE8# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE8# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE8# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE8 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE8# pin input. 0 0 0 1: Samples the input from the POE8# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE8# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE8# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE8# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE8# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE8# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE8M2[3:0]	—	—	POE8 sampling count select bit
	INV	—	—	POE8# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR4	POE10M[1:0] (RX24T/RX24U) POE10M[3:0] (RX26T)	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Samples the low level of the POE10# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE10# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE10# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE10 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE10# pin input. 0 1: Samples the low level of the POE10# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE10# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE10# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE10 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE10# pin input. 0 0 0 1: Samples the input from the POE10# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE10# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE10# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE10# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE10# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE10# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE10M2[3:0]	—	—	POE10 sampling count select bit
	INV	—	—	POE10# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR5	POE11M[1:0] (RX24T/RX24U) POE11M[3:0] (RX26T)	POE11 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Samples the low level of the POE11# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE11# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE11# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE11 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE11# pin input. 0 1: Samples the low level of the POE11# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE11# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE11# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE11 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE11# pin input. 0 0 0 1: Samples the input from the POE11# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE11# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE11# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE11# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE11# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE11# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE11M2[3:0]	—	—	POE11 sampling count select bit
	INV	—	—	POE11# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR7	POE12M[1:0] (RX24T/RX24U) POE12M[3:0] (RX26T)	POE12 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Samples the low level of the POE12# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE12# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE12# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE12 mode select bits b1 b0 0 0: Accepts a request on the falling edge of POE12# pin input. 0 1: Samples the low level of the POE12# pin input 16 times at PCLK/8 clock pulses, and accepts a request when all are low level. 1 0: Samples the low level of the POE12# pin input 16 times at PCLK/16 clock pulses, and accepts a request when all are low level. 1 1: Samples the low level of the POE12# pin input 16 times at PCLK/128 clock pulses, and accepts a request when all are low level.	POE12 mode select bits b3 b0 0 0 0 0: Accepts a request on the falling edge or rising edge of POE12# pin input. 0 0 0 1: Samples the input from the POE12# pin by PCLK/8, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 0: Samples the input from the POE12# pin by PCLK/16, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 0 1 1: Samples the input from the POE12# pin by PCLK/128, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 0: Samples the input from the POE12# pin by PCLK, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 0 1: Samples the input from the POE12# pin by PCLK/2, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. 0 1 1 0: Samples the input from the POE12# pin by PCLK/4, and accepts a request when low-level or high-level results are detected consecutively for the specified number of times. Settings other than the above are prohibited.
	POE12M2[3:0]	—	—	POE12 sampling count select bit
	INV	—	—	POE12# pin input invert bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
ICSR8	—	—	—	Input level control/status register 8
OCSR3	—	—	Output level control/status register 3	Output level control/status register 3
OCSR4	—	—	—	Output level control/status register 4
OCSR5	—	—	—	Output level control/status register 5
ALR1	OLSG0A	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B/GTIOC0A (P71) pin active level setting bit	MTIOC3B pin active level setting bit
	OLSG0B	MTIOC3D/GTIOC0B (P74) pin active level setting bit	MTIOC3D/GTIOC0B (P74) pin active level setting bit	MTIOC3D pin active level setting bit
	OLSG1A	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A/GTIOC1A (P72) pin active level setting bit	MTIOC4A pin active level setting bit
	OLSG1B	MTIOC4C/GTIOC1B (P75) pin active level setting bit	MTIOC4C/GTIOC1B (P75) pin active level setting bit	MTIOC4C pin active level setting bit
	OLSG2A	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B/GTIOC2A (P73) pin active level setting bit	MTIOC4B pin active level setting bit
	OLSG2B	MTIOC4D/GTIOC2B (P76) pin active level setting bit	MTIOC4D/GTIOC2B (P76) pin active level setting bit	MTIOC4D pin active level setting bit
ALR3	OLSG0A	—	MTIOC3B/GTIOC0A (P12) pin active level setting bit	GTIOC0A (PD7/PD2/P71) pin active level setting bit
	OLSG0B	—	MTIOC3D/GTIOC0B (P15) pin active level setting bit	GTIOC0B (PD6/PD1/P74) pin active level setting bit
	OLSG1A	—	MTIOC4A/GTIOC1A (P13) pin active level setting bit	GTIOC1A (PD5/PD0/P72) pin active level setting bit
	OLSG1B	—	MTIOC4C/GTIOC1B (P16) pin active level setting bit	GTIOC1B (PD4/PB7/P75) pin active level setting bit
	OLSG2A	—	MTIOC4B/GTIOC2A (P14) pin active level setting bit	GTIOC2A (PD3/PB6/P73) pin active level setting bit
	OLSG2B	—	MTIOC4D/GTIOC2B (P17) pin active level setting bit	GTIOC2B (PD2/PB5/P76) pin active level setting bit
ALR4	—	—	—	Active level register 4
ALR5	—	—	—	Active level register 5
SPOER	—	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is an 8-bit register.	Software port output enable register SPOER is a 16-bit register.
	MTUCH34HIZ	MTU3 and MTU4 or GPT0 to GPT2 pin output stop enable bit	MTU3 and MTU4 or GPT0 to GPT2 pin output stop enable bit	MTU3 and MTU4 pin output stop enable bit
	GPT01HIZ	—	—	GPTW0 and GPTW1 pin output stop enable bit
	GPT23HIZ	—	—	GPTW2 and GPTW3 pin output stop enable bit
	GPT02HIZ	—	GPT0 to GPT2 or MTU3 and MTU4 pin output stop enable bit (b3)	GPTW0 to GPTW2 pin output stop enable bit (b8)
	GPT03HIZ	GPT0 to GPT3 pin output stop enable bit*1	GPT0 to GPT3 pin output stop enable bit	—
	GPT46HIZ	—	—	GPTW4 to GPTW6 pin output stop enable bit
	GPT79HIZ	—	—	GPTW7 pin output stop enable bit
POECR1	MTU0A1ZE	MTIOC0A (P31) pin high-impedance enable bit	MTIOC0A (P31) pin high-impedance enable bit	—
	MTU0B1ZE	MTIOC0B (P30) pin high-impedance enable bit	MTIOC0B (P30) pin high-impedance enable bit	—
POECR3*2	GPT0AZE	—	GTIOC0A (P12) pin high-impedance enable bit	—
	GPT0BZE	—	GTIOC0B (P15) pin high-impedance enable bit	—
	GPT1AZE	—	GTIOC1A (P13) pin high-impedance enable bit	—

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
POECR3*2	GPT1BZE	—	GTIOC1B (P16) pin high-impedance enable bit	—
	GPT2AZE	—	GTIOC2A (P14) pin high-impedance enable bit	—
	GPT2BZE	—	GTIOC2B (P17) pin high-impedance enable bit	—
	GPT0ABZE	—	—	GTIOC0A/GTIOC0B pin high-impedance enable bit
	GPT1ABZE	—	—	GTIOC1A/GTIOC1B pin high-impedance enable bit
	GPT2ABZE	—	—	GTIOC2A/GTIOC2B pin high-impedance enable bit
	GPT3ABZE	—	—	GTIOC3A/GTIOC3B pin high-impedance enable bit
	GPT4ABZE	—	—	GTIOC4A/GTIOC4B pin high-impedance enable bit
	GPT5ABZE	—	—	GTIOC5A/GTIOC5B pin high-impedance enable bit
	GPT6ABZE	—	—	GTIOC6A/GTIOC6B pin high-impedance enable bit
	GPT7ABZE	—	—	GTIOC7A/GTIOC7B pin high-impedance enable bit
	GPT0A1ZE	GTIOC0A (PD2) pin high-impedance enable bit	GTIOC0A (PD2) pin high-impedance enable bit	—
	GPT0B1ZE	GTIOC0B (PD1) pin high-impedance enable bit	GTIOC0B (PD1) pin high-impedance enable bit	—
	GPT1A1ZE	GTIOC1A (PD0) pin high-impedance enable bit	GTIOC1A (PD0) pin high-impedance enable bit	—
	GPT1B1ZE	GTIOC1B (PB7) pin high-impedance enable bit	GTIOC1B (PB7) pin high-impedance enable bit	—
	GPT2A1ZE	GTIOC2A (PB6) pin high-impedance enable bit	GTIOC2A (PB6) pin high-impedance enable bit	—
	GPT2B1ZE	GTIOC2B (PB5) pin high-impedance enable bit	GTIOC2B (PB5) pin high-impedance enable bit	—
	GPT3A1ZE	GTIOC3A high-impedance enable bit	GTIOC3A high-impedance enable bit	—
	GPT3B1ZE	GTIOC3B high-impedance enable bit	GTIOC3B high-impedance enable bit	—
POECR4	—	Port output enable control register 4	Port output enable control register 4	Port output enable control register 4
		Initial value after a reset differs.		
	IC1ADDMT34ZE	—	—	Bit for adding POE0F to the MTU3 and MTU4 output stop conditions
	IC8ADDMT34ZE	—	—	Bit for adding POE9F to the MTU3 and MTU4 output stop conditions
	CMADDMT67ZE	Bit for adding CFLAG to the MTU6 and MTU7 output stop conditions	Bit for adding CFLAG to the MTU6 and MTU7 output stop conditions	—
	IC1ADDMT67ZE	Bit for adding POE0F to the MTU6 and MTU7 output stop conditions	Bit for adding POE0F to the MTU6 and MTU7 output stop conditions	—
	IC3ADDMT67ZE	Bit for adding POE8F to the MTU6 and MTU7 output stop conditions	Bit for adding POE8F to the MTU6 and MTU7 output stop conditions	—
	IC4ADDMT67ZE	Bit for adding POE10F to the MTU6 and MTU7 output stop conditions	Bit for adding POE10F to the MTU6 and MTU7 output stop conditions	—
	IC5ADDMT67ZE	Bit for adding POE11F to the MTU6 and MTU7 output stop conditions	Bit for adding POE11F to the MTU6 and MTU7 output stop conditions	—

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
POECR4	IC6ADDMT67ZE	Bit for adding POE12F to the MTU6 and MTU7 output stop conditions	Bit for adding POE12F to the MTU6 and MTU7 output stop conditions	—
POECR4B	—	—	—	Port output enable control register 4B
POECR5	IC3ADDMT0ZE	—	—	Bit for adding POE8F to the MTU0 output stop conditions
	IC8ADDMT0ZE	—	—	Bit for adding POE9F to the MTU0 output stop conditions
POECR6*2	—	Port output enable control register 6	Port output enable control register 6	Port output enable control register 6
		Initial value after a reset differs.		
	CMADDGPT01ZE	—	—	Bit for adding CFLAG to the GPTW0 and GPTW1 output stop conditions
	IC1ADDGPT01ZE	—	—	Bit for adding POE0F to the GPTW0 and GPTW1 output stop conditions
	IC2ADDGPT01ZE	—	—	Bit for adding POE4F to the GPTW0 and GPTW1 output stop conditions
	IC3ADDGPT01ZE	—	—	Bit for adding POE8F to the GPTW0 and GPTW1 output stop conditions
	IC4ADDGPT01ZE	—	—	Bit for adding POE10F to the GPTW0 and GPTW1 output stop conditions
	IC5ADDGPT01ZE	—	—	Bit for adding POE11F to the GPTW0 and GPTW1 output stop conditions
	IC6ADDGPT01ZE	—	—	Bit for adding POE12F to the GPTW0 and GPTW1 output stop conditions
	IC8ADDGPT01ZE	—	—	Bit for adding POE9F to the GPTW0 and GPTW1 output stop conditions
	CMADDGPT02ZE	—	Bit for adding CFLAG to the GPT0 to GPT2 output stop conditions	—
	IC1ADDGPT02ZE	—	Bit for adding POE0F to the GPT0 to GPT2 output stop conditions	—
	IC2ADDGPT02ZE	—	Bit for adding POE4F to the GPT0 to GPT2 output stop conditions	—
	IC3ADDGPT02ZE	—	Bit for adding POE8F to the GPT0 to GPT2 output stop conditions	—
	IC5ADDGPT02ZE	—	Bit for adding POE11F to the GPT0 to GPT2 output stop conditions	—
	IC6ADDGPT02ZE	—	Bit for adding POE12F to the GPT0 to GPT2 output stop conditions	—
	CMADDGPT03ZE	Bit for adding CFLAG to the GPT0 to GPT3 output stop conditions	Bit for adding CFLAG to the GPT0 to GPT3 output stop conditions	—
	IC1ADDGPT03ZE	Bit for adding POE0F to the GPT0 to GPT3 output stop conditions	Bit for adding POE0F to the GPT0 to GPT3 output stop conditions	—
	IC2ADDGPT03ZE	Bit for adding POE4F to the GPT0 to GPT3 output stop conditions	Bit for adding POE4F to the GPT0 to GPT3 output stop conditions	—

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
POECR6*2	IC3ADDGPT03ZE	Bit for adding POE8F to the GPT0 to GPT3 output stop conditions	Bit for adding POE8F to the GPT0 to GPT3 output stop conditions	—
	IC4ADDGPT03ZE	Bit for adding POE10F to the GPT0 to GPT3 output stop conditions	Bit for adding POE10F to the GPT0 to GPT3 output stop conditions	—
	IC6ADDGPT03ZE	Bit for adding POE12F to the GPT0 to GPT3 output stop conditions	Bit for adding POE12F to the GPT0 to GPT3 output stop conditions	—
POECR6B	—	—	—	Port output enable control register 6B
POECR7	MTU9A1ZE	MTIOC9A (P21) pin high-impedance enable bit	MTIOC9A (P21) pin high-impedance enable bit	—
	MTU9B1ZE	MTIOC9B (P10) pin high-impedance enable bit	MTIOC9B (P10) pin high-impedance enable bit	—
	MTU9C1ZE	MTIOC9C (P20) pin high-impedance enable bit	MTIOC9C (P20) pin high-impedance enable bit	—
	MTU9D1ZE	MTIOC9D (P02) pin high-impedance enable bit	MTIOC9D (P02) pin high-impedance enable bit	—
	MTU9A2ZE	—	MTIOC9A (P26) pin high-impedance enable bit	—
	MTU9C2ZE	—	MTIOC9C (P25) pin high-impedance enable bit	—
POECR8	—	Port output enable control register 8	Port output enable control register 8	Port output enable control register 8
		Initial value after a reset differs.		
	IC6ADDMT9ZE	—	—	Bit for adding POE12F to the MTU9 output stop conditions
	IC8ADDMT9ZE	—	—	Bit for adding POE9F to the MTU9 output stop conditions
POECR9	—	—	—	Port output enable control register 9
POECR10	—	—	—	Port output enable control register 10
POECR11	—	—	—	Port output enable control register 11
PMMCR0*2	—	Port mode mask control register 0*2 PMMCR0 is an 8-bit register.	Port mode mask control register 0 PMMCR0 is an 8-bit register.	Port mode mask control register 0 PMMCR0 is a 16-bit register.
	MTU0A1ME	MTIOC0A (P31) pin port mode mask enable bit	MTIOC0A (P31) pin port mode mask enable bit	—
	MTU0B1ME	MTIOC0B (P30) pin port mode mask enable bit	MTIOC0B (P30) pin port mode mask enable bit	—
	MTU9AME	—	—	MTIOC9A pin port mode mask enable bit
	MTU9BME	—	—	MTIOC9B pin port mode mask enable bit
	MTU9CME	—	—	MTIOC9C pin port mode mask enable bit
	MTU9DME	—	—	MTIOC9D pin port mode mask enable bit
PMMCR1*2	MTU4BME	MTIOC4B/GTIOC2A (P73) pin port mode mask enable bit	MTIOC4B/GTIOC2A (P73) pin port mode mask enable bit	MTIOC4B pin port mode mask enable bit
	MTU4AME	MTIOC4A/GTIOC1A (P72) pin port mode mask enable bit	MTIOC4A/GTIOC1A (P72) pin port mode mask enable bit	MTIOC4A pin port mode mask enable bit
	MTU3BME	MTIOC3B/GTIOC0A (P71) pin port mode mask enable bit	MTIOC3B/GTIOC0A (P71) pin port mode mask enable bit	MTIOC3B pin port mode mask enable bit
	MTU4DME	MTIOC4D/GTIOC2B (P76) pin port mode mask enable bit	MTIOC4D/GTIOC2B (P76) pin port mode mask enable bit	MTIOC4D pin port mode mask enable bit
	MTU4CME	MTIOC4C/GTIOC1B (P75) pin port mode mask enable bit	MTIOC4C/GTIOC1B (P75) pin port mode mask enable bit	MTIOC4C pin port mode mask enable bit
	MTU3DME	MTIOC3D/GTIOC0B (P74) pin port mode mask enable bit	MTIOC3D/GTIOC0B (P74) pin port mode mask enable bit	MTIOC3D pin port mode mask enable bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
PMMCR2*2	GPT0AME	—	GTIOC0A/MTIOC3B (P12) pin port mode mask enable bit	GTIOC0A (PD7/PD2/P71) pin port mode mask enable bit
	GPT0BME	—	GTIOC0B/MTIOC3D (P15) pin port mode mask enable bit	GTIOC0B (PD6/PD1/P74) pin port mode mask enable bit
	GPT1AME	—	GTIOC1A/MTIOC4A (P13) pin port mode mask enable bit	GTIOC1A (PD5/PD0/P72) pin port mode mask enable bit
	GPT1BME	—	GTIOC1B/MTIOC4C (P16) pin port mode mask enable bit	GTIOC1B (PD4/PB7/P75) pin port mode mask enable bit
	GPT2AME	—	GTIOC2A/MTIOC4B (P14) pin port mode mask enable bit	GTIOC2A (PD3/PB6/P73) pin port mode mask enable bit
	GPT2BME	—	GTIOC2B/MTIOC4D (P17) pin port mode mask enable bit	GTIOC2B (PD2/PB5/P76) pin port mode mask enable bit
	GPT3AME	—	—	GTIOC3A pin port mode mask enable bit
	GPT3BME	—	—	GTIOC3B pin port mode mask enable bit
	GPT4AME	—	—	GTIOC4A pin port mode mask enable bit
	GPT4BME	—	—	GTIOC4B pin port mode mask enable bit
	GPT5AME	—	—	GTIOC5A pin port mode mask enable bit
	GPT5BME	—	—	GTIOC5B pin port mode mask enable bit
	GPT6AME	—	—	GTIOC6A pin port mode mask enable bit
	GPT6BME	—	—	GTIOC6B pin port mode mask enable bit
	GPT7AME	—	—	GTIOC7A pin port mode mask enable bit
	GPT7BME	—	—	GTIOC7B pin port mode mask enable bit
	GPT0A1ME	GTIOC0A (PD2) pin port mode mask enable bit	GTIOC0A (PD2) pin port mode mask enable bit	—
	GPT0B1ME	GTIOC0B (PD1) pin port mode mask enable bit	GTIOC0B (PD1) pin port mode mask enable bit	—
	GPT1A1ME	GTIOC1A (PD0) pin port mode mask enable bit	GTIOC1A (PD0) pin port mode mask enable bit	—
	GPT1B1ME	GTIOC1B (PB7) pin port mode mask enable bit	GTIOC1B (PB7) pin port mode mask enable bit	—
	GPT2A1ME	GTIOC2A (PB6) pin port mode mask enable bit	GTIOC2A (PB6) pin port mode mask enable bit	—
	GPT2B1ME	GTIOC2B (PB5) pin port mode mask enable bit	GTIOC2B (PB5) pin port mode mask enable bit	—
	GPT3A1ME	GTIOC3A/MTIOC9A (PD7) pin port mode mask enable bit	GTIOC3A/MTIOC9A (PD7) pin port mode mask enable bit	—
	GPT3B1ME	GTIOC3B/MTIOC9C (PD6) pin port mode mask enable bit	GTIOC3B/MTIOC9C (PD6) pin port mode mask enable bit	—
PMMCR3*2	MTU9A2ME	—	MTIOC9A (P26) pin port mode mask enable bit	—
	MTU9C2ME	—	MTIOC9C (P25) pin port mode mask enable bit	—
POECMPFR	C4FLAG	—	—	Comparator channel 4 output detection flag
	C5FLAG	—	—	Comparator channel 5 output detection flag
POECMPSEL	POEREQ4	—	—	Comparator channel 4 output stop enable bit
	POEREQ5	—	—	Comparator channel 5 output stop enable bit

Register	Bit	RX24T (POE3b, POE3A)	RX24U (POE3A)	RX26T (POE3D)
POECMPEXm *2	—	Port output enable comparator request extension select register m (m = 0 to 2, 4, 5)	Port output enable comparator request extension select register m (m = 0 to 5)	Port output enable comparator request extension select register m (m = 0 to 8)
	POEREQ4	—	—	Comparator channel 4 output stop enable bit
	POEREQ5	—	—	Comparator channel 5 output stop enable bit
M0SELR1	—	—	—	MTU0 pin select register 1
M0SELR2	—	—	—	MTU0 pin select register 2
M3SELR	—	—	—	MTU3 pin select register
M4SELR1	—	—	—	MTU4 pin select register 1
M4SELR2	—	—	—	MTU4 pin select register 2
M6SELR	—	—	—	MTU6 pin select register
M7SELR1	—	—	—	MTU7 pin select register 1
M7SELR2	—	—	—	MTU7 pin select register 2
M9SELR1	—	—	—	MTU9 pin select register 1
M9SELR2	—	—	—	MTU9 pin select register 2
G0SELR	—	—	—	GPTW0 pin select register
G1SELR	—	—	—	GPTW1 pin select register
G2SELR	—	—	—	GPTW2 pin select register
G3SELR	—	—	—	GPTW3 pin select register
G4SELR	—	—	—	GPTW4 pin select register
G5SELR	—	—	—	GPTW5 pin select register
G6SELR	—	—	—	GPTW6 pin select register
G7SELR	—	—	—	GPTW7 pin select register
IMCR0	—	—	—	Input signal mask control register 0
IMCR1	—	—	—	Input signal mask control register 1
IMCR2	—	—	—	Input signal mask control register 2
IMCR3	—	—	—	Input signal mask control register 3
IMCR4	—	—	—	Input signal mask control register 4
IMCR5	—	—	—	Input signal mask control register 5
IMCR6	—	—	—	Input signal mask control register 6
IMCR9	—	—	—	Input signal mask control register 9
IMCR10	—	—	—	Input signal mask control register 10
IMCR11	—	—	—	Input signal mask control register 11
IMCR12	—	—	—	Input signal mask control register 12
IMCR13	—	—	—	Input signal mask control register 13
IMCR14	—	—	—	Input signal mask control register 14

Notes: 1. These bits are reserved on chip version A of the RX24T Group. These bits are read as 0. The write value should be 0.
2. Implemented on chip version B only on the RX24T Group.

2.17 General Purpose PWM Timer

Table 2.57 is Comparative Overview of General Purpose PWM Timers, Table 2.58 is Comparison of General Purpose PWM Timer Registers, and
Table 2.59 is Comparison of GTIOA/GTIOB Bit Settings.

Table 2.57 Comparative Overview of General Purpose PWM Timers

Item	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWa)
Functions	• Selectable from 16 bits × 4 channels, 16 bits × 2 channels + 32 bits × 1 channel, and 32 bits × 2 channels	• 32 bits × 8 channels
	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter.	• Up-counting or down-counting (sawtooth waves) or up/down-counting (triangle waves) for each counter.
	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3	• Operating modes Sawtooth-wave PWM mode Sawtooth-wave one-shot pulse mode Triangle-wave PWM mode 1 Triangle-wave PWM mode 2 Triangle-wave PWM mode 3 Complementary PWM mode 1 (transfer at crest) Complementary PWM mode 2 (transfer at trough) Complementary PWM mode 3 (transfer at crest and trough) Complementary PWM mode 4 (immediate transfer)
	• Clock sources (nine internal clocks and four external clocks) independently selectable for each channel	• Clock sources (11 internal clocks) independently selectable for each channel
	• Two I/O pins per channel	• Two I/O pins per channel
	• Two output compare/input capture registers per channel	• Two output compare/input capture registers per channel
	• For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use.	• For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as compare registers when buffering is not in use.
	• In output compare operation, buffering can be performed at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms.	• In output compare operation, buffering can be performed at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms.
	• Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow)	• Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow)
	• Generation of dead time during PWM operation	• Generation of dead time during PWM operation
		• High-precision generation of approximately 0% and 100% duty PWM output

Item	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWa)
Functions	• Generation of three-phase PWM waveforms incorporating dead time by combining three counters	• Generation of PWM waveform incorporating a dead time by reflecting compare register settings immediately in output compare operation
	• Synchronous operation of the several counters • Synchronous operation modes: simultaneous start or phase shifting start by desired times	• Simultaneous start/stop/clearing of desired channel counters
		• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of eight ELC events based on ELC settings • Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by detecting two input signal conditions
	• Starting, stopping, and clearing counters in response to external or internal triggers (hardware sources)	• Operation of count start/count stop/counter clearing/up-counting/down-counting/input capture by maximum of four external triggers
	• Internal trigger sources: comparator output, MTU count start, software, and compare match	
		• Function to control output negation due to a dead time error or by requests for disabling of output from the POEG
	• A/D converter start trigger generation function	• A/D converter start trigger generation function • Event signals for compare match A to F and for overflow/underflow can be output to the ELC.
	• Ability to select noise filter for each input path	• Input capture input can select noise filter function. • Periodic count function • Measurement function of the pulse width of external input • Logic operation of inter-channel compare match output • Synchronous setting/clearing/input capture between channels • Bus clock: PCLKA GPTWA count reference clock: PCLKC Frequency ratio PCLKA: PCLKC = 1:N (N = 1/2)

Table 2.58 Comparison of General Purpose PWM Timer Registers

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTWP	—	General purpose PWM timer write-protection register GTWP is a 16-bit register.	General purpose PWM timer write-protection register GTWP is a 32-bit register.
	WP0 to WP3 (RX24T/RX24U) WP (RX26T)	GPT0, GPT1/GPT01, GPT2, GPT3/GPT23 register write disable bit	Register write disable bit
	STRWP	—	GTSTR.CSTRT bit write disable bit
	STPWP	—	GTSTP.CSTOP bit write disable bit
	CLRWP	—	GTCLR.CCLR bit write disable bit
	CMNWP	—	Common register write disable bit
	PRKEY[7:0]	—	GTWP key code bit
GTSTR	—	General purpose PWM timer software start register GTSTR is a 16-bit register.	General purpose PWM timer software start register GTSTR is a 32-bit register.
	CST0 (RX24T/RX24U) CSTRT0 (RX26T)	GPT0.GTCNT count start bit	Channel 0 count start bit
	CST1 (RX24T/RX24U) CSTRT1 (RX26T)	GPT1.GTCNT/GPT01.GTCNTLW count start bit	Channel 1 count start bit
	CST2 (RX24T/RX24U) CSTRT2 (RX26T)	GPT2.GTCNT count start bit	Channel 2 count start bit
	CST3 (RX24T/RX24U) CSTRT3 (RX26T)	GPT3.GTCNT/GPT23.GTCNTLW count start bit	Channel 3 count start bit
	CSTRT4	—	Channel 4 count start bit
	CSTRT5	—	Channel 5 count start bit
	CSTRT6	—	Channel 6 count start bit
	CSTRT7	—	Channel 7 count start bit
GTSTP	—	—	General purpose PWM timer software stop register
GTCLR	—	—	General purpose PWM timer software clear register
GTSSR	—	—	General purpose PWM timer start source select register
GTPSR	—	—	General purpose PWM timer stop source select register
GTCSR	—	—	General purpose PWM timer clear source select register
GTUPSR	—	—	General purpose PWM timer count-up source select register
GTDNSR	—	—	General purpose PWM timer count-down source select register
GTICASR	—	—	General purpose PWM timer input capture source select register A
GTICBSR	—	—	General purpose PWM timer input capture source select register B

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTCR	—	General purpose PWM timer control register GTCR is a 16-bit register.	General purpose PWM timer control register GTCR is a 32-bit register.
	CST	—	Count start bit
	ICDS	—	Input capture operation select at count stop bit
	SCGTIOC	—	GTIOC input source synchronous clear enable bit
	SSOGRP [1:0]	—	Synchronous set/clear group select bit
	CPSCD	—	Complementary PWM mode synchronous clear disable bit
	SSCEN	—	Synchronous set/reset enable bit
	MD[2:0] (RX24T/RX24U) MD[3:0] (RX26T)	Mode select bits b2 b0 0 0 0: Sawtooth-wave PWM mode (single buffer or double buffer possible) 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (16-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (16-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (32-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited	Mode select bits b19 b16 0 0 0 0: Sawtooth-wave PWM mode 1 (single buffer or double buffer possible) 0 0 0 1: Sawtooth-wave one-shot pulse mode (fixed buffer operation) 0 0 1 0: Sawtooth-wave PWM mode 2 (single buffer or double buffer possible) 0 0 1 1: Setting prohibited 0 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 0 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 0 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 0 1 1 1: Setting prohibited 1 0 0 0: Setting prohibited 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: Complementary PWM mode 1 (transfer at crest) 1 1 0 1: Complementary PWM mode 2 (transfer at trough) 1 1 1 0: Complementary PWM mode 3 (transfer at crest and trough) 1 1 1 1: Complementary PWM mode 4 (immediate transfer)

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTCR	TPCS[3:0]	Timer prescaler select bits b11 b8 0 0 0 0: PCLKA 0 0 0 1: PCLKA/2 0 0 1 0: PCLKA/4 0 0 1 1: PCLKA/8 0 1 0 0: PCLKA/16 0 1 0 1: PCLKA/32 0 1 1 0: PCLKA/64 0 1 1 1: PCLKA/256 1 0 0 0: PCLKA/1024 1 0 0 1: Setting prohibited 1 0 1 0: Setting prohibited 1 0 1 1: Setting prohibited 1 1 0 0: GTECLKA 1 1 0 1: GTECLKB 1 1 1 0: GTECLKC 1 1 1 1: GTECLKD	Timer prescaler select bits b26 b23 0 0 0 0: PCLKC 0 0 0 1: PCLKC/2 0 0 1 0: PCLKC/4 0 0 1 1: PCLKC/8 0 1 0 0: PCLKC/16 0 1 0 1: PCLKC/32 0 1 1 0: PCLKC/64 0 1 1 1: PCLKC/128 1 0 0 0: PCLKC/256 1 0 0 1: PCLKC/512 1 0 1 0: PCLKC/1024 1 0 1 1: Setting prohibited 1 1 0 0: GTETRGA (via POEG) 1 1 0 1: GTETRGB (via POEG) 1 1 1 0: GTETRGC (via POEG) 1 1 1 1: GTETRGD (via POEG)
	CCLR[1:0]	Counter clear source select bits	—
	CKEG[1:0]	—	Clock edge select bits
GTUDDTYC	—	—	General purpose PWM timer count direction and duty setting register
GTIOR	—	General purpose PWM timer I/O control register (n = 0 to 3) GTIOR is a 16-bit register.	General purpose PWM timer I/O control register (n = 0 to 7) GTIOR is a 32-bit register.
	GTIOA[5:0] (RX24T/RX24U) GTIOA[4:0] (RX26T)	GTIOCnA pin function select bits (b5-b0) For details, see Table 2.59.	GTIOCnA pin function select bits (b4-b0) For details, see Table 2.59.
	CPSCIR	—	Complementary PWM mode synchronous clear initial output suppression bit
	OAE	—	GTIOCnA pin output enable bit
	OADF[1:0]	—	GTIOCnA pin negate value setting bits
	OAEOCD	—	Cycle end output setting disable at GTCCRA register compare match bit
	PSYE	—	PWM cycle synchronous output enable bit
	NFAEN	—	GTIOCnA pin input noise filter enable bit
	NFCSA[1:0]	—	GTIOCnA pin input noise filter sampling clock select bits
	GTIOB[5:0] (RX24T/RX24U) GTIOB[4:0] (RX26T)	GTIOCnB pin function select bits (b13 to b8) For details, see Table 2.59.	GTIOCnB pin function select bits (b20 to b16) For details, see Table 2.59.
	OBDFLT	GTIOCnB pin output value setting at the count stop bit (b14)	GTIOCnB pin output value setting at the count stop bit (b22)
	OBHLD	GTIOCnB pin output setting at the start/stop count bit (b15)	GTIOCnB pin output setting at the start/stop count bit (b23)
	OBE	—	GTIOCnB pin output enable bit
	OBDF[1:0]	—	GTIOCnB pin negate value setting bits

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTIOR	OBEOCD	—	Cycle end output setting disable at GTCCRB register compare match bit

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTIOR	NFBEN	—	GTIOCnB pin input noise filter enable bit
	NFCSB[1:0]	—	GTIOCnB pin input noise filter sampling clock select bits
GTINTAD	—	General purpose PWM timer interrupt output setting register GTINTAD is a 16-bit register.	General purpose PWM timer interrupt output setting register GTINTAD is a 32-bit register.
	GTINTA	GTCCRA(LW) compare match/input capture interrupt enable bit	—
	GTINTB	GTCCRB(LW) compare match/input capture interrupt enable bit	—
	GTINTC	GTCCRC(LW) compare match interrupt enable bit	—
	GTINTD	GTCCRD(LW) compare match interrupt enable bit	—
	GTINTE	GTCCRE(LW) compare match interrupt enable bit	—
	GTINTF	GTCCRF(LW) compare match interrupt enable bit	—
	GTINTPR[1:0]	GTPR(LW) compare match interrupt enable bit	—
	SCFA	—	GTCCRA register compare match/input capture source synchronous clear enable bit
	SCFB	—	GTCCRB register compare match/input capture source simultaneous clear enable bit
	SCFC	—	GTCCRC register compare match source simultaneous clear enable bit
	SCFD	—	GTCCRD register compare match source simultaneous clear enable bit
	SCFE	—	GTCCRE register compare match source simultaneous clear enable bit
	SCFF	—	GTCCRF register compare match source simultaneous clear enable bit
	SCFPO	—	Overflow source simultaneous clear enable bit
	SCFPU	—	Underflow source simultaneous clear enable bit
	EINT	Dead time error interrupt enable bit	—
	ADTRAUEN	GTADTRA(LW) compare match (up-counting) A/D converter start request enable bit (b12)	GTADTRA register compare match (up-counting) A/D converter start request enable bit (b16)
	ADTRADEN	GTADTRA(LW) compare match (down-counting) A/D converter start request enable bit (b13)	GTADTRA register compare match (down-counting) A/D converter start request enable bit (b17)
	ADTRBUEN	GTADTRB(LW) compare match (up-counting) A/D converter start request enable bit (b14)	GTADTRB register compare match (up-counting) A/D converter start request enable bit (b18)
	ADTRBDEN	GTADTRB(LW) compare match (down-counting) A/D converter start request enable bit (b15)	GTADTRB register compare match (down-counting) A/D converter start request enable bit (b19)
	GRP[1:0]	—	Output stop group select bits
	GRPDTE	—	Dead time error output stop detection enable bit
	GRPABH	—	Simultaneous high output stop detection enable bit

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTINTAD	GRPABL	—	Simultaneous low output stop detection enable bit
	GTINTPC	—	Cycle count function end interrupt enable bit
GTST	—	General purpose PWM timer status register GTST is a 16-bit register.	General purpose PWM timer status register GTST is a 32-bit register.
	TCFA	—	Compare match/input capture flag A
	TCFB	—	Compare match/input capture flag B
	TCFC	—	Compare match flag C
	TCFD	—	Compare match flag D
	TCFE	—	Compare match flag E
	TCFF	—	Compare match flag F
	TCFPO	—	Overflow flag
	TCFPU	—	Underflow flag
	DTEF	Dead time error flag (b11)	Dead time error flag (b28)
	ADTRAUF	—	GTADTRA register compare match (up-counting) A/D converter start request flag
	ADTRADF	—	GTADTRA register compare match (down-counting) A/D converter start request flag
	ADTRBUF	—	GTADTRB register compare match (up-counting) A/D converter start request flag
	ADTRBDF	—	GTADTRB register compare match (down-counting) A/D converter start request flag
	ODF	—	Output stop request flag
	OABHF	—	Simultaneous high output flag
	OABLF	—	Simultaneous low output flag
	PCF	—	Periodic count function end flag
GTBER	—	General purpose PWM timer buffer enable register GTBER is a 16-bit register.	General purpose PWM timer buffer enable register GTBER is a 32-bit register.
	BD[0]	—	GTCCRA/GTCCRB registers buffer operation disable bit
	BD[1]	—	GTPR register buffer operation disable bit
	BD[2]	—	GTADTRA/GTADTRB register buffer operation disable bit
	BD[3]	—	GTDVU/GTDVD register buffer operation disable bit
	DBRTECA	—	GTCCRA register double buffer repeat operation enable bit
	DBRTSCA	—	GTCCRA register double buffer repeat operation period select bit
	DBRTECB	—	GTCCRB register double buffer repeat operation enable bit
	DBRTSCB	—	GTCCRB register double buffer repeat operation period select bit
	DBRTEADA	—	GTADTRA register double buffer repeat operation enable bit
	DBRTSADA	—	GTADTRA register double buffer repeat period select bit

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTBER	DBRTEADB	—	GTADTRB register double buffer repeat operation enable bit
	DBRTSADB	—	GTADTRB register double buffer repeat period select bit
	CCRA[1:0]	GTCCRA(LW) buffer operation bits (b1, b0)	GTCCRA register buffer operation bits (b17, b16)
	CCRB[1:0]	GTCCRB(LW) buffer operation bits (b3, b2)	GTCCRB register buffer operation bits (b19, b18)
	PR[1:0]	GTPR(LW) buffer operation bits (b5, b4)	GTPR register buffer operation bits (b21, b20)
	CCRSWT	GTCCRA(LW) and GTCCRB(LW) forcible buffer operation bit (b6)	GTCCRA/GTCCRB register forcible buffer operation bit (b22)
	ADTTA[1:0]	GTADTRA(LW) buffer transfer timing select bits • For triangle waves b9 b8 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • For sawtooth waves b9 b8 0 0: No transfer Other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clear	GTADTRA register buffer transfer timing select bits • For triangle waves and complementary PWM mode b25 b24 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • For sawtooth waves b25 b24 0 0: No transfer Other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clear
	ADTDA	GTADTRA(LW) double buffer operation bit (b10)	GTADTRA register double buffer operation bit (b26)
	ADTTB[1:0]	GTADTRB(LW) buffer transfer timing select bits • For triangle waves b13 b12 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • For sawtooth waves b13 b12 0 0: No transfer Other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clear	GTADTRB register buffer transfer timing select bits • For triangle waves and complementary PWM mode b29 b28 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough • For sawtooth waves b29 b28 0 0: No transfer Other than 0 0: Transfer at underflow (during down-counting), overflow (during up-counting), or counter clear
	ADTDB	GTADTRB(LW) double buffer operation bit (b14)	GTADTRB register double buffer operation bit (b30)
GTITC		General purpose PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 16-bit register.	General purpose PWM timer interrupt and A/D converter start request skipping setting register GTITC is a 32-bit register.

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTCNTLW (RX24T/24U) GTCNT (RX26T)	—	General purpose PWM timer longword counter	General purpose PWM timer counter*1
GTCCRmLW (RX24T/24U) GTCCRm (RX26T)	—	General purpose PWM timer longword compare capture register m (m = A to F)	General purpose PWM timer compare capture register m (m = A to F)*1
GTPRLW (RX24T/24U) GTPR (RX26T)	—	General purpose PWM timer longword period setting register	General purpose PWM timer period setting register*1
GTPBRLW (RX24T/24U) GTPBR (RX26T)	—	General purpose PWM timer longword period setting buffer register	General purpose PWM timer period setting buffer register*1
GTPDBRLW (RX24T/24U) GTPDBR (RX26T)	—	General purpose PWM timer longword period setting double buffer register	General purpose PWM timer period setting double buffer register*1
GTADTRmLW (RX24T/24U) GTADTRm (RX26T)	—	Longword A/D converter start request timing register m (m = A, B)	A/D converter start request timing register m (m = A, B)*1
GTADTBRmLW (RX24T/24U) GTADTBRm (RX26T)	—	Longword A/D converter start request timing buffer register m (m = A, B)	A/D converter start request timing buffer register m (m = A, B)*1
GTADTDBRmLW (RX24T/24U) GTADTDBRm (RX26T)	—	Longword A/D converter start request timing double buffer register m (m = A, B)	A/D converter start request timing double buffer register m (m = A, B)*1
GTDTCR	—	General purpose PWM timer dead time control register GTDTCR is a 16-bit register.	General purpose PWM timer dead time control register GTDTCR is a 32-bit register.
GTDVmLW (RX24T/24U) GTDVm (RX26T)	—	General purpose PWM timer longword dead time value register m (m = U, D)	General purpose PWM timer dead time value register m (m = U, D)*1
GTDBmLW (RX24T/24U) GTDBm (RX26T)	—	General purpose PWM timer longword dead time buffer register m (m = U, D)	General purpose PWM timer dead time buffer register m (m = U, D)*1
GTSOS	—	General purpose PWM timer output protection function status register GTSOS is a 16-bit register.	General purpose PWM timer output protection function status register GTSOS is a 32-bit register.
GTSOTR	—	General purpose PWM timer output protection function temporary release register GTSOTR is a 16-bit register.	General purpose PWM timer output protection function temporary release register GTSOTR is a 32-bit register.

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTADSMR	ADSMS0[3:0] (RX24T/RX24U) ADSMS0[1:0] (RX26T)	A/D converter start request signal monitor 0 selection bits b3 b0 0 0 0 0: A/D converter start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D converter start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D converter start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D converter start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D converter start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D converter start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D converter start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D converter start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting 1 0 0 0: A/D converter start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D converter start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D converter start request signal generated by the GPT2.GTADTRB register during up-counting 1 0 1 1: A/D converter start request signal generated by the GPT2.GTADTRB register during down-counting	A/D converter start request signal monitor 0 selection bits b1 b0 0 0: A/D converter start request signal generated by the GTADTRA register during up-counting 0 1: A/D converter start request signal generated by the GTADTRA register during down-counting 1 0: A/D converter start request signal generated by the GTADTRB register during up-counting 1 1: A/D converter start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTADSMR	ADSMS0[3:0] (RX24T/RX24U) ADSMS0[1:0] (RX26T)	1 1 0 0: A/D converter start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D converter start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D converter start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D converter start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	
	ADSMS1[3:0] (RX24T/RX24U) ADSMS1[1:0] (RX26T)	A/D converter start request signal monitor 1 selection bits b19 b16 0 0 0 0: A/D converter start request signal generated by the GPT0.GTADTRA register during up-counting 0 0 0 1: A/D converter start request signal generated by the GPT0.GTADTRA register during down-counting 0 0 1 0: A/D converter start request signal generated by the GPT0.GTADTRB register during up-counting 0 0 1 1: A/D converter start request signal generated by the GPT0.GTADTRB register during down-counting 0 1 0 0: A/D converter start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during up-counting 0 1 0 1: A/D converter start request signal generated by the GPT1.GTADTRA/GPT01.GTADTRALW register during down-counting 0 1 1 0: A/D converter start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during up-counting 0 1 1 1: A/D converter start request signal generated by the GPT1.GTADTRB/GPT01.GTADTRBLW register during down-counting	A/D converter start request signal monitor 1 selection bits b17 b16 0 0: A/D converter start request signal generated by the GTADTRA register during up-counting 0 1: A/D converter start request signal generated by the GTADTRA register during down-counting 1 0: A/D converter start request signal generated by the GTADTRB register during up-counting 1 1: A/D converter start request signal generated by the GTADTRB register during down-counting

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTADSMR	ADSMS1[3:0] (RX24T/RX24U) ADSMS1[1:0] (RX26T)	1 0 0 0: A/D converter start request signal generated by the GPT2.GTADTRA register during up-counting 1 0 0 1: A/D converter start request signal generated by the GPT2.GTADTRA register during down-counting 1 0 1 0: A/D converter start request signal generated by the GPT2.GTADTRB register during up-counting 1 0 1 1: A/D converter start request signal generated by the GPT2.GTADTRB register during down-counting 1 1 0 0: A/D converter start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during up-counting 1 1 0 1: A/D converter start request signal generated by the GPT3.GTADTRA/GPT23.GTADTRALW register during down-counting 1 1 1 0: A/D converter start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during up-counting 1 1 1 1: A/D converter start request signal generated by the GPT3.GTADTRB/GPT23.GTADTRBLW register during down-counting	
GTEITC	—	—	General purpose PWM timer extended interrupt skipping counter control register
GTEITLI1	—	—	General purpose PWM timer extended interrupt skipping setting register 1
GTEITLI2	—	—	General purpose PWM timer extended interrupt skipping setting register 2
GTEITLB	—	—	General purpose PWM timer extended buffer transfer skipping setting register
GTICLF	—	—	General purpose PWM timer inter-channel logical operation register
GTPC	—	—	General purpose PWM timer cycle count register
GTADCMSC	—	—	General purpose PWM timer A/D converter start request compare match skipping setting register
GTADCMSS	—	—	General purpose PWM timer A/D converter start request compare match skipping setting register
GTSECSR	—	—	General purpose PWM timer operation enable bit simultaneous control channel select register
GTSECR	—	—	General purpose PWM timer operation enable bit simultaneous control register

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTBER2	—	—	General purpose PWM timer buffer enable register 2
GTOLBR	—	—	General purpose PWM timer output level buffer register
GTICCR	—	—	General purpose PWM timer inter-channel coordinated input capture control register
OPSCR	—	—	Output phase switch control register
NFCR	—	Noise filter control register	—
GTHSCR	—	General purpose PWM timer hardware source start/stop control register	—
GTHCCR	—	General purpose PWM timer hardware source clear control register	—
GTHSSR	—	General purpose PWM timer hardware start source select register	—
GTHPSR	—	General purpose PWM timer hardware stop/clear source select register	—
GTSYNC	—	General purpose PWM timer sync register	—
GTETINT	—	General purpose PWM timer external trigger input interrupt register	—
GTBDR	—	General purpose PWM timer buffer operation disable register	—
GTSWP	—	General purpose PWM timer start write-protection register	—
GTCWP	—	General purpose PWM timer clearing write-protection register	—
GTCMNWP	—	General purpose PWM timer common register write-protection register	—
GTMDR	—	General purpose PWM timer mode register	—
GTECNFCR	—	General purpose PWM timer external clock noise filter control register	—
GTUDC	—	General purpose PWM timer count direction register	—
GTCNTLW	—	General purpose PWM timer longword counter register	—
GTCCRmLW	—	General purpose PWM timer longword compare capture register m (m = A to F)	—
GTPRLW	—	General purpose PWM timer longword period setting register	—
GTPBRLW	—	General purpose PWM timer longword period setting buffer register	—
GTPDBRLW	—	General purpose PWM timer longword period setting double buffer register	—
GTADTRmLW	—	Longword A/D converter start request timing register m (m = A, B)	—
GTADTBRmLW	—	Longword A/D converter start request timing buffer register m(m = A, B)	—
GTADTDBRmLW	—	Longword A/D converter start request timing double buffer register m (m = A, B)	—
GTONCR	—	General purpose PWM timer output negate control register	—
GTDVmLW	—	General purpose PWM timer longword dead time value register m (m = U, D)	—

Register	Bit	RX24T (GPTB)/RX24U (GPTB)	RX26T (GPTWA)
GTDBmLW	—	General purpose PWM timer longword dead time buffer register m (m = U, D)	—

Note: 1. For products with a RAM capacity of 48 KB, upper 16 bits are reserved. These bits are read as 0.

Table 2.59 Comparison of GTIOA/GTIOB Bit Settings

Bit	RX24T (GPTB)/RX24U (GPTB) GTIOA/B[5:0] Bits	RX26T (GPTWA) GTIOA/B[4:0] Bits
b5	0: Compare match 1: Input capture	—
b4	• When b5 = 0 0: Initial output is low 1: Initial output is high • When b5 = 1 x: Don't care	0: Initial output is low 1: Initial output is high
b3, b2	• When b5 = 0 0 0: Output retained at end of cycle 0 1: Low output at end of cycle 1 0: High output at end of cycle 1 1: Output toggled at end of cycle • When b5 = 1 x: Don't care	0 0: Output retained at end of cycle 0 1: Low output at end of cycle 1 0: High output at end of cycle 1 1: Output toggled at end of cycle
b1, b0	• When b5 = 0 0 0: Output retained at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 0 1: Low output at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 1 0: High output at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match 1 1: Output toggled at GPTn.GTCCRA(LW)/GTCCRB(LW) compare match • When b5 = 1 0 0: Input capture at rising edge 0 1: Input capture at falling edge 1 0: Input capture at both edges 1 1: Input capture at both edges	0 0: Output retained at GTCCRA/GTCCRB compare match 0 1: Low output at GTCCRA/GTCCRB compare match 1 0: High output at GTCCRA/GTCCRB compare match 1 1: Output toggled at GTCCRA/GTCCRB compare match

2.18 8-Bit Timer

Table 2.60 is Comparative Overview of 8-Bit Timers, and Table 2.61 is Comparison of 8-Bit Timer Registers.

Table 2.60 Comparative Overview of 8-Bit Timers

Item	RX24T (TMR)/RX24U (TMR)	RX26T (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 4 units	(8 bits × 2 channels) × 4 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal	Selectable among compare match A or B, or an external counter reset signal
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, and TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, and TMR7 can be used to count TMR6 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits, TMR4 for the upper 8 bits and TMR5 for the lower 8 bits, and TMR6 for the upper 8 bits and TMR7 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches, TMR5 can be used to count TMR4 compare matches, and TMR7 can be used to count TMR6 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	—	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	—	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of trigger to start A/D converter	Compare match A of TMR0, TMR2, TMR4, or TMR6	Compare match A of TMR0, TMR2, TMR4, or TMR6
Generation of baud rate clock for SCI	Generation of baud rate clock for SCI	Generation of SCI basic clock

Item	RX24T (TMR)/RX24U (TMR)	RX26T (TMRb)
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

Table 2.61 Comparison of 8-Bit Timer Registers

Register	Bit	RX24T (TMR)/RX24U (TMR)	RX26T (TMRb)
TCSTR	—	—	Timer counter start register

2.19 Compare Match Timer

Table 2.62 is Comparative Overview of Compare Match Timers.

Table 2.62 Comparative Overview of Compare Match Timers

Item	RX24T (CMT)/RX24U (CMT)	RX26T (CMT)
Count clocks	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	• Four frequency dividing clocks: One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	—	An event signal is output upon a CMT1 compare match.
Event link function (input)	—	• Linking to the specified module is possible. • CMT1 count start, event counter, or count restart operation is possible.
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

2.20 Independent Watchdog Timer

Table 2.63 is Comparative Overview of Independent Watchdog Timers, and Table 2.64 is Comparison of Independent Watchdog Timer Registers.

Table 2.63 Comparative Overview of Independent Watchdog Timers

Item	RX24T (IWDTa)/RX24U (IWDTa)	RX26T (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock divide ratio	Divide by 1, 16, 32, 64, 128, or 256	Divide by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting automatically starts after a reset (auto-start mode) • Counting is started (register start mode) by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting is started by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • A counter underflows or a refresh error occurs — Counting restarts (In auto-start mode, counting automatically restarts after a reset or after a non-maskable interrupt request is output. In register start mode, counting restarts after refreshing.)	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (by means of register setting) • Underflow or refresh error (register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	—	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX24T (IWDTa)/RX24U (IWDTa)	RX26T (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)

Table 2.64 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX24T (IWDTa)/RX24U (IWDTa)	RX26T (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)	Timeout period select bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request or interrupt request output is enabled. 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, and deep sleep mode.	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering sleep, software standby, and all-module clock stop mode.

2.21 Serial Communications Interface

Table 2.65 is Comparative Overview of Serial Communications Interfaces, Table 2.66 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.67 is Comparison of Serial Communications Interface Registers.

Table 2.65 Comparative Overview of Serial Communications Interfaces

Item		RX24T (SCIg)	RX24U (SCIg)	RX26T (SCIk, SCIh)
Number of channels		• SCIg: 3 channels	• SCIg: 6 channels	• SCIk: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	—	The levels of input and output signals can be inverted independently (SCI1, SCI5, SCI6).
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1, SCI5, SCI6) • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX24T (SCIg)	RX24U (SCIg)	RX26T (SCIk, SCIh)
Asynchronous mode	Data match detection	—	—	Compares receive data and comparison data register, and generates interrupt when they match (SCI1, SCI5, SCI6).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point. (SCI1, SCI5, SCI6)
	Transmit signal change timing adjustment	—	—	Either the falling or rising edge of the transmit data can be delayed (SCI1, SCI5, SCI6).
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX24T (SCIg)	RX24U (SCIg)	RX26T (SCIk, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	—	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates

Item		RX24T (SCIg)	RX24U (SCIg)	RX26T (SCIk, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	—	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	—	—	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		—	—	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.66 Comparison of Serial Communications Interface Channel Specifications

Item	RX24T (SCIg)	RX24U (SCIg)	RX26T (SCIk, SCIh)
Asynchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI1, SCI5, SCI6	SCI1, SCI5, SCI6, SCI8, SCI9, SCI11	SCI1, SCI5, SCI6, SCI12
Data match detection	—	—	SCI1, SCI5, SCI6
Extended serial mode	—	—	SCI12
TMR clock input	SCI5, SCI6	SCI5, SCI6	SCI5, SCI6, SCI12
Event link function	—	—	SCI5
Peripheral module clock	PCLKB: SCI1, SCI5, SCI6	PCLKB: SCI1, SCI5, SCI6, SCI8, SCI9 PCLKA: SCI11	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.67 Comparison of Serial Communications Interface Registers

Register	Bit	RX24T (SCIg)/RX24U (SCIg)	RX26T (SCIk, SCIh)
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5 and SCI6 only) Available compare match output varies per SCI channel.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6 and SCI12 only) Available compare match output varies per SCI channel.
	ITE	—	Immediate transmission enable bit*1
	ABCSE	—	Asynchronous mode base clock select extended bit*1
SPMR	MSS	Master/slave select bit 0: TXDn pin: Transmit, RXDn pin: Receive (master mode) 1: TXDn pin: Receive, RXDn pin: Transmit (slave mode)	Master/slave select bit 0: SMOSIn pin: Transmit, SMISOn pin: Receive (master mode) 1: SMOSIn pin: Receive, SMISOn pin: Transmit (slave mode)
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register
PRDFR0	—	—	Product function select register 0

Note: 1. These bits are reserved in SCI12. These bits are read as 0. The write value should be 0.

2.22 I²C Bus Interface

Table 2.68 is Comparative Overview of I2C Bus Interfaces.

Table 2.68 Comparative Overview of I²C Bus Interfaces

Item	RX24T (RIICa)/RX24U (RIICa)	RX26T (RIICa)
Communication format	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C-bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode is supported (up to 400 kbps)	Fast-mode is supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.	For master operation, the duty cycle of the SCL clock is selectable in the range from 4 to 96%.
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.	• Start, restart, and stop conditions are automatically generated. • Start conditions (including restart conditions) and stop conditions are detectable.
Slave address	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Up to three different slave addresses can be set. • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. — Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. — If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level. — Waiting between the eighth and ninth clock cycles — Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Change timing of the output of transmitted data, including the acknowledge bit, can be delayed.

Item	RX24T (RIICa)/RX24U (RIICa)	RX26T (RIICa)
Arbitration	• For multi-master operation — Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation — Operation to synchronize the SCL in cases of conflict with the SCL signal from another master is possible. — When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to detection of the start condition while the bus is busy is detectable (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • Loss of arbitration due to non-matching of internal and line levels for data is detectable in slave transmission.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock.	The internal timeout function is capable of detecting long-interval stop of the SCL.
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA signals, and the width for noise cancellation by the filters is adjustable by software.
Interrupt sources	• Four sources: — Error in transfer or occurrence of events Detection of arbitration, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end	• Four sources: — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Item	RX24T (RIICa)/RX24U (RIICa)	RX26T (RIICa)
RIIC operating modes	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode	• 4 modes: — Master transmit mode — Master receive mode — Slave transmit mode — Slave receive mode
Event link function (output)	—	• Four sources (RIIC0): — Error in transfer or occurrence of events Detection of arbitration lost, NACK, timeout, a start condition including a restart condition, or a stop condition — Receive data full (including matching with a slave address) — Transmit data empty (including matching with a slave address) — Transmit end

2.23 CAN Module and CAN FD Module

Table 2.69 is Comparative Overview of CAN Module and CAN FD Module, and Table 2.70 is Comparison of CAN Module/CAN FD Module Registers.

Table 2.69 Comparative Overview of CAN Module and CAN FD Module

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD)
Protocol	Conforming to the ISO 11898-1 standard	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX24T/RX24U) Data transfer rate (RX26T)	Maximum of 1 Mbps	Arbitration phase: Maximum of 1 Mbps Data phase: Maximum 8 Mbps*1
Operating frequency	PCLKB: 40 MHz (max.) CANMCLK: 20 MHz (max.)	Register block: Maximum of 60 MHz (PCLKB) Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Buffer (RX24T/RX24U) Message buffer (RX26T)	A total of 20 buffers • Individual buffers: 4 buffers (4 buffers for one channel) Transmit buffer: 4 buffers per channel • Shared buffers: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per channel (up to 16 buffers allocatable to each)	• Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported. • 32 receive message buffers
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD*1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Interrupts can be enabled or disabled for each FIFO. • Mirror function (to receive messages transmitted from the own CAN node)	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes*1
Receive filter function (RX24T/RX24U) Acceptance filter (RX26T)	• Receive messages can be selected according to 16 receive rules. • The number of receive rules (0 to 16) can be set for each channel. • Acceptance filter processing: ID and mask can be set for each receive rule. • DLC filter processing: A DLC check value can be set for each receive rule.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Receive message transfer function	• Routing function to transfer receive messages to arbitrary destinations (can be transferred to up to two buffers). Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Label information can be stored together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or transmit buffer priority transmission mode can be selected. • Transmission can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each transmit buffer, or transmit/receive FIFO buffer.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD)
FIFO	• Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) • Transmit/receive FIFO buffer: A FIFO buffer per channel (up to 16 buffers allocatable to each)	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Interval transmission function (RX24T/RX24U) Automatic transmission interval adjustment (RX26T)	The message transmission interval time can be set. (transmit mode of transmit/receive FIFO buffers)	Available when the common FIFO is configured as a transmit FIFO The interval between messages sent from the FIFO can be adjusted.
Transmit history function	Stores the history information of transmitted messages.	—
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to channel halt mode when bus off starts. • The mode automatically changes to channel halt mode when bus off ends. • A program causes a transition to channel halt mode. • A program causes a transition to error active state (forcible return from the bus off state).	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CH_Halt mode when bus off ends. • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timer	Time stamp function (recording of 16-bit timer value indicating time message received)	Transmission and reception timestamp function
Interrupt function	• Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) — Channel transmission interrupt Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Channel error interrupt — Transmit/receive FIFO receive interrupt	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
Software support	—	Label information is automatically added to received messages.

Item	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD)
Test modes	Test function for user evaluation • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback) • RAM test (read/write test)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback mode) • Self test mode 1 (internal loopback mode)
Low power consumption function (RX24T/RX24U) Power down function (RX26T)	Ability to specify module stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.70 Comparison of CAN Module/CAN FD Module Registers

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD-Lite)
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFO n status register (n = 0, 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD-Lite)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	Transmit message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register
CFGL	—	Bit configuration register L	—
CFGH	—	Bit configuration register H	—
CTRL	—	Control register L	—
CTRH	—	Control register H	—
STSL	—	Status register L	—
STSH	—	Status register H	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD-Lite)
ERFLL	—	Error flag register L	—
ERFLH	—	Error flag register H	—
GCFGL	—	Global configuration register L	—
GCFGH	—	Global configuration register H	—
GCTRL	—	Global control register L	—
GCTRH	—	Global control register H	—
GSTS	—	Global status register	—
GERFLL	—	Global error flag register	—
GTINTSTS	—	Global transmit interrupt status register	—
GTSC	—	Timestamp register	—
GAFLCFG	—	Receive rule number configuration register	—
GAFLIDLj	—	Receive rule entry register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive rule entry register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive rule entry register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive rule entry register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive rule entry register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive rule entry register jCH (j = 0 to 15)	—
RMNB	—	Receive buffer number configuration register	—
RMND0	—	Receive buffer receive complete flag register	—
RMIDLn	—	Receive buffer register nAL (n = 0 to 15)	—
RMIDHn	—	Receive buffer register nAH (n = 0 to 15)	—
RMTSn	—	Receive buffer register nBL (n = 0 to 15)	—
RMPTRn	—	Receive buffer register nBH (n = 0 to 15)	—
RMDF0n	—	Receive buffer register nCL (n = 0 to 15)	—
RMDF1n	—	Receive buffer register nCH (n = 0 to 15)	—
RMDF2n	—	Receive buffer register nDL (n = 0 to 15)	—
RMDF3n	—	Receive buffer register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO control register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO status register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO pointer control register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO access register mAL (m = 0, 1)	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD-Lite)
RFIDHm	—	Receive FIFO access register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO access register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO access register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO access register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO access register mCH (m = 0, 1)	—
RFDF2m	—	Receive FIFO access register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO access register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/receive FIFO control register 0L	—
CFCCH0	—	Transmit/receive FIFO control register 0H	—
CFSTS0	—	Transmit/receive FIFO status register 0	—
CFPCTR0	—	Transmit/receive FIFO pointer control register 0	—
CFIDL0	—	Transmit/receive FIFO access register 0AL	—
CFIDH0	—	Transmit/receive FIFO access register 0AH	—
CFTS0	—	Transmit/receive FIFO access register 0BL	—
CFPTR0	—	Transmit/receive FIFO access register 0BH	—
CFDF00	—	Transmit/receive FIFO access register 0CL	—
CFDF10	—	Transmit/receive FIFO access register 0CH	—
CFDF20	—	Transmit/receive FIFO access register 0DL	—
CFDF30	—	Transmit/receive FIFO access register 0DH	—
RFMSTS	—	Receive FIFO message lost status register	—
CFMSTS	—	Transmit/receive FIFO message lost status register	—
RFISTS	—	Receive FIFO interrupt status register	—
CFISTS	—	Transmit/receive FIFO receive interrupt status register	—
TMCp	—	Transmit buffer control register p (p = 0 to 3)	—
TMSTSp	—	Transmit buffer status register p (p = 0 to 3)	—
TMTRSTS	—	Transmit buffer transmit request status register	—
TMTCSTS	—	Transmit buffer transmit complete status register	—

Register	Bit	RX24T (RSCAN)/RX24U (RSCAN)	RX26T (CANFD-Lite)
TMTASTS	—	Transmit buffer transmit abort status register	—
TMIEC	—	Transmit buffer interrupt enable register	—
TMIDLp	—	Transmit buffer register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit buffer register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit buffer register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit buffer register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit buffer register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit buffer register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit buffer register pDH (p = 0 to 3)	—
THLCC0	—	Transmit history buffer control register	—
THLSTS0	—	Transmit history buffer status register	—
THLACC0	—	Transmit history buffer access register	—
THLPCTR0	—	Transmit history buffer pointer control register	—
GRWCR	—	Global RAM window control register	—
GTSTCFG	—	Global test configuration register	—
GTSTCTRL	—	Global test control register	—
GLOCKK	—	Global test protection unlock register	—
RPGACCr	—	RAM test register r (r = 0 to 127)	—

2.24 Serial Peripheral Interface

Table 2.71 is Comparative Overview of Serial Peripheral Interfaces, and Table 2.72 is Comparison of Serial Peripheral Interface Registers.

Table 2.71 Comparative Overview of Serial Peripheral Interfaces

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX26T (RSPId)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). — Width at high level: 3 cycles of PCLK — Width at low level: 3 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX26T (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: — SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — RSPI error interrupt (mode fault, overrun, underrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt

Item	RX24T (RSPIb)/RX24U (RSPIb)	RX26T (RSPId)
Event link function (output)	—	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle events — Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.72 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX24T (RSPIb)/RX24U (RSPIb)	RX26T (RSPId)
SPSR	SPCF	—	Communication completion flag
SPDR	—	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1, SPDCR.SPBYT = 0) • Word access (SPDCR.SPLW = 0, SPDCR.SPBYT = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPCR2	SPPE	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed (when SPCR.TXMD = 0). A parity bit is added to transmit data, but no parity checking of receive data is performed (when SPCR.TXMD = 1).	Parity enable bit 0: A parity bit is not added to transmit data, and no parity checking of receive data is performed. 1: A parity bit is added to transmit data, and parity checking of receive data is performed.
SPDCR2	—	—	RSPI data control register 2
SPCR3	—	—	RSPI control register 3

2.25 CRC Calculator

Table 2.73 is Comparative Overview of CRC Calculators, and Table 2.74 is Comparison of CRC Calculator Registers.

Table 2.73 Comparative Overview of CRC Calculators

Item	RX24T (CRC)/RX24U (CRC)	RX26T (CRCA)	
Data size	8 bits	8 bits	32 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	8-bit parallel processing	32-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of three generating polynomials is selectable • 8-bit CRC: $X^8 + X^2 + X + 1$ • 16-bit CRC: $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.74 Comparison of CRC Calculator Registers

Register	Bit	RX24T (CRC)/RX24U (CRC)	RX26T (CRCA)
CRCCR	GPS[1:0] (RX24T/ RX24U) GPS[2:0] (RX26T)	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X_9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.
	LMS	CRC calculation switching bit (b2)	CRC calculation switching bit (b6)
CRCDIR	—	CRC data input register Supported access sizes • Byte access	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)
CRCDOR	—	CRC data output register Supported access sizes • Word access The lower byte (b7 to b0) is used when generating 8-bit CRC.	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)

2.26 12-Bit A/D Converter

Table 2.75 is Comparative Overview of 12-Bit A/D Converters, Table 2.76 is Comparison of 12-Bit A/D Converter Registers, Table 2.77 is Comparative Listing of A/D Conversion Startup Sources That Can Be Set in ADSTRGR Register, and Table 2.78 is Listing of A/D Conversion Startup Sources That Can Be Set in ADGCTRGR and ADGCTRGR2 Registers.

Table 2.75 Comparative Overview of 12-Bit A/D Converters

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Number of units	Three units (S12AD, S12AD1, and S12AD2)	Three units (S12AD, S12AD1, and S12AD2) (For products with a RAM capacity of 64 KB) Two units (S12AD and S12AD2) (For products with a RAM capacity of 48 KB)
Input channels	S12AD: 5 channels S12AD1: 5 channels S12AD2: 12 channels	S12AD: 4 channels S12AD1: 4 channels S12AD2: 14 channels (For products with a RAM capacity of 64 KB) S12AD: 7 channels S12AD2: 8 channels (For products with a RAM capacity of 48 KB)
Extended analog function	Internal reference voltage (S12AD2 only)	Temperature sensor output, internal reference voltage (S12AD2 only)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1 µs per channel (when A/D conversion clock (ADCLK) = 40 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	• Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLK to ADCLK frequency division ratio = 1:1, 1:2, 2:1, 4:1, 8:1 • ADCLK is set by using the clock generation circuit.	• Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Data registers	• 22 registers for analog input (S12AD: 5 registers, S12AD1: 5 registers, S12AD2: 12 registers), one register for A/D-converted data duplication in double trigger mode, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for internal reference (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode • Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• 22 registers for analog input (S12AD: 4 registers, S12AD1: 4 registers, S12AD2: 14 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD2) • One register for internal reference (S12AD2) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode • Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	The operating mode can be set individually for each of three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the internal reference voltage (S12AD2).	The operating mode can be set individually for each of three units. • Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output (S12AD2). — A/D conversion is performed only once on the internal reference voltage (S12AD2).

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Operating modes	• Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Analog inputs arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. — The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.	• Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) — Arbitrarily selected analog input channels, the temperature sensor output (S12AD2), and the internal reference voltage (S12AD2) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) — If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. — The priority order is group A (highest) > group B > group C (lowest). — Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), general purpose PWM timer (GPT), or 8-bit timer (TMR) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units.)	• Software trigger • Synchronous trigger — Trigger by the multi-function timer pulse unit (MTU), general purpose PWM timer (GPTW), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger — A/D conversion can be triggered by the external trigger ADTRG0# (S12AD), ADTRG1# (S12AD1), and ADTRG2# (S12AD2) pins (individually for each of three units.)
Functions	• Channel-dedicated sample-and-hold function (three channels for S12AD1 only) • Variable sampling state count (settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Input signal amplification function using the programmable gain amplifier (1 channel for S12AD and 3 channels for S12AD1)	• Channel-dedicated sample-and-hold function (three channels for S12AD and three channels for S12AD1) (Constant sampling can be set.) • Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Order of channel conversion can be specified for each unit. • Input signal amplification function using the programmable gain amplifier (each unit has 3 channels) (Only for products with a RAM capacity of 64 KB)

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each of 3 units). • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each of 3 units). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (GBADI, GBADI1, or GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (GCADI, GCADI1, or GBADI2) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (GBADI/GCADI, GBADI1/GCADI1, or GBADI2/GCADI2) can be generated on completion of a group B or group C scan. • The S12ADI/S12ADI1/S12ADI2, GBADI/GBADI1/GBADI2, and GCADI/GCADI1/GCADI2 interrupts can activate the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of single scan (individually for each unit.) • In double trigger mode, A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of double scan (individually for each unit). • In group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI, S12GBADI1, or S12GBADI2) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI, S12GCADI1, or S12GCADI2) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI, S12ADI1, or S12ADI2) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI, S12GBADI1/S12GCADI1, or S12GBADI2/S12GCADI2) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPAI2, S12CMPBI, S12CMPBI1, or S12CMPBI2) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1/S12ADI2, S12GBADI/S12GBADI1/S12GBADI2, and S12GCADI/S12GCADI1/ S12GCADI2 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).
Event link function	—	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.

Item	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.76 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
ADDRy	—	A/D data register y (y = 0 to 3, 16: S12AD and S12AD1, y = 0 to 11: S12AD2)	A/D data register y (y = 0 to 3, 16: S12AD and S12AD1, y = 0 to 11: S12AD2)	A/D data register y (y = 0 to 3: S12AD, y = 0 to 3: S12AD1, y = 0 to 11, 16, 17: S12AD2)
ADTSDR	—	—	—	A/D temperature sensor data register
ADCSR	DBLANS[4:0] (S12AD)	Double trigger target channel select bits 00000: AN000 00001: AN001 00010: AN002 00011: AN003 10000: AN016	Double trigger target channel select bits 00000: AN000 00001: AN001 00010: AN002 00011: AN003 10000: AN016	Double trigger target channel select bits 00000: AN000 00001: AN001 00010: AN002 00011: AN003 00100: AN004 00101: AN005 00110: AN006
	DBLANS[4:0] (S12AD1)	Double trigger target channel select bits 00000: AN100 00001: AN101 00010: AN102 00011: AN103 10000: AN116	Double trigger target channel select bits 00000: AN100 00001: AN101 00010: AN102 00011: AN103 10000: AN116	Double trigger target channel select bits 00000: AN100 00001: AN101 00010: AN102 00011: AN103
	DBLANS[4:0] (S12AD2)	Double trigger target channel select bits 00000: AN200 00001: AN201 00010: AN202 00011: AN203 00100: AN204 00101: AN205 00110: AN206 00111: AN207 01000: AN208 01001: AN209 01010: AN210 01011: AN211	Double trigger target channel select bits 00000: AN200 00001: AN201 00010: AN202 00011: AN203 00100: AN204 00101: AN205 00110: AN206 00111: AN207 01000: AN208 01001: AN209 01010: AN210 01011: AN211	Double trigger target channel select bits 00000: AN200 00001: AN201 00010: AN202 00011: AN203 00100: AN204 00101: AN205 00110: AN206 00111: AN207 01000: AN208 01001: AN209 01010: AN210 01011: AN211 10000: AN216 10001: AN217
S12AD. ADANSA0	ANSA004	—	—	A/D conversion channel select bit
	ANSA005	—	—	A/D conversion channel select bit

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
S12AD. ADANSA0	ANSA006	—	—	A/D conversion channel select bit
S12AD. ADANSA1	—	A/D channel select register A1	A/D channel select register A1	—
S12AD1. ADANSA1	—	A/D channel select register A1	A/D channel select register A1	—
S12AD2. ADANSA1	—	—	—	A/D channel select register A1
S12AD. ADANSB0	ANSB004	—	—	A/D conversion channel select bit
	ANSB005	—	—	A/D conversion channel select bit
	ANSB006	—	—	A/D conversion channel select bit
S12AD. ADANSB1	—	A/D channel select register B1	A/D channel select register B1	—
S12AD1. ADANSB1	—	A/D channel select register B1	A/D channel select register B1	—
S12AD2. ADANSB1	—	—	—	A/D channel select register B1
S12AD. ADANSC0	ANSC004	—	—	A/D conversion channel select bit
	ANSC005	—	—	A/D conversion channel select bit
	ANSC006	—	—	A/D conversion channel select bit
S12AD. ADANSC1	—	A/D channel select register C1	A/D channel select register C1	—
S12AD1. ADANSC1	—	A/D channel select register C1	A/D channel select register C1	—
S12AD2. ADANSC1	—	—	—	A/D channel select register C1
ADSCSn	—	—	—	A/D channel conversion order setting register n (n = 0 to 13)
S12AD. ADADS0	ADS004	—	—	A/D-converted value addition/average channel select bit
	ADS005	—	—	A/D-converted value addition/average channel select bit
	ADS006	—	—	A/D-converted value addition/average channel select bit
S12AD. ADADS1	—	A/D-converted value addition/average channel select register 1	A/D-converted value addition/average channel select register 1	—
S12AD1. ADADS1	—	A/D-converted value addition/average channel select register 1	A/D-converted value addition/average channel select register 1	—
S12AD2. ADADS1	—	—	—	A/D-converted value addition/average channel select register 1
ADCER	ASE	—	—	A/D data register automatic setting enable bit

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
ADSTRGR	TRSB[5:0] (RX24T/ RX24U) TRSB[6:0] (RX26T)	A/D conversion start trigger select bits for Group B	A/D conversion start trigger select bits for Group B	A/D conversion start trigger select bits for Group B
	TRSA[5:0] (RX24T/ RX24U) TRSA[6:0] (RX26T)	A/D conversion start trigger select bits	A/D conversion start trigger select bits	A/D conversion start trigger select bits
ADEXICR	TSSAD	—	—	Temperature sensor output A/D-converted value addition/average mode select bit
	TSSA	—	—	Temperature sensor output A/D conversion select bit
	TSSB	—	—	Group B temperature sensor output A/D conversion select bit
	OCSB	—	—	Group B internal reference voltage A/D conversion select bit
ADGCEXCR	—	—	—	A/D group C extended input control register
ADGCTRGR2	—	—	—	A/D group C trigger select register 2
ADSSTRn	—	A/D sampling state register n (n = 0 to 11, L, O)	A/D sampling state register n (n = 0 to 11, L, O)	A/D sampling state register n (n = 0 to 11, L, T, O)
		Initial value after a reset differs.		
ADSHCR	—	A/D sample and hold circuit control register	A/D sample and hold circuit control register	A/D sample and hold circuit control register
		Initial value after a reset differs.		
ADSHCR	SSTSH[7:0]	These bits set a sampling time in the range from 4 to 255 state cycles.	These bits set a sampling time in the range from 4 to 255 state cycles.	These bits set a sampling time between 12 and 252 clock cycles.
ADSHCR	SHANS[2:0] (RX24T/ RX24U) SHANS[0] SHANS[1] SHANS[2] (RX26T)	Channel-dedicated sample and hold circuit bypass select bits Whether to use the channel-dedicated sample & hold circuit for AN100 to AN102 or bypass it without using it can be selected. 0: The channel-dedicated sample and hold circuit is bypassed. 1: The channel-dedicated sample and hold circuit is used.	Channel-dedicated sample and hold circuit bypass select bits Whether to use the channel-dedicated sample & hold circuit for AN100 to AN102 or bypass it without using it can be selected. 0: The channel-dedicated sample and hold circuit is bypassed. 1: The channel-dedicated sample and hold circuit is used.	Channel-dedicated sample and hold circuit bypass select bits Whether to use the channel-dedicated sample & hold circuit for AN000 or AN100 channel/AN001 or AN101 channel/AN002 or AN102 channel or bypass it without using it can be selected. 0: The channel-dedicated sample and hold circuit is disabled. 1: The channel-dedicated sample and hold circuit is enabled.
ADSHMSR	—	—	—	A/D sample and hold operating mode select register

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
ADDISCR	—	Disconnection detection assist setting bits ADNDIS[4]: Discharge or precharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Discharge or precharge period b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 0 to 1 1 1 1: Number of states in precharge/discharge period Settings other than the above are prohibited.	Disconnection detection assist setting bits ADNDIS[4]: Discharge or precharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0]: Discharge or precharge period b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 0 to 1 1 1 1: Number of states in precharge/discharge period Settings other than the above are prohibited.	Disconnection detection assist setting bits ADNDIS[4] Discharge or precharge selection b4 0: Discharge 1: Precharge ADNDIS[3:0] The discharge/precharge period is specified by the number of ADCLK clock cycles. b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 1: Charge period of 3 clock cycles 0 1 1 0: Charge period of 6 clock cycles 1 0 0 1: Charge period of 9 clock cycles 1 1 0 0: Charge period of 12 clock cycles 1 1 1 1: Charge period of 15 clock cycles Settings other than the above are prohibited.
ADELCCR	—	—	—	A/D event link control register
ADCMPCR	—	—	—	A/D compare function control register
ADCMPANSR0	—	—	—	A/D compare function window A channel select register 0
ADCMPANSR1	—	—	—	A/D compare function window A channel select register 1
ADCMPANSER	—	—	—	A/D compare function window A extended input select register
ADCMPLR0	—	—	—	A/D compare function window A compare condition setting register 0
ADCMPLR1	—	—	—	A/D compare function window A compare condition setting register 1
ADCMPLER	—	—	—	A/D compare function window A extended input compare condition setting register
ADCMPDR0	—	—	—	A/D compare function window A lower level setting register

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
ADCMPDR1	—	—	—	A/D compare function window A upper level setting register
ADCMPSR0	—	—	—	A/D compare function window A channel status register 0
ADCMPSR1	—	—	—	A/D compare function window A channel status register 1
ADCMPSER	—	—	—	A/D compare function window A extended input channel status register
ADWINMON	—	—	—	A/D compare function window A/B status monitoring register
ADCMPBNSR	—	—	—	A/D compare function window B channel select register
ADWINLLB	—	—	—	A/D compare function window B lower level setting register
ADWINULB	—	—	—	A/D compare function window B upper level setting register
ADCMPBSR	—	—	—	A/D compare function window B channel status register
S12AD. ADPGACR	—	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register
		Initial value after a reset differs.		
	P000SEL1	PGA P000 amplifier pass-through enable bit	PGA P000 amplifier pass-through enable bit	—
	P000ENAMP	PGA P000 amplifier enable bit	PGA P000 amplifier enable bit	—
	P000CR[3:0]	—	—	P000 amplifier control bits
	P001CR[3:0]	—	—	P001 amplifier control bits
	P002CR[3:0]	—	—	P002 amplifier control bits
S12AD1. ADPGACR	—	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register	A/D programmable gain amplifier control register
		Initial value after a reset differs.		
S12AD1. ADPGACR	P100SEL1	PGA P100 amplifier pass-through enable bit	PGA P100 amplifier pass-through enable bit	—
	P100ENAMP	PGA P100 amplifier enable bit	PGA P100 amplifier enable bit	—
	P100CR[3:0]	—	—	P100 amplifier control bits
	P101SEL1	PGA P101 amplifier pass-through enable bit	PGA P101 amplifier pass-through enable bit	—
	P101ENAMP	PGA P101 amplifier enable bit	PGA P101 amplifier enable bit	—
	P101CR[3:0]	—	—	P101 amplifier control bits
	P102SEL1	PGA P102 amplifier pass-through enable bit	PGA P102 amplifier pass-through enable bit	—
	P102ENAMP	PGA P102 amplifier enable bit	PGA P102 amplifier enable bit	—
	P102CR[3:0]	—	—	P102 amplifier control bits

Register	Bit	RX24T (S12ADF)	RX24U (S12ADF)	RX26T (S12ADHa)
S12AD. ADPGAGS0	P000GAIN [3:0]	PGA P000 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than the above are prohibited.	PGA P000 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333 Settings other than the above are prohibited.	P000 amplifier gain setting bits b3 b0 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited.
	P001GAIN [3:0]	—	—	P001 amplifier gain setting bits
	P002GAIN [3:0]	—	—	P002 amplifier gain setting bits
S12AD1. ADPGAGS0	P100GAIN [3:0] P101GAIN [3:0] P102GAIN [3:0]	PGA P100/ PGA P101/ PGA P102 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 Settings other than the above are prohibited.	PGA P100/ PGA P101/ PGA P102 gain setting bits The relationship between each setting and the amplification factor (gain) is as follows: 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 1 0 0: × 3.077 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333 Settings other than the above are prohibited.	P100/ P101 /P102 amplifier gain setting bits 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 1: × 3.077 0 1 0 1: × 3.636 0 1 1 0: × 4.000 0 1 1 1: × 4.444 1 0 0 0: × 5.000 1 0 1 0: × 6.667 1 0 1 1: × 8.000 1 1 0 0: × 10.000 1 1 0 1: × 13.333 1 1 1 0: × 20.000 Settings other than the above are prohibited.
ADVMONCR	—	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	—	A/D internal reference voltage monitoring circuit output enable register

Table 2.77 Comparative Listing of A/D Conversion Startup Sources That Can Be Set in ADSTRGR Register

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
TRSB[5:0] (RX24T/ RX24U) TRSB[6:0] (RX26T)	A/D conversion start trigger select bits for Group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	A/D conversion start trigger select bits for Group B b6 b0 0111111: Trigger source deselection state 1111111: Trigger source deselection state 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N 0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
TRSB[5:0] (RX24T/ RX24U) TRSB[6:0] (RX26T)		1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N 1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N 1010011: GTADTRB7N 1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N 0011101: TMTRG0AN_0 0011110: TMTRG0AN_1 0011111: TMTRG0AN_2 0100000: TMTRG0AN_3 0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3
TRSA[5:0] (RX24T/ RX24U) TRSA[6:0] (RX26T)	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N	A/D conversion start trigger select bits b14 b8 0111111: Trigger source deselection state 1111111: Trigger source deselection state 0000000: ADTRGn# 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
TRSA[5:0] (RX24T/ RX24U) TRSA[6:0] (RX26T)	0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N 1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N 1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N 1010011: GTADTRB7N 1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N 0011101: TMTRG0AN_0 0011110: TMTRG0AN_1 0011111: TMTRG0AN_2 0100000: TMTRG0AN_3 0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

Table 2.78 Listing of A/D Conversion Startup Sources That Can Be Set in ADGCTRGR and ADGCTRGR2 Registers

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
TRSC[5:0] (RX24T/ RX24U) TRSC[5:0], TRSC6 (RX26T)	A/D conversion start trigger select bits for Group C b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 0 1 1 0: TRGA6N 0 0 0 1 1 1: TRGA7N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN 0 0 1 1 0 1: TRG7AN 0 0 1 1 1 0: TRG7BN 0 0 1 1 1 1: TRG7AN or TRG7BN 0 1 0 0 0 0: TRG7ABN 0 1 0 0 1 1: TRGA9N 0 1 0 1 0 0: TRG9N 0 1 1 0 0 1: TRGA0N or TRG0N 0 1 1 0 1 0: TRGA9N or TRG9N 0 1 1 0 1 1: TRGA0N or TRGA9N 0 1 1 1 0 0: TRG0N or TRG9N 0 1 1 1 0 1: TMTRG0AN_0 0 1 1 1 1 0: TMTRG0AN_1 0 1 1 1 1 1: TMTRG0AN_2 1 0 0 0 0 0: TMTRG0AN_3 1 0 0 0 0 1: TRG9AEN 1 0 0 0 1 0: TRG0AEN 1 0 0 0 1 1: TRGA09N 1 0 0 1 0 0: TRG09N 1 1 0 0 1 0: GTADTRA0N 1 1 0 0 1 1: GTADTRB0N 1 1 0 1 0 0: GTADTRA1N 1 1 0 1 0 1: GTADTRB1N 1 1 0 1 1 0: GTADTRA2N 1 1 0 1 1 1: GTADTRB2N 1 1 1 0 0 0: GTADTRA3N 1 1 1 0 0 1: GTADTRB3N 1 1 1 0 1 0: GTADTRA0N or GTADTRB0N 1 1 1 0 1 1: GTADTRA1N or GTADTRB1N 1 1 1 1 0 0: GTADTRA2N or GTADTRB2N 1 1 1 1 0 1: GTADTRA3N or GTADTRB3N	A/D conversion start trigger select bits for Group C A/D conversion start trigger select bit 6 for Group C b6 b0 0111111: Trigger source deselection state 1111111: Trigger source deselection state 0000001: TRGA0N 0000010: TRGA1N 0000011: TRGA2N 0000100: TRGA3N 0000101: TRGA4N 0000110: TRGA6N 0000111: TRGA7N 0001000: TRG0N 0001001: TRG4AN 0001010: TRG4BN 0001011: TRG4AN or TRG4BN 0001100: TRG4ABN 0001101: TRG7AN 0001110: TRG7BN 0001111: TRG7AN or TRG7BN 0010000: TRG7ABN 0010011: TRGA9N 0010100: TRG9N 0011001: TRGA0N or TRG0N 0011010: TRGA9N or TRG9N 0011011: TRGA0N or TRGA9N 0011100: TRG0N or TRG9N 0100001: TRG9AEN 0100010: TRG0AEN 0100011: TRGA09N 0100100: TRG09N 1000000: GTADTRA0N 1000001: GTADTRB0N 1000010: GTADTRA1N 1000011: GTADTRB1N 1000100: GTADTRA2N 1000101: GTADTRB2N 1000110: GTADTRA3N 1000111: GTADTRB3N 1001000: GTADTRA0N or GTADTRB0N 1001001: GTADTRA1N or GTADTRB1N 1001010: GTADTRA2N or GTADTRB2N 1001011: GTADTRA3N or GTADTRB3N

Bit	RX24T (S12ADF)/RX24U (S12ADF)	RX26T (S12ADHa)
TRSC[5:0] (RX24T/ RX24U) TRSC[5:0], TRSC6 (RX26T)		1001100: GTADTRA4N 1001101: GTADTRB4N 1001110: GTADTRA5N 1001111: GTADTRB5N 1010000: GTADTRA6N 1010001: GTADTRB6N 1010010: GTADTRA7N 1010011: GTADTRB7N 1010100: GTADTRA4N or GTADTRB4N 1010101: GTADTRA5N or GTADTRB5N 1010110: GTADTRA6N or GTADTRB6N 1010111: GTADTRA7N or GTADTRB7N 0011101: TMTRG0AN_0 0011110: TMTRG0AN_1 0011111: TMTRG0AN_2 0100000: TMTRG0AN_3 0110010: ELCTRG00N*1 ELCTRG10N*2 ELCTRG20N*3 0110011: ELCTRG01N*1 ELCTRG11N*2 ELCTRG21N*3 0111010: ELCTRG00N or ELCTRG01N*1 ELCTRG10N or ELCTRG11N*2 ELCTRG20N or ELCTRG21N*3

Notes: 1. Unit 0
2. Unit 1
3. Unit 2

2.27 D/A Converter and 12-Bit D/A Converter

Table 2.79 is Comparative Overview of D/A Converters, and Table 2.80 is Comparison of D/A Converter Registers.

Table 2.79 Comparative Overview of D/A Converters

Item	RX24T (DA, DAa)	RX24U (DAa)	RX26T (R12DAb)
Resolution	8 bits	8 bits	12 bits
Output channels	[In case of chip version A] 1 channel [In case of chip version B] 2 channels	2 channels	2 channels
Measure against interference between analog modules	• Measure against interference between D/A and A/D converters: — D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 8-bit D/A converter inrush current with the enable signal.	• Measure against interference between D/A and A/D converters: — D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 8-bit D/A converter inrush current with the enable signal.	• Measure against interference between D/A and A/D converters: — D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter (unit 2). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	—	—	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	—	—	Output to external pins and to comparator C can be controlled independently.

Table 2.80 Comparison of D/A Converter Registers

Register	Bit	RX24T (DA, DAa)	RX24U (DAa)	RX26T (R12DAb)
DACR	DAE	—	—	D/A enable bit
DAADSCR*1	DAADST	D/A A/D synchronous conversion bit 0: The 8-bit D/A converter does not perform conversion in synchronization with the 12-bit A/D converter (unit 2) (to disable the measure against interference between D/A and A/D conversion). 1: The 8-bit D/A converter performs conversion in synchronization with the 12-bit A/D converter (unit 2) (to enable the measure against interference between D/A and A/D conversion).	D/A A/D synchronous conversion bit 0: The 8-bit D/A converter does not perform conversion in synchronization with the 12-bit A/D converter (unit 2) (to disable the measure against interference between D/A and A/D conversion). 1: The 8-bit D/A converter performs conversion in synchronization with the 12-bit A/D converter (unit 2) (to enable the measure against interference between D/A and A/D conversion).	D/A A/D synchronous conversion bit 0: The 12-bit D/A converter does not perform conversion in synchronization with the 12-bit A/D converter (unit 2) (to disable the measure against interference between D/A and A/D conversion). 1: The 12-bit D/A converter performs conversion in synchronization with the 12-bit A/D converter (unit 2) (to enable the measure against interference between D/A and A/D conversion).
DADSELR	—	—	—	D/A destination select register

Note: 1. Implemented only on chip version B on the 24T Group.

2.28 Comparator C

Table 2.81 is Comparative Overview of Comparator C Modules, and Table 2.82 is Comparison of Comparator C Registers.

Table 2.81 Comparative Overview of Comparator C Modules

Item	RX24T (CMPC)	RX24U (CMPC)	RX26T (CMPCa)
Number of channels	4 channels (comparator C0 to comparator C3)	4 channels (comparator C0 to comparator C3)	6 channels (comparator C0 to comparator C5)
Analog input voltage	• Input voltage to CMPCnm pin (n = channel number, m = 0 to 3)	• Input voltage to CMPCnm pin (n = channel number, m = 0 to 3)	• Input voltage on CMPCnm pin (n = channel number, m = 0 to 3)
Reference input voltage	[In case of chip version A] • Input voltage on CVREFC0/CVREFC1 pin or output voltage from on-chip D/A converter 0 [In case of chip version B] • Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	• Output voltage from on-chip D/A converter 0 or on-chip D/A converter 1	• Input voltage from CVREFC0/CVREFC1 pin, output voltage from on-chip D/A converter 0, or output voltage from on-chip D/A converter 1 • Input voltage from CVREFC0/CVREFC1 pin, output voltage from on-chip D/A converter 0, or output voltage from on-chip D/A converter 1
Comparison result	The comparison result can be output externally.	The comparison result can be output externally.	The comparison result can be output externally.
Digital filter function	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate the interrupt request output, POE source output, and GPT internal trigger source output, and the signal can be used to read the comparison result via registers.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output, event output to the ELC, and POE cause output*1, and comparison results can be read from registers.
Interrupt request signal	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected.	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state	Ability to transition to module stop state

Note: 1. The POE only uses the level detection signal, and the POEG uses the level detection and edge detection signals

Table 2.82 Comparison of Comparator C Registers

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX26T (CMPCa)
CMPSEL0	CMPSEL[3:0]	Comparator input select bits • For Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. 0 0 1 0: CMPC31 is selected. 0 1 0 0: CMPC32 is selected. 1 0 0 0: CMPC33 is selected. Settings other than the above are prohibited.	Comparator input select bits • For Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. 0 0 1 0: CMPC31 is selected. 0 1 0 0: CMPC32 is selected. 1 0 0 0: CMPC33 is selected. Settings other than the above are prohibited.	Comparator input select bits • For Comparator C0 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC00 is selected. 0 0 1 0: CMPC01 is selected. 0 1 0 0: CMPC02 is selected. 1 0 0 0: CMPC03 is selected. Settings other than the above are prohibited. • For Comparator C1 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC10 is selected. 0 0 1 0: CMPC11 is selected. 0 1 0 0: CMPC12 is selected. 1 0 0 0: CMPC13 is selected. Settings other than the above are prohibited. • For Comparator C2 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC20 is selected. 0 0 1 0: CMPC21 is selected. 0 1 0 0: CMPC22 is selected. 1 0 0 0: CMPC23 is selected. Settings other than the above are prohibited. • For Comparator C3 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC30 is selected. 0 0 1 0: CMPC31 is selected. 0 1 0 0: CMPC32 is selected. 1 0 0 0: CMPC33 is selected. Settings other than the above are prohibited.

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX26T (CMPCa)
CMPSEL0	CMPSEL[3:0]			• For Comparator C4 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC40 is selected. 0 0 1 0: CMPC41 is selected. 0 1 0 0: CMPC42 is selected. 1 0 0 0: CMPC43 is selected. Settings other than the above are prohibited. • For Comparator C5 b3 b0 0 0 0 0: No input 0 0 0 1: CMPC50 is selected. 0 0 1 0: CMPC51 is selected. 0 1 0 0: CMPC52 is selected. 1 0 0 0: CMPC53 is selected. Settings other than the above are prohibited.
CMPSEL1	CVRS[1:0] (RX24T/ RX24U) CVRS[3:0] (RX26T)	Reference input voltage select bits [In case of chip version A] • For Comparator C1 to C3 b1 b0 0 0: No input 0 1: CVREFC1 input is selected for the reference input voltage. 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. Settings other than the above are prohibited. • For Comparator C0 b1 b0 0 0: No input 0 1: CVREFC0 input is selected for the reference input voltage. 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. Settings other than the above are prohibited.	Reference input voltage select bits	Reference input voltage select bits b3 b0 0 0 0 0: No input 0 0 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 0 0 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. 0 1 0 0: CVREFC1 input is selected for the reference input voltage. 1 0 0 0: CVREFC0 input is selected for the reference input voltage. Settings other than the above are prohibited.

Register	Bit	RX24T (CMPC)	RX24U (CMPC)	RX26T (CMPCa)
CMPSEL1	CVRS[1:0] (RX24T/ RX24U) CVRS[3:0] (RX26T)	[In case of chip version B] b1 b0 0 0: No input 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. Settings other than the above are prohibited.	b1 b0 0 0: No input 0 1: Output of on-chip D/A converter 1 is selected for the reference input voltage. 1 0: Output of on-chip D/A converter 0 is selected for the reference input voltage. Settings other than the above are prohibited.	
CMPCTL2	—	—	—	Comparator control register 2

2.29 Data Operation Circuit

Table 2.83 is Comparative Overview of Data Operation Circuits, and Table 2.84 is Comparison of Data Operation Circuit Registers.

Table 2.83 Comparative Overview of Data Operation Circuits

Item	RX24T (DOC)/RX24U (DOC)	RX26T (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32-bit data
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh • The result of data subtraction is less than 0000h	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	—	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.84 Comparison of Data Operation Circuit Registers

Register	Bit	RX24T (DOC)/RX24U (DOC)	RX26T (DOCA)
DOCR	DCSEL (RX24T/ RX24U) DCSEL[2:0] (RX26T)	Detection condition select bit b2 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPSZ	—	Data operation size select bit
	DOPCIE	Data operation circuit interrupt enable bit (b4)	Data operation circuit interrupt enable bit (b7)
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register DODIR is a 16-bit register.	DOC data input register DODIR is a 32-bit register.
DODSR	—	DOC data setting register	—
DODSR0	—	—	DOC data setting register 0
DODSR1	—	—	DOC data setting register 1

2.30 RAM

Table 2.85 is Comparative Overview of RAMs, and Table 2.86 is Comparison of RAM Registers.

Table 2.85 Comparative Overview of RAMs

Item	RX24T	RX24U	RX26T
RAM capacity	Maximum 32 KB (RAM0: 32 KB)	32 KB (RAM0: 32 KB)	64 KB
RAM address	• For RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • For RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh	RAM0: 0000 0000h to 0000 7FFFh	• For products with a RAM capacity of 64 KB: 0000 0000h to 0000 FFFFh • For products with a RAM capacity of 48 KB: 0000 0000h to 0000 BFFFh
Memory buses	Memory bus 1	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Low power consumption function	The module stop state is selectable for RAM0.	The module stop state is selectable for RAM0.	Ability to transition to module stop state
Error checking	—	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Table 2.86 Comparison of RAM Registers

Register	Bit	RX24T/RX24U	RX26T
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.31 Flash Memory

Table 2.87 is Comparative Overview of Flash Memories, and Table 2.88 is Comparison of Flash Memory Registers.

Table 2.87 Comparative Overview of Flash Memories

Item		RX24T	RX24U	RX26T
Common	Programming/ erasing method	• The following software commands are implemented: — Program, blank check, block erase, all-block erase	• The following software commands are implemented: — Program, blank check, block erase, all-block erase	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).
	Security function	Protects against illicit tampering with or reading of data in flash memory.	Protects against illicit tampering with or reading of data in flash memory.	Protects against illicit tampering with or reading of data in flash memory.
	Protection function	Protects against erroneous programming of the flash memory. (Protection by software protection, start-up program protection, and area protection)	Protects against erroneous programming of the flash memory. (Protection by software protection, start-up program protection, and area protection)	Protects against erroneous programming of the flash memory. (Protection by software protection, error protection, start-up program protection, and area protection)
	Background operation (BGO) function	Programs in the ROM area can run while the E2 DataFlash is being programmed or erased.	Programs in the ROM area can run while the E2 DataFlash is being programmed or erased.	• Code flash memory can be read while it is being programmed or erased. • Data flash memory can be read while code flash memory is being programmed or erased. • Code flash memory can be read while data flash memory is being programmed or erased.
	Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.

Item		RX24T	RX24U	RX26T
Common	On-board programming (serial programming and self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are programmable. • Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. • Self-programming in single-chip mode — The user area and data area are programmable using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are programmable. • Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. • Self-programming in single-chip mode — The user area and data area are programmable using a flash programming routine in a user program.	• Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. • Programming/erasure in boot mode (FINE interface) — FINE is used. • Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.
	Unique ID	A unique 16-byte ID code is provided for each MCU.	A unique 16-byte ID code is provided for each MCU.	A unique 12-byte ID code is provided for each MCU.
ROM (RX24T/ RX24U) Code flash memory (RX26T)	Memory capacity	• User area: Max. 512 KB	• User area: Max. 512 KB	• Max. 512 KB
	Address	• Products with capacity of 512 KB: — FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: — FFFA 0000h to FFFF FFFFh	• Products with capacity of 512 KB: — FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: — FFFA 0000h to FFFF FFFFh	• Products with capacity of 512 KB: Linear mode — FFF8 0000h to FFFF FFFFh Dual mode (when BANKSEL. BANKSWP[2:0] = 111b) — Bank 1: FFF8 0000h to FFFB FFFFh — Bank 0: FFFC 0000h to FFFF FFFFh

Item		RX24T	RX24U	RX26T
ROM (RX24T/ RX24U) Code flash memory (RX26T)	Address	• Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh	• Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh	• Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh
	ROM cache	• Capacity: 2 KB	• Capacity: 2 KB	—
	Read cycle	• No ROM wait cycles when ICLK ≤ 32 MHz • ROM wait cycle when ICLK > 32 MHz	• No ROM wait cycles when ICLK ≤ 32 MHz • ROM wait cycle when ICLK > 32 MHz	One cycle
	Value after erasure	FFh	FFh	FFh
	Dual bank function	—	—	The dual bank configuration allows safe updating even upon interruption during a rewrite operation. • Linear mode: In this mode, code flash memory is used as a single area. • Dual mode: In this mode, code flash memory is used as two separate areas.
	Trusted Memory (TM) function	—	—	Protects against illicit reading in code flash memory. • Linear mode: Blocks 8 and 9 • Dual mode: Blocks 8, 9, 30, and 31
	Units of programming and erasure	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Units of programming for the user area: 8 bytes • Units of erasure for the user area: Block units	• Programming: 128 bytes • Erasure: Block units
	Off-board programming (programming and erasure using a parallel programmer)	The user area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	The user area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	—

Item		RX24T	RX24U	RX26T
E2 DataFlash (RX24T/ RX24U) Data flash memory (RX26T)	Memory capacity	• Data area: 8 KB	• Data area: 8 KB	• 16 KB
	Address	0010 0000h to 0010 1FFFh	0010 0000h to 0010 1FFFh	0010 0000h to 0010 3FFFh
	Read cycle	—	—	16-bit or 8-bit read access requires 8 FCLK clock cycles.
	Value after erasure	FFh	FFh	Undefined
	Units of programming and erasure	• Programming the data area: 1-byte units • Erasing the data area: block units	• Programming the data area: 1-byte units • Erasing the data area: block units	• Programming: 4-byte units • Erasure: block units
	Off-board programming (programming and erasure using a parallel programmer)	The data area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	The data area is rewritable using a flash programmer (serial programmer or parallel programmer) compatible with this MCU.	—

Table 2.88 Comparison of Flash Memory Registers

Register	Bit	RX24T/RX24U	RX26T
FWEPROR	—	—	Flash P/E protect register
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR	—	—	Flash status register
FENTRYR	—	—	Flash P/E mode entry register
FSUINITR	—	—	Flash sequencer set-up initialization register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FAWMON	—	—	Flash access window monitor register
FCPSR	—	—	Flash sequencer processing switching register
FPCKAR	—	—	Flash sequencer processing clock notification register
FSUACR	—	—	Start-up area control register
DFLCTL	—	E2 DataFlash control register	—
FENTRYR	—	Flash P/E mode entry register	—
FPR	—	Protection unlock register	—
FPSR	—	Protection unlock status register	—

Register	Bit	RX24T/RX24U	RX26T
FPMCR	—	Flash P/E mode control register	—
FISR	—	Flash initial setting register	—
FRESETR	—	Flash reset register	—
FASR	—	Flash area select register	—
FCR	—	Flash control register	—
FEXCR	—	Flash extra area control register	—
FSARH	—	Flash processing start address register H	—
FSARL	—	Flash processing start address register L	—
FEARH	—	Flash processing end address register H	—
FEARL	—	Flash processing end address register L	—
FWBn	—	Flash write buffer n register (n = 0 to 3)	—
FSTATR0	—	Flash status register 0	—
FSTATR1	—	Flash status register 1	—
FEAMH	—	Flash error address monitor register H	—
FEAML	—	Flash error address monitor register L	—
FSCMR	—	Flash start-up setting monitor register	—
FAWSMR	—	Flash access window start address monitor register	—
FAWEMR	—	Flash access window end address monitor register	—
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache disable register	—

2.32 Packages

As indicated in Table 2.89, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.89 Packages

Package Type	RENESAS Code		
	RX24T	RX24U	RX26T
144-pin LFQFP	×	○	×
80-pin LQFP	○	×	×
80-pin LFQFP	○	×	○
64-pin LQFP	○	×	×
64-pin LFQFP	○	×	○
64-pin HWQFN	×	×	○
48-pin LFQFP	×	×	○
48-pin HWQFN	×	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. Black text indicates there is no differences in the item's specifications between groups.

3.1 100-Pin LFQFP Package (RX24T: Chip Version A)

Table 3.1 is Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version A).

Table 3.1 Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version A)

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
1	PE5/IRQ0	PE5/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK009/ CTS009#/RTS009#/SS009#/TXDB009/IRQ0/ ADST0
2	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
3	VSS	VSS
4	P00/IRQ2/ADST1	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED/PN6
7	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/SCK009/TXDB009/IRQ1
9	PE3/MTCLKD/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/CTS009#/RTS009#/SS009#/ DE009/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
16	PE1/MTIOC9D/TMO5/CTS5#/RTS5#/SS5#/ SSLA3	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/CTS12#/RTS12#/SS12#/ SSLA3/SSL03/IRQ15
17	PE0/MTIOC9B/TMCI1/TMCI5/SSLA2	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ GTIV/RXD5/SMISO5/SSCL5/SSLA2/SSL02/ CRX0/IRQ7

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
18	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/SCK009/TXD008/TXDA008/SMOSI008/SSDA008/TXDB009/SSLA1/SSL01/CTX0/IRQ8
19	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTIW/CTS1#/RTS1#/SS1#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/DE011/SSLA0/SSL00/IRQ5/ADST0
20	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/TMRI0/TMRI6/GTIOC1A/GTETRGA/GTIOC1A#/GTIOC7A/RXD1/SMISO1/SSCL1/RXD011/SMISO011/SSCL011/SSL00/IRQ6
21	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/GTETRGB/GTIOC1B#/SCK1/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SCK011/TXDB011/SSL02/IRQ2
22	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/GTIOC2A#/GTIOC7B/TXD1/SMOSI1/SSDA1/TXD011/TXDA011/SMOSI011/SSDA011/MOSI0
23	PD2/TMCI1/TMO4/SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/GTIOC2B#/GTIOC0A#/SCK5/SCK008/TXDB008/MOSIA/MOSI0
24	PD1/TMO2/MISOA	PD1/TMO2/GTIOC3A/GTIOC0B/GTIOC3A#/GTIOC0B#/RXD008/SMISO008/SSCL008/MISOA/MISO0
25	PD0/TMO6/RSPCKA	PD0/TMO6/GTIOC3B/GTIOC1A/GTIOC3B#/GTIOC1A#/TXD008/TXDA008/SMOSI008/SSDA008/RSPCKA/RSPCK0
26	PB7/SCK5	PB7/GTIOC1B/GTIOC1B#/SCK5/SCK12/SCK011/TXDB011/SSL03
27	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/RXD12/SMISO12/SSCL12/RXDX12/RXD011/SMISO011/SSCL011/MISO0/CRX0/IRQ2
28	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD011/TXDA011/SMOSI011/SSDA011/RSPCK0/CTX0
29	VCC	VCC
30	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTCPPO0/CTS5#/RTS5#/SS5#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/SCK011/TXDB011/MISOA/SSL01/CRX0/IRQ3
31	VSS	VSS

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
32	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
33	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
34	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
35	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
36	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
37	PA4/MTIOC1B/TMCI7/SCK6/RSPCKA/ ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD008/TXDA008/SMOSI008/SSDA008/ RSPCKA/RSPCK0/ADTRG0#
38	PA3/MTIOC2A/TMRI7/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
39	PA2/MTIOC2B/TMO7/CTS6#/RTS6#/SS6#/ SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/RXD009/ SMISO009/SSCL009/SSLA1/SSL01
40	PA1/MTIOC6A/TMO4/SSLA2/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/GTCPPO4/ TXD009/TXDA009/SMOSI009/SSDA009/ RXD011/SMISO011/SSCL011/SSLA2/ SSL02/CRX0/IRQ14/ADTRG0#
41	PA0/MTIOC6C/TMO2/SSLA3	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/RSPCK0/ IRQ4
44	VSS	VSS
45	P95/MTIOC6B	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
46	P94/MTIOC7A	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
47	P93/MTIOC7B	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
48	P92/MTIOC6D	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
49	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
50	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
51	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
52	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
53	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
54	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
55	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
56	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
57	P70/POE0#/IRQ5	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
58	P33/MTIOC3A/MTCLKA/TMO0/SSLA3	P33/MTIOC3A/MTCLKA/MTIOC3A#/ MTCLKA#/TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/GTCPPO0/SSLA3/ SSL03/IRQ13
59	P32/MTIOC3C/MTCLKB/TMO6/SSLA2	P32/MTIOC3C/MTCLKB/MTIOC3C#/ MTCLKB#/TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#/SSLA2/SSL02/IRQ12
60	VCC	VCC
61	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
62	VSS	VSS

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
63	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
64	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
65	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ CTS008#/RTS008#/SS008#/SCK008/DE008/ RSPCKA/RSPCK0/IRQ4/COMP0
66	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
68	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
69	P65/AN205	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22/CVREFC1
80	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12/CVREFC0
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003

100-Pin LFQFP	RX24T (Chip Version A)	RX26T
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/TMO4/SCK6	P82/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/ IRQ3/COMP5
97	P81/MTIC5V/TMCI4/TXD6/SMOSI6/SSDA6	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/TMRI4/RXD6/SMISO6/SSCL6	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
100	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.2 100-Pin LFQFP Package (RX24T: Chip Version B)

Table 3.2 is Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version B).

Table 3.2 Comparative Listing of 100-Pin LFQFP Package Pin Functions (RX24T: Chip Version B)

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
1	PE5/IRQ0	PE5/MTIOC9D/MTIOC9D#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/SCK009/ CTS009#/RTS009#/SS009#/TXDB009/IRQ0/ ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/ SS1#/IRQ5/ADST0	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
3	VSS	VSS
4	P00/IRQ2/ADST1	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009/SMISO009/SSCL009/IRQ2/ADST1/ COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED/PN6
7	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009/TXDA009/ SMOSI009/SSDA009/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/SCK009/TXDB009/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/CTS009#/RTS009#/SS009#/ DE009/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/SSLA3	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/ RTS5#/SS5#/CTS12#/RTS12#/SS12#/ SSLA3/SSL03/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ RXD5/SMISO5/SSCL5/SSLA2	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/ GTIV/RXD5/SMISO5/SSCL5/SSLA2/SSL02/ CRX0/IRQ7
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/ SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/SSLA0/ IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/IRQ3	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	PD1/TMO2/GTIOC3A/GTIOC0B/GTIOC3A#/ GTIOC0B#/RXD008/SMISO008/SSCL008/ MISOA/MISO0
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	PD0/TMO6/GTIOC3B/GTIOC1A/GTIOC3B#/ GTIOC1A#/TXD008/TXDA008/SMOSI008/ SSDA008/RSPCKA/RSPCK0
26	PB7/GTIOC1B/GTIOC1B#/SCK5	PB7/GTIOC1B/GTIOC1B#/SCK5/SCK12/ SCK011/TXDB011/SSL03
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
29	VCC	VCC
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD008/TXDA008/SMOSI008/SSDA008/ RSPCKA/RSPCK0/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/RXD009/ SMISO009/SSCL009/SSLA1/SSL01
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/GTCPPO4/ TXD009/TXDA009/SMOSI009/SSDA009/ RXD011/SMISO011/SSCL011/SSLA2/ SSL02/CRX0/IRQ14/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/RSPCK0/ IRQ4
44	VSS	VSS
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
57	P70/POE0#/IRQ5	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/MTIOC3A/MTCLKA/MTIOC3A#/ MTCLKA#/TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/GTCPPO0/SSLA3/ SSL03/IRQ13
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/MTIOC3C/MTCLKB/MTIOC3C#/ MTCLKB#/TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#/SSLA2/SSL02/IRQ12
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
64	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
65	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ CTS008#/RTS008#/SS008#/SCK008/DE008/ RSPCKA/RSPCK0/IRQ4/COMP0
66	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/CTX0/IRQ11/COMP1
67	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
68	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
69	P65/AN205	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
70	P64/AN204	P65/IRQ9/AN211/CMPC53/DA1
71	AVCC2	P64/IRQ8/AN210/CMPC33/DA0
72	VREF	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/IRQ6/AN208/CMPC43
76	P61/AN201/IRQ5	P61/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22/CVREFC1
80	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12/CVREFC0
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P51/AN207	P51/AN205/CMPC52
83	P50/AN206	P50/AN204/CMPC42
84	P47/AN103	P47/AN103
85	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
86	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
87	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
88	P43/AN003	P43/AN003
89	P42/AN002	P42/AN002/CMPC20/CMPC21
90	P41/AN001	P41/AN001/CMPC10/CMPC11
91	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0

100-Pin LFQFP	RX24T (Chip Version B)	RX26T
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/SMISO6/SSCL6/RXD12/SMISO12/SSCL12/RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/MTCLKC#/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/MTCLKC#/TMO3/POE9#/MTIOC9D/GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/GTCPPO0/TOC3/SCK009/SCK008/TXDB009/IRQ1
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/MTCLKD#/TMRI3/POE12#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/GTIV/TIC3/CTS6#/RTS6#/SS6#/TXD009/TXDA009/SMOSI009/SSDA009/IRQ0

3.3 100-Pin LFQFP Package (RX24U)

Table 3.3 is Comparative Listing of 100-Pin Package Pin Functions (RX24U).

Table 3.3 Comparative Listing of 100-Pin Package Pin Functions (RX24U)

100-Pin LFQFP	RX24U	RX26T
1	PE5/IRQ0	PE5/MTIOC9D/MTIOC9D#/GTIOC3A/GTETRGB/GTIOC3A#/GTETRGD/SCK009/CTS009#/RTS009#/SS009#/TXDB009/IRQ0/ADST0
2	P02/MTIOC9D/MTIOC9D#/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ADST0
3	VSS	VSS
4	P00/IRQ2/ADST1	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/TIC3/RXD12/SMISO12/SSCL12/RXDX12/RXD009/SMISO009/SSCL009/IRQ2/ADST1/COMP0
5	VCL	VCL
6	MD/FINED	MD/FINED/PN6
7	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/POE12#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD009/TXDA009/SMOSI009/SSDA009/IRQ4/ADST2/COMP1
8	PE4/MTCLKC/MTCLKC#/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/SCK009/TXDB009/IRQ1
9	PE3/MTCLKD/MTCLKD#/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/CTS009#/RTS009#/SS009#/DE009/IRQ2
10	RES#	RES#
11	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
14	VCC	VCC
15	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
16	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/SSLA3	PE1/MTIOC9D/MTIOC9D#/TMO5/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/SSLA3/SSL03/IRQ15
17	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/RXD5/SMISO5/SSCL5/SSLA2	PE0/MTIOC9B/MTIOC9B#/TMCI1/TMCI5/GTIV/RXD5/SMISO5/SSCL5/SSLA2/SSL02/CRX0/IRQ7

100-Pin LFQFP	RX24U	RX26T
18	PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/ GTIOC3A/GTIOC3A#/TXD5/SMOSI5/ SSDA5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009/TXD008/TXDA008/SMOSI008/ SSDA008/TXDB009/SSLA1/SSL01/CTX0/ IRQ8
19	PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC3B/ GTIOC3B#/CTS1#/RTS1#/SS1#/CTS11#/ RTS11#/SS11#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#/ RTS011#/SS011#/DE011/SSLA0/SSL00/ IRQ5/ADST0
20	PD5/TMRI0/TMRI6/GTECLKA/RXD1/ SMISO1/SSCL1/RXD11/SMISO11/SSCL11/ IRQ3	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011/SMISO011/ SSCL011/SSL00/IRQ6
21	PD4/TMCI0/TMCI6/GTECLKB/SCK1/SCK11/ IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011/TXDB011/SSL02/IRQ2
22	PD3/TMO0/GTECLKC/TXD1/SMOSI1/ SSDA1/TXD11/SMOSI11/SSDA11	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
23	PD2/TMCI1/TMO4/GTIOC0A/GTIOC0A#/ SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
24	PD1/TMO2/GTIOC0B/GTIOC0B#/MISOA	PD1/TMO2/GTIOC3A/GTIOC0B/GTIOC3A#/ GTIOC0B#/RXD008/SMISO008/SSCL008/ MISOA/MISO0
25	PD0/TMO6/GTIOC1A/GTIOC1A#/RSPCKA	PD0/TMO6/GTIOC3B/GTIOC1A/GTIOC3B#/ GTIOC1A#/TXD008/TXDA008/SMOSI008/ SSDA008/RSPCKA/RSPCK0
26	PB7/GTIOC1B/GTIOC1B#/SCK5	PB7/GTIOC1B/GTIOC1B#/SCK5/SCK12/ SCK011/TXDB011/SSL03
27	PB6/GTIOC2A/GTIOC2A#/RXD5/SMISO5/ SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
28	PB5/GTIOC2B/GTIOC2B#/TXD5/SMOSI5/ SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
29	VCC	VCC

100-Pin LFQFP	RX24U	RX26T
30	PB4/POE8#/GTETRG/GTECLKD/CTS5#/ RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
31	VSS	VSS
32	PB3/MTIOC0A/MTIOC0A#/CACREF/SCK6/ RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
33	PB2/MTIOC0B/MTIOC0B#/TMRI0/ADSM0/ TXD6/SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
34	PB1/MTIOC0C/MTIOC0C#/TMCI0/ADSM1/ RXD6/SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
35	PB0/MTIOC0D/MTIOC0D#/TMO0/TXD6/ SMOSI6/SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8
36	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
37	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ RSPCKA/ADTRG0#	PA4/MTIOC1B/MTIOC1B#/TMCI7/SCK6/ TXD008/TXDA008/SMOSI008/SSDA008/ RSPCKA/RSPCK0/ADTRG0#
38	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
39	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/SSLA1	PA2/MTIOC2B/MTIOC2B#/TMO7/ GTADSM1/CTS6#/RTS6#/SS6#/RXD009/ SMISO009/SSCL009/SSLA1/SSL01
40	PA1/MTIOC6A/MTIOC6A#/TMO4/SSLA2/ CRXD0/ADTRG0#	PA1/MTIOC6A/MTIOC6A#/TMO4/GTCPPO4/ TXD009/TXDA009/SMOSI009/SSDA009/ RXD011/SMISO011/SSCL011/SSLA2/ SSL02/CRX0/IRQ14/ADTRG0#
41	PA0/MTIOC6C/MTIOC6C#/TMO2/SSLA3/ CTXD0	PA0/MTIOC6C/MTIOC6C#/TMO2/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/CTX0
42	VCC	VCC
43	P96/POE4#/IRQ4	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/RSPCK0/ IRQ4
44	VSS	VSS

100-Pin LFQFP	RX24U	RX26T
45	P95/MTIOC6B/MTIOC6B#	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
46	P94/MTIOC7A/MTIOC7A#	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
47	P93/MTIOC7B/MTIOC7B#	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
48	P92/MTIOC6D/MTIOC6D#	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
49	P91/MTIOC7C/MTIOC7C#	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
50	P90/MTIOC7D/MTIOC7D#	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
51	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC2B#	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
52	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC1B#	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
53	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC0B#	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
54	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC2A#	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
55	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC1A#	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
56	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC0A#	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
57	P70/POE0#/IRQ5	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5

100-Pin LFQFP	RX24U	RX26T
58	P33/MTIOC3A/MTIOC3A#/MTCLKA/ MTCLKA#/TMO0/SSLA3	P33/MTIOC3A/MTCLKA/MTIOC3A#/ MTCLKA#/TMO0/GTIOC3B/GTIOC7B/ GTIOC3B#/GTIOC7B#/GTCPPO0/SSLA3/ SSL03/IRQ13
59	P32/MTIOC3C/MTIOC3C#/MTCLKB/ MTCLKB#/TMO6/SSLA2	P32/MTIOC3C/MTCLKB/MTIOC3C#/ MTCLKB#/TMO6/GTIOC3A/GTIOC7A/ GTIOC3A#/GTIOC7A#/SSLA2/SSL02/IRQ12
60	VCC	VCC
61	P31/MTIOC0A/MTIOC0A#/MTCLKC/ MTCLKC#/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6
62	VSS	VSS
63	P30/MTIOC0B/MTIOC0B#/MTCLKD/ MTCLKD#/TMCI6/SSLA0/IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
64	P27/MTIOC1A/MTIOC1A#	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
65	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ RSPCKA/COMP0/DA0	P24/MTIC5U/MTIC5U#/TMCI2/TMO6/ CTS008#/RTS008#/SS008#/SCK008/DE008/ RSPCKA/RSPCK0/IRQ4/COMP0
66	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ MOSIA/COMP1/DA1	P23/MTIC5V/MTIC5V#/TMO2/CACREF/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/CTX0/IRQ11/COMP1
67	P22/MTIC5W/MTIC5W#/TMRI2/TMO4/ MISOA/ADTRG2#/COMP2	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
68	P21/MTCLKA/MTCLKA#/MTIOC9A/ MTIOC9A#/TMCI4/IRQ6/ADTRG1#/AN116	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
69	P20/MTCLKB/MTCLKB#/MTIOC9C/ MTIOC9C#/TMRI4/IRQ7/ADTRG0#/AN016	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
70	P65/AN205	P65/IRQ9/AN211/CMPC53/DA1
71	P64/AN204	P64/IRQ8/AN210/CMPC33/DA0
72	AVCC2	AVCC2
73	AVSS2	AVSS2
74	P63/AN203/IRQ7	P63/IRQ7/AN209/CMPC23
75	P62/AN202/IRQ6	P62/IRQ6/AN208/CMPC43

100-Pin LFQFP	RX24U	RX26T
76	P61/AN201/IRQ5	P61/IRQ5/AN207/CMPC13
77	P60/AN200/IRQ4	P60/IRQ4/AN206/CMPC03
78	P55/AN211/IRQ3	P55/IRQ3/AN203/CMPC32
79	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22/CVREFC1
80	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12/CVREFC0
81	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
82	P47/AN103	P51/AN205/CMPC52
83	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P50/AN204/CMPC42
84	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P47/AN103
85	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P46/AN102/CMPC50/CMPC51
86	PGAVSS1	P45/AN101/CMPC40/CMPC41
87	P43/AN003	P44/AN100/CMPC30/CMPC31
88	P42/AN002	P43/AN003
89	P41/AN001	P42/AN002/CMPC20/CMPC21
90	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P41/AN001/CMPC10/CMPC11
91	PGAVSS0	P40/AN000/CMPC00/CMPC01
92	AVCC1	AVCC1
93	AVCC0	AVCC0
94	AVSS0	AVSS0
95	AVSS1	AVSS1
96	P82/MTIC5U/MTIC5U#/TMO4/SCK6	P82/MTIC5U/MTIC5U#/TMO4/SCK6/SCK12/ IRQ3/COMP5
97	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6	P81/MTIC5V/MTIC5V#/TMCI4/TXD6/ SMOSI6/SSDA6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/COMP4
98	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6	P80/MTIC5W/MTIC5W#/TMRI4/RXD6/ SMISO6/SSCL6/RXD12/SMISO12/SSCL12/ RXDX12/IRQ5/COMP3
99	P11/MTIOC3A/MTIOC3A#/MTCLKC/ MTCLKC#/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
100	P10/MTIOC9B/MTIOC9B#/MTCLKD/ MTCLKD#/TMRI3/POE12#/CTS6#/RTS6#/ SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.4 80-Pin LFQFP Package

Table 3.4 is Comparative Listing of 80-Pin LFQFP Package Pin Functions. Note that the RX24U Group does not have an 80-pin package version.

Table 3.4 Comparative Listing of 80-Pin LFQFP Package Pin Functions

80-Pin LFQFP	RX24T	RX26T
1	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ADST0	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ADST0
2	VSS	VSS
3	P00/IRQ2/ADST1	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/TIC3/RXD12/SMISO12/SSCL12/RXDX12/RXD009/SMISO009/SSCL009/IRQ2/ADST1/COMP0
4	VCL	VCL
5	MD/FINED	MD/FINED/PN6
6	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/POE12#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/TXD009/TXDA009/SMOSI009/SSDA009/IRQ4/ADST2/COMP1
7	PE4/MTCLKC/POE10#/IRQ1	PE4/MTCLKC/MTCLKC#/POE10#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/SCK009/TXDB009/IRQ1
8	PE3/MTCLKD/POE11#/IRQ2	PE3/MTCLKD/MTCLKD#/POE11#/GTETRGA/GTETRGB/GTETRGC/GTETRGD/CTS009#/RTS009#/SS009#/DE009/IRQ2
9	RES#	RES#
10	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
11	VSS	VSS
12	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
13	VCC	VCC
14	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
15	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/SCK009/TXD008/TXDA008/SMOSI008/SSDA008/TXDB009/SSLA1/SSL01/CTX0/IRQ8
16	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#/SSLA0/IRQ5/ADST0	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTIW/CTS1#/RTS1#/SS1#/RXD12/SMISO12/SSCL12/RXDX12/CTS011#/RTS011#/SS011#/DE011/SSLA0/SSL00/IRQ5/ADST0
17	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1/IRQ3	TDI/PD5/TMRI0/TMRI6/GTIOC1A/GTETRGA/GTIOC1A#/GTIOC7A/RXD1/SMISO1/SSCL1/RXD011/SMISO011/SSCL011/SSL00/IRQ6
18	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/GTETRGB/GTIOC1B#/SCK1/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SCK011/TXDB011/SSL02/IRQ2

80-Pin LFQFP	RX24T	RX26T
19	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011/TXDA011/SMOSI011/ SSDA011/MOSI0
20	PD2/TMCI1/TMO4/SCK5/MOSIA	PD2/TMCI1/TMO4/GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/SCK5/SCK008/ TXDB008/MOSIA/MOSI0
21	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011/SMISO011/SSCL011/MISO0/CRX0/ IRQ2
22	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011/TXDA011/SMOSI011/SSDA011/ RSPCK0/CTX0
23	VCC	VCC
24	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#/SS011#/ SCK011/TXDB011/MISOA/SSL01/CRX0/ IRQ3
25	VSS	VSS
26	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#/RTS009#/ SS009#/DE009/RSPCKA/CTX0/IRQ9
27	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00/ADSM0
28	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00/ IRQ4/ADSM1
29	PB0/MTIOC0D/TMO0/TXD6/SMOSI6/ SSDA6/MOSIA/ADTRG2#	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008/TXDA008/ SMOSI008/SSDA008/CTS011#/RTS011#/ SS011#/DE011/MOSIA/MOSI0/IRQ8/ ADTRG2#
30	PA5/MTIOC1A/TMCI3/RXD6/SMISO6/ SSCL6/MISOA/IRQ1/ADTRG1#	PA5/MTIOC1A/MTIOC1A#/TMCI3/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/MISO0/IRQ1/ADTRG1#
31	PA3/MTIOC2A/TMRI7/SSLA0	PA3/MTIOC2A/MTIOC2A#/TMRI7/ GTADSM0/TXD009/TXDA009/SMOSI009/ SSDA009/SCK008/TXDB008/SSLA0/SSL00
32	VCC	VCC
33	P96/POE4#/IRQ4	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/CTS008#/ RTS008#/SS008#/DE008/SSL03/RSPCK0/ IRQ4
34	VSS	VSS

80-Pin LFQFP	RX24T	RX26T
35	P95/MTIOC6B	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008/SMISO008/ SSCL008/MISOA/SSL02/MISO0/IRQ1/ ADTRG1#
36	P94/MTIOC7A	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009/TXDA009/ SMOSI009/SSDA009/SCK008/TXDB008/ SSLA0/SSL00
37	P93/MTIOC7B	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009/TXDA009/SMOSI009/ SSDA009/RXD011/SMISO011/SSCL011/ SSLA2/SSL02/MOSI0/CRX0/IRQ14/ ADTRG0#
38	P92/MTIOC6D	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009/ TXD011/TXDA011/SMOSI011/SSDA011/ TXDB009/SSLA3/SSL03/MISO0/CTX0
39	P91/MTIOC7C	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0
40	P90/MTIOC7D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01
41	P76/MTIOC4D	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03
42	P75/MTIOC4C	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02
43	P74/MTIOC3D	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01
44	P73/MTIOC4B	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00
45	P72/MTIOC4A	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0
46	P71/MTIOC3B	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0
47	P70/POE0#/IRQ5	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#/RTS009#/ SS009#/DE009/SSLA0/RSPCK0/IRQ5
48	VCC	VCC
49	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6	P31/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/GTIU/SSLA1/SSL01/IRQ6

80-Pin LFQFP	RX24T	RX26T
50	VSS	VSS
51	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P30/MTIOC0B/MTCLKD/MTIOC0B#/ MTCLKD#/TMCI6/GTIV/SCK008/CTS008#/ RTS008#/SS008#/DE008/SSLA0/SSL00/ IRQ7/COMP3
52	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P27/MTIOC1A/MTIOC0C/MTIOC1A#/ MTIOC0C#/TMO2/TMO6/POE9#/RSPCKA/ RSPCK0/IRQ15
53	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008/SMISO008/SSCL008/SCK008/ TXDB008/MISOA/MISO0/CRX0/IRQ10/ ADTRG2#/COMP2
54	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008/TXDA008/SMOSI008/SSDA008/ MOSIA/MOSI0/IRQ6/AN217/ADTRG1#/ COMP5
55	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#/ RTS008#/SS008#/RXD008/SMISO008/ SSCL008/DE008/RSPCKA/RSPCK0/IRQ7/ AN216/ADTRG0#/COMP4
56	P20/MTCLKB/MTIOC9C/TMRI4/IRQ7/ ADTRG0#/AN016/CVREFC0	P65/IRQ9/AN211/CMPC53/DA1
57	AVCC2	P64/IRQ8/AN210/CMPC33/DA0
58	VREF	AVCC2
59	AVSS2	AVSS2
60	P62/AN202/IRQ6	P60/IRQ4/AN206/CMPC03
61	P55/AN211/IRQ3	P55/IRQ3/AN203/CMPC32
62	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22/CVREFC1
63	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12/CVREFC0
64	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
65	P51/AN207	P51/AN205/CMPC52
66	P50/AN206	P50/AN204/CMPC42
67	P47/AN103	P47/AN103
68	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P46/AN102/CMPC50/CMPC51
69	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P45/AN101/CMPC40/CMPC41
70	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P44/AN100/CMPC30/CMPC31
71	P43/AN003	P43/AN003
72	P42/AN002	P42/AN002/CMPC20/CMPC21
73	P41/AN001	P41/AN001/CMPC10/CMPC11
74	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01
75	AVCC1	AVCC1
76	AVCC0	AVCC0
77	AVSS0	AVSS0

80-Pin LFQFP	RX24T	RX26T
78	AVSS1	AVSS1
79	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009/SCK008/ TXDB009/IRQ1
80	P10/MTIOC9B/MTCLKD/TMRI3/POE12#/ CTS6#/RTS6#/SS6#/IRQ0	P10/MTIOC9B/MTCLKD/MTIOC9B#/ MTCLKD#/TMRI3/POE12#/GTIOC3A/ GTETRGB/GTIOC3A#/GTETRGD/GTIV/ TIC3/CTS6#/RTS6#/SS6#/TXD009/ TXDA009/SMOSI009/SSDA009/IRQ0

3.5 64-Pin Package

Table 3.5 is Comparative Listing of 64-Pin Package Pin Functions. Note that the RX24U Group does not have a 64-pin package version.

Table 3.5 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX24T (64-Pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
1	P02/MTIOC9D/CTS1#/RTS1#/SS1#/IRQ5/ ADST0	EMLE/PN7/MTIOC9D/MTIOC9D#/IRQ5/ ADST0
2	P00/IRQ2/ADST1	P00/MTIOC9A/MTIOC9A#/CACREF/GTIU/ TIC3/RXD12/SMISO12/SSCL12/RXDX12/ RXD009*1/SMISO009*1/SSCL009*1/IRQ2/ ADST1*1/COMP0
3	VCL	VCL
4	MD/FINED	MD/FINED/PN6
5	P01/POE12#/IRQ4/ADST2	P01/MTIOC9C/MTIOC9C#/POE12#/ GTETRGA/GTETRGB/GTETRGC/ GTETRGD/GTIW/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/IRQ4/ADST2/ COMP1
6	RES#	RES#
7	XTAL/P37	XTAL/P37/RXD5/SMISO5/SSCL5
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/TXD5/SMOSI5/SSDA5
10	VCC	VCC
11	PE2/POE10#/NMI	PE2/POE10#/NMI/IRQ0
12	PD7/MTIOC9A/TMRI1/TMRI5/SSLA1	TRST#/PD7/MTIOC9A/MTIOC9A#/TMRI1/ TMRI5/GTIOC0A/GTIOC3A/GTIOC0A#/ GTIOC3A#/GTIU/TXD5/SMOSI5/SSDA5/ SCK009*1/TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/TXDB009*1/SSLA1/SSL01*1/ CTX0/IRQ8
13	PD6/MTIOC9C/TMO1/CTS1#/RTS1#/SS1#	TMS/PD6/MTIOC9C/MTIOC9C#/TMO1/ GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTIW/CTS1#/RTS1#/SS1#/RXD12/ SMISO12/SSCL12/RXDX12/CTS011#*1/ RTS011#*1/SS011#*1/DE011/SSLA0*1/ SSL00*1/IRQ5/ADST0
14	PD5/TMRI0/TMRI6/RXD1/SMISO1/SSCL1	TDI/PD5/TMRI0/TMRI6/GTIOC1A/ GTETRGA/GTIOC1A#/GTIOC7A/RXD1/ SMISO1/SSCL1/RXD011*1/SMISO011*1/ SSCL011*1/SSL00*1/IRQ6
15	PD4/TMCI0/TMCI6/SCK1/IRQ2	TCK/PD4/TMCI0/TMCI6/GTIOC1B/ GTETRGB/GTIOC1B#/SCK1/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SCK011*1/TXDB011*1/SSL02*1/IRQ2
16	PD3/TMO0/TXD1/SMOSI1/SSDA1	TDO/PD3/TMO0/GTIOC2A/GTETRGC/ GTIOC2A#/GTIOC7B/TXD1/SMOSI1/ SSDA1/TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/MOSI0

64-Pin	RX24T (64-Pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
17	PB6/RXD5/SMISO5/SSCL5/IRQ5	PB6/GTIOC2A/GTIOC3A/GTIOC2A#/ GTIOC3A#/TOC0/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ RXD011*1/SMISO011*1/SSCL011*1/MISO0*1/ CRX0/IRQ2
18	PB5/TXD5/SMOSI5/SSDA5	PB5/GTIOC2B/GTIOC3B/GTIOC2B#/ GTIOC3B#/TIC0/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/RSPCK0*1/CTX0
19	PB4/POE8#/CTS5#/RTS5#/SS5#/IRQ3	PB4/POE8#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO0/CTS5#/ RTS5#/SS5#/RXD12/SMISO12/SSCL12/ RXDX12/CTS011#/RTS011#*1/SS011#*1/ SCK011*1/TXDB011*1/MISOA/SSL01*1/CRX0/ IRQ3
20	PB3/MTIOC0A/CACREF/SCK6/RSPCKA	PB3/MTIOC0A/MTIOC0A#/CACREF/GTIU/ TOC1/SCK6/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/RSPCKA/CTX0/IRQ9
21	PB2/MTIOC0B/TMRI0/ADSM0/TXD6/ SMOSI6/SSDA6/SDA0	PB2/MTIOC0B/MTIOC0B#/TMRI0/ GTADSM0/GTIOC7A/GTIOC7A#/GTIV/TIC1/ TXD6/SMOSI6/SSDA6/SDA0/SDA00*1/ ADSM0
22	PB1/MTIOC0C/TMCI0/ADSM1/RXD6/ SMISO6/SSCL6/SCL0	PB1/MTIOC0C/MTIOC0C#/TMCI0/ GTADSM1/GTIOC7B/GTIOC7B#/GTIW/ TOC2/RXD6/SMISO6/SSCL6/SCL0/SCL00*1/ IRQ4/ADSM1
23	VCC	PB0/MTIOC0D/MTIOC0D#/TMO0/TIC2/ TXD6/SMOSI6/SSDA6/TXD008*1/TXDA008*1/ SMOSI008*1/SSDA008*1/CTS011#*1/ RTS011#*1/SS011#*1/DE011*1/MOSIA/ MOSI0*1/IRQ8/ADTRG2#
24	P96/POE4#/IRQ4	VCC
25	VSS	P96/POE4#/GTETRGA/GTETRGB/ GTETRGC/GTETRGD/GTCPPO4/ CTS008#*1/RTS008#*1/SS008#*1/DE008*1/ SSL03*1/RSPCK0*1/IRQ4
26	P95/MTIOC6B	VSS
27	P94/MTIOC7A	P95/MTIOC6B/MTIOC1A/MTIOC6B#/ MTIOC1A#/TMCI3/GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A#/GTOUUP/RXD6/ SMISO6/SSCL6/RXD008*1/SMISO008*1/ SSCL008*1/MISOA/SSL02*1/MISO0*1/IRQ1/ ADTRG1#*1
28	P93/MTIOC7B	P94/MTIOC7A/MTIOC2A/MTIOC7A#/ MTIOC2A#/TMRI7/GTIOC5A/GTADSM0/ GTIOC5A#/GTOVUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/SCK008*1/ TXDB008*1/SSLA0/SSL00

64-Pin	RX24T (64-Pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
29	P92/MTIOC6D	P93/MTIOC7B/MTIOC6A/MTIOC7B#/ MTIOC6A#/TMO4/GTIOC6A/GTIOC6A#/ GTOWUP/TXD009*1/TXDA009*1/ SMOSI009*1/SSDA009*1/RXD011*1/ SMISO011*1/SSCL011*1/SSLA2/SSL02*1/ MOSI0*1/CRX0/IRQ14/ADTRG0#
30	P91/MTIOC7C	P92/MTIOC6D/MTIOC6C/MTIOC6D#/ MTIOC6C#/TMO2/GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B#/GTOULO/SCK009*1/ TXD011*1/TXDA011*1/SMOSI011*1/ SSDA011*1/TXDB009*1/SSLA3/SSL03*1/ MISO0*1/CTX0*1
31	P90/MTIOC7D	P91/MTIOC7C/MTIOC7C#/GTIOC5B/ GTIOC5B#/GTOVLO/RXD5/SMISO5/SSCL5/ RSPCK0*1
32	P76/MTIOC4D	P90/MTIOC7D/MTIOC7D#/GTIOC6B/ GTIOC6B#/GTOWLO/TXD5/SMOSI5/ SSDA5/SSL01*1
33	P75/MTIOC4C	P76/MTIOC4D/MTIOC4D#/GTIOC2B/ GTIOC6B/GTIOC2B#/GTIOC6B#/GTOWLO/ SSL03*1
34	P74/MTIOC3D	P75/MTIOC4C/MTIOC4C#/GTIOC1B/ GTIOC5B/GTIOC1B#/GTIOC5B#/GTOVLO/ SSL02*1
35	P73/MTIOC4B	P74/MTIOC3D/MTIOC3D#/GTIOC0B/ GTIOC4B/GTIOC0B#/GTIOC4B#/GTOULO/ SSL01*1
36	P72/MTIOC4A	P73/MTIOC4B/MTIOC4B#/GTIOC2A/ GTIOC6A/GTIOC2A#/GTIOC6A#/GTOWUP/ SSL00*1
37	P71/MTIOC3B	P72/MTIOC4A/MTIOC4A#/GTIOC1A/ GTIOC5A/GTIOC1A#/GTIOC5A#/GTOVUP/ MOSI0*1
38	P70/POE0#/IRQ5	P71/MTIOC3B/MTIOC3B#/GTIOC0A/ GTIOC4A/GTIOC0A#/GTIOC4A#/GTOUUP/ MISO0*1
39	VCC	P70/MTIOC0A/MTCLKC/MTIOC0A#/ MTCLKC#/TMRI6/POE0#/GTETRGA/ GTETRGB/GTETRGC/GTETRGD/ GTCPPO0/SCK5/CTS009#*1/RTS009#*1/ SS009#*1/DE009*1/SSLA0/RSPCK0*1/IRQ5
40	P31/MTIOC0A/MTCLKC/TMRI6/SSLA1/IRQ6	VCC
41	VSS	VSS
42	P30/MTIOC0B/MTCLKD/TMCI6/SSLA0/ IRQ7/COMP3	P22/MTIC5W/MTCLKD/MTIC5W#/ MTCLKD#/TMRI2/TMO4/MTIOC9B/GTIV/ RXD12/SMISO12/SSCL12/RXDX12/ RXD008*1/SMISO008*1/SSCL008*1/SCK008*1/ TXDB008*1/MISOA/MISO0*1/CRX0/IRQ10/ ADTRG2#/COMP2

64-Pin	RX24T (64-Pin LFQFP)	RX26T (64-Pin LFQFP, 64-Pin HWQFN)
43	P24/MTIC5U/TMCI2/TMO6/RSPCKA/ COMP0	P21/MTIOC9A/MTCLKA/MTIOC9A#/ MTCLKA#/TMCI4/TMO6/GTIU/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ TXD008*1/TXDA008*1/SMOSI008*1/ SSDA008*1/MOSIA/MOSI0*1/IRQ6/AN217/ ADTRG1#*1/COMP5
44	P23/MTIC5V/TMO2/CACREF/MOSIA/ COMP1	P20/MTIOC9C/MTCLKB/MTIOC9C#/ MTCLKB#/TMRI4/TMO2/GTIW/CTS008#*1/ RTS008#*1/SS008#*1/RXD008*1/SMISO008*1/ SSCL008*1/DE008*1/RSPCKA/RSPCK0*1/ IRQ7/AN216/ADTRG0#/COMP4
45	P22/MTIC5W/TMRI2/TMO4/MISOA/ ADTRG2#/COMP2	P65/IRQ9/AN211/CMPC53/DA1
46	P21/MTCLKA/MTIOC9A/TMCI4/IRQ6/ ADTRG1#/AN116/CVREFC1	P64/IRQ8/AN210/CMPC33/CMPC52*2/DA0
47	AVCC2/VREF	AVCC2
48	AVSS2	AVSS2
49	P54/AN210/IRQ2	P54/IRQ2/AN202/CMPC22/CVREFC1
50	P53/AN209/IRQ1	P53/IRQ1/AN201/CMPC12/CVREFC0
51	P52/AN208/IRQ0	P52/IRQ0/AN200/CMPC02
52	P51/AN207	P47/AN103*1/AN206*2/CMPC03*2
53	P50/AN206	P46/AN102/CMPC50/CMPC51
54	P46/AN102/CMPC12/CMPC13/CMPC30/ CMPC31	P45/AN101*1/AN005*2/CMPC40*1/CMPC41*1/ CMPC11*2
55	P45/AN101/CMPC02/CMPC03/CMPC20/ CMPC21	P44/AN100*1/AN004*2/CMPC30*1/CMPC31*1/ CMPC01*2
56	P44/AN100/CMPC10/CMPC11/CMPC32/ CMPC33	P43/AN003/CMPC23*2/CMPC50*2
57	P42/AN002	P42/AN002/CMPC20/CMPC21*1
58	P41/AN001	P41/AN001/CMPC10/CMPC11*1
59	P40/AN000/CMPC00/CMPC01/CMPC22/ CMPC23	P40/AN000/CMPC00/CMPC01*1/CMPC13*2
60	AVCC1	AVCC1*1/NC*2
61	AVCC0	AVCC0
62	AVSS0	AVSS0
63	AVSS1	AVSS1*1/NC*2
64	P11/MTIOC3A/MTCLKC/TMO3/IRQ1	P11/MTIOC3A/MTCLKC/MTIOC3A#/ MTCLKC#/TMO3/POE9#/MTIOC9D/ GTIOC3B/GTETRGA/GTIOC3B#/GTETRGC/ GTCPPO0/TOC3/SCK009*1/SCK008*1/ TXDB009*1/IRQ1

Notes: 1. Not present on products with a RAM capacity of 48 KB.
2. Not present on products with a RAM capacity of 64 KB.

4. Important Information When Migrating Between MCUs

This section describes important information on differences between the RX26T Group and the RX24T/RX24U Group.

For notes regarding hardware, see section 4.1, Notes on Pin Design. For notes regarding software, see section 4.2, Notes on Functional Design.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

When connecting a smoothing capacitor to the VCL pin to stabilize the internal power supply, select a capacitor rated at 4.7 µF for the RX24T and RX24U Groups, and 0.47 µF on the RX26T Group.

4.1.2 Main Clock Oscillator

When connecting an oscillator to the EXTAL or XTAL pin of the RX26T Group, use an oscillator whose resonator frequency is 8 MHz to 24 MHz.

4.1.3 Connecting Capacitors to Analog Power Supply Pins

When using an A/D conversion clock frequency higher than 40 MHz on the RX26T Group, add a 0.01 µF-capacitor between the 0.1 µF capacitor and the power supply pin.

4.2 Notes on Functional Design

Software operating on the RX24T and RX24U Groups is compatible with some software written for the RX26T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

This section describes software-related considerations regarding function settings that differ between the RX26T Group and RX24T/RX24U Group.

For differences between modules and functions, see section 2, Comparative Overview of Specifications. For further information, refer to the User’s Manual: Hardware of each MCU group, listed in section 5, Reference Documents.

4.2.1 Changing the Option-Setting Memory Though Self-Programming

In the RX26T Group, when changing the option setting memory through self-programming, use the configuration setting command to program the option setting memory to the configuration setting area.

For details on the configuration setting command, refer to the RX26T Group Flash Memory User's Manual: Hardware listed in section 5, Reference Documents.

4.2.2 Software Configurable Interrupt

On the RX24T and RX24U Groups, the interrupt sources have fixed vector numbers, but on the RX26T Group, the MTU and GPTW interrupt sources are classified as software configurable interrupt A and set in software configurable interrupt A source select register n (SLIARn), allowing interrupt sources to be allocated to 208 to 255 in the interrupt vector table.

4.2.3 Using Flash Memory Commands

On the RX24T and RX24U Groups, programming and erasing of the flash memory is accomplished by first transitioning to the dedicated sequencer mode for ROM programming and erasing and then issuing software commands. On the RX26T Group, programming and erasing of the flash memory is accomplished by setting FACI commands in the FACI command-issuing area to control the FCU.

Table 4.1 is Comparison of Specifications of Software Commands and FACI Commands.

Table 4.1 Comparison of Specifications of Software Commands and FACI Commands

Item	Software Command (RX24T/RX24U)	FACI command (RX26T)
Command-issuing area	—	FACI command issuing area (007E 0000h)
Usable commands Programming	• Programming • Block erase • All-block erase • Blank check • Start-up area information program • Access window information program	• Programming • Block erase • P/E suspend • P/E resume • Status clear • Forced stop • Blank check • Configuration setting

4.2.4 Flash Access Window Setting Register

In the RX26T Group, the access window protect bit (FSPR) in the flash access window setting register (FAW) cannot be set back to 1 once it is set to 0.

For details, refer to the RX26T Group User's Manual: Hardware listed in section 5, Reference Documents.

4.2.5 Clock Frequency Settings

The clock frequency setting restrictions differ between the RX24T/RX24U Group and RX26T Group. For details, see Table 4.2.

Table 4.2 Comparison of Clock Frequency Setting Restrictions

Item	RX24T/RX24U	RX26T
Clock frequency setting restrictions	ICLK ≥ PCLK	PCLKC ≥ PCLKA ≥ PCLKB
Clock frequency setting restrictions when using CANFD	—	PCLKA:PCLKB = 2:1 PCLKB ≥ CANFDCLK PCLKB ≥ CANFDMCLK
Clock frequency ratio restrictions	ICLK:FCLK = N:1 ICLK:PCLKA = N:1 ICLK:PCLKB = N:1 ICLK:PCLKD = N:1	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKC = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKC = 1:1 or 1:2 PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2

4.2.6 RIIC Operating Voltage Setting

When using the RIIC on the RX26T Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics.

VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC.

For details, refer to the description of the VOLSR.RICVLS bit in RX26T Group User's Manual: Hardware.

4.2.7 Voltage Level Setting

On the RX26T Group, the operating mode setting in the voltage level setting register (VOLSR), the voltage detection circuit setting in the voltage detection level select register (LVDLVLR), and the option-setting memory setting in the option function select register 1 (OFS1) need to be changed as appropriate to match the operating voltage. Use a program to set these values.

4.2.8 Option-Setting Memory

On the RX24T/RX24U Group, the ID code protection codes and ID code protection codes for the on-chip debugger are located in the ROM, but on the RX26T Group, they are located in the option-setting memory. Note that the setting configuration procedures are different.

4.2.9 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to 4 to 15.5 (in 0.5 increments) on the RX24T/RX24U Group and to 10 to 30 (in 0.5 increments) on the RX26T Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value. Also, on the RX26T Group, use a program to switch the PLL clock.

4.2.10 All-Module Clock Stop Mode

The RX24T/RX24U Group does not have an all-module clock stop mode.

On the RX26T Group, it is necessary to write 1 to the MSTPA24, MSTPA27, and MSTPA29 bits to transition to the all-module clock stop mode.

4.2.11 MTU/GPTW Operating Frequency

On the RX26T Group, the PCLKC is used as the MTU/GPTW count clock, and PCLKA is used as the bus clock. Note that limitations apply regarding the usable frequency combinations.

4.2.12 DMAC Activation by MTU

When the DMAC is activated by the MTU on the RX26T Group, the activation source is cleared when the DMAC requests ownership of the internal bus. Accordingly, the state of the internal bus may delay the start of a DMAC transfer, even if the activation source has been cleared.

4.2.13 Performing RAM Self-Diagnostics on Save Register Banks

On the RX26T Group save register banks are configured in the RAM. The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells. When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

(1) Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
(2) Use the SAVE instruction to write data to a bank other than that written to in step 1.
(3) Use the RSTR instruction to read data from the bank written to in step 1.

4.2.14 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX26T Group is subject to the following restrictions.

(1) The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
(2) It is necessary to specify single scan mode when using match or mismatch event outputs.
(3) When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
(4) When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
(5) It is not possible to set the same channel for window A and window B.
(6) It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.2.15 Eliminating I^2C Bus Interface Noise

The RX24T/RX24U Group has integrated analog noise filters on the SCL and SDA lines, but the RX26T Group has no integrated analog noise filters.

4.2.16 Control When a Port Output Enable 3 Output Stop Request Is Generated

On the RX26T Group, when an output stop request occurs, the pins with the corresponding bits of the POECR1 to POECR3 and POECR7 registers set to 1 are put in a high-impedance state and the pins with the corresponding bits of the PMMCR0 to PMMCR2 registers set to 1 are switched to the general I/O ports.

When both bits are set to 1 for the same pin, the POECR1 to POECR3 and POECR7 register settings take precedence and the pin is placed in a high-impedance state. After switching to the general I/O port, the state of the pins is determined by the PDR and PODR register settings.

4.2.17 Comparator C Operation with 12-Bit A/D Converter in Module Stop Mode

On the RX26T Group, the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so it is not possible to compare the following PGA outputs when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

It is not possible to compare the following analog pins when the 12-bit A/D converter is in the module stop state:

- AN000 pin PGA output
- AN001 pin PGA output
- AN002 pin PGA output
- AN100 pin PGA output
- AN101 pin PGA output
- AN102 pin PGA output

4.2.18 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX24T/RX24U Group and RX26T Group, even on products with the same pin count.

4.2.19 Pulse Width of Count Clock Source

The pulse width of the MTU's count clock source differs between the RX24T/RX24U Group and RX26T Group. For details, see Table 4.2. Correct operation cannot be achieved if the pulse width is less than the appropriate value listed below.

Table 4.3 Comparison of Count Clock Source Pulse Widths

Item		RX24T/RX24U	RX26T
Single edge		3 or more PCLKA cycles	1.5 or more PCLKC cycles
Both edges		5 or more PCLKA cycles	2.5 or more PCLKC cycles
Phase counting mode	Phase difference and overlap	3 or more PCLK cycles	1.5 or more PCLKC cycles
	Pulse width	5 or more PCLKA cycles	2.5 or more PCLKC cycles

4.2.20 Note on General I/O Port Switching Using POE3

When an output disabling request specified by the POE3 is generated on the RX26T Group, pins for which the corresponding bits in the PMMCRn registers (n = 0 to 3) are set to 1 are switched to general I/O port pins. The corresponding bits in the POECRn registers (n = 0 to 3) should be cleared to 0 beforehand.

4.2.21 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX26T Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.2.22 Active Level Setting for MTU/GPTW Inverted Output

On the RX26T Group, either normal output or inverted output can be selected for MTU and GPTW outputs by making settings in the MPC.PmnPFS registers.

When MTU inverted output is selected, the active level specified in the MTU.TOCR1j and MTU.TOCR2j registers (j = A or B) and the active level of the signals output to the pins are inverted. To use output short detection in this case, specify active levels in the ALR1 and ALR2 registers based on the signals actually output to the pins.

When GPTW inverted output is selected, the active level of the signals output to the pins is inverted. To use output short detection in this case, specify active levels in the ALR3 to ALR5 registers based on the signals actually output to the pins.

4.2.23 Note on Using Both POE and POEG

When using the POE and POEG together on the RX26T Group, do not use both the POE and POEG to control output disabling for the same GPTW output pins.

4.2.24 Reading Pins in High-Impedance State

When pins are put into the high-impedance state by the POE on the RX26T Group, the level of those pins cannot be read. The value when read is undefined. To read the level of the pins, release them from the high-impedance state.

This restriction does not apply when port switching control is selected instead of high-impedance control.

5. Reference Documents

User's Manual: Hardware

RX24T Group User's Manual: Hardware Rev.2.00 (R01UH0576EJ0200)
(The latest version can be downloaded from the Renesas Electronics website.)

RX24U Group User's Manual: Hardware Rev.1.00 (R01UH0658EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX26T Group User's Manual: Hardware Rev.1.01 (R01UH0979EJ0101)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A151A/E

TN-RX*-A163A/E

TN-RX*-A173A/E

TN-RX*-A193A/E

TN-RX*-A194A/E

TN-RX*-A200A/E

TN-RX*-A0206A/E

TN-RX*-A0213A/E

TN-RX*-A0216A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.22.23	—	First edition issued
1.01	Aug.24.23	213 to 216	Modified typos and added notes in Table 3.5.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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