RX260/RX261 Group, RX660 Group

Differences Between the RX260/RX261 Group and the RX660 Group

Introduction

This application note is intended as a reference to differences in the peripheral functions, I/O registers, and pin functions between the RX261 Group and RX660 Group, and includes key points to consider when performing group migration.

Unless noted otherwise, the information in this application note applies to the 100-pin package versions of the RX261 Group and RX660 Group MCUs, which provide the highest hardware specifications. To confirm details of differences in electrical specifications, usage notes, and setting procedures, refer to the User's Manual: Hardware for the products in question.

Target Devices

RX260/RX261 Group, RX660 Group

Contents

1. Comparison of Built-In Functions of the RX260/RX261 Group and the RX660 Group

A comparison of the built-in functions of the RX260/RX261 Group and the RX660 Group is provided below. For details of the functions, refer to section 2, “Comparative Overview of Specifications” and section 5, “Reference Documents”.

Table 1.1 shows a Comparison of Built-In Functions of RX660 Group, RX260 Group, and RX261 Group.

Table 1.1 Comparison of Built-In Functions of RX660 Group, RX260 Group, and RX261 Group

Function	RX660	RX260/ RX261
CPU	▲/■	
Operating mode	●/▲/■	
Address space	▲/■	
Reset	■	
Option-setting memory (OFSM)	▲/■	
Voltage detection circuit (LVDA for RX660; LVDAb for RX261)	●/▲/■	
Clock generation circuit	●/▲/■	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●/▲/■	
Register write protection function	▲	
Exception handling	○	
Interrupt controller (ICUF for RX660; ICUb for RX261)	●/▲/■	
Buses	▲/■	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa for RX660; DMACA for RX261)	▲	
Data transfer controller (DTCb)	○	
Event link controller (ELC)	▲/■	
I/O port	●/▲/■	
Multi-function pin controller (MPC)	●/▲/■	
General-purpose PWM timer (GPTWa)	×	○
Port output enable for GPTW (POEGc)	×	○
Multi-function timer pulse unit 3 (MTU3a)	○	×
Port output enable 3 (POE3a)	○	×
8-bit timer (TMRb for RX660; TMRa for RX261)	▲/■	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	○	×
Realtime clock (RTCC for RX660; RTCBa for RX261)	▲/■	
Low-power timer (LPTa)	×	○
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	▲/■	
USB 2.0 FS host/function module (USBe)*1	×	○
Serial communications interface (SCIk/SCIm/SCIh for RX660; SCIk/SCIh for RX261)	▲/■	
Serial communications interface (RSCI)	▲/■	

Function	RX660	RX260/ RX261
I²C bus interface (RIICa)	▲	
CAN FD module (CANFD)*1	▲	
Serial peripheral interface (RSPId for RX660; RSPIc for RX261)	▲/■	
CRC calculator (CRCA for RX660; CRC for RX261)	▲	
Remote control signal receiver (REMCa)	●	
Renesas Secure IP (RSIP-E11A)*1	×	○
Capacitive touch sensing unit (CTSU2SLa)	×	○
Trigonometric function calculator (TFU)	○	×
12-bit A/D converter (S12ADH for RX660; S12ADE for RX261)	●/▲/■	
D/A converter (DAa)	×	○
12-bit D/A converter (R12DAb)	○	×
Temperature sensor (TEMPS for RX660; TEMPSA for RX261)	▲	
Comparator B (CMPBa)	×	○
Comparator C (CMPC)	○	×
Data operation circuit (DOCA for RX660; DOC for RX261)	▲/■	
RAM	■	
Flash memory (FLASH)	●/▲/■	
Packages	●/■	

Note: 1. This function is not provided by the RX260 Group.

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, **red text** indicates specifications which are included only in one of the MCU groups, and specifications that differ between the two groups.

In the register comparison, **red text** indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Register specifications that do not differ are not listed.

2.1 CPU

Table 2.1 shows a Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX660	RX261
CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Registers — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • 32-bit multiplier: 32 bits × 32 bits→ 64 bits • Divider: 32 bits / 32 bits → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 64 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Registers — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard provided instructions: 111 Basic instructions: 77 Single-precision floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • 32-bit multiplier: 32 bits × 32 bits → 64 bits • Divider: 32 bits / 32 bits → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions that conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions that conform to IEEE 754 standard
Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks	—

2.2 Operating Modes

Table 2.2 shows a Comparative Overview of Operating Modes, and Table 2.3 shows a Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX660	RX261
Operating mode by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (FINE interface)	Boot mode (FINE interface)
	User boot mode	—
	—	Boot mode (USB interface)
Selecting the operating mode by using registers	Single-chip mode, user boot mode	—
	Extended mode with on-chip ROM disabled	—
	Extended mode with on-chip ROM enabled	—

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX660	RX261
MDSR	—	Mode status register	—
SYSCR0	—	System control register 0	—
SYSCR1	—	System control register 1	System control register 1
		These registers have different initial values.	
VOLSR	—	Voltage level setting register	—

2.3 Address Space

Figure 2.1 shows a Comparison of Memory Maps in Single-Chip Mode.

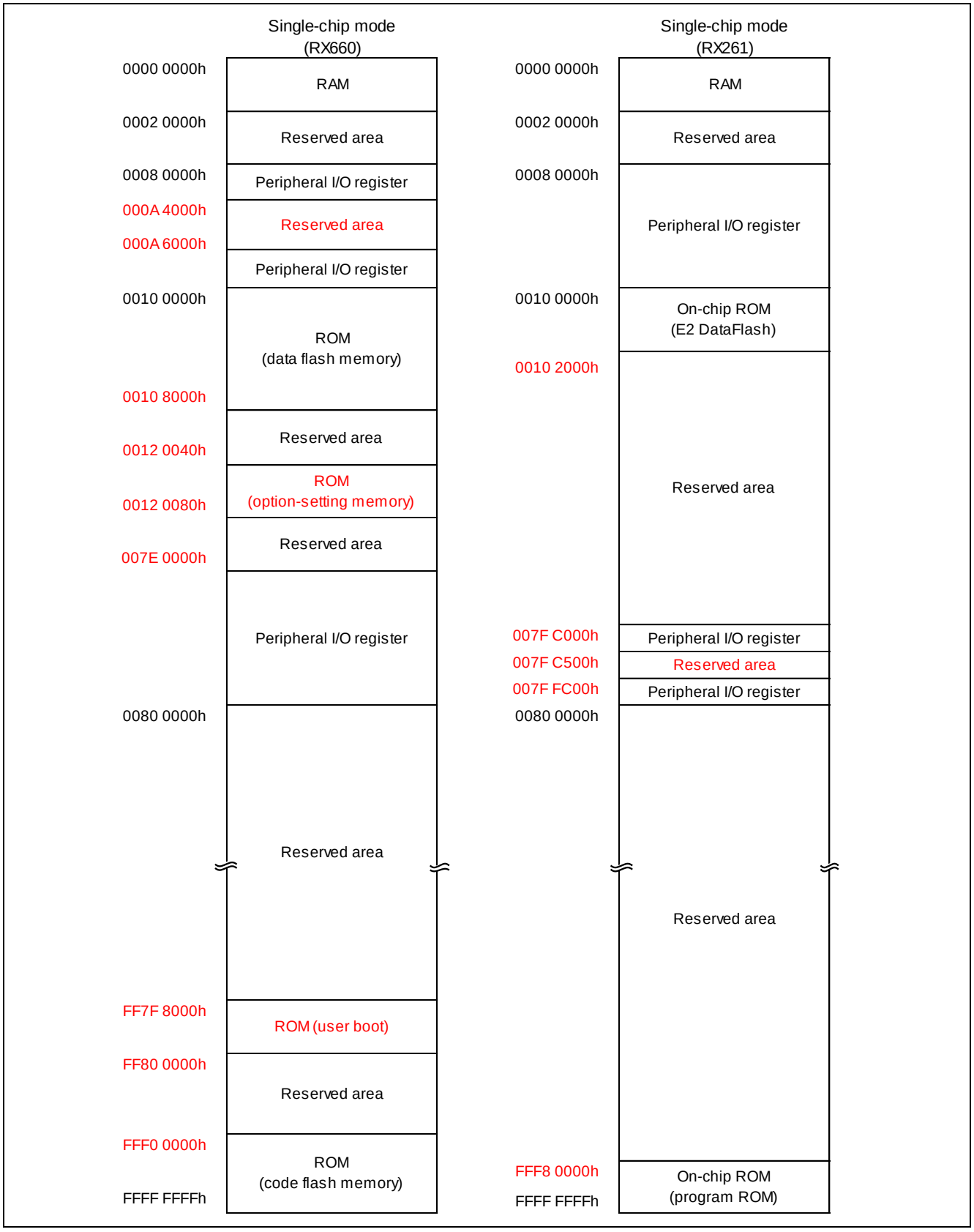

Figure 2.1 Comparison of Memory Maps in Single-Chip Mode

2.4 Resets

Table 2.4 shows a Comparison of Reset Sources, and Table2.5 shows a Comparison of Reset-Related Registers.

Table 2.4 Comparison of Reset Sources

Item	RX660	RX261
RES# pin reset	Voltage input to the RES# pin is driven low.	Voltage input to the RES# pin is driven low.
Power-on reset	VCC rises (voltage monitored: VPOR)	VCC rises (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC falls (voltage monitored: Vdet0)	VCC falls (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC falls (voltage monitored: Vdet1)	VCC falls (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC falls (voltage monitored: Vdet2)	VCC falls (voltage monitored: Vdet2)
Deep software standby reset	Exiting deep software standby mode by interrupt	—
Independent watchdog timer reset	Independent watchdog timer underflow or refresh error	Independent watchdog timer underflow or refresh error
Watchdog timer reset	Watchdog timer underflow or refresh error	Watchdog timer underflow or refresh error
Software reset	Register setting	Register setting

Table2.5 Comparison of Reset-Related Registers

Register	Bit	RX660	RX261
RSTSR0	DPSRSTF	Deep software standby reset flag	—

2.5 Option-Setting Memory

Figure 2.2 shows a Comparison of Option-Setting Memory Areas, and Table 2.6 shows a Comparison of Option-Setting Memory Registers.

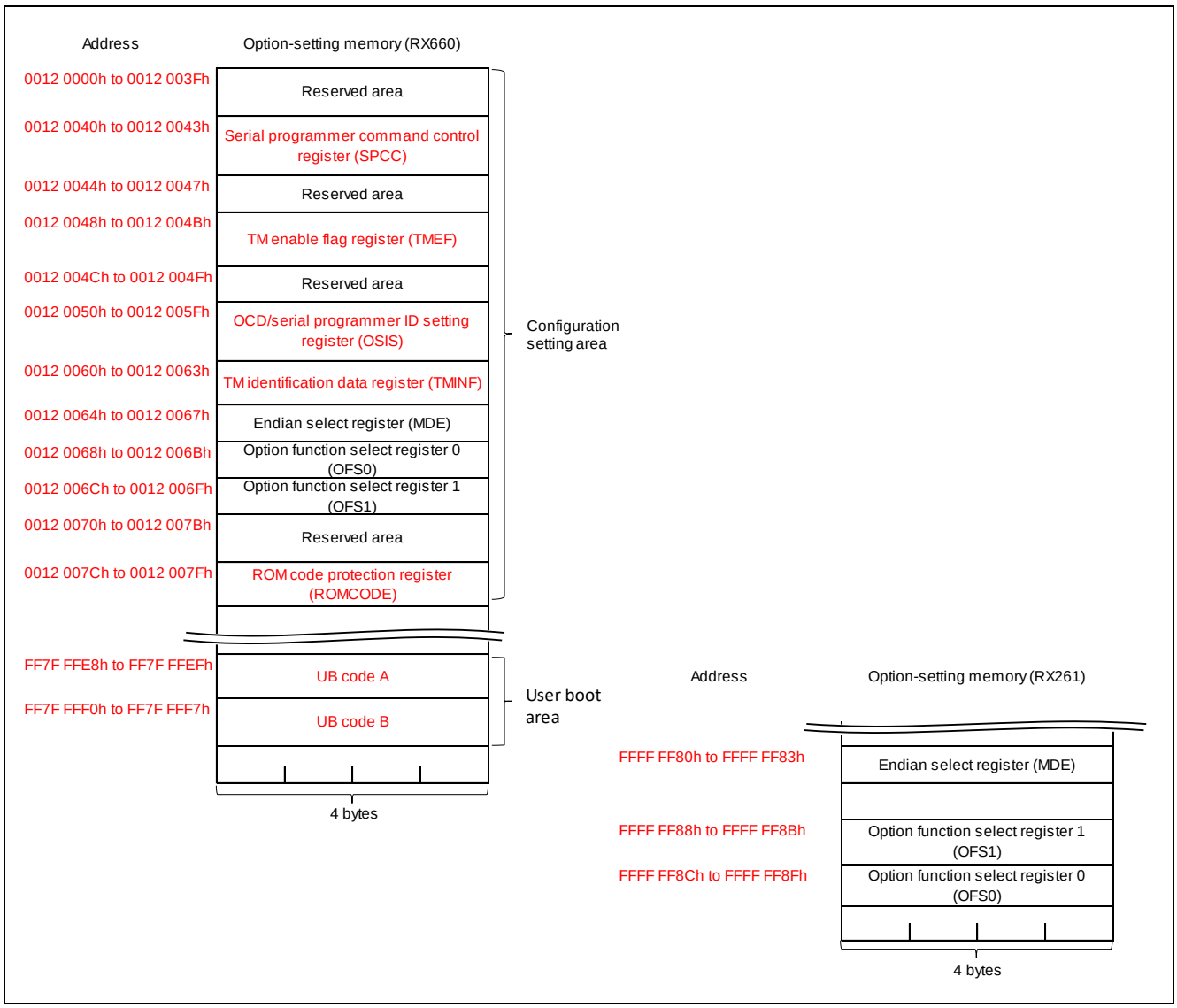

Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.6 Comparison of Option-Setting Memory Registers

Register	Bit	RX660 (OFSM)	RX261 (OFSM)
SPCC	—	Serial programmer command control register	—
OSIS	—	OCD/serial programmer ID setting register	—
OFS0	IWDTTOPS[1:0]	IWDT timeout period select bits b3 b2 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)
	IWDTRSTIRQS	IWDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled	IWDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering the following modes: sleep, software standby, deep software standby, and all-module clock stop.	IWDT sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering the following modes: sleep, software standby, and deep sleep.
	WDTRSTIRQS	WDT reset interrupt request select bit 0: Non-maskable interrupt request or plain interrupt request is enabled 1: Reset is enabled	WDT reset interrupt request select bit 0: Non-maskable interrupt request is enabled 1: Reset is enabled
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected 1 1: 4.22 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.85 V is selected 0 1: 2.85 V is selected 1 0: 2.53 V is selected 1 1: 1.90 V is selected
	FASTSTUP	—	Power-on fast startup time bit
	VDSEL2	—	Voltage detection 0 level select bit 2
	HOCOFRQ[1:0]	—	HOCO frequency select bits
TMEF	—	TM enable flag register	—
TMINF	—	TM identification data register	—
ROMCODE	—	ROM code protection register	—

2.6 Voltage Detection Circuit

Table 2.7 shows a Comparative Overview of Voltage Detection Circuits, and Table 2.8 shows a Comparison of Voltage Detection Circuit Registers.

Table 2.7 Comparative Overview of Voltage Detection Circuits

Item		RX660 (LVDA)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above, or drops below, Vdet1	When voltage rises above, or drops below, Vdet2	When voltage drops below Vdet0	When voltage rises above, or drops below, Vdet1	When voltage rises above, or drops below, Vdet2
							Input voltage can be switched to VCC or CMPA2 pin using the LVCMPCR. EXVCCINP2 bit.
	Detection voltage	Selectable from 2 levels using OFS1. VDSEL[1:0] bits	Selectable from 5 levels using LVDLVLR. LVD1LVL [3:0] bits	Selectable from 5 levels using LVDLVLR. LVD2LVL [1:0] bits	Selectable from 5 levels using the OFS1 register	Selectable from 16 levels using LVDLVLR. LVD1LVL [3:0] bits	Selectable from 4 levels using LVDLVLR. LVD2LVL [1:0] bits
	Monitoring flag	Not available	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	Not available	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection

Item		RX660 (LVDA)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Process upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin: CPU restart timing selectable among after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin
	Interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	Not available	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 >VCC and/or VCC > Vdet1	Interrupt request issued when Vdet2 > VCC and/or VCC > Vdet2		Interrupt request issued when Vdet1 > VCC and/or VCC > Vdet1	Interrupt request issued when Vdet2 > VCC or CMPA2 pin, and/or VCC or CMPA2 pin > Vdet2
Event link function		Not available	Available Output of event signals on detection of Vdet1 crossings	Available Output of event signals on detection of Vdet2 crossings	Not available	Available Output of event signals on detection of Vdet1 crossings	Available Output of event signals on detection of Vdet2 crossings

Item		RX660 (LVDA)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Digital filter	Enable/ disable switching	Digital filter function not available	Available	Available	—	—	—
	Sampling time	—	LOCO/n × 2 (n: 2, 4, 8, 16)	LOCO/n × 2 (n: 2, 4, 8, 16)	—	—	—

Table 2.8 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX660 (LVDA)	RX261 (LVDAb)
LVD1CR1	LVD1IDTSEL [1:0]	Voltage monitoring 1 interrupt generation condition select bits	Voltage monitoring 1 interrupt/ELC event generation condition select bits
LVD2CR1	LVD2IDTSEL [1:0]	Voltage monitoring 2 interrupt generation condition select bits b1 b0 0 0: When VCC ≥ Vdet2 (rise) detected 0 1: When VCC < Vdet2 (fall) detected 1 0: When rise and fall detected 1 1: Setting prohibited	Voltage monitoring 2 interrupt/ELC event generation condition select bits b1 b0 0 0: When VCC or CMPA2 pin ≥ Vdet2 (rise) detected 0 1: When VCC or CMPA2 pin < Vdet2 (fall) detected 1 0: When rise and fall detected 1 1: Setting prohibited
LVD2SR	LVD2MON	Voltage monitoring 2 signal monitor flag 0: VCC < Vdet2 1: VCC ≥ Vdet2, or LVD2MON disabled	Voltage monitoring 2 signal monitor flag 0: VCC or CMPA2 pin< Vdet2 1: VCC or CMPA2 pin ≥ Vdet2, or LVD2MON disabled
LVCMPCR	EXVCCINP2	—	Voltage detection 2 comparison voltage external input select bit
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V 1 1 1 0: 1.75 V 1 1 1 1: 1.65 V Settings other than the above are prohibited.

Register	Bit	RX660 (LVDA)	RX261 (LVDAb)
LVDLVLR	LVD2LVL[3:0] (RX660) LVD2LVL[1:0] (RX261)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V
		The initial value after a reset differs.	
LVD1CR0	LVD1DFDIS	Voltage monitoring 1 digital filter disable mode select bit	—
	LVD1FSAMP [1:0]	Sampling clock select bits	—
LCD2CR0	LVD2DFDIS	Voltage monitoring 2 digital filter disable mode select bit	—
	LVD2FSAMP [1:0]	Sampling clock select bits	—
	LVD2RN	Voltage monitoring 2 reset negate select bit 0: Negate when specified time (tLVD2) elapses after detecting that VCC > Vdet2 1: Negate when specified time (tLVD2) elapses after assertion of LVD2 reset	Voltage monitoring 2 reset negate select bit 0: Negate when specified time (tLVD2) elapses after detecting that VCC or CMPA2 pin > Vdet2 1: Negate when specified time (tLVD2) elapses after assertion of voltage monitoring 2 reset

2.7 Clock Generation Circuit

Table 2.9 a shows Comparative Overview of Clock Generation Circuits, and Table 2.10 shows a Comparison of Clock Generation Circuit Registers.

Table 2.9 Comparative Overview of Clock Generation Circuits

Item	RX660	RX261
Use	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to RSPI, SCIm, RSCI, MTU, and CANFD. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external-bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to CANFD (message buffer RAM) and GPTW. • Generates the peripheral module clock (PCLKB) to be supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC.

Item	RX660	RX261
Operating frequency	• ICLK: 120 MHz (max.) • PCLKA: 120 MHz (max.) • PCLKB: 60 MHz (max.) • PCLKD: 8 to 60 MHz (when performing conversion using a 12-bit A/D converter) • FCLK: — 4 to 60 MHz (when programming or erasing the code flash memory or data flash memory) — 60 MHz (max.) (when reading from the data flash memory) • BCLK: 60 MHz (max.) • BCLK pin output: 40 MHz (max.) • CANFDCLK: 60 MHz (max.) • CANFDMCLK: 24 MHz (max.) • REMSCLK: 32.768 kHz • CACCLK: Same as the clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 120 kHz	• ICLK: 64 MHz (max.) • PCLKA: 64 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 64 MHz (max.) • FCLK: — 1 to 64 MHz (when programming or erasing ROM or E2 data flash memory) — 64 MHz (max.) (when reading from the E2 data flash memory) • UCLK: 48 MHz • CANFDCLK: 32 MHz (max.) • CANFDMCLK: 20 MHz (max.) • LPTCLK: — 32.768 kHz (when the sub-clock is selected) — 15 kHz (when the IWDT-dedicated clock (IWDTCLK) is selected) — 1 MHz (when LOCO/4 is selected) • REMCLK: Same as the clock from selected oscillator • CACCLK: Same as the clock from selected oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz
Main clock oscillator	• Resonator frequency: 8 to 24 MHz • External clock input frequency: 24 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the MTU pin is driven to high-impedance state. • Drive capacity switching function	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO, and the GPTW pin is driven to high-impedance state. • Drive capacity switching function

Item	RX660	RX261
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • External clock input frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT • Sub-clock external input pin: EXCIN • Drive capacity switching function
PLL frequency synthesizer (RX660) PLL circuit (RX261)	• Input clock source: Main clock and HOCO	• Input clock source: Main clock
	• Input pulse frequency division ratio: Selectable from 1, 2, and 3	• Input pulse frequency division ratio: Selectable from 1, 2, and 4
	• Input frequency: 8 to 24 MHz	• Input frequency: 4 to 12.5 MHz
	• Frequency multiplication ratio: Selectable in the range from 10 to 30	• Frequency multiplication ratio: Selectable in the range from 4 to 15.5 (increments of 0.5)
	• Output clock frequency of the PLL frequency synthesizer: 120 to 240 MHz	• Oscillation frequency: 24 to 64 MHz
PLL2 circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 to 12.5 MHz • Frequency multiplication ratio: Selectable in the range from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 24 to 64 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function (Cannot be used for products that do not have sub-clock oscillator)	• Oscillation frequency: 24 MHz, 32 MHz, 48 MHz, 64 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 15 kHz
BCLK pin output control function	• Selectable from BCLK clock output and high output • Output clock can be selected from BCLK or 1/2 frequency of BCLK	—
Event link function (output)	Detection of stopping of the main clock oscillator	—
Event link function (input)	Switching of the clock source for the low-speed on-chip oscillator	—

Table 2.10 Comparison of Clock Generation Circuit Registers

Register	Bit	RX660	RX261
SCKCR	PCKD[3:0]	Peripheral module clock D (PCLKD) select bits	Peripheral module clock D (PCLKD) select bits
		The initial value after a reset differs.	
	PCKC[3:0]	Peripheral module clock C (PCLKC) select bits	—
	PCKB[3:0]	Peripheral module clock B (PCLKB) select bits	Peripheral module clock B (PCLKB) select bits
		The initial value after a reset differs.	
	PCKA[3:0]	Peripheral module clock A (PCLKA) select bit	Peripheral module clock A (PCLKA) select bit
		The initial value after a reset differs.	
	BCK[3:0]	Peripheral module clock B (PCLKB) select bit	—
	PSTOP1	BCLK pin output control bit	—
	ICK[3:0]	System clock (ICLK) select bit	System clock (ICLK) select bit
		The initial value after a reset differs.	
	FCK[3:0]	FlashIF clock (FCLK) select bit	FlashIF clock (FCLK) select bit
		The initial value after a reset differs.	
SCKCR2	—	System clock control register 2	—
PLLCR	PLIDIV[1:0]	b1 b0 0 0: Division by 1 0 1: Division by 2 1 0: Division by 3 1 1: Setting prohibited	b1 b0 0 0: Division by 1 0 1: Division by 2 1 0: Division by 4 1 1: Setting prohibited
	PLLSRCSEL	PLL clock source select bit	—
	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0

Register	Bit	RX660	RX261
PLLCR	STC[5:0]	0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 0 1 1 1 1 1: ×16.0 1 0 0 0 0 0: ×16.5 1 0 0 0 0 1: ×17.0 1 0 0 0 1 0: ×17.5 1 0 0 0 1 1: ×18.0 1 0 0 1 0 0: ×18.5 1 0 0 1 0 1: ×19.0 1 0 0 1 1 0: ×19.5 1 0 0 1 1 1: ×20.0 1 0 1 0 0 0: ×20.5 1 0 1 0 0 1: ×21.0 1 0 1 0 1 0: ×21.5 1 0 1 0 1 1: ×22.0 1 0 1 1 0 0: ×22.5 1 0 1 1 0 1: ×23.0 1 0 1 1 1 0: ×23.5 1 0 1 1 1 1: ×24.0 1 1 0 0 0 0: ×24.5 1 1 0 0 0 1: ×25.0 1 1 0 0 1 0: ×25.5 1 1 0 0 1 1: ×26.0 1 1 0 1 0 0: ×26.5 1 1 0 1 0 1: ×27.0 1 1 0 1 1 0: ×27.5 1 1 0 1 1 1: ×28.0 1 1 1 0 0 0: ×28.5 1 1 1 0 0 1: ×29.0 1 1 1 0 1 0: ×29.5 1 1 1 0 1 1: ×30.0 Settings other than the above are prohibited.	0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.
PLL2CR		—	PLL2 control register
PLL2CR2	—	—	PLL2 control register 2
BCKCR	—	External bus clock control register	—
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
FLLCR1	—	FLL control register 1	—
FLLCR2	—	FLL control register 2	—
OSCOVFSR	SOOVF	Sub-clock oscillation stabilization flag	—
	ILCOVF	IWDT-dedicated clock oscillation stabilization flag	—
	PL2OVF	—	PLL2 clock oscillation stabilization flag

Register	Bit	RX660	RX261
CKOCR	—	—	CLKOUT output control register
OSCOVFSR	—	Oscillation stabilization flag register	—
OSTDCR	OSTDIE	Oscillation stop detection interrupt enable bit 0: Disable oscillation stop detection interrupt and disable oscillation stop detection notification to POE. 1: Enable oscillation stop detection interrupt and enable oscillation stop detection notification to POE.	Oscillation stop detection interrupt enable bit 0: Disable oscillation stop detection interrupt and disable oscillation stop detection notification to POEG. 1: Enable oscillation stop detection interrupt and enable oscillation stop detection notification to POEG.
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRR0	—	—	High-speed on-chip oscillator trimming register 0
CANFDCKDIVCR	—	—	CANFD clock division control register
USBCKCR	—	—	USB clock control register
CANFDCKCR	—	—	CANFD clock control register
SOMCR	—	—	Sub-clock oscillator mode control register
MOSCWTCR	MSTS[7:0] (RX660) MSTS[4:0] (RX261)	Main clock oscillator wait time setting bits The setting value of the MSTS[7:0] bits are obtained by the following formula using the maximum frequency of fLOCO so that the waiting time always becomes equal to or larger than the oscillation stabilization time of the main clock. MSTS[7:0] > [tMAINOSC × (fLOCO_max) + 16] / 32 tMAINOSC: Main clock oscillation stabilization time fLOCO_max: Maximum fLOCO frequency	Main clock oscillator wait time setting bits b4 b0 0 0 0 0 0: Wait time = 0 cycles (0µs) 0 0 0 0 1: Wait time = 1024 cycles (256 µs)

Register	Bit	RX660	RX261
MOSCWTCR	MSTS[7:0] (RX660) MSTS[4:0] (RX261)		0 0 0 1 0: Wait time = 2048 cycles (512 µs) 0 0 0 1 1: Wait time = 4096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131072 cycles (32.768 ms) Settings other than the above are prohibited. The above wait times are on the assumption that LOCO = 4.0 MHz (0.25 µs, TYP).
MOFCR	—	—	Main clock oscillator forced oscillation control register
SOSCWTCR	—	Sub-clock oscillator wait control register	—
SOFCR	—	Sub-clock oscillator forced oscillation control register	—
MOFCR	—	Main clock oscillator function control register	—
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—

2.8 Low Power Consumption Function

Table 2.11 shows a Comparative Overview of Low Power Consumption Functions, Table 2.12 shows a Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.13 shows a Comparison of Low Power Consumption Registers.

Table 2.11 Comparative Overview of Low Power Consumption Functions

Item	RX660	RX261
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the following clocks: system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external-bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the following clocks: system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), and FlashIF clock (FCLK).
BCLK output control function	• Selectable from BCLK output and high output	—
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption state	Can be transitioned to a low power consumption mode, in which the CPU, peripheral modules, and oscillators are stopped.	Can be transitioned to a low power consumption mode, in which the CPU, peripheral modules, and oscillators are stopped.
Low power consumption state	• Sleep mode • Software standby mode • Deep software standby mode • All-module clock stop mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	—	• Power consumption in the following operating modes can be reduced by selecting an appropriate operating power control mode according to the operating frequency and operating voltage: normal operation, sleep mode, deep sleep mode, and snooze mode. • Four operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.12 Comparison of Methods for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX660	RX261
Sleep mode	Method for entering the mode	Control register + instruction	Control register + instruction
	Method for exiting the mode (except a reset)	Interrupt	Interrupt
	State after exiting the mode	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PLL2	—	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0001 FFFFh)	Operation possible (retained)	Operation possible (retained)
	DMAC	—	Operation possible
	DTC	—	Operation possible
	Flash memory	Operating	Operating
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	—
	8-bit timer (unit 0/1) (TMR)	Operation possible	—
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operating	Operating
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Deep sleep mode	Method for entering the mode	—	Control register + instruction
	Method for exiting the mode (except a reset)	—	Interrupt
	State after exiting the mode	—	Program execution state (interrupt processing)
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX660	RX261
Deep sleep mode	PLL	—	Operation possible
	PLL2	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0001 FFFFh)	—	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operating
	Peripheral modules	—	Operation possible
	I/O ports	—	Operating
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Software standby mode	Method for entering the mode	Control register + instruction	Control register + instruction
	Method for exiting the mode (except a reset)	Interrupt	Interrupt
	State after exiting the mode	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	PLL2	—	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0001 FFFFh)	Stopped (retained)	Stopped (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Stopped (retained)	Operation possible
	Remote control signal receiver (REMC)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (retained)	—
	8-bit timer (unit 0/1) (TMR)	Stopped (retained)	—

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX660	RX261
Software standby mode	Low-power timer (LPT)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operating	Operating
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible
Snooze mode	Method for entering the mode	—	A condition for entering snooze mode occurs in software standby mode.
	Method for exiting the mode (except a reset)	—	An interrupt or condition for exiting snooze mode occurs.
	State after exiting the mode	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	PLL2	—	Operation possible
	CPU	—	Stopped (retained)
	RAM0 (0000 0000h to 0001 FFFFh)	—	Operation possible (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Operation possible
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operating
	Peripheral modules	—	Operation possible
	I/O ports	—	Operating
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible

Mode	Methods for Entering and Exiting Low Power Consumption Modes and Operating States	RX660	RX261
All-module clock stop mode	Method for entering the mode	Control register + instruction	—
	Method for exiting the mode (except a reset)	Interrupt	—
	State after exiting the mode	Program execution state (interrupt processing)	—
	Main clock oscillator	Operation possible	—
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	—
	Low-speed on-chip oscillator	Operation possible	—
	IWDT-dedicated on-chip oscillator	Operation possible	—
	PLL	Operation possible	—
	CPU	Stopped (retained)	—
	RAM	Stopped (retained)	—
	Flash memory	Stopped (retained)	—
	Watchdog timer (WDT)	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	—
	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Port output enable (POE)	Operation possible	—
	8-bit timer (unit 0/1) (TMR)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	—
	Power-on reset circuit	Operating	—
	Peripheral modules	Stopped (retained)	—
	I/O ports	Retained	—

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.13 Comparison of Low Power Consumption Registers

Register	Bit	RX660	RX261
SBYCR	OPE	Output port enable bit	—
MSTPCRA	MSTPA0	Compare match timer W (Unit 1) module stop bit	—
	MSTPA1	Compare match timer W (Unit 0) module stop bit	—
	MSTPA7	—	General-purpose PWM timer module stop bit
	MSTPA9	Multi-function timer pulse unit 3 module stop bit	—
	MSTPA19	Target module: 12-bit DA 0: Exit module-stop state 1: Enter module-stop state	Target module: DA 0: Exit module-stop state 1: Enter module-stop state
	MSTPA24	Module stop A24 bit	—
	MSTPA27	Module stop A27 bit	—
	MSTPA29	Module stop A29 bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB10	Comparator C module stop bit	Comparator B module stop bit
	MSTPB19	—	USB 2.0 FS host/function module stop bit
	MSTPB24	Serial communication interface 7 module stop bit	—
	MSTPB27	Serial communication interface 4 module stop bit	—
	MSTPB28	Serial communication interface 3 module stop bit	—
	MSTPB29	Serial communication interface 2 module stop bit	—
	MSTPB31	Target module: SCI0 0: Exit module-stop state 1: Enter module-stop state	Target module: RSCI0 0: Exit module-stop state 1: Enter module-stop state
MSTPCRC	MSTPC17	I^2C bus interface 2 module stop bit	—
	MSTPC24	Serial communications interface 11 module stop bit	—
	MSTPC25	Serial communications interface 10 module stop bit	—
	MSTPC26	Target module: SCI9 0: Exit module-stop state 1: Enter module-stop state	Target module: RSCI9 0: Exit module-stop state 1: Enter module-stop state
	MSTPC27	Target module: SCI8 0: Exit module-stop state 1: Enter module-stop state	Target module: RSCI8 0: Exit module-stop state 1: Enter module-stop state
	MSTPC29	—	Remote control signal receiver module stop bit
	DSLPE	—	Deep sleep mode enable bit

Register	Bit	RX660	RX261
MSTPCRD	MSTPD2	Serial communications interface 11 module stop bit	—
	MSTPD3	Serial communications interface 10 module stop bit	—
	MSTPD7	Remote control signal receiver module stop bit	—
	MSTPD9	—	CANFD0 module stop bit
	MSTPD10	CANFD module stop bit	Touch sensor control unit module stop bit
	MSTPD31	—	RSIP module stop bit
OPCCR	—	—	Operating power control register
SOPCCR	—	—	Sub-operating power control register
RSTCKCR	RSTCKSEL [2:0]	Sleep mode return clock source select bits b2 b0 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than the above are prohibited when the RSTCKEN bit is 1.	Sleep mode return clock source select bits b2 b0 0 0 0: LOCO is selected. 0 0 1: HOCO is selected. 0 1 0: Main clock oscillator is selected. Settings other than the above are prohibited when the RSTCKEN bit is 1.
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2
RPSCR	—	—	RAM power-saving control register
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER1	—	Deep standby interrupt enable register 1	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR1	—	Deep standby interrupt flag register 1	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR1	—	Deep standby interrupt edge register 1	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—
DPSBKRy	—	Deep standby backup register y (y = 0 to 31)	—

2.9 Register Write Protection Function

Table 2.14 shows a Comparative Overview of Register Write Protection Functions, and Table 2.15 shows a Comparison of Register Write Protection Function Registers.

Table 2.14 Comparative Overview of Register Write Protection Functions

Item	RX660	RX261
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, PLL2CR, PLL2CR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR, CANFDCKCR, CANFDCKDIVCR, USBCKCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: BYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, RPSCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	—	• Registers related to low-power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.15 Comparison of Register Write Protection Function Registers

Register	Bit	RX660	RX261
PRCR	PRC2	—	Protect bit 2

2.10 Interrupt Controller

Table 2.16 shows a Comparative Overview of Interrupt Controllers, and Table 2.17 shows a Comparison of Interrupt Controller Registers.

Table 2.16 Comparative Overview of Interrupt Controllers

Item		RX660 (ICUF)	RX261 (ICUb)
Interrupts	Peripheral interrupts	• Interrupts from peripheral modules • Interrupt detection method: Edge detection/level detection (The detection method is fixed for each interrupt source.) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use ICLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each interrupt source of connected peripheral modules.

Item		RX660 (ICUF)	RX261 (ICUb)
Interrupts	External pin interrupts	• Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source.	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source.
	External pin interrupts	• A digital filter can be used to remove noise.	• Digital filter function: Supported
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupt	—	ELSR8I, ELSR18I, and ELSR19I interrupts are generated by an ELC event.
	Interrupt priority	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).	Specified by registers.
	Fast interrupt function	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.	Faster CPU interrupt handling can be enabled. This can be enabled for a single interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
Non-maskable interrupts	NMI pin interrupt	• Interrupt by the input signal on the NMI pin • Interrupt detection: — Falling edge — Rising edge • A digital filter can be used to remove noise.	• Interrupt from the NMI pin • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported
	Oscillation stop interrupt	Interrupt occurs when the main clock oscillator stop is detected.	Interrupt on detection of oscillation having stopped
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt on an underflow of the down counter or occurrence of a refresh error
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Interrupt from voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Interrupt from voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in RAM.	Interrupt occurs when a parity check error is detected in RAM.

Item		RX660 (ICUF)	RX261 (ICUb)
Return from low power consumption state	Sleep mode	Exits this mode by any interrupt source.	Exits this mode by any non-maskable interrupt or any plain interrupt.
	Deep sleep mode	—	Exits this mode by any non-maskable interrupt or any plain interrupt.
	Software standby mode	Exits this mode by NMI pin interrupt, external pin interrupt (IRQ0 to IRQ15), or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC period, IWDT, or REMC interrupt).	Exits this mode by NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm/period, REMC, or USB0 resume), ELSR8I interrupt (LPT-dedicated interrupt).
	Snooze mode	—	Exits this mode by NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral function interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm/period, REMC, or USB0 resume), SNZI interrupt (interrupt causing exit from snooze mode).
	Deep software standby mode	Exits this mode by NMI pin interrupt, specific external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or RTC period).	—
	All-module clock stop mode	Exits this mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection, RTC alarm, RTC period, IWDT, REMC interrupt, or software configurable interrupts 146 to 157).	—

Table 2.17 Comparison of Interrupt Controller Registers

Register	Bit	RX660 (ICUF)	RX261 (ICUb)
SWINT2R	—	Software interrupt 2 generation register	—
DTCERn	—	DTC transfer request enable register n (n = 026 to 255)	DTC transfer request enable register n (n = 027 to 255)
IRQCRi	—	IRQ control register i (i = 0 to 15)	IRQ control register i (i = 0 to 7)
IRQFLTE1	—	IRQ pin digital filter enable register 1	—
IRQFLTC1	—	IRQ pin digital filter setting register 1	—
GRPAL0 GRPBL0 GRPBL1 GRPBL2	—	Group BL0/BL1/BL2 interrupt request register, Group AL0 interrupt request register	—

Register	Bit	RX660 (ICUF)	RX261 (ICUb)
GENBL0 GENBL1 GENBL2 GENAL0	—	Group BL0/BL1/BL2 interrupt request enable register, Group AL0 interrupt request enable register	—
PIBRk	—	Software configurable interrupt B request register k (k = 0h, 1h, 5h, 6h, 8h to Ah, Ch, Dh)	—
PIARk	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)	—
SLIBXRn	—	Software configurable interrupt B source select register Xn (n = 128 to 143)	—
SLIBRn	—	Software configurable interrupt B source select register n (n = 144 to 207)	—
SLIARn	—	Software configurable interrupt A source select register n (n = 208 to 255)	—
SLIPRCR	—	Software configurable interrupt source select register write protect register	—

2.11 Buses

Table 2.18 shows a Comparative Overview of Buses, and Table 2.19 shows a Comparison of Bus-Related Registers.

Table 2.18 Comparative Overview of Buses

Item		RX660	RX261
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to code flash memory	• Connected to ROM
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral modules other than internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (peripheral modules other than internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (DOC, REMC, CANFD, and CMPC) • Operates in synchronization with the peripheral module clock (PCLKB)	• Connected to peripheral modules (USB0, CANFD, CTSU, REMC, and RSCI) • Operates in synchronization with the peripheral module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU, RSPI, and SCIi) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral module (GPTW) • Operates in synchronization with the peripheral module clock (PCLKA)

Item		RX660	RX261
Internal peripheral buses	Internal peripheral bus 5	• Connected to peripheral modules (RSCI and CANFD) • Operates in synchronization with the peripheral module clock (PCLKA)	• Connected to peripheral module (CANFD (message buffer RAM)) • Operates in synchronization with the peripheral module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash memory (in P/E) and data flash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (in P/E) and E2 data flash • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to external devices • Operates in synchronization with the external-bus clock (BCLK)	—

Table 2.19 Comparison of Bus-Related Registers

Register	Bit	RX660	RX261
CSnCR	—	CSn control register (n = 0 to 3)	—
CSnREC	—	CSn recovery cycle register (n = 0 to 3)	—
CSRECEN	—	CS recovery cycle insertion enable register	—
CSnMOD	—	CSn mode register (n = 0 to 3)	—
CSnWCR1	—	CSn wait control register 1 (n = 0 to 3)	—
CSnWCR2	—	CSn wait control register 2 (n = 0 to 3)	—
BUSPRI	BPEB[1:0]	External bus priority control bits	—

2.12 DMA Controller

Table 2.20 shows a Comparative Overview of DMA Controllers, and Table 2.21 shows a Comparison of DMA Controller Registers.

Table 2.20 Comparative Overview of DMA Controllers

Item		RX660 (DMACAa)	RX261 (DMACA)
Number of channels		8 channels (DMACm (m = 0 to 7))	4 channels (DMACm (m = 0 to 3))
Transfer space		512 MB (within 00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)	512 MB (within 00000000h to 0FFFFFFFh and F0000000h to FFFFFFFFh, excluding reserved areas)
Maximum transfer volume		64 M data units (Maximum number of data units in block transfer mode: 1024 data units × 65536 blocks)	1 M data units (Maximum number of data units in block transfer mode: 1024 data units × 1024 blocks)
DMAC activation source		• An activation source can be selected for each channel. — Software trigger — Interrupt request from a peripheral modules or trigger input on the external interrupt input pin	• An activation source can be selected for each channel. — Software trigger — Interrupt request from a peripheral modules or trigger input on the external interrupt input pin
Channel priority order		Channel 0 > Channel 1 > Channel 2 > Channel 3 > ... > Channel 7 (Channel 0 has the highest priority.)	Channel 0 > Channel 1 > Channel 2 > Channel 3 (Channel 0 has the highest priority.)
Transferred data	Single data unit	Bit length: 8, 16, or 32 (bits)	Bit length: 8, 16, or 32 (bits)
	Block size	Number of data units: 1 to 1024	Number of data units: 1 to 1024
Transfer modes	Normal transfer mode	• Transfers 1 data unit in 1 DMA transfer request • Transfer setting without the specification of the total number of data units (free running mode) is possible	• Transfers 1 data unit in 1 DMA transfer request • Transfer setting without the specification of the total number of data units (free running mode) is possible
	Repeat transfer mode	• Transfers 1 data unit in 1 DMA transfer request • The transfer address returns to the transfer start address when the number of data transfers equals the repeat size specified by the transfer source or transfer destination. • The maximum repeat size that can be set is 1024.	• Transfers 1 data unit in 1 DMA transfer request • The transfer address returns to the transfer start address when the number of data transfers equals the repeat size specified by the transfer source or transfer destination. • The maximum repeat size that can be set is 1024.
	Block transfer mode	• Transfers 1 data block in 1 DMA transfer request • The maximum block size that can be set is 1024 data units.	• Transfers 1 data block in 1 DMA transfer request • The maximum block size that can be set is 1024 data units.

Item		RX660 (DMACAa)	RX261 (DMACA)
Selective functions	Extended repeat area function	• A specific area of address can be repeated by fixing upper bits of the transfer address register. • An extended repeat area of 2 bytes to 128 MB can be set to each transfer source and transfer destination.	• A specific area of address can be repeated by fixing upper bits of the transfer address register. • An extended repeat area of 2 bytes to 128 MB can be set to each transfer source and transfer destination.
Interrupt request	Transfer end interrupt	• In normal transfer mode, it is generated when the specified number of transfers is finished. • In repeat transfer mode, it is generated when the transfer of the specified number of repeats is finished. • In block transfer mode, it is generated when the transfer of the specified number of blocks is finished.	Generated when the transfer of the number of data units being set in the transfer counter is finished
	Transfer escape end interrupt	Generated when the data transfer of the repeat size is finished or the extended repeat area overflows	Generated when the data transfer of the repeat size is finished or the extended repeat area overflows
Low power consumption function		Ability to specify module stop state	Ability to specify module stop state
Event link function		An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).

Table 2.21 Comparison of DMA Controller Registers

Register	Bit	RX660 (DMACAa)	RX261 (DMACA)
DMCRB	—	DMA block transfer count register (b15 to b0) 0001h to FFFFh (1 to 65535 times) 0000h (65536 times)	DMA block transfer count register (b9 to b0) 001h to 3FFh (1 to 1023 times) 000h (1024 times)
DMIST	—	DMAC74 interrupt status monitor register	—

2.13 Event Link Controllers

Table 2.22 shows a Comparative Overview of Event Link Controllers, Table 2.23 shows a Comparison of Event Link Controller Registers, Table 2.24 shows a Correspondence Between the ELSRn Registers and Peripheral Modules, and Table 2.25 shows a Correspondence between Event Signal Names and Signal Numbers set in ELSRn.ELS[7:0].

Table 2.22 Comparative Overview of Event Link Controllers

Item	RX660 (ELC)	RX261 (ELC)
Event link function	• Event signals of 83 types can be directly linked to peripheral modules. • An operation to be executed at event signal input can be selected for timer peripheral modules. • Event link operation is possible for port B and port E. — Single port: An event link operation can be set for a specified single port. — Port group: An event link operation can be specified for a group of ports selected from a maximum of 8 ports.	• Event signals of 116 types can be directly linked to peripheral modules. • An operation to be executed at event signal input can be selected for timer peripheral modules. • Event link operation is possible for port B and port E. — Single port: An event link operation can be set for a specified single port. — Port group: An event link operation can be specified for a group of ports selected from a maximum of 8 ports.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.23 Comparison of Event Link Controller Registers

Register	Bit	RX660 (ELC)	RX261 (ELC)
ELSRn	—	Event link setting register n (n = 0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 32, 56)	Event link setting register n (n = 7, 8, 10, 12, 14 to 16, 18 to 28, 48 to 56)
	ELS[7:0]	Event link select bits 00h: Event output to the target peripheral module is disabled. 01h to F1h: Specify the number for the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the target peripheral module is disabled. 1Fh to C6h: Specify the number for the event signal to be linked. Settings other than the above are prohibited.
ELOPA	—	Event link option setting register A	—
ELOPB	—	Event link option setting register B	—
ELOPC	LPTMD[1:0]	—	LPT operation select bits
ELOPD	TMR1MD [1:0]	TMR1 operation select bits	—
ELOPD	TMR3MD [1:0]	TMR3 operation select bits	—
ELOPE	—	Event link option setting register E	—

Table 2.24 Correspondence Between the ELSRn Registers and Peripheral Modules

Register	RX660 (ELC)	RX261 (ELC)
ELSR0	MTU0	—
ELSR3	MTU3	—
ELSR4	MTU4	—
ELSR7	CMT1	CMT1
ELSR8	—	ICU (LPT-dedicated interrupt)
ELSR10	TMR0	TMR0
ELSR11	TMR1	—
ELSR12	TMR2	TMR2
ELSR13	TMR3	—
ELSR14	—	CTSU
ELSR15	S12AD (ELCTRG00N)	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source is switched to LOCO.	Clock source is switched to LOCO.
ELSR30	MTU6	—
ELSR31	MTU7	—
ELSR32	MTU8	—
ELSR48	—	GPTW event source A (common to all channels)
ELSR49	—	GPTW event source B (common to all channels)
ELSR50	—	GPTW event source C (common to all channels)
ELSR51	—	GPTW event source D (common to all channels)
ELSR52	—	GPTW event source E (common to all channels)
ELSR53	—	GPTW event source F (common to all channels)
ELSR54	—	GPTW event source G (common to all channels)
ELSR55	—	GPTW event source H (common to all channels)
ELSR56	S12AD (ELCTRG01N)	S12AD (ELCTRG01N)

Table 2.25 Correspondence between Event Signal Names and Signal Numbers set in ELSRn.ELS[7:0]

Value of ELS[7:0] Bits	RX660 (ELC)	RX261 (ELC)
01h	MTU0 compare match 0A	—
02h	MTU0 compare match 0B	—
03h	MTU0 compare match 0C	—
04h	MTU0 compare match 0D	—
05h	MTU0 compare match 0E	—
06h	MTU0 compare match 0F	—
07h	MTU0 overflow	—
10h	MTU3 compare match 3A	—
11h	MTU3 compare match 3B	—
12h	MTU3 compare match 3C	—
13h	MTU3 compare match 3D	—
14h	MTU3 overflow	—
15h	MTU4 compare match 4A	—
16h	MTU4 compare match 4B	—
17h	MTU4 compare match 4C	—
18h	MTU4 compare match 4D	—
19h	MTU4 overflow	—
1Ah	MTU4 underflow	—
1Eh	MTU6 compare match 6A	—
1Fh	MTU6 compare match 6B	CMT1 compare match 1
20h	MTU6 compare match 6C	—
21h	MTU6 compare match 6D	—
22h	MTU6 overflow	TMR0 compare match A0
23h	MTU7 compare match 7A	TMR0 compare match B0
24h	MTU7 compare match 7B	TMR0 overflow
25h	MTU7 compare match 7C	—
26h	MTU7 compare match 7D	—
27h	MTU7 overflow	—
28h	MTU7 underflow	TMR2 compare match A2
29h	MTU8 compare match 8A	TMR2 compare match B2
2Ah	MTU8 compare match 8B	TMR2 overflow
2Bh	MTU8 compare match 8C	—
2Ch	MTU8 compare match 8D	—
2Dh	MTU8 overflow	—
2Eh	—	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	—	IWDT underflow or refresh error
32h	—	LPT compare match 0
33h	—	LPT compare match 1
34h	—	S12AD compare condition match
35h	—	S12AD compare condition mismatch
37h	CMT1 compare match 1	—
3Ah	—	SCI5 error (receive error or error signal detection)
3Bh	—	SCI5 receive data full
3Ch	TMR0 compare match A0	SCI5 transmit data empty
3Dh	TMR0 compare match B0	SCI5 transmit end

Value of ELS[7:0] Bits	RX660 (ELC)	RX261 (ELC)
3Eh	TMR0 overflow	—
3Fh	TMR1 compare match A1	—
40h	TMR1 compare match B1	—
41h	TMR1 overflow	—
42h	TMR2 compare match A2	—
43h	TMR2 compare match B2	—
44h	TMR2 overflow	—
45h	TMR3 compare match A3	—
46h	TMR3 compare match B3	—
47h	TMR3 overflow	—
4Eh	—	RIIC0 communication error or event generation
4Fh	—	RIIC0 receive data full
50h	—	RIIC0 transmit data empty
51h	—	RIIC0 transmit end
52h	—	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h	—	RSPI0 idle
54h	—	RSPI0 receive buffer full
55h	—	RSPI0 transmit buffer empty
56h	—	RSPI0 transmit end
58h	—	S12AD A/D conversion end
59h	—	Comparison result change of comparator B0
5Ah	—	Comparison result change of comparator B0/B1
5Bh	—	LVD1 voltage detection
5Ch	—	LVD2 voltage detection
5Dh	—	DMAC0 transfer end
5Eh	—	DMAC1 transfer end
5Fh	—	DMAC2 transfer end
60h	—	DMAC3 transfer end
61h	—	DTC transfer end
62h	—	Oscillation stop detection of clock generation circuit
63h	—	Input edge detection of input port group 1
64h	—	Input edge detection of input port group 2
65h	—	Input edge detection of single input port 0
66h	—	Input edge detection of single input port 1
67h	—	Input edge detection of single input port 2
68h	—	Input edge detection of single input port 3
69h	—	Software event
6Ah	—	DOC data operation condition met
80h	—	GPTW0 compare match A
81h	—	GPTW0 compare match B
82h	—	GPTW0 compare match C
83h	—	GPTW0 compare match D
84h	—	GPTW0 compare match E
85h	—	GPTW0 compare match F
86h	—	GPTW0 overflow

Value of ELS[7:0] Bits	RX660 (ELC)	RX261 (ELC)
87h	—	GPTW0 underflow
88h	—	GPTW0 A/D conversion start request A
89h	—	GPTW0 A/D conversion start request B
8Ah	—	GPTW1 compare match A
8Bh	—	GPTW1 compare match B
8Ch	—	GPTW1 compare match C
8Dh	—	GPTW1 compare match D
8Eh	—	GPTW1 compare match E
8Fh	—	GPTW1 compare match F
90h	—	GPTW1 overflow
91h	—	GPTW1 underflow
92h	—	GPTW1 A/D conversion start request A
93h	—	GPTW1 A/D conversion start request B
94h	—	GPTW2 compare match A
95h	—	GPTW2 compare match B
96h	—	GPTW2 compare match C
97h	—	GPTW2 compare match D
98h	—	GPTW2 compare match E
99h	—	GPTW2 compare match F
9Ah	—	GPTW2 overflow
9Bh	—	GPTW2 underflow
9Ch	—	GPTW2 A/D conversion start request A
9Dh	—	GPTW2 A/D conversion start request B
9Eh	—	GPTW3 compare match A
9Fh	—	GPTW3 compare match B
A0h	—	GPTW3 compare match C
A1h	—	GPTW3 compare match D
A2h	—	GPTW3 compare match E
A3h	—	GPTW3 compare match F
A4h	—	GPTW3 overflow
A5h	—	GPTW3 underflow
A6h	—	GPTW4 compare match A
A7h	—	GPTW4 compare match B
A8h	—	GPTW4 compare match C
A9h	—	GPTW4 compare match D
AAh	—	GPTW4 compare match E
ABh	—	GPTW4 compare match F
ACh	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	GPTW4 overflow
ADh	—	GPTW4 underflow
AEh	—	GPTW5 compare match A
AFh	IWDT underflow or refresh error	GPTW5 compare match B
B0h	—	GPTW5 compare match C
B1h	—	GPTW5 compare match D
B2h	—	GPTW5 compare match E
B3h	—	GPTW5 compare match F
B4h	—	GPTW5 overflow
B5h	—	GPTW5 underflow
B6h	—	GPTW6 compare match A

Value of ELS[7:0] Bits	RX660 (ELC)	RX261 (ELC)
B7h	—	GPTW6 compare match B
B8h	SCI5 error (receive error or error signal detection)	GPTW6 compare match C
B9h	SCI5 receive data full	GPTW6 compare match D
BAh	SCI5 transmit data empty	GPTW6 compare match E
BBh	SCI5 transmit end	GPTW6 compare match F
BCh	—	GPTW6 overflow
BDh	—	GPTW6 underflow
BEh	—	GPTW7 compare match A
BFh	—	GPTW7 compare match B
C0h	—	GPTW7 compare match C
C1h	—	GPTW7 compare match D
C2h	—	GPTW7 compare match E
C3h	—	GPTW7 compare match F
C4h	—	GPTW7 overflow
C5h	—	GPTW7 underflow
C6h	—	GPTW (OPS) U-/V-/W-phase input edge detected
CCh	RIIC0 communication error or event generation	—
CDh	RIIC0 receive data full	—
CEh	RIIC0 transmit data empty	—
CFh	RIIC0 transmit end	—
D0h	RSPI0 error (mode fault, overrun, underrun, or parity error)	—
D1h	RSPI0 idle	—
D2h	RSPI0 receive buffer full	—
D3h	RSPI0 transmit buffer empty	—
D4h	RSPI0 transmit end	—
D6h	S12AD A/D conversion end	—
DCh	Comparison result change of comparator C0	—
DDh	Comparison result change of comparator C1	—
DEh	Comparison result change of comparator C2	—
DFh	Comparison result change of comparator C3	—
E2h	LVD1 voltage detection	—
E3h	LVD2 voltage detection	—
E4h	DMAC0 transfer end	—
E5h	DMAC1 transfer end	—
E6h	DMAC2 transfer end	—
E7h	DMAC3 transfer end	—
E8h	DTC transfer end	—
E9h	Oscillation stop detection of clock generation circuit	—
EAh	Input edge detection of input port group 1	—
EBh	Input edge detection of input port group 2	—
ECh	Input edge detection of single input port 0	—

Value of ELS[7:0] Bits	RX660 (ELC)	RX261 (ELC)
EDh	Input edge detection of single input port 1	—
EEh	Input edge detection of single input port 2	—
EFh	Input edge detection of single input port 3	—
F0h	Software event	—
F1h	DOC data operation condition met	—
Settings other than the above are prohibited.		

2.14 I/O Ports

Table 2.26 to Table 2.29 show a comparative overview of I/O ports, Table 2.30 shows a Comparison of I/O Port Functions, Table 2.31 shows a Comparison of Driving Ability Switching on I/O Ports, and Table 2.32 shows a Comparison of I/O Port Registers.

Table 2.26 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX660 (100-Pin)	RX261 (100-Pin)
PORT0	P03 to P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTG	Not available	PG7
PORTH*1	PH0 to PH3, PH6, PH7	PH0, PH3, PH6, PH7
PORTJ	PJ1, PJ3, PJ6, PJ7	PJ1, PJ3, PJ6, PJ7
PORTN	PN6	—

Note: 1. There are ports PH1 and PH2 on the RX260.

Table 2.27 Comparative Overview of I/O Ports (80-Pin)

Port Symbol	RX660 (80-Pin)	RX261 (80-Pin)
PORT0	P03 to P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20, P21, P26, P27	P20, P21, P26, P27
PORT3	P30 to P32, P34 to P37	P30 to P32, P34 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0 to PA6	PA0 to PA6
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTD	PD0 to PD2	PD0 to PD2
PORTE	PE0 to PE5	PE0 to PE5
PORTG	Not available	PG7
PORTH*1	PH0 to PH3, PH6, PH7	PH0, PH3, PH6, PH7
PORTJ	PJ1, PJ6, PJ7	PJ1, PJ6, PJ7
PORTN	PN6	—

Note: 1. There are ports PH1 and PH2 on the RX260.

Table 2.28 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX660 (64-Pin)	RX261 (64-Pin)
PORT0	P03, P07	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	Not available	PG7
PORTH*1	PH0 to PH3, PH6, PH7	PH0, PH3, PH6, PH7
PORTJ	PJ6, PJ7	PJ6, PJ7
PORTN	PN6	—

Note: 1. There are ports PH1 and PH2 on the RX260.

Table 2.29 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX660 (48-Pin)	RX261 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P45 to P47	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	Not available	PG7
PORTH*1	PH0 to PH3	PH0, PH3
PORTJ	PJ6, PJ7	PJ6, PJ7
PORTN	PN6	—

Note: 1. There are ports PH1 and PH2 on the RX260.

Table 2.30 Comparison of I/O Port Functions

Item	Port Symbol	RX660	RX261
Input pull-up function	PORT0	P00 to P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34,P36,P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P56	P50 to P55
	PORT6	P60 to P67	—
	PORT7	P70 to P77	—
	PORT8	P80 to P83, P86, P87	—
	PORT9	P90 to P93	—
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5 to PF7	—
	PORTG	—	PG7
	PORTH*1	PH0 to PH3, PH6, PH7	PH0, PH3
	PORTJ	PJ1, PJ3 to PJ5, PJ6, PJ7	PJ1, PJ3, PJ6, PJ7
	PORTK	PK2 to PK5	—
	PORTL	PL0, PL1	—
	PORTN	PN6, PN7	—
Open drain output function	PORT0	P00 to P07	—
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34,P36, P37	P30 to P34,P36,P37
	PORT4	P40 to P47	—
	PORT5	P50 to P56	P50 to P52, P54
	PORT6	P60 to P67	—
	PORT7	P70 to P77	—
	PORT8	P80 to P83, P86, P87	—
	PORT9	P90 to P93	—
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF5 to PF7	—
	PORTG	—	PG7
	PORTH	PH0 to PH3, PH6, PH7	—
	PORTJ	PJ1, PJ3 to PJ5, PJ6, PJ7	—
	PORTK	PK2 to PK5	—
	PORTL	PL0, PL1	—
	PORTN	PN6, PN7	—
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17

Note: 1. There are ports PH1 and PH2 on the RX260.

Table 2.31 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX660	RX261
PORT0	Fixed to normal output	P03, P05 to P07	—
	Normal drive/high drive	P00 to P02, P04	—
PORT1	Fixed to normal output	—	—
	Normal drive/high drive	P12 to P17	—
PORT2	Fixed to normal output	—	—
	Normal drive/high drive	P20 to P27	—
PORT3	Fixed to normal output	P36, P37	—
	Normal drive/high drive	P30 to P34	—
PORT4	Fixed to normal output	P40 to P47	—
	Normal drive/high drive	—	—
PORT5	Fixed to normal output	—	—
	Normal drive/high drive	P50 to P56	—
PORT6	Fixed to normal output	—	—
	Normal drive/high drive	P60 to P67	—
PORT7	Fixed to normal output	—	—
	Normal drive/high drive	P70 to P77	—
PORT8	Fixed to normal output	—	—
	Normal drive/high drive	P80 to P83, P86, P87	—
PORT9	Fixed to normal output	—	—
	Normal drive/high drive	P90 to P93	—
PORTA	Fixed to normal output	—	—
	Normal drive/high drive	PA0 to PA7	—
PORTB	Fixed to normal output	—	—
	Normal drive/high drive	PB0 to PB7	—
PORTC	Fixed to normal output	—	—
	Normal drive/high drive	PC0 to PC7	—
PORTD	Fixed to normal output	—	—
	Normal drive/high drive	PD0 to PD7	—
PORTE	Fixed to normal output	—	—
	Normal drive/high drive	PE0 to PE7	—
PORTF	Fixed to normal output	—	—
	Normal drive/high drive	PF5 to PF7	—
PORTH	Fixed to normal output	—	—
	Normal drive/high drive	PH0 to PH3, PH6, PH7	—
PORTJ	Fixed to normal output	PJ6, PJ7	—
	Normal drive/high drive	PJ1, PJ3 to PJ5	—
PORTK	Fixed to normal output	—	—
	Normal drive/high drive	PK2 to PK5	—
PORTL	Fixed to normal output	—	—
	Normal drive/high drive	PL0, PL1	—
PORTN	Fixed to normal output	—	—
	Normal drive/high drive	PN6, PN7	—

Table 2.32 Comparison of I/O Port Registers

Register	Bit	RX660	RX261
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B6	Pm0 to Pm6 pin mode control bits (m = 0 to 9, A to F, H, J to L, N)	Pm0 to Pm6 pin mode control bits (m = 0 to 5, A to E, G, H, J)
	B7	Pm7 pin mode control bit (m = 0 to 9, A to F, H, J to L, N) b7 0: Use the port as a general-purpose I/O port. 1: Use the port as a peripheral module.	Pm7 pin mode control bit (m = 0 to 5, A to E, G, H, J) • PG7 b7 0: Use the port as a general-purpose I/O port. 1: Use the port as the MD function (initial value). • Others b7 0: Use the port as a general-purpose I/O port. (initial value) 1: Use the port as a peripheral function.
ODR0	B2	Pm1 output type select bit (m = 0 to 9, A to E, H, J to L) 0: CMOS output 1: N-channel open drain	Pm1 output type select bit (m = 1 to 3, 5, A to E, J) • P21, P31, P51, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N-channel open drain • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited
	B3	—	Pm1 output type select bit (m = 1 to 3, 5, A to E,J) • P21, P31, P51, PA1, PB1, PC1, PD1 b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited

Register	Bit	RX660	RX261
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 5, A to C, E, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
PSRA	—	—	Port switching register A
PSRB	—	—	Port switching register B
PRWCNTR	—	—	Port read wait control register
DSCR	—	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)	—

2.15 Multi-Function Pin Controller

Table 2.33 shows a Comparison of Multiplexed Pin Assignments, and Table 2.35 to Table 2.53 show a Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, **orange text** indicates pins that are present in the RX660 Group only, and **blue text** indicates pins that are present in the RX261 Group only. A circle (○) indicates that a function is assigned to the pin, a cross (×) indicates that the pin is not present or that no function is assigned, and grayed out items indicate functions that are not implemented.

Table 2.33 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○	○				
	IRQ0 (input)	P30	×	×	×	×	○	○	○	○
		P50	○	×	×	×	×	×	×	×
		PA0	○	○	○	×	×	×	×	×
		PD0	○	○	×	×	○	○	×	×
		PH1	○	○	○	○	○	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○				
	IRQ1 (input)	P51	○	×	×	×	×	×	×	×
		PD1	○	○	×	×	○	○	×	×
		PH2	○	○	○	○	○	○	○	○
		P31	×	×	×	×	○	○	○	○
	IRQ2-DS (input)	P32	○	○	○	×				
	IRQ2 (input)	P12	○	○	×	×	○	○	×	×
		P52	○	×	×	×	×	×	×	×
		PB2	○	○	×	×	×	×	×	×
		PD2	○	○	×	×	○	○	×	×
		P32	×	×	×	×	○	○	○	×
		P36	×	×	×	×	○	○	○	○
	IRQ3-DS (input)	P33	○	×	×	×				
	IRQ3 (input)	P13	○	○	×	×	○	○	×	×
		P23	○	×	×	×	×	×	×	×
		P53	○	×	×	×	×	×	×	×
		PB3	○	○	○	○	×	×	×	×
		PD3	○	×	×	×	○	×	×	×
		P33	×	×	×	×	○	×	×	×
	IRQ4-DS (input)	PB1	○	○	○	○				
	IRQ4 (input)	P14	○	○	○	○	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		P37	○	○	○	○	○	○	○	○
		P54	○	○	○	×	×	×	×	×
		PB4	○	○	×	×	×	×	×	×
		PD4	○	×	×	×	○	×	×	×
		PB1	×	×	×	×	○	○	○	○
	IRQ5-DS (input)	PA4	○	○	○	○				
	IRQ5 (input)	P15	○	○	○	○	○	○	○	○
		P25	○	×	×	×	×	×	×	×
		P36	○	○	○	○	×	×	×	×

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	IRQ5 (input)	PA5	○	○	×	×	×	×	×	×
		PC5	○	○	○	○	×	×	×	×
		PD5	○	×	×	×	○	×	×	×
		PE5	○	○	○	×	○	○	○	×
		PA4	×	×	×	×	○	○	○	○
	IRQ6-DS (input)	PA3	○	○	○	○				
	IRQ6 (input)	P16	○	○	○	○	○	○	○	○
		P26	○	○	○	○	×	×	×	×
		PB6	○	○	○	×	×	×	×	×
		PD6	○	×	×	×	○	×	×	×
		PE6	○	×	×	×	○	×	×	×
		PA3	×	×	×	×	○	○	○	○
	IRQ7-DS (input)	PE2	○	○	○	○				
	IRQ7 (input)	P17	○	○	○	○	○	○	○	○
		P27	○	○	○	○	×	×	×	×
		PA7	○	×	×	×	×	×	×	×
		PD7	○	×	×	×	○	×	×	×
		PE7	○	×	×	×	○	×	×	×
		PE2	×	×	×	×	○	○	○	○
	IRQ8-DS (input)	P40	○	○	○	○				
	IRQ8 (input)	P20	○	○	×	×				
		PE0	○	○	○	×				
	IRQ9-DS (input)	P41	○	○	○	○				
	IRQ9 (input)	P21	○	○	×	×				
		PE1	○	○	○	○				
	IRQ10-DS (input)	P42	○	○	○	○				
	IRQ10 (input)	P55	○	○	○	×				
		PA2	○	○	×	×				
		PC2	○	○	○	×				
	IRQ11-DS (input)	P43	○	○	○	×				
	IRQ11 (input)	P03	○ *1	○	○	×				
		PA1	○	○	○	○				
		PC3	○	○	○	×				
		PE3	○	○	○	○				
		PJ3	○	×	×	×				
	IRQ12-DS (input)	P44	○	○	○	×				
	IRQ12 (input)	P24	○	×	×	×				
		PB0	○	○	○	○				
		PC1	○	×	×	×				
		PC4	○	○	○	○				
		PE4	○	○	○	○				
	IRQ13-DS (input)	P45	○	○	○	○				
	IRQ13 (input)	P05	○	○	×	×				
		PB5	○	○	○	○				
		PC6	○	○	○	○				
	IRQ14-DS (input)	P46	○	○	○	○				
	IRQ14 (input)	PA6	○	○	○	○				
		PC0	○	×	×	×				
		PC7	○	○	○	○				

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Interrupt	IRQ15-DS (input)	P47	○	○	○	○				
	IRQ15 (input)	P07	○	○	○	×				
		P22	○	×	×	×				
		PB7	○	○	○	×				
Multi-function timer unit 3	MTIOC0A (input/output)	P34	○	○	×	×				
		PB3	○	○	○	○				
		PC4	○	○	○	○				
	MTIOC0B (input/output)	P13	○	○	×	×				
		P15	○	○	○	○				
		PA1	○	○	○	○				
	MTIOC0C (input/output)	P32	○	○	○	×				
		PB1	○	○	○	○				
		PC5	○	○	○	○				
	MTIOC0D (input/output)	P33	○	×	×	×				
		PA3	○	○	○	○				
	MTIOC1A (input/output)	P20	○	○	×	×				
		PE4	○	○	○	○				
	MTIOC1B (input/output)	P21	○	○	×	×				
		PB5	○	○	○	○				
		PE3	○	○	○	○				
	MTIOC2A (input/output)	P26	○	○	○	○				
		PB5	○	○	○	○				
	MTIOC2B (input/output)	P27	○	○	○	○				
		PE5	○	○	○	×				
	MTIOC3A (input/output)	P14	○	○	○	○				
		P17	○	○	○	○				
		PC1	○	×	×	×				
		PC7	○	○	○	○				
		PJ1	○	○	×	×				
	MTIOC3B (input/output)	P17	○	○	○	○				
		P22	○	×	×	×				
		PA1	○	○	○	○				
		PB7	○	○	○	×				
		PC5	○	○	○	○				
		PE1	○	○	○	○				
		PH0	○	○	○	○				
	MTIOC3C (input/output)	P16	○	○	○	○				
		PC0	○	×	×	×				
		PC6	○	○	○	○				
		PJ3	○	×	×	×				
	MTIOC3D (input/output)	P16	○	○	○	○				
		P23	○	×	×	×				
		PA6	○	○	○	○				
		PB0	○	○	○	○				
		PB6	○	○	○	×				
		PC4	○	○	○	○				
		PE0	○	○	○	×				
		PH1	○	○	○	○				

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTIOC4A (input/output)	P21	○	○	×	×				
		P24	○	×	×	×				
		P55	○	○	○	×				
		PA0	○	○	○	×				
		PB3	○	○	○	○				
		PE2	○	○	○	○				
		PE4	○	○	○	○				
	MTIOC4B (input/output)	P17	○	○	○	○				
		P30	○	○	○	○				
		P54	○	○	○	×				
		PC2	○	○	○	×				
		PD1	○	○	×	×				
		PE3	○	○	○	○				
	MTIOC4C (input/output)	P25	○	×	×	×				
		PA4	○	○	○	○				
		PB1	○	○	○	○				
		PE1	○	○	○	○				
		PE5	○	○	○	×				
		PH2	○	○	○	○				
	MTIOC4D (input/output)	P31	○	○	○	○				
		P55	○	○	○	×				
		PA3	○	○	○	○				
		PC3	○	○	○	×				
		PD2	○	○	×	×				
		PE4	○	○	○	○				
		PH3	○	○	○	○				
	MTIC5U (input)	P12	○	○	×	×				
		PA4	○	○	○	○				
		PD7	○	×	×	×				
	MTIC5V (input)	PA3	○	○	○	○				
		PA6	○	○	○	○				
		PD6	○	×	×	×				
	MTIC5W (input)	PB0	○	○	○	○				
		PD5	○	×	×	×				
	MTIOC6A (input/output)	PE7	○	×	×	×				
	MTIOC6B (input/output)	PA5	○	○	×	×				
		PA6	○	○	○	×				
	MTIOC6C (input/output)	PE6	○	×	×	×				
	MTIOC6D (input/output)	PA0	○	○	○	×				
	MTIOC7A (input/output)	PA2	○	○	×	×				
		PE2	○	○	○	○				
	MTIOC7B (input/output)	PA1	○	○	○	○				
	MTIOC7C (input/output)	PA4	○	○	○	○				
	MTIOC7D (input/output)	PE4	○	○	○	○				
	MTIOC8A (input/output)	PD6	○	×	×	×				
	MTIOC8B (input/output)	PD4	○	×	×	×				
	MTIOC8C (input/output)	PD5	○	×	×	×				
	MTIOC8D (input/output)	PD3	○	×	×	×				

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Multi-function timer unit 3	MTCLKA (input)	P14	○	○	○	○				
		P24	○	×	×	×				
		PA4	○	○	○	○				
		PC6	○	○	○	○				
	MTCLKB (input)	P15	○	○	○	○				
		P25	○	×	×	×				
		PA6	○	○	○	○				
		PC7	○	○	○	○				
	MTCLKC (input)	P22	○	×	×	×				
		PA1	○	○	○	○				
		PC4	○	○	○	○				
	MTCLKD (input)	P23	○	×	×	×				
		PA3	○	○	○	○				
		PC5	○	○	○	○				
Port output enable 3	POE0# (input)	P32	○	○	○	×				
		PC4	○	○	○	○				
		PD1	○	○	×	×				
		PD7	○	×	×	×				
	POE4# (input)	P33	○	×	×	×				
		PB5	○	○	○	○				
		PD0	○	○	×	×				
		PD6	○	×	×	×				
	POE8# (input)	P17	○	○	○	○				
		P30	○	○	○	○				
		PD3	○	×	×	×				
		PE3	○	○	○	○				
	POE10# (input)	P32	○	○	○	×				
		P34	○	○	×	×				
		PA6	○	○	○	○				
		PD5	○	×	×	×				
	POE11# (input)	P33	○	×	×	×				
		PB3	○	○	○	○				
		PD4	○	×	×	×				
8-bit timer	TMO0 (output)	P22	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
		PH1	○	○	○	○	○	○	○	○
	TMCI0 (input)	P21	○	○	×	×	○	○	×	×
		PB1	○	○	○	○	○	○	○	○
		PH3	○	○	○	○	○	○	○	○
	TMRI0 (input)	P20	○	○	×	×	○	○	×	×
		PA4	○	○	○	○	○	○	○	○
		PH2	○	○	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	TMCI1 (input)	P12	○	○	×	×	○	○	×	×
		P54	○	○	○	×	○	○	○	×
		PC4	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
8-bit timer	TMRI1 (input)	P24	○	×	×	×	○	×	×	×
		PB5	○	○	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○	○	○
		PC7	○	○	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	×	×	○	○	×	×
		P32	○	○	○	×	○	○	○	×
		P55	○	○	○	×	○	○	○	×
	TMCI3 (input)	P27	○	○	○	×	○	○	○	○
		P34	○	○	×	×	○	○	×	×
		PA6	○	○	○	×	○	○	○	○
	TMRI3 (input)	P30	○	○	○	×	○	○	○	○
		P33	○	×	×	×	○	×	×	×
Compare match timer W	TOC0 (output)	PC7	○	○	○	○				
	TIC0 (input)	PC6	○	○	○	○				
	TOC1 (output)	PE7	○	×	×	×				
		PH2	○	○	○	○				
	TIC1 (input)	PE6	○	×	×	×				
		PH1	○	○	○	○				
	TOC2 (output)	PB5	○	○	○	○				
		PD3	○	×	×	×				
	TIC2 (input)	PB3	○	○	○	○				
		PD2	○	○	×	×				
	TOC3 (output)	PE3	○	○	○	○				
	TIC3 (input)	PE2	○	○	○	○				
Realtime Clock	RTCOUT output	P16	○	○	○	×	○	○	○	×
		P32	○	○	○	×	○	○	○	×
	RTCIC0 (input)*2, *3	P30	○	○	○	×	○	○	○	×
	RTCIC1 (input)*2, *3	P31	○	○	○	×	○	○	○	×
	RTCIC2 (input)*2, *3	P32	○	○	○	×	○	○	○	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	×	×				
		P33	○	×	×	×				
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○	×	×				
		P32	○	○	×	×				
	SCK0 (input/output)	P22	○	×	×	×				
		P34	○	○	×	×				
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	×	×	×				
		PJ3	○	×	×	×				
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○	○	○
		P30	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○	○	○
		P26	○	○	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○	○	○
		P27	○	○	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○	○	○
		P31	○	○	○	○	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	×	×	×				
		P52	○	×	×	×				
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	○	×	×	×				
		P50	○	×	×	×				
	SCK2 (input/output)	P51	○	×	×	×				
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	×	×	×				
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○	○				
		P25	○	×	×	×				
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	○	○	○	○				
		P23	○	×	×	×				
	SCK3 (input/output)	P15	○	○	○	○				
		P24	○	×	×	×				
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○	○				
	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	○	○	○				
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	○	○	○	○				
	SCK4 (input/output)	PB3	○	○	○	○				
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	○	×	×				
		PE6	○	×	×	×				
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	×	×	○	○	×	×
		PA3	○	○	○	○	○	○	○	○
		PC2	○	○	○	×	○	○	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC3	○	○	○	×	○	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
		PC4	○	○	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○	○	○
		PC0	○	×	×	×	○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P33	○	×	×	×	○	×	×	×
		PB0	○	○	○	○	○	○	○	○
		PD1	×	×	×	×	○	○	×	×
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	○	○	×	○	○	○	×
		PB1	○	○	○	○	○	○	○	○
		PD0	×	×	×	×	○	○	×	×
	SCK6 (input/output)	P34	○	○	×	×	○	○	×	×
		PB3	○	○	○	○	○	○	○	○
		PD2	×	×	×	×	○	○	×	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	×	×	○	○	×	×
		PJ3	○	×	×	×	○	×	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○				
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○				
	SCK8 (input/output)	PC5	○	○	○	○				
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○				
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	×				
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○	×				
	SCK9 (input/output)	PB5	○	○	○	×				
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	○	×	×				
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	PC6	○	○	○	○				
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	PC7	○	○	○	○				
	SCK10 (input/output)	PC5	○	○	○	○				
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○				
	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	PB6	○	○	○	×				
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	PB7	○	○	○	×				
	SCK11 (input/output)	PB5	○	○	○	×				

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	×	×				
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PA2	○	○	×	×	×	×	×	×
		PE2	○	○	○	○	○	○	○	○ *5
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PA4	○	○	○	○	×	×	×	×
		PE1	○	○	○	○	○	○	○	○ *6
	SCK12 (input/output)	PA1	○	○	○	○	×	×	×	×
		PE0	○	○	○	×	○	○	○	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PA6	○	○	○	○	×	×	×	×
		PE3	○	○	○	○	○	○	○	○ *7
	RXD000 (input)/ SMISO000 (input/output)/ SSCL000 (input/output)	P21					○	○	×	×
	TXD000 (output)/ TXDA000 (output)/ SMOSI000 (input/output)/ SSDA000 (input/output)	P20					○	○ *8	×	×
	SCK000 (input/output)	P22					○	×	×	×
	TXDB000 (output)	P22					○	×	×	×
	CTS000# (input)/ RTS000# (output)/ SS000# (input)	P23					○	×	×	×
	DE000 (output)	P23					○	×	×	×
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	PC6					○	○	○	○
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	PC7					○	○	○	○
	SCK008 (input/output)	PC5					○	○	○	○
	TXDB008 (output)	PC5					○	○	○	○
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	PC4					○	○	○	○
	DE008 (output)	PC4					○	○	○	○
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	PB6					○	○	○	×
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	PB7					○	○	○	×
	SCK009 (input/output)	PB5					○	○	○	×
	TXDB009 (output)	PB5					○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial communications interface	CTS009# (input)/ RTS009# (output)/ SS009# (input)	PB4					○	○	×	×
	DE009 (output)	PB4					○	○	×	×
	RXD010 (input)/ SMISO010 (input/output)/ SSCL010 (input/output)	PC6	○	○	○	○				
	TXD010 (output)/ SMOSI010 (input/output)/ SSDA010 (input/output)	PC7	○	○	○	○				
	SCK010 (input/output)	PC5	○	○	○	○				
	CTS010# (input)/ RTS010# (output)/ SS010# (input)/ DE010 (output)	PC4	○	○	○	○				
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	PB6	○	○	○	×				
		PC0	○	×	×	×				
	TXD011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	PB7	○	○	○	×				
		PC1	○	×	×	×				
	SCK011 (input/output)	PB5	○	○	○	×				
	TXDA011 (output)	PC1	○	×	×	×				
	TXDB011 (output)	PC2	○	○	○	×				
	CTS011# (input)/ RTS011# (output)/ SS011# (input)/ DE011 (output)	PB4	○	○	×	×				
I²C Bus Interface	SCL0 (input/output)	P12	○	○	×	×	○	○	×	×
		P16	×	×	×	×	○	○	○	○
	SDA0 (input/output)	P13	○	○	×	×	○	○	×	×
		P17	×	×	×	×	○	○	○	○
	SCL2 (input/output)	P16	○	○	○	○				
	SDA2 (input/output)	P17	○	○	○	○				
CAN FD module	CRX0 (input)	P15	○	○	○	○	○	○	○	○
		P33	○	×	×	×	○	×	×	×
		P55	○	○	○	×	○	○	○	×
		PD2	○	○	×	×	○	○	×	×
	CTX0 (output)	P14	○	○	○	○	○	○	○	○
		P32	○	○	○	×	○	○	○	×
		P54	○	○	○	×	○	○	○	×
		PD1	○	○	×	×	○	○	×	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	×	○	○	×	×
		PB0	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○	○	○
		PA6	○	○	○	○	○	○	○	○
		PC6	○	○	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Serial peripheral interface	MISOA (input/output)	P17	○	○	○	○	○	○	○	○
		PA7	○	×	×	×	○	×	×	×
		PC7	○	○	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○	○	○
		PC4	○	○	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	○	×	○	○	○	×
		PC0	○	×	×	×	○	×	×	×
	SSLA2 (output)	PA1	○	○	○	○	○	○	○	○
		PC1	○	×	×	×	○	×	×	×
	SSLA3 (output)	PA2	○	○	×	×	○	○	×	×
		PC2	○	○	○	×	○	○	○	×
12-bit A/D converter	AN000 (input)*3	P40	○	○	○	○	○	○	○	○
	AN001 (input)*3	P41	○	○	○	○	○	○	○	○
	AN002 (input)*3	P42	○	○	○	○	○	○	○	○
	AN003 (input)*3	P43	○	○	○	×	○	○	○	×
	AN004 (input)*3	P44	○	○	○	×	○	○	○	×
	AN005 (input)*3	P45	○	○	○	○	○	○	○	○
	AN006 (input)*3	P46	○	○	○	○	○	○	○	○
	AN007 (input)*3	P47	○	○	○	○	○	○	○	○
	AN008 (input)*3	PE0	○	○	○	×				
	AN009 (input)*3	PE1	○	○	○	○				
	AN010 (input)*3	PE2	○	○	○	○				
	AN011 (input)*3	PE3	○	○	○	○				
	AN012 (input)*3	PE4	○	○	○	○				
	AN013 (input)*3	PE5	○	○	○	×				
	AN014 (input)*3	PE6	○	×	×	×				
	AN015 (input)*3	PE7	○	×	×	×				
	AN016 (input)*3	PD0	○	○	×	×	×	×	×	×
		PE0	×	×	×	×	○	○	○	×
	AN017 (input)*3	PD1	○	○	×	×	×	×	×	×
		PE1	×	×	×	×	○	○	○	○
	AN018 (input)*3	PD2	○	○	×	×	×	×	×	×
		PE2	×	×	×	×	○	○	○	○
	AN019 (input)*3	PD3	○	×	×	×	×	×	×	×
		PE3	×	×	×	×	○	○	○	○
	AN020 (input)*3	PD4	○	×	×	×	×	×	×	×
		PE4	×	×	×	×	○	○	○	○
	AN021 (input)*3	PD5	○	×	×	×	×	×	×	×
		PE5	×	×	×	×	○	○	○	×
	AN022 (input)*3	PD6	○	×	×	×	×	×	×	×
		PE6	×	×	×	×	○	×	×	×
	AN023 (input)*3	PD7	○	×	×	×	×	×	×	×
		PE7	×	×	×	×	○	×	×	×
	AN024 (input)*3	PD0					○	○	×	×
	AN025 (input)*3	PD1					○	○	×	×
	AN026 (input)*3	PD2					○	○	×	×
	AN027 (input)*3	PD3					○	×	×	×
	AN028 (input)*3	PD4					○	×	×	×
	AN029 (input)*3	PD5					○	×	×	×
	AN030 (input)*3	PD6					○	×	×	×
	AN031 (input)*3	PD7					○	×	×	×

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
12-bit A/D converter	ADST0 (output)	PA4	○	○	○	○				
		PH1	○	○	○	○				
	ADTRG0# (input)	P07	○	○	○	×	○	○	×	×
		P16	○	○	○	○	○	○	○	○
		P25	○	×	×	×	○	×	×	×
		PA1	○	○	○	○	×	×	×	×
		PH0	○	○	○	○	×	×	×	×
D/A converter	DA0 (output)*4	P03	○ *1	○	○	×	○	○	○	×
	DA1 (output)*4	P05	○	○	×	×	○	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	○	×	○	○	○	×
		PC7	○	○	○	○	○	○	○	○
		PH0	○	○	○	○	○	○	○	○
Remote control signal receiver	PMC0 (input)	P51	○	×	×	×	○	×	×	×
		P53	○	×	×	×	○	×	×	×
		PB3	○	○	○	○	○	○	○	○
		PC3	○	○	○	×	○	○	○	×
		PC4	○	○	○	○	○	○	○	○
		PC5	○	○	○	○	○	○	○	○
Comparator C	CMPC00 (input)	PE1	○	○	○	○				
	CMPC10 (input)	PA3	○	○	○	○				
	CMPC20 (input)	P15	○	○	○	○				
	CMPC30 (input)	P26	○	○	○	○				
	COMP0 (output)	PE5	○	○	○	×				
	COMP1 (output)	PB1	○	○	○	○				
	COMP2 (output)	P17	○	○	○	○				
	COMP3 (output)	P30	○	○	○	○				
	CVREFC0 (input)	PE2	○	○	○	○				
	CVREFC1 (input)	PA4	○	○	○	○				
	CVREFC2 (input)	P14	○	○	○	○				
	CVREFC3 (input)	P27	○	○	○	○				
Clock generation circuit	CLKOUT (output)	PE3					○	○	○	○
		PE4					○	○	○	○
General-purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P17					○	○	○	○
		P22					○	×	×	×
		PA0					○	○	○	×
		PA1					○	○	○	○
		PB7					○	○	○	×
		PC5					○	○	○	○
		PH0					○	○	○	○
	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P16					○	○	○	○
		P17					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PA6					○	○	○	○
		PB0					○	○	○	○
		PB6					○	○	○	×
		PC4					○	○	○	○
		PH1					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P24					○	×	×	×
		P32					○	○	○	×
		P55					○	○	○	×
		PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P25					○	×	×	×
		P33					○	×	×	×
		PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
		PE5					○	○	○	×
		PH2					○	○	○	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P21					○	○	×	×
		P30					○	○	○	○
		P54					○	○	○	×
		PB0					○	○	○	○
		PC2					○	○	○	×
		PD1					○	○	×	×
		PE3					○	○	○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P20					○	○	×	×
		P31					○	○	○	○
		P55					○	○	○	×
		PA3					○	○	○	○
		PB1					○	○	○	○
		PC3					○	○	○	×
		PD2					○	○	×	×
		PE4					○	○	○	○
		PH3					○	○	○	○
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P22					○	×	×	×
		P34					○	○	×	×
		PB2					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P13					○	○	×	×
		P15					○	○	○	○
		P23					○	×	×	×
		PA1					○	○	○	○
		PB3					○	○	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P20					○	○	×	×
		PA4					○	○	○	○
		PE4					○	○	○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P16					○	○	○	○
		P21					○	○	×	×
		PA5					○	○	×	×
		PB5					○	○	○	○
		PE3					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P26					○	○	○	○
		PA6					○	○	○	○
		PB5					○	○	○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P15					○	○	○	○
		P27					○	○	○	○
		PA7					○	×	×	×
		PE5					○	○	○	×
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P14					○	○	○	○
		P17					○	○	○	○
		P25					○	×	×	×
		PB4					○	○	×	×
		PC1					○	×	×	×
		PC7					○	○	○	○
		PJ1					○	○	×	×
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P16					○	○	○	○
		P24					○	×	×	×
		PB5					○	○	○	○
		PC0					○	×	×	×
		PC6					○	○	○	○
		PJ3					○	×	×	×
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P13					○	○	×	×
		P32					○	○	○	×
		PB1					○	○	○	○
		PB6					○	○	○	×
		PC5					○	○	○	○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P14					○	○	○	○
		P33					○	×	×	×
		PA3					○	○	○	○
		PB7					○	○	○	×
	GTETRGA (input)	P14					○	○	○	○
		P24					○	×	×	×
		PA4					○	○	○	○
		PC2					○	○	○	×
		PC6					○	○	○	○
	GTETRGB (input)	P15					○	○	○	○
		P25					○	×	×	×
		PA3					○	○	○	○
		PA6					○	○	○	○
		PC3					○	○	○	×
		PC7					○	○	○	○
	GTETRGC (input)	P16					○	○	○	○
		P22					○	×	×	×
		PA1					○	○	○	○
		PB2					○	○	×	×
		PC0					○	×	×	×
		PC4					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
General-purpose PWM timer	GTETRGD (input)	P17					○	○	○	○
		P23					○	×	×	×
		PA3					○	○	○	○
		PB3					○	○	○	○
		PC1					○	×	×	×
		PC5					○	○	○	○
	GTCPPO0 (output)	P14					○	○	○	○
		P17					○	○	○	○
		PC1					○	×	×	×
		PC7					○	○	○	○
		PJ1					○	○	×	×
	GTIU (input)	P34					○	○	×	×
		PB3					○	○	○	○
		PC4					○	○	○	○
	GTIV (input)	P13					○	○	×	×
		P15					○	○	○	○
		PA1					○	○	○	○
	GTIW (input)	P32					○	○	○	×
		PB1					○	○	○	○
		PC5					○	○	○	○
	GTOULO (output)	P16					○	○	○	○
		PA6					○	○	○	○
		PC4					○	○	○	○
		PH1					○	○	○	○
	GTOUUP (output)	P17					○	○	○	○
		PA1					○	○	○	○
		PC5					○	○	○	○
		PH0					○	○	○	○
	GTOVLO (output)	PA3					○	○	○	○
		PA4					○	○	○	○
		PB1					○	○	○	○
		PE1					○	○	○	○
	GTOVUP (output)	PA0					○	○	○	×
		PB3					○	○	○	○
		PE2					○	○	○	○
		PE4					○	○	○	○
	GTOWLO (output)	P31					○	○	○	○
		PA3					○	○	○	○
		PB1					○	○	○	○
		PE4					○	○	○	○
	GTOWUP (output)	P30					○	○	○	○
		PB0					○	○	○	○
		PC2					○	○	○	×
		PE3					○	○	○	○
Low-power timer	LPTO (output)	P26					○	○	○	○
		PB3					○	○	○	○
		PC7					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
USB 2.0 FS host/function module	USB0_DP (input/output)	PH1*2					○	○	○	○
	USB0_DM (input/output)	PH2*2					○	○	○	○
	USB0_VBUS (input)	P16					○	○	○	○
		PB5					○	○	○	○
	USB0_EXICEN (output)	P21					○	○	×	×
		PC6					○	○	○	○
	USB0_VBUSEN (output)	P16					○	○	○	○
		P24					○	×	×	×
		P26					○	○	○	○
		P32					○	○	○	×
	USB0_OVRCURA (input)	P14					○	○	○	○
	USB0_OVRCURB (input)	P16					○	○	○	○
		P22					○	×	×	×
	USB0_ID (input)	P20					○	○	×	×
		PC5					○	○	○	○
LVD voltage detection input	CMPA2 (input)	PE4					○	○	○	○
Comparator B	CMPB0 (input)*3	PE1					○	○	○	○
	CVREFB0 (input)*3	PE2					○	○	○	○
	CMPOB0 (output)	PE5					○	○	○	×
	CMPB1 (input)*3	PA3					○	○	○	○
	CVREFB1 (input)*3	PA4					○	○	○	○
	CMPOB1 (output)	PB1					○	○	○	○
Capacitive touch sensing unit	TSCAP (—)	PC4					○	○	○	○
	TS0 (input/output)	P32					○	○	○	×
	TS1 (input/output)	P31					○	○	○	○
	TS2 (input/output)	P30					○	○	○	○
	TS3 (input/output)	P27					○	○	○	○
	TS4 (input/output)	P26					○	○	○	○
	TS5 (input/output)	P15					○	○	○	○
	TS6 (input/output)	P14					○	○	○	○
	TS7 (input/output)	PH3					○	○	○	○
	TS8 (input/output)	PH2					○	○	○	○
	TS9 (input/output)	PH1					○	○	○	○
	TS10 (input/output)	PH0					○	○	○	○
	TS11 (input/output)	P55					○	○	○	×
	TS12 (input/output)	P54					○	○	○	×
	TS13 (input/output)	PC7					○	○	○	○
	TS14 (input/output)	PC6					○	○	○	○
	TS15 (input/output)	PC5					○	○	○	○
	TS16 (input/output)	PC3					○	○	○	×
	TS17 (input/output)	PC2					○	○	○	×
	TS18 (input/output)	PB7					○	○	○	×
	TS19 (input/output)	PB6					○	○	○	×
	TS20 (input/output)	PB5					○	○	○	○
	TS21 (input/output)	PB4					○	○	×	×
	TS22 (input/output)	PB3					○	○	○	○
	TS23 (input/output)	PB2					○	○	×	×
	TS24 (input/output)	PB1					○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX660				RX261			
			100-Pin	80-Pin	64-Pin	48-Pin	100-Pin	80-Pin	64-Pin	48-Pin
Capacitive touch sensing unit	TS25 (input/output)	PB0					○	○	○	○
	TS26 (input/output)	PA6					○	○	○	○
	TS27 (input/output)	PA5					○	○	×	×
	TS28 (input/output)	PA4					○	○	○	○
	TS29 (input/output)	PA3					○	○	○	○
	TS30 (input/output)	PA2					○	○	×	×
	TS31 (input/output)	PA1					○	○	○	○
	TS32 (input/output)	PA0					○	○	○	×
	TS33 (input/output)	PE4					○	○	○	○
	TS34 (input/output)	PE3					○	○	○	○
	TS35 (input/output)	PE2					○	○	○	○

Notes: 1. Not available for RX660 Group products with the JTAG interface.
2. Not available for RX660 Group products that do not have a sub-clock oscillator.
3. To use this pin, configure its settings to general input (by setting the PORTm.PDR.Bn and PORTm.PMR.Bn bits to “0”).
4. To use this pin on an RX261 Group product, configure the settings of the pin to general input (by setting the PORTm.PDR.Bn and PORTm.PMR.Bn bits to “0”).
5. The SMISO12 function is not available.
6. The SMOSI12 function is not available.
7. The SS12# function is not available.
8. The TXDA000 function is not available.

Table 2.34 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX660 (n = 0 to 3, 5, 7)	RX261 (n = 3, 5, 7)
P00PFS	PSEL[5:0]	Pin function select bits	—
P01PFS	PSEL[5:0]	Pin function select bits	—
P02PFS	PSEL[5:0]	Pin function select bits	—
P05PFS	PSEL[4:0]	—	Pin function select bits
P0nPFS	ISEL	Interrupt input function select bit	—

Table 2.35 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX660 (n = 2 to 7)	RX261 (n = 2 to 7)
P12PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 01111b: SCL0

Register	Bit	RX660 (n = 2 to 7)	RX261 (n = 2 to 7)
P13PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIV 00101b: TMO3 01111b: SDA0 10100b: GTIOC3B 10101b: GTIOC7A 10110b: GTIOC3B# 10111b: GTIOC7A#
P14PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTX0 10001b: USB0_OVRCURA 10100b: GTIOC6A 10101b: GTIOC7B 10110b: GTIOC6A# 10111b: GTIOC7B# 11000b: GTETRGA 11001b: TS6
P15PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIV 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRX0 10100b: GTIOC3B 10101b: GTIOC5B 10110b: GTIOC3B# 10111b: GTIOC5B# 11000b: GTETRGB 11001b: TS5

Register	Bit	RX660 (n = 2 to 7)	RX261 (n = 2 to 7)
P16PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6B# 00010b: GTETRGC 00011b: GTOULO 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL0 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB 10100b: GTIOC0B 10101b: GTIOC4B 10110b: GTIOC0B# 10111b: GTIOC4B# 11000b: GTIOC6B
P17PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6A# 00010b: GTETRGD 00011b: GTCPPO0 00100b: GTOUUP 00101b: TMO1 01010b: SCK1 01101b: MISOA 01111b: SDA0 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC6A
P1nPFS	ASEL	Analog function select bit	—

Table 2.36 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
P20PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: TXD0/SMOSI0/SSDA0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 01010b: TXD000/TXDA000/ SMOSI000/SSDA000 10001b: USB0_ID 10100b: GTIOC2B 10101b: GTIOC4A 10110b: GTIOC2B# 10111b: GTIOC4A#
P21PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 01010b: RXD000/SMISO000/ SSCL000 10001b: USB0_EXICEN 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B#
P22PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000101b: TMO0 001010b: SCK0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO0 01010b: SCK000 01100b: TXDB000 10001b: USB0_OVRCURB 10100b: GTIOC0A 10101b: GTIOC3A 10110b: GTIOC0A# 10111b: GTIOC3A# 11000b: GTETRGC

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
P23PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS000#/RTS000#/ SS000# 01100b: DE000 10100b: GTIOC0B 10101b: GTIOC3B 10110b: GTIOC0B# 10111b: GTIOC3B# 11000b: GTETRGD
P24PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001010b: SCK3	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI1 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC6B 10110b: GTIOC1A# 10111b: GTIOC6B# 11000b: GTETRGA
P25PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3	Pin function select bits b4 b0 00000b: Hi-Z 01001b: ADTRG0# 10100b: GTIOC1B 10101b: GTIOC6A 10110b: GTIOC1B# 10111b: GTIOC6A# 11000b: GTETRGB

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
P26PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3#	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10001b: USB0_VBUSEN 10100b: GTIOC5A 10110b: GTIOC5A# 11001b: TS4 11011b: LPTO
P27PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 001010b: SCK1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI3 01010b: SCK1 10100b: GTIOC5B 10110b: GTIOC5B# 11001b: TS3
P2nPFS	ISEL	Interrupt input function select bit	—
	ASEL	Analog function select bit	—

Table 2.37 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX660 (n = 0 to 4, 6, 7)	RX261 (n = 0 to 4, 6, 7)
P30PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 00101b: TMRI3 01010b: RXD1/SMISO1/SSCL1 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS2
P31PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 001011b: CTS1#/RTS1#/SS1#	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWLO 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS1
P32PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTIW 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 10000b: CTX0 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC7A 10110b: GTIOC1A# 10111b: GTIOC7A# 11001b: TS0

Register	Bit	RX660 (n = 0 to 4, 6, 7)	RX261 (n = 0 to 4, 6, 7)
P33PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000101b: TMRI3 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 100001b: POE11#	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI3 01011b: RXD6/SMISO6/SSCL6 10000b: CRX0 10100b: GTIOC1B 10101b: GTIOC7B 10110b: GTIOC1B# 10111b: GTIOC7B#
P34PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIU 00101b: TMCI3 01011b: SCK6 10100b: GTIOC3A 10110b: GTIOC3A#
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48-pin) P31: IRQ1-DS (144/100/80/64/48-pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/80/64/48-pin) P31: IRQ1 (100/80/64/48-pin) P32: IRQ2 (100/80/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin) P36: IRQ2 (80/64/48-pin) P37: IRQ4 (80/64/48-pin)

Table 2.38 Comparison of P4n Pin Function Control Registers (P4nPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
P4nPFS	ISEL	Interrupt input function select bit	—

Table 2.39 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX660 (n = 0 to 6)	RX261 (n = 1, 3 to 5)
P50PFS	PSEL[5:0]	Pin function select bits	—
P51PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001010b: SCK2 100110b: PMC0	Pin function select bits b4 b0 00000b: Hi-Z 11100b: PMC0
P52PFS	PSEL[5:0]	Pin function select bits	—
P53PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 100110b: PMC0	Pin function select bits b4 b0 00000b: Hi-Z 11100b: PMC0
P54PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 010000b: CTX0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI1 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS12
P55PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC4A 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 010000b: CRX0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMO3 10000b: CRX0 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11001b: TS11
P56PFS	PSEL[5:0]	Pin function select bits	—
P5nPFS	ISEL	Interrupt input function select bit	—

Table 2.40 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261
P6nPFS	—	P6n pin function control register	—

Table 2.41 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261
P7nPFS	—	P7n pin function control register	—

Table2.42 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX660 (n = 0 to 3, 6, 7)	RX261
P8nPFS	—	P8n pin function control register	—

Table2.43 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX660 (n = 0 to 3)	RX261
P9nPFS	—	P9n pin function control register	—

Table 2.44 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PA0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVUP 00111b: CACREF 01101b: SSLA1 10100b: GTIOC0A 10101b: GTIOC1A 10110b: GTIOC0A# 10111b: GTIOC1A# 11001b: TS32
PA1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGC 00011b: GTIV 00100b: GTOUUP 01010b: SCK5 01101b: SSLA2 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC3B 11001b: TS31

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PA2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLA3	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30
PA3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC7B# 00010b: GTETRGB 00011b: GTETRGD 00100b: GTOVLO 01000b: GTOWLO 01010b: RXD5/SMISO5/SSCL5 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7B 11001b: TS29
PA4PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 001101b: SSLA0 100111b: MTIOC7C	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVLO 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10100b: GTIOC1B 10101b: GTIOC4A 10110b: GTIOC1B# 10111b: GTIOC4A# 11000b: GTETRGA 11001b: TS28

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PA5PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 01101b: RSPCKA 10100b: GTIOC4B 10110b: GTIOC4B# 11001b: TS27
PA6PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOULO 00101b: TMCI3 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10100b: GTIOC0B 10101b: GTIOC5A 10110b: GTIOC0B# 10111b: GTIOC5A# 11000b: GTETRGB 11001b: TS26
PA7PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001101b: MISOA	Pin function select bits b4 b0 00000b: Hi-Z 01101b: MISOA 10100b: GTIOC5B 10110b: GTIOC5B#
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (100/80/64/48-pin) PA4: IRQ5 (100/80/64/48-pin)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PAnPFS	ASEL	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PA3: CMPC10 (144/100/80/64/48-pin) PA4: CVREFC1 (144/100/80/64/48-pin)	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PA3: CMPB1 (100/80/64/48-pin) PA4: CVREFB1 (100/80/64/48-pin)

Table 2.45 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PB0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 10100b: GTIOC0B 10101b: GTIOC2A 10110b: GTIOC0B# 10111b: GTIOC2A# 11001b: TS25
PB1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC7A# 00010b: GTOVLO 00011b: GTIW 00100b: GTOWLO 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7A 11001b: TS24

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PB2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC3A 10110b: GTIOC3A# 11000b: GTETRGC 11001b: TS23
PB3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGD 00011b: GTIU 00100b: GTOVUP 00101b: TMO0 01011b: SCK6 10100b: GTIOC1A 10101b: GTIOC3A 10110b: GTIOC1A# 10111b: GTIOC3A# 11000b: GTIOC3B 11001b: TS22 11011b: LPTO 11100b: PMC0
PB4PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/ SS011# 101110b: DE011	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS009#/RTS009#/ SS009# 01100b: DE009 10100b: GTIOC6A 10110b: GTIOC6A# 11001b: TS21

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PB5PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC6B# 00101b: TMRI1 01010b: SCK009 01100b: TXDB009 10001b: USB0_VBUS 10100b: GTIOC4B 10101b: GTIOC5A 10110b: GTIOC4B# 10111b: GTIOC5A# 11000b: GTIOC6B 11001b: TS20
PB6PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/ SSCL11 101100b: RXD011/SMISO011/ SSCL011	Pin function select bits b4 b0 00000b: Hi-Z 01010b: RXD009/SMISO009/ SSCL009 10100b: GTIOC0B 10101b: GTIOC7A 10110b: GTIOC0B# 10111b: GTIOC7A# 11001b: TS19
PB7PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/ SSDA11 101100b: TXD011/SMOSI011/ SSDA011	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD009/TXDA009/ SMOSI009/SSDA009 10100b: GTIOC0A 10101b: GTIOC7B 10110b: GTIOC0A# 10111b: GTIOC7B# 11001b: TS18

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/80/64/48-pin)

Table 2.46 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PC0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1 101100b: RXD011/SMISO011/SSCL011	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGC
PC1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 001010b: SCK5 001101b: SSLA2 101100b: TXD011/SMOSI011/SSDA011/TXDA011	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 01010b: SCK5 01101b: SSLA2 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGD

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PC2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10100b: GTIOC2A 10110b: GTIOC2A# 11000b: GTETRGA 11001b: TS17
PC3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0	Pin function select bits b4 b0 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5 10100b: GTIOC2B 10110b: GTIOC2B# 11000b: GTETRGB 11001b: TS16 11100b: PMC0
PC4PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/ SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/ SS010# 101110b: DE010	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIU 00011b: GTOULO 00101b: TMCI1 01010b: SCK5 01011b: CTS008#/RTS008#/ SS008# 01100b: DE008 01101b: SSLA0 10100b: GTIOC0B 10101b: GTIOC3A 10110b: GTIOC0B# 10111b: GTIOC3A# 11000b: GTETRGC 11001b: TSCAP 11100b: PMC0

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PC5PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOUUP 00011b: GTIW 00101b: TMRI2 01010b: SCK008 01100b: TXDB008 01101b: RSPCKA 10001b: USB0_ID 10100b: GTIOC0A 10101b: GTIOC7A 10110b: GTIOC0A# 10111b: GTIOC7A# 11000b: GTETRGD 11001b: TS15 11100b: PMC0
PC6PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/ SSCL10 101100b: RXD010/SMISO010/ SSCL010	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI2 01010b: RXD008/SMISO008/ SSCL008 01101b: MOSIA 10001b: USB0_EXICEN 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGA 11001b: TS14

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PC7PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA 011101b: TOC0 100100b: TXD10/SMOSI10/ SSDA10 101100b: TXD010/SMOSI010/ SSDA010	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMO2 00111b: CACREF 01010b: TXD008/TXDA008/ SMOSI008/SSDA008 01101b: MISOA 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGB 11001b: TS13 11011b: LPTO
PCnPFS	ISEL	Interrupt input function select bit	—

Table 2.47 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PD0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001000b: POE4#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: TXD6/SMOSI6/SSDA6
PD1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0	Pin function select bits b4 b0 00000b: Hi-Z 01011b: RXD6/SMISO6/SSCL6 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A#
PD2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2	Pin function select bits b4 b0 00000b: Hi-Z 01011b: SCK6 10000b: CRX0 10100b: GTIOC2B 10110b: GTIOC2B#
PD3PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PD4PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PD5PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PD6PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PD7PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PDnPFS	ASEL	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PD0: AN016 (144/100/80-pin) PD1: AN017 (144/100/80-pin) PD2: AN018 (144/100/80-pin) PD3: AN019 (144/100-pin) PD4: AN020 (144/100-pin) PD5: AN021 (144/100-pin) PD6: AN022 (144/100-pin) PD7: AN023 (144/100-pin)	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PD0: AN024 (100/80-pin) PD1: AN025 (100/80-pin) PD2: AN026 (100/80-pin) PD3: AN027 (100-pin) PD4: AN028 (100-pin) PD5: AN029 (100-pin) PD6: AN030 (100-pin) PD7: AN031 (100-pin)

Table 2.48 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PE0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12	Pin function select bits b4 b0 00000b: Hi-Z 01100b: SCK12
PE1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVLO 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 10100b: GTIOC1B 10110b: GTIOC1B#
PE2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/RXDX12/ SMISO12/SSCL12 011101b: TIC3	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOVUP 01100b: RXD12/RXDX12/ SMISO12/SSCL12 10100b: GTIOC1A 10110b: GTIOC1A# 11001b: TS35
PE3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOWUP 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B# 11001b: TS34

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PE4PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTIOC4A# 00010b: GTOVUP 00011b: GTOWLO 01001b: CLKOUT 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11000b: GTIOC4A 11001b: TS33
PE5PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0	Pin function select bits b4 b0 00000b: Hi-Z 10000b: CMPOB0 10100b: GTIOC1B 10101b: GTIOC5B 10110b: GTIOC1B# 10111b: GTIOC5B#
PE6PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PE7PFS	PSEL[5:0] (RX660)	Pin function select bits	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (144/100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (100-pin) PE7: IRQ7 (100-pin)

Register	Bit	RX660 (n = 0 to 7)	RX261 (n = 0 to 7)
PEnPFS	ASEL	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PE0: AN008 (144/100/80/64-pin) PE1: AN009 (144/100/80/64/48-pin) PE2: AN010 (144/100/80/64/48-pin) PE3: AN011 (144/100/80/64/48-pin) PE4: AN012 (144/100/80/64/48-pin) PE5: AN013 (144/100/80/64-pin) PE6: AN014 (144/100-pin) PE7: AN015 (144/100-pin)	Analog function select bit 0: Used as other than an analog pin 1: Used as an analog pin PE0: AN016 (100/80/64-pin) PE1: AN017, CMPB0 (100/80/64/48-pin) PE2: AN018, CVREFB0 (100/80/64/48-pin) PE3: AN019 (100/80/64/48-pin) PE4: AN020, CMPA2 (100/80/64/48-pin) PE5: AN021 (100/80/64-pin) PE6: AN022 (100-pin) PE7: AN023 (100-pin)

Table 2.49 Comparison of PF5 Pin Function Control Registers (PF5PFS)

Register	Bit	RX660	RX261
PF5PFS	—	PF5 pin function control register	—

Table 2.50 Comparison of PHn Pin Function Control Registers (PHnPFS)

Register	Bit	RX660 (n = 0 to 3)	RX261 (n = 0 to 3)
PH0PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3B 000111b: CACREF 001001b: ADTRG0#	Pin function select bits b4 b0 00000b: Hi-Z 00010b: GTOUUP 00111b: CACREF 10100b: GTIOC0A 10110b: GTIOC0A# 11001b: TS10
PH1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3D 000101b: TMO0 001001b: ADST0 011101b: TIC1	Pin function select bits b4 b0 00000b: Hi-Z 00011b: GTOULO 00101b: TMO0 10100b: GTIOC0B 10110b: GTIOC0B# 11001b: TS9
PH2PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4C 000101b: TMRI0 011101b: TOC1	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMRI0 10100b: GTIOC1B 10110b: GTIOC1B# 11001b: TS8
PH3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI0	Pin function select bits b4 b0 00000b: Hi-Z 00101b: TMCI0 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS7

Table 2.51 Comparison of PJn Pin Function Control Registers (PJnPFS)

Register	Bit	RX660 (n = 1, 3, 5)	RX261 (n = 1, 3, 6, 7)
PJ1PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3A	Pin function select bits b4 b0 00000b: Hi-Z 00001b: GTCPPO0 10100b: GTIOC6A 10110b: GTIOC6A#
PJ3PFS	PSEL[5:0] (RX660) PSEL[4:0] (RX261)	Pin function select bits b5 b0 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0#	Pin function select bits b4 b0 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC6B 10110b: GTIOC6B#
PJ5PFS	PSEL[5:0]	Pin function select bits	—
PJnPFS	ISEL	Interrupt input function select bit	—
	ASEL	—	Analog function select bit

Table 2.52 Comparison of PKn Pin Function Control Registers (PKnPFS)

Register	Bit	RX660 (n = 2 to 5)	RX261
PKnPFS	—	PKn pin function control register	—

Table 2.53 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX660	RX261
PFCSE	—	CS output enable register	—
PFCSS0	—	CS output pin select register 0	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—
PFBCR2	—	External bus control register 2	—
PFBCR3	—	External bus control register 3	—

2.16 8-Bit Timer

Table 2.54 shows a Comparative Overview of 8-Bit Timers, and Table 2.55 shows a Comparison of 8-Bit Timer Registers.

Table 2.54 Comparative Overview of 8-Bit Timers

Item	RX660 (TMRb)	RX261 (TMRa)
Count clock	• Frequency dividing clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal	Selectable among compare match A or B, or an external counter reset signal
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (3) Counter restart (TMR0 to TMR3)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0, TMR2) (2) Event counter (TMR0, TMR2) (3) Counter restart (TMR0, TMR2)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
A/D conversion start trigger of the A/D converter	Compare match A of TMR0 or TMR2	—
Generation of SCI basic clock	Generation of SCI basic clock	Generation of SCI basic clock
Generation of REMC operating clock	Generation of operating clock of REMC (remote control signal receiver)	Generation of operating clock of REMC (remote control signal receiver)
Low power consumption function	Can transition to module stop state at the unit level	Can transition to module stop state at the unit level

Table 2.55 Comparison of 8-Bit Timer Registers

Register	Bit	RX660 (TMRb)	RX261 (TMRa)
TCSR	ADTE	A/D trigger enable bit	—

2.17 Realtime Clock

Table 2.56 shows a Comparative Overview of Realtime Clocks, and Table 2.57 shows a Register Comparison of Realtime Clocks.

Table 2.56 Comparative Overview of Realtime Clocks

Item	RX660 (RTCC)	RX261 (RTCBa)
Count mode	Calendar count mode/ binary count mode	Calendar count mode/ binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (crystal or external clock) or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, day, day of the week, hour, minute, and second are counted and displayed in BCD. — 12 hour/24 hour mode switching function — 30-seconds adjustment function (Less than 30 seconds are rounded down to 00 seconds; 30 seconds or more are rounded up to 1 minute.) — Automatic adjustment function for leap years • Binary count mode Seconds are counted by 32 bits, and displayed in binary. • Common to both modes — Start/stop function — Binary display of digits of second and lower (1, 2, 4, 8, 16, 32, or 64 Hz) — Clock error correction function — Clock (1 Hz/64 Hz) output	• Calendar count mode — Year, month, day, day of the week, hour, minute, and second are counted and displayed in BCD. — 12 hour/24 hour mode switching function — 30-seconds adjustment function (Less than 30 seconds are rounded down to 00 seconds; 30 seconds or more are rounded up to 1 minute.) — Automatic adjustment function for leap years • Binary count mode Seconds are counted by 32 bits, and displayed in binary. • Common to both modes — Start/stop function — Binary display of digits of second and lower (1, 2, 4, 8, 16, 32, or 64 Hz) — Clock error correction function — Clock (1 Hz/64 Hz) output
Interrupts	• Alarm interrupt (ALM) One of the following can be selected as the comparison condition for alarm interrupt. — Calendar count mode: Year, month, day, day of the week, hour, minute, and second — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period.	• Alarm interrupt (ALM) One of the following can be selected as the comparison condition for alarm interrupt. — Calendar count mode: Year, month, day, day of the week, hour, minute, and second — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period.

Item	RX660 (RTCC)	RX261 (RTCBa)
Interrupts	• Carry interrupt (CUP) Interrupt request occurs at one of the following timings. — When a carry from the 64 Hz counter to the second counter occurs — When change of the 64 Hz counter and read of the R64CNT register occur at the same time • Exit from software standby mode or deep software standby mode is possible by an alarm interrupt or a periodic interrupt.	• Carry interrupt (CUP) Interrupt request occurs at one of the following timings. — When a carry from the 64 Hz counter to the second counter occurs — When change of the 64 Hz counter and read of the R64CNT register occur at the same time • Exit from software standby mode is possible by an alarm interrupt or a periodic interrupt.
Time capture function	• Time can be captured by the edge detection of the time capture event input pin. For each event input, month, day, hour, minute, and second are captured or the 32-bit binary counter value is captured.	• Time can be captured by the edge detection of the time capture event input pin. For each event input, month, day, hour, minute, and second are captured or the 32-bit binary counter value is captured.
Event link function	Periodic event output	Periodic event output

Table 2.57 Register Comparison of Realtime Clocks

Register	Bit	RX660 (RTCC)	RX261 (RTCBa)
RCR3	—	RTC control register 3	—
RCR4	—	RTC control register 4	—

2.18 Watchdog Timer

Table 2.58 shows a Comparative Overview of Watchdog Timers, and Table 2.59 shows Comparison of Watchdog Timer Registers.

Table 2.58 Comparative Overview of Watchdog Timers

Item	RX660 (WDTA)	RX261 (WDTA)
Count source	Peripheral module clock (PCLK)	Peripheral module clock (PCLK)
Clock division ratio	1/4, 1/64, 1/128, 1/512, 1/2048, 1/8192	1/4, 1/64, 1/128, 1/512, 1/2048, 1/8192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the WDTRR register).	• Auto-start mode: Counting starts automatically after a reset. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the WDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state • Underflow or refresh error (in register start mode only)	• Reset • Low power consumption state • Underflow or refresh error (in register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Watchdog timer Reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources (RX660) Non-maskable interrupt sources (RX261)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read by the WDTSR register.	The down-counter value can be read by the WDTSR register.

Table 2.59 Comparison of Watchdog Timer Registers

Register	Bit	RX660 (WDTA)	RX261 (WDTA)
WDTRCR	RSTIRQS	Reset interrupt request select bit 0: Output of a non-maskable interrupt request or plain interrupt request is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.

2.19 Independent Watchdog Timer

Table 2.60 shows a Comparative Overview of Independent Watchdog Timers, and Table 2.61 shows Comparison of Independent Watchdog Timer Registers.

Table 2.60 Comparative Overview of Independent Watchdog Timers

Item	RX660 (IWDTa)	RX261 (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	1/1, 1/16, 1/32, 1/64, 1/128, 1/256	1/1, 1/16, 1/32, 1/64, 1/128, 1/256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto-start mode: Counting starts automatically after cancellation is released. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the IWDTRR register).	• Auto-start mode: Counting starts automatically after cancellation is released. • Register start mode: Counting starts by refreshing the counter (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • Low power consumption state (depends on register setting) • Underflow or refresh error (in register start mode only)	• Reset • Low power consumption state (depends on register setting) • Underflow or refresh error (in register start mode only)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
Reset output sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources (RX660) Non-maskable interrupt sources (RX261)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading the counter value	• The down-counter value can be read by the IWDTSR register.	• The down-counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX660 (IWDTa)	RX261 (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selecting the clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selecting the reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by the IWDT registers)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selecting the clock frequency division ratio after refreshing (IWDTCR.CKS[3:0] bits) • Selecting the timeout period of the independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selecting the window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selecting the window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selecting the reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selecting the down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.61 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX660 (IWDTa)	RX261 (IWDTa)
IWDTCR	TOPS[1:0]	Timeout period select bits b1 b0 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh)	Timeout period select bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh)

Register	Bit	RX660 (IWDTa)	RX261 (IWDTa)
IWDTRCR	RSTIRQS	Reset interrupt request select bit 0: Output of a non-maskable interrupt request or plain interrupt request is enabled. 1: Reset output is enabled.	Reset interrupt request select bit 0: Non-maskable interrupt request output is enabled. 1: Reset output is enabled.
IWDTCSTPR	SLCSTP	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering the following modes: sleep, software standby, deep software standby, and all-module clock stop.	Sleep mode count stop control bit 0: Counting stop is disabled 1: Counting stop is enabled when entering the following modes: sleep, software standby, and deep sleep.

2.20 Serial Communications Interface (SCI)

Table 2.62 shows a Comparative Overview of the Serial Communications Interface (SCI), Table 2.63 shows a Comparison of Serial Communications Interface Channel Specifications, and Table 2.64 shows a Comparative Overview of the Registers for the Serial Communications Interface (SCI).

Table 2.62 Comparative Overview of the Serial Communications Interface (SCI)

Item		RX660 (SCIk, SCIm, SCIh)	RX261 (SCIk, SCIh)
Number of channels		• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel	• SCIk: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		LSB first or MSB first can be selected.	LSB first or MSB first can be selected.
I/O signal level inversion		The levels of input and output signals can be inverted independently. (SCI0 to SCI11 only)	The levels of input and output signals can be inverted independently. (SCI1, SCI5, and SCI6 only)
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match (SCI0 to SCI11 only) • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	• Transmit end, transmit data empty, receive data full, receive error, and data match (SCI1, SCI5, and SCI6 only) • Completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, and framing error	Parity error, overrun error, and framing error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	FIFO of 16 lines is available for transmission and FIFO of 16 lines is available for reception. (SCI10 and SCI11 only)	—
	Data match detection	Compares receive data with the contents of a comparison data register and generates an interrupt request when they match. (SCI0 to SCI11 only)	Compares receive data with the contents of a comparison data register and generates an interrupt request when they match. (SCI1, SCI5, and SCI6 only)

Item		RX660 (SCIk, SCIm, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	The receive data sampling point can be shifted from the center of the data forward or backward to a base point. (SCI0 to SCI11 only)	The receive data sampling point can be shifted from the center of the data forward or backward to a base point. (SCI1, SCI5, and SCI6 only)
	Transmit signal change timing adjustment	Either the falling or rising edge of the transmit data can be delayed. (SCI0 to SCI11 only)	Either the falling or rising edge of the transmit data can be delayed. (SCI1, SCI5, and SCI6 only)
	Break detection	• When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag. (SCI0 to SCI11 only) • When a framing error occurs, a break can be detected by reading the RXDn pin level directly. (SCI12)	• When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag. (SCI1, SCI5, and SCI6 only) • When a framing error occurs, a break can be detected by reading the RXDn pin level directly. (SCI12)
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, and SCI12)	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used. (SCI5, SCI6, and SCI12)
	Double-speed mode	Baud rate generator double-speed mode can be selected.	Baud rate generator double-speed mode can be selected.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	FIFO of 16 lines is available for transmission and FIFO of 16 lines is available for reception. (SCI10 and SCI11 only)	—
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX660 (SCIk, SCIm, SCIh)	RX261 (SCIk, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode supported	Fast mode supported
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two types of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity for TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing of receive data sampling for RXDX12 pin	• Ability to select polarity for TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select timing of receive data sampling for RXDX12 pin
	Timer function	Usable as reload timer	Usable as reload timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error event output (receive error or error signal detection) • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.63 Comparison of Serial Communications Interface Channel Specifications

Item	RX660 (SCIk, SCIm, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	SCI0 to SCI12	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI0 to SCI12	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI0 to SCI12	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI0 to SCI12	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI0 to SCI12	SCI1, SCI5, SCI6, SCI12
FIFO mode	SCI10, SCI11	—
Data match detection	SCI0 to SCI11	SCI1, SCI5, SCI6
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0 to SCI9, SCI12 PCLKA: SCI10, SCI11	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.64 Comparative Overview of the Registers for the Serial Communications Interface (SCI)

Register	Bit	RX660 (SCIk, SCIm, SCIh)	RX261 (SCIk, SCIh)
FRDR	—	Receive FIFO data register	—
FTDR	—	Transmit FIFO data register	—
SSR/SSRFIFO (RX660) SSR (RX261)	—	Serial status register When not in smart card interface mode and in FIFO mode (SCMR.SMIF bit = 0, and FCR.FM bit = 1)	Serial status register
FCR	—	FIFO control register	—
FDR	—	FIFO data count register	—
LSR	—	Line status register	—

2.21 Serial Communications Interface (RSCI)

Table 2.65 shows a Comparative Overview of the Serial Communications Interface (RSCI), Table 2.66 shows a Comparison of Specifications among the RSCI Channels, and Table 2.67 shows a Comparative Overview of the Registers for the Serial Communications Interface (RSCI).

Table 2.65 Comparative Overview of the Serial Communications Interface (RSCI)

Item		RX660 (RSCI)	RX261 (RSCI)
Number of channels		2 channels	3 channels
Serial communications modes		• Asynchronous • Manchester • Clock synchronous • Smart card interface • Simple I^2C • Simple SPI (4-wire serial bus) • Extended serial	• Asynchronous • Manchester • Clock synchronous • Smart card interface • Simple I^2C • Simple SPI (4-wire serial bus) • Extended serial
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Half-duplex communication		Half-duplex communication using the TXDn pin is possible.	Half-duplex communication using the TXDn pin is possible.
Data transfer		LSB first or MSB first can be selected.	LSB first or MSB first can be selected.
I/O signal level inversion		The levels of input and output signals can be inverted independently.	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and receive data match • Break field detection/transmission, bus collision detection, valid edge detection • Generation of start condition, restart condition, or stop condition ended	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and receive data match • Break Field detection/transmission, bus collision detection, valid edge detection • Generation of start condition, restart condition, or stop condition ended
RS-485 driver control function		Outputs the DE signal that enables the transmit mode of the external transceiver.	Outputs the DE signal that enables the transmit mode of the external transceiver.
Loopback function		Ability to self-diagnose the communication functions by connecting TXD and RXD inside the IP	Ability to self-diagnose the communication functions by connecting TXD and RXD inside the IP
Low power consumption function		Ability to enter the module stop state for each channel	Ability to enter the module stop state for each channel
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity function	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity error, overrun error, or framing error	Parity error, overrun error, or framing error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX660 (RSCI)	RX261 (RSCI)
Asynchronous mode	Transmitter/ receiver	Selectable between the 1-stage register and 32-stage FIFO buffer configurations	Double buffer configuration
	Data match detection function	Ability to output an interrupt request upon detecting that the receive data and the comparison data matched	Ability to output an interrupt request upon detecting that the receive data and the comparison data matched
	Start-bit detection	Detection of low level or falling edge on the RXDn pin can be selected.	Detection of low level or falling edge on the RXDn pin can be selected.
	Receive data sampling timing adjustment	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.
	Transmit signal change timing adjustment	The falling or rising edge of the transmit data can be delayed	The falling or rising edge of the transmit data can be delayed
	Break detection	A break can be detected by reading a register when a framing error occurs.	A break can be detected by reading a register when a framing error occurs.
	Clock source	An internal or external clock can be selected.	An internal or external clock can be selected.
	Double-speed mode	Double-speed mode can be selected for the baud rate generator.	Double-speed mode can be selected for the baud rate generator.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
	HBS support mode	Transmission/reception using inverted RZI (Return to Zero, Inverted) code is possible.	Transmission/reception using inverted RZI (Return to Zero, Inverted) code is possible.
Manchester mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Receive error detection function	Parity error, overrun error, framing error, Manchester code error, preface error, start bit error, receive sync error	Parity error, overrun error, framing error, Manchester code error, preface error, start bit error, receive sync error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Clock source	Internal clock (An external clock cannot be set because it is not supported in Manchester mode.)	Internal clock (An external clock cannot be set because it is not supported in Manchester mode.)
	Double-speed mode	Double-speed mode can be selected for the baud rate generator.	Double-speed mode can be selected for the baud rate generator.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
	Manchester encoder/decoder	A function that enables communication based on Manchester code by encoding and decoding transmit data and receive data	A function that enables communication based on Manchester code by encoding and decoding transmit data and receive data

Item		RX660 (RSCI)	RX261 (RSCI)
Manchester mode	Preface setting/detection function	The beginning of a frame can be detected by using a preface pattern. One of four preface patterns can be selected. The length can be changed in the range from 0 to 15 bits.	The beginning of a frame can be detected by using a preface pattern. One of four preface patterns can be selected. The length can be changed in the range from 0 to 15 bits.
	Start-bit setting/detection function	Either 1 bit or 3 bits can be set as the start bit length. If 3 bits is selected, the type of the subsequent data can be determined by using one of two patterns.	Either 1 bit or 3 bits can be set as the start bit length. If 3 bits is selected, the type of the subsequent data can be determined by using one of two patterns.
	Reception retiming function	This is a function that corrects the timing at each inter-bit edge by using Manchester code's characteristic rising edge between bits.	This is a function that corrects the timing at each inter-bit edge by using Manchester code's characteristic rising edge between bits.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Extended serial mode	Start frame transmission	The break field can be transmitted, the break field transmission completion interrupt can be output, bus collision can be detected, and the bus collision detection interrupt can be output.	The break field can be transmitted, the break field transmission completion interrupt can be output, bus collision can be detected, and the bus collision detection interrupt can be output.
	Start frame reception	• The break field can be detected and the break field detection interrupt can be output. • Control field 0/1 data comparison function • Ability to set two types (primary and secondary) of comparison data in control field 1 • Ability to specify priority interrupt bit in control field 1 • The bit rate measurement function is available.	• The break field can be detected and the break field detection interrupt can be output. • Control field 0/1 data comparison function • Ability to set two types (primary and secondary) of comparison data in control field 1 • Ability to specify priority interrupt bit in control field 1 • The bit rate measurement function is available.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (multi-master mode not supported)	Master (multi-master mode not supported)
	Transfer speed	400 kbps, max.	Fast mode supported
	Noise cancellation	• The signal paths from input on the SCL and SDA pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SCL and SDA pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.

Item		RX660 (RSCI)	RX261 (RSCI)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive sampling timing adjustment function	The receive sampling timing can be adjusted backward from the default timing only when an internal clock is used.	The receive sampling timing can be adjusted backward from the default timing only when an internal clock is used.
	Receive error detection	Overrun error	Overrun error
	Clock source	Selectable between the internal clock (master) and external clock (slave)	Selectable between the internal clock (master) and external clock (slave)
	Double-speed mode	Double-speed mode can be selected for the baud rate generator.	Double-speed mode can be selected for the baud rate generator.
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmitter/ receiver	Selectable between the 1-stage register and 32-stage FIFO buffer configurations	Double buffer configuration
Simple SPI (4-wire serial bus) mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	Clock source	Selectable between the internal clock (master) and external clock (slave)	Selectable between the internal clock (master) and external clock (slave)
	Double-speed mode	Double-speed mode can be selected for the baud rate generator.	Double-speed mode can be selected for the baud rate generator.
	Receive sampling timing adjustment function	The receive sampling timing can be adjusted backward from the default timing only when an internal clock is used.	The receive sampling timing can be adjusted backward from the default timing only when an internal clock is used.
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
	Transmitter/ receiver	Selectable between the 1-stage register and 32-stage FIFO buffer configurations	Double buffer configuration
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.

Table 2.66 Comparison of Specifications among the RSCI Channels

Item	RX660 (RSCI)	RX261 (RSCI)
Asynchronous mode	RSCI10, 11	RSCI0, RSCI8, RSCI9
Manchester mode	RSCI10, 11	RSCI9
Smart card interface mode	RSCI10, 11	RSCI0, RSCI8, RSCI9
Extended serial mode	RSCI10, 11	RSCI9
Simple I^2C mode	RSCI10, 11	RSCI0, RSCI8, RSCI9
Clock synchronous mode	RSCI10, 11	RSCI0, RSCI8, RSCI9
Simple SPI mode	RSCI10, 11	RSCI0, RSCI8, RSCI9
Peripheral module clock	PCLKA	PCLKB

Table 2.67 Comparative Overview of the Registers for the Serial Communications Interface (RSCI)

Register	Bit	RX660 (RSCI)	RX261 (RSCI)
RDR	DR	Receive data ready flag	—
	PER	Parity error flag	—
	FER	Framing error flag	—
SCR2	CKS[1:0]	Clock select bits b21 b20 0 0: PCLKA (n = 0) 0 1: PCLKA/4 (n = 1) 1 0: PCLKA/16 (n = 2) 1 1: PCLKA/64 (n = 3)	Clock select bits b21 b20 0 0: PCLK (n = 0) 0 1: PCLK/4 (n = 1) 1 0: PCLK/16 (n = 2) 1 1: PCLK/64 (n = 3)
SCR3	SYNDIS	—	Synchronizer disable bit
	FM	FIFO mode select bit	—
SCR4	RTMG[3:0]	Receive data sampling timing select bits In the case of clock synchronous or simple SPI mode: b27 b24 0 0 0 0: Delay by 1 cycle of PCLKA 0 0 0 1: Delay by 2 cycles of PCLKA 0 0 1 0: Delay by 3 cycles of PCLKA 0 0 1 1: Delay by 4 cycles of PCLKA Other than above: Setting prohibited.	Receive data sampling timing select bits In the case of clock synchronous or simple SPI mode: b27 b24 0 0 0 0: Delay by 1 cycle of PCLK 0 0 0 1: Delay by 2 cycles of PCLK 0 0 1 0: Delay by 3 cycles of PCLK 0 0 1 1: Delay by 4 cycles of PCLK Other than above: Setting prohibited.
FCR	—	FIFO control register	—
XCR0	TCSS[1:0]	Timer count clock source select bits Selects the clock source of the timer counter in the extended serial module. b1 b0 0 0: PCLKA 0 1: PCLKA/4 1 0: PCLKA/16 1 1: PCLKA/64	Timer count clock source select bits Selects the clock source of the timer counter in the extended serial module. b1 b0 0 0: PCLK 0 1: PCLK/4 1 0: PCLK/16 1 1: PCLK/64
SSR	APER	Aggregate parity error flag [In non-FIFO mode (SCR3.FM bit = 0)] 0: There are no parity errors. 1: There are parity errors. [In FIFO mode (SCR3.FM bit = 1)] 0: There are no parity errors in all receive data in the FIFO buffer. 1: There are parity errors in one or more receive data units in the FIFO buffer.	Aggregate parity error flag 0: There are no parity errors. 1: There are parity errors.

Register	Bit	RX660 (RSCI)	RX261 (RSCI)
SSR	AFER	Aggregate framing error flag [In non-FIFO mode (SCR3.FM bit = 0)] 0: There are no framing errors. 1: There are framing errors. [In FIFO mode (SCR3.FM bit = 1)] 0: There are no framing errors in all receive data in the FIFO buffer. 1: There are framing errors in one or more receive data units in the FIFO buffer.	Aggregate framing error flag 0: There are no framing errors. 1: There are framing errors.
	TDRE	Transmit data empty flag [In non-FIFO mode (SCR3.FM bit = 0)] 0: There is data written in the TDR register. 1: There is no data written in the TDR register. [In FIFO mode (SCR3.FM bit = 1)] 0: The number of transmit data units written in the transmit FIFO buffer is larger than the transmit FIFO buffer threshold value. 1: The number of transmit data units written in the transmit FIFO buffer is no more than the transmit FIFO buffer threshold value.	Transmit data empty flag 0: There is data written in the TDR register. 1: There is no data written in the TDR register.
	RDRF	Receive data full flag [In non-FIFO mode (SCR3.FM bit = 0)] 0: There is no receive data in the RDR register. 1: There is receive data in the RDR register. [In FIFO mode (SCR3.FM bit = 1)] 0: The number of receive data units stored in the receive FIFO buffer (RDR register) is smaller than the receive FIFO buffer threshold value. 1: The number of receive data units stored in the receive FIFO buffer (RDR register) is equal to or larger than the receive FIFO buffer threshold value.	Receive data full flag 0: There is no receive data in the RDR register. 1: There is receive data in the RDR register.
RFSR	—	Receive FIFO status register	—
TFSR	—	Transmit FIFO status register	—
RFSCR	—	Receive FIFO status clear register	—

2.22 I²C Bus Interface

Table 2.68 shows a Comparative Overview of the I2C Bus Interface, and Table 2.69 shows a Comparison of the Registers for the I2C Bus Interface.

Table 2.68 Comparative Overview of the I²C Bus Interface

Item	RX660 (RIICa)	RX261 (RIICa)
Number of channels	2 channels	1 channel
Communication format	• I²C bus format/SMBus format • Selectable between the master and slave • The hold time, bus free time, and several setup times are automatically secured according to the preset transfer speed.	• I²C bus format/SMBus format • Selectable between the master and slave • The hold time, bus free time, and several setup times are automatically secured according to the preset transfer speed.
Transfer speed	Fast mode supported (up to 400 kbps)	Fast mode supported (up to 400 kbps)
Serial clock (SCL)	If the MCU is operating as master, the duty cycle of the SCL can be set in the range from 4% to 96%.	If the MCU is operating as master, the duty cycle of the SCL can be set in the range from 4% to 96%.
Generation and detection of conditions	Conditions that can be generated automatically: start conditions, restart conditions, and stop conditions Conditions that can be detected: start conditions (including restart conditions) and stop conditions	Conditions that can be generated automatically: start conditions, restart conditions, and stop conditions Conditions that can be detected: start conditions (including restart conditions) and stop conditions
Slave address	• Up to 3 different slave addresses can be set. • 7-bit and 10-bit address formats supported (mix of both formats permitted) • Addresses that can be detected: general call address, device ID address, and System Management Bus host address	• Up to 3 different slave addresses can be set. • 7-bit and 10-bit address formats supported (mix of both formats permitted) • Addresses that can be detected: general call address, device ID address, and System Management Bus host address
Acknowledge response	• During transmission: The acknowledge bit is automatically loaded. — When NACK is received, the transfer of the next transmit data can be suspended automatically. • During reception: The acknowledge bit is automatically transmitted. — If insertion of a wait between the 8th and 9th clock cycles is enabled, acknowledge response can be controlled by software according to the content of the receive data.	• During transmission: The acknowledge bit is automatically loaded. — When NACK is received, the transfer of the next transmit data can be suspended automatically. • During reception: The acknowledge bit is automatically transmitted. — If insertion of a wait between the 8th and 9th clock cycles is enabled, acknowledge response can be controlled by software according to the content of the receive data.
Wait function	• Waits can be inserted by holding the SCL line at the low level during reception. — A wait is inserted between the 8th and 9th clock cycles. — A wait is inserted between the 9th and 1st clock cycles.	• Waits can be inserted by holding the SCL line at the low level during reception. — A wait is inserted between the 8th and 9th clock cycles. — A wait is inserted between the 9th and 1st clock cycles.

Item	RX660 (RIICa)	RX261 (RIICa)
SDA output delay function	The timing to change the output of data transmission (including acknowledge transmission) can be delayed.	The timing to change the output of data transmission (including acknowledge transmission) can be delayed.
Arbitration	• Multi-master configuration supported — If a competition between masters occurs on the SCL, the SCL can perform synchronous operations. — When generating the start condition would create conflict on the bus, loss in arbitration is detected by testing for non-matching between the internal data level and the actual level on the SDA line. — During master operation, loss in arbitration is detected by testing for non-matching between the actual level on the SDA line and the internal data level. • Arbitration loss can be detected when a start condition is issued while the bus is busy (to prevent a double issuance of start conditions). • Loss in arbitration in transfer of a not-acknowledge signal due to the internal signal (NACK) and the actual level on the SDA line not matching is detectable. • Loss in arbitration due to non-matching of internal data level and the actual level on the SDA line is detectable in slave transmission.	• Multi-master configuration supported — If a competition between masters occurs on the SCL, the SCL can perform synchronous operations. — When generating the start condition would create conflict on the bus, loss in arbitration is detected by testing for non-matching between the internal data level and the actual level on the SDA line. — During master operation, loss in arbitration is detected by testing for non-matching between the actual level on the SDA line and the internal data level. • Arbitration loss can be detected when a start condition is issued while the bus is busy (to prevent a double issuance of start conditions). • Loss in arbitration in transfer of a not-acknowledge signal due to the internal signal (NACK) and the actual level on the SDA line not matching is detectable. • Loss in arbitration due to non-matching of internal data level and the actual level on the SDA line is detectable in slave transmission.
Timeout detection function	An on-chip timeout detection function can detect long-time stoppage of the SCL.	An on-chip timeout detection function can detect long-time stoppage of the SCL.
Noise cancellation	An on-chip digital noise filter for the SCA and SDA inputs is available. The interval for noise cancellation can be adjusted by using software.	An on-chip digital noise filter for the SCA and SDA inputs is available. The interval for noise cancellation can be adjusted by using software.
Interrupt sources	4 sources • Communication errors and events — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (or a restart condition) — Detection of a stop condition • Receive-data-full state (including when a slave address match occurs) • Transmit-data-empty state (including when a slave address match occurs) • End of transmission	4 sources • Communication errors and events — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (or a restart condition) — Detection of a stop condition • Receive-data-full state (including when a slave address match occurs) • Transmit-data-empty state (including when a slave address match occurs) • End of transmission

Item	RX660 (RIICa)	RX261 (RIICa)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating mode	• 4 modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode	• 4 modes Master transmit mode, master receive mode, slave transmit mode, and slave receive mode
Event link function (output)	Four sources (RIIC0) • Communication errors and events — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (or a restart condition) — Detection of a stop condition • Receive-data-full state (including when a slave address match occurs) • Transmit-data-empty state (including when a slave address match occurs) • End of transmission	Four sources (RIIC0) • Communication errors and events — Detection of arbitration loss — Detection of NACK — Detection of a timeout — Detection of a start condition (or a restart condition) — Detection of a stop condition • Receive-data-full state (including when a slave address match occurs) • Transmit-data-empty state (including when a slave address match occurs) • End of transmission

Table 2.69 Comparison of the Registers for the I²C Bus Interface

Register	Bit	RX660 (RIICa)	RX261 (RIICa)
ICCR1	SDAI	SDA line monitor bit 0: SDAn line is Low 1: SDAn line is High	SDA line monitor bit 0: SDA0 line is Low 1: SDA0 line is High
	SCLI	SCL line monitor bit 0: SCLn line is Low 1: SCLn line is High	SCL line monitor bit 0: SCL0 line is Low 1: SCL0 line is High
	SDAO	SDA output control/monitor bit • During a read 0: SDAn pin is set to Low 1: SDAn pin is opened • During a write 0: Sets the SDAn pin to Low 1: Opens the SDAn pin (High is output by external pull-up resistor.)	SDA output control/monitor bit • During a read 0: SDA0 pin is set to Low 1: SDA0 pin is opened • During a write 0: Sets the SDA0 pin to Low 1: Opens the SDA0 pin (High is output by external pull-up resistor.)
	SCLO	SCL output control/monitor bit • During a read 0: SCLn pin is set to Low 1: SCLn pin is opened • During a write 0: Sets the SCLn pin to Low 1: Opens the SCLn pin (High is output by external pull-up resistor.)	SCL output control/monitor bit • During a read 0: SCL0 pin is set to Low 1: SCL0 pin is opened • During a write 0: Sets the SCL0 pin to Low 1: Opens the SCL0 pin (High is output by external pull-up resistor.)

Register	Bit	RX660 (RIICa)	RX261 (RIICa)
ICCR1	ICE	I^2C bus interface enable bit 0: Disabled (SCLn and SDAn pins inactive) 1: Enabled (SCLn and SDAn pins active) (RIIC reset or internal reset is selected by the combination with the IICRST bit.)	I^2C bus interface enable bit 0: Disabled (SCL0 and SDA0 pins inactive) 1: Enabled (SCL0 and SDA0 pins active) (RIIC reset or internal reset is selected by the combination with the IICRST bit.)
ICMR2	TMOL	Timeout L count control bit 0: Counting-up is disabled when the SCLn line is Low 1: Counting-up is enabled when the SCLn line is Low	Timeout L count control bit 0: Counting-up is disabled when the SCL0 line is Low 1: Counting-up is enabled when the SCL0 line is Low
	TMOH	Timeout H count control bit 0: Counting-up is disabled when the SCLn line is High 1: Counting-up is enabled when the SCLn line is High	Timeout H count control bit 0: Counting-up is disabled when the SCL0 line is High 1: Counting-up is enabled when the SCL0 line is High

2.23 CAN FD Module

Table 2.70 shows a Comparative Overview of the CAN FD Module.

Table 2.70 Comparative Overview of the CAN FD Module

Item	RX660 (CANFD)	RX261 (CANFD)
Number of channels	1 channel	1 channel
Protocol	Conforming to the ISO 11898-1:2015 specifications	Conforming to the ISO 11898-1:2015 specifications
Data transfer rate	• Arbitration phase: Maximum of 1 Mbps • Data phase: Maximum of 8 Mbps	• Arbitration phase: Maximum of 1 Mbps • Data phase: Maximum of 5 Mbps
Operating frequency	• Register block: Maximum of 60 MHz (PCLKB) • Message buffer RAM: Maximum of 120 MHz (PCLKA)	• Register block: Maximum of 32 MHz (PCLKB) • Message buffer RAM: Maximum of 64 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)	Maximum of 32 MHz (either CANFDMCLK or CANFDCLK can be selected)
Frame type	• Classic CAN (CAN 2.0) — Data frame in base format (11-bit ID) — Data frame in extended format (29-bit ID) — Remote frame in base format (11-bit ID) — Remote frame in extended format (29-bit ID) • CAN FD — Data frame in base format (11-bit ID) — Data frame in extended format (29-bit ID)	• Classic CAN (CAN 2.0) — Data frame in base format (11-bit ID) — Data frame in extended format (29-bit ID) — Remote frame in base format (11-bit ID) — Remote frame in extended format (29-bit ID) • CAN FD — Data frame in base format (11-bit ID) — Data frame in extended format (29-bit ID)
Data length	• Classic CAN: 0 to 8 bytes • CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes	• Classic CAN: 0 to 8 bytes • CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes
Message buffer	• Receive message buffer × 32 • Transmit message buffer × 4 • Transmit queue × 1 Automatic transfer of messages to the transmit queue is supported.	• Receive message buffer × 32 • Transmit message buffer × 4 • Transmit queue × 1 Automatic transfer of messages to the transmit queue is supported.
FIFO	The FIFO buffer size is programmable. • Receive FIFO buffer × 2 • Common FIFO buffer × 1 (Whether to use the FIFO buffer for reception or transmission can be selected.)	The FIFO buffer size is programmable. • Receive FIFO buffer × 2 • Common FIFO buffer × 1 (Whether to use the FIFO buffer for reception or transmission can be selected.)
Automatic transmission interval adjustment	• Available when the common FIFO buffer is configured for transmission use • The interval between messages sent from the FIFO can be adjusted.	• Available when the common FIFO buffer is configured for transmission use • The interval between messages sent from the FIFO can be adjusted.

Item	RX660 (CANFD)	RX261 (CANFD)
Acceptance filter	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Software support	Label information is automatically added to received messages.	Label information is automatically added to received messages.
Timer	Transmission and reception timestamp function	Transmission and reception timestamp function
Power down function	• Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) • Ability to transition to module stop state	• Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) • Ability to transition to module stop state
RAM	RAM with ECC protection	RAM with ECC protection

2.24 Serial Peripheral Interface

Table 2.71 shows a Comparative Overview of the Serial Peripheral Interface, and Table 2.72 shows Comparison of Registers for the Serial Peripheral Interface.

Table 2.71 Comparative Overview of the Serial Peripheral Interface

Item	RX660 (RSPId)	RX261 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (Master out/slave in), MISO (Master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX660 (RSPId)	RX261 (RSPIc)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Item	RX660 (RSPId)	RX261 (RSPIc)
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt
Event link function (output)	• The following events can be output to the event link controller (RSPI0): — Receive buffer full event — Transmit buffer empty event — Error event (mode fault, overrun, underrun, or parity error) — Idle event — Communication end event	• The following events can be output to the event link controller (RSPI0): — Receive buffer full event — Transmit buffer empty event — Error event (mode fault, overrun, underrun, or parity error) — Idle event — Transmission end event
Others	• Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.72 Comparison of Registers for the Serial Peripheral Interface

Register	Bit	RX660 (RSPId)	RX261 (RSPIc)
SPSR	SPCF	Communication end flag	—
SPDCR2	DINV	Transfer data invert bit	—
SPCR3	—	RSPI control register 3	—

2.25 CRC Calculator

Table 2.73 shows a Comparative Overview of the CRC Calculator, and Table 2.74 shows a Comparison of the Registers for the CRC Calculator.

Table 2.73 Comparative Overview of the CRC Calculator

Item	RX660 (CRCA)		RX261 (CRC)
Data size	8 bits	32 bits	8 bits
Data for CRC calculation	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 32n-bit units (where n is a whole number)	CRC codes are generated for any desired data in 8n-bit units (where n is a whole number)
CRC processor unit	8-bit parallel processing	32-bit parallel processing	8-bit parallel processing
CRC generating polynomial	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$	One of two generating polynomials is selectable • 32-bit CRC: — $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ — $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$	One of three generating polynomials is selectable • 8-bit CRC: — $X^8 + X^2 + X + 1$ • 16-bit CRC: — $X^{16} + X^{15} + X^2 + 1$ $X^{16} + X^{12} + X^5 + 1$
CRC calculation switching	The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication		The order of the bits produced by CRC calculation can be switched for LSB first or MSB first communication
Low power consumption function	Ability to transition to module stop state		Ability to specify module stop state

Table 2.74 Comparison of the Registers for the CRC Calculator

Register	Bit	RX660(CRCA)	RX261(CRC)
CRCCR	GPS[2:0] (RX660) GPS[1:0] (RX261)	CRC generating polynomial switching bits b2 b0 0 0 0: No calculation is executed. 0 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 1 1 0: No calculation is executed. 1 1 1: No calculation is executed.	CRC generating polynomial switching bits b1 b0 0 0: No calculation is executed. 0 1: 8-bit CRC ($X^8 + X^2 + X + 1$) 1 0: 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$) 1 1: 16-bit CRC ($X^{16} + X^{12} + X^5 + 1$)
	LMS	CRC calculation switching bit (b6)	CRC calculation switching bit (b2)
CRCDIR	—	CRC data input register Supported access sizes • Longword access (32-bit CRC selected) • Byte access (16-bit or 8-bit CRC selected)	CRC data input register Supported access sizes • Byte access
CRCDOR	—	CRC data output register Supported access sizes • Longword access (32-bit CRC selected) • Word access (16-bit CRC selected) • Byte access (8-bit CRC selected)	CRC data output register Supported access sizes • Word access The low-order byte (b7 to b0) is used when an 8-bit CRC is to be generated.

2.26 Remote Control Signal Receiver

Table 2.75 shows a Comparative Overview of the Remote Control Signal Receiver, and Table 2.76 shows Comparison of the Registers for the Remote Control Signal Receiver.

Table 2.75 Comparative Overview of the Remote Control Signal Receiver

Item	RX660 (REMCa)	RX261 (REMCa)
External pulse input	PMC0	PMC0
Operating clock source	• Sub-clock • TMR compare match output (TMO0) • PCLKB	• IWDTCLK • Sub-clock • TMR compare match output (TMO0) • PCLKB
Inspection pattern	• Header pattern • Data “0” pattern • Data “1” pattern • Special data pattern	• Header pattern • Data “0” pattern • Data “1” pattern • Special data pattern
Receive buffer	8 bytes (64 bits)	8 bytes (64 bits)
Interrupt request signal	REMCI0	REMCI0
Interrupt sources	• Compare match (number of bits to compare with: 1 to 16) • Receive error • Completion of data reception • Receive-buffer-full state • Match of the header pattern Match of data “0” pattern or data “1” pattern • Match of the special data pattern	• Compare match (number of bits to compare with: 1 to 16) • Receive error • Completion of data reception • Receive-buffer-full state • Match of the header pattern Match of data “0” pattern or data “1” pattern • Match of the special data pattern
Interrupt mode	Either of the following two interrupt modes can be selected for the following four interrupt sources: a compare match, completion of data reception, a match of the header pattern, and a match of the special data pattern. • Normal interrupt mode An interrupt request is generated when the interrupt request generation conditions for any interrupt sources are met. • Sequential interrupt mode An interrupt request is generated when the interrupt request generation conditions for all enabled interrupt sources are met.	Either of the following two interrupt modes can be selected for the following four interrupt sources: a compare match, completion of data reception, a match of the header pattern, and a match of the special data pattern. • Normal interrupt mode An interrupt request is generated when the interrupt request generation conditions for any interrupt sources are met. • Sequential interrupt mode An interrupt request is generated when the interrupt request generation conditions for all enabled interrupt sources are met.
Function selection	• Input signal inversion • Digital filter (matching three or two times) • Pattern end setting	• Input signal inversion • Digital filter (matching three or two times) • Pattern end setting
Low power consumption function	• Ability to transition to module stop state • Return from the low power consumption state can be triggered by reception of a signal or an REMC interrupt request.	• Ability to transition to module stop state • Return from the low power consumption state can be triggered by reception of a signal or an REMC interrupt request.

Table 2.76 Comparison of the Registers for the Remote Control Signal Receiver

Register	Bit	RX660 (REMCa)	RX261 (REMCa)
REMCON1	CSRC[3:0]	Operating clock select bits b6 b3 x 0 1 0: TMR compare match output x 1 0 0: Sub-clock 0 1 1 0: PCLKB/64 1 1 1 0: PCLKB/512 Settings other than the above are prohibited.	Operating clock select bits b6 b3 x 0 0 0: IWDTCLK x 0 1 0: TMR compare match output x 1 0 0: Sub-clock 0 1 1 0: PCLKB/64 1 1 1 0: PCLKB/512 Settings other than the above are prohibited.
REMSTC	—	—	Receiver standby control register

2.27 12-Bit A/D converter

Table 2.77 shows a Comparative Overview of the 12-Bit A/D Converter, and Table 2.78 shows a Comparison of the Registers for the 12-Bit A/D Converter.

Table 2.77 Comparative Overview of the 12-Bit A/D Converter

Item	RX660 (S12ADH)	RX261 (S12ADE)
Number of units	1 unit (S12AD)	1 unit
Input channels	24 channels	25 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	Time per channel: 0.9 µs (when A/D conversion clock (ADCLK) = 60 MHz)	Time per channel: 0.7 µs (ADCCR.CCS bit = 0), 0.5 µs (ADCCR.CCS bit = 1) (when A/D conversion clock ADCLK = 64 MHz)
A/D conversion clock	The peripheral module clock PCLKB and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLKB to ADCLK frequency ratio = 1:1, 2:1, 4:1, or 1:2 • ADCLK is set by using the clock generation circuit. • The A/D conversion clock (ADCLK) can operate at a frequency in the range from 8 to 60 MHz.	The peripheral module clock PCLKB and A/D conversion clock ADCLK can be set to the following frequency ratios: — PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, or 8:1 • ADCLK is set by using the clock generation circuit.
Data register	• 24 registers for analog input; 1 register for duplication of A/D-converted data in double trigger mode; 2 registers for duplication of A/D-converted data for extended operation in double trigger mode • 1 register for temperature sensor • 1 register for internal reference voltage • 1 register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bits for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.	• 25 registers for analog input; 1 register for duplication of A/D-converted data in double trigger mode • 1 register for temperature sensor • 1 register for internal reference voltage • 1 register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bits for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode.

Item	RX660 (S12ADH)	RX261 (S12ADE)
Data register	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) — A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.
Operating mode	• Single scan mode: — A/D conversion is performed only once on arbitrarily selected analog inputs. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — As the number of groups to be used, 2 (groups A and B) or 3 (groups A, B, and C) can be selected. (If 2 is selected, a combination of groups A and B only can be selected.) — Analog inputs, temperature sensor output, and internal reference voltage that are arbitrarily selected are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 25 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 25 arbitrarily selected channels. • Group scan mode: — Analog inputs of up to 25 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — The scanning start condition for groups A and B (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently.

Item	RX660 (S12ADH)	RX261 (S12ADE)
Operating mode	• Group scan mode (when group priority control selected): If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Restart of scanning (rescan) can be set for the lower-priority group after processing for the higher-priority group completes. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.	• Group scan mode (when group A priority control selected): — At a trigger input on group A during A/D conversion of group B, the A/D conversion of group B is suspended and the A/D conversion of group A is performed. — Restart (re-scan) setting is possible to restart the A/D conversion of group B at the completion of the A/D conversion of group A.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the general-purpose PWM timer (GPTW) or event link controller (ELC) • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.
Functions	• Variable sampling time (can be set per channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) — Ability to specify the channel conversion priority	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when using the compare function
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan.

Item	RX660 (S12ADH)	RX261 (S12ADE)
Interrupt sources	• In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan. An A/D scan end interrupt request (S12GBADI) for group B can be generated on completion of group B scan. An A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of a double scan of group A. When the scans of group B and group C are completed, their respective scan end interrupt requests (S12GBADI and S12GCADI) can be generated. • A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan. An A/D scan end interrupt request (GBADI) only for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan of group A. An A/D scan end interrupt request (GBADI) only for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).
Event link function	• An event can be output upon completion of all scans. • Scan can be started by a trigger output by the ELC. • In single scan mode, an event can be output when the compare function window condition is met.	• In group scan mode, an ELC event occurs at the completion of an A/D scan of a group other than group B. • In group scan mode, an ELC event occurs at the completion of an A/D scan of group B. • An ELC event occurs at the completion of all scans. • Scan can be started by a trigger output by the ELC. • In single scan mode, an ELC event occurs when the event condition of the window compare function is satisfied.
Low power consumption function	Ability to transition to module stop state	Ability to specify module stop state

Table 2.78 Comparison of the Registers for the 12-Bit A/D Converter

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADDRy	—	A/D data registers y (y = 0 to 23)	A/D data registers y (y = 0 to 8,16 to 31)
ADDBLDRA	—	A/D data duplication register A	—
ADDBLDRB	—	A/D data duplication register B	—

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADCSR	GBADIE	Group B scan end interrupt enable bit 0: Disable the scan end interrupt for group B 1: Enable the scan end interrupt for group B	Group B scan end interrupt enable bit 0: Disable generation of the GBADI interrupt after a scan of group B ends 1: Enable generation of the GBADI interrupt after a scan of group B ends
	ADHSC	—	A/D conversion operation select bit
	ADIE	Scan end interrupt enable bit 0: Disable the scan end interrupt 1: Enable the scan end interrupt	Scan end interrupt enable bit 0: Disable generation of the S12ADI0 interrupt after a scan ends 1: Enable generation of the S12ADI0 interrupt after a scan ends
ADANSA0	ANSA009 to ANSA015	A/D conversion channel select bits	—
ADANSA1	ANSA108 to ANSA115	—	A/D conversion channel select bits
ADANSB0	ANSB009 to ANSB015	A/D conversion channel select bits	—
ADANSB1	ANSB108 to ANSB115	—	A/D conversion channel select bits
ADANSC0	—	A/D channel select register C0	—
ADANSC1	—	A/D channel select register C1	—
ADSCSn	—	A/D channel conversion order setting register n (n = 0 to 23)	—
ADADS0	ADS009 to ADS015	A/D-converted value addition/average channel select bits	—
ADADS1	ADS108 to ADS115	—	A/D-converted value addition/average channel select bits
ADEXICR	TSSB	Group B temperature sensor output A/D conversion select bit	—
	OCSB	Group B internal reference voltage A/D conversion select bit	—
ADGCEXCR	—	A/D group C extended input control register	—
ADGCTRGR	—	A/D group C trigger select register	—
ADSSTRn	—	A/D sampling state register n (n = 0 to 15, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADDISCR	ADNDIS[4:0]	A/D disconnection detection assist setting bits b4 ADNDIS[4]: Selection of discharge or precharge 0: Discharge 1: Precharge The discharge/precharge period is specified by the number of ADCLK clock cycles. b3-b0 ADNDIS[3:0]: Period of discharge or precharge b3 b0 0 0 0 0: No charging (disconnection detection assist function disabled) 0 0 1 1: Charge period of 3 clock cycles 0 1 1 0: Charge period of 6 clock cycles 1 0 0 1: Charge period of 9 clock cycles 1 1 0 0: Charge period of 12 clock cycles 1 1 1 1: Charge period of 15 clock cycles Settings other than the above are prohibited.	A/D disconnection detection assist setting bits b4 ADNDIS[4]: Selection of discharge or precharge 0: Discharge 1: Precharge b3-b0 ADNDIS[3:0]: Period of discharge or precharge
ADELCCR	ELCC[2:0] (RX660) ELCC[1:0] (RX261)	Event link control bits b2 b0 0 0 0: An event is output upon completion of the scan of group A. 0 0 1: An event is output upon completion of the scan of group B. 0 1 0: An event is output upon completion of the scan of group A, group B, or group C. 1 0 0: An event is output upon completion of the scan of group C. Settings other than the above are prohibited.	Event link control bits b1 b0 0 0: In group scan mode, an event occurs upon completion of the scan of a group other than group B. 0 1: In group scan mode, an event occurs upon completion of the scan of group B. 1 x: An event occurs upon completion of all scans.

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADGSPCR	PGS	Group priority control setting bit 0: Priority control of a group is not performed. 1: Priority control of a group is performed.	Group A priority control setting bit 0: Priority control of group A is not performed. 1: Priority control of group A is performed.
	GBRSCN	Low priority group restart setting bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Restart is not made for the group suspended by group priority control. 1: Restart is made for the group suspended by group priority control.	Group B restart setting bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: In group A priority control, the A/D conversion of group B is not restarted after suspension. 1: In group A priority control, the A/D conversion of group B is restarted after suspension.
	LGRRS	Restart channel select bit	—
	GBRP	Single scan continuous start bit (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Single scan consecutive operation is not made. 1: Single scan consecutive operation is started for the group of the lowest priority.	Single scan continuous start bit for group B (Effective only when PGS = 1. This bit is reserved when PGS = 0.) 0: Single scan consecutive operation is not made for group B. 1: Single scan consecutive operation is started for group B.
ADCMPCR	CMPAB[1:0]	Window A/B complex conditions setting bits b1 b0 0 0: Sets the following complex condition: "<window A comparison condition is satisfied> OR <window B comparison condition is satisfied>" 0 1: Sets the following complex condition: "<window A comparison condition is satisfied> XOR <window B comparison condition is satisfied>"	Window A/B complex conditions setting bits b1 b0 0 0: If complex condition "<window A comparison condition is satisfied> OR <window B comparison condition is satisfied>" is true, S12ADWMELC is output. In other cases, S12ADWUMELC is output. 0 1: If complex condition "<window A comparison condition is satisfied> EXOR <window B comparison condition is satisfied>" is true, S12ADWMELC is output. In other cases, S12ADWUMELC is output.

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADCMPCR	CMPAB[1:0]	1 0: Sets the following complex condition: "<window A comparison condition is satisfied> AND <window B comparison condition is satisfied>" 1 1: Setting prohibited	1 0: If complex condition "<window A comparison condition is satisfied> AND <window B comparison condition is satisfied>" is true, S12ADWMELC is output. In other cases, S12ADWUMELC is output. 1 1: Setting prohibited.
	CMPBE	Compare window B operation enable bit 0: Compare window B operation is disabled. 1: Compare window B operation is enabled.	Compare window B operation enable bit 0: Compare window B operation is disabled. S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window B operation is enabled.
	CMPAE	Compare window A operation enable bit 0: Compare window A operation is disabled. 1: Compare window A operation is enabled.	Compare window A operation enable bit 0: Compare window A operation is disabled. S12ADWMELC and S12ADWUMELC outputs are disabled. 1: Compare window A operation is enabled.
	CMPBIE	Compare B interrupt enable bit	
	CMPAIE	Compare A interrupt enable bit	
ADCMPANSR0	CMPCHA009 to CMPCHA015	Compare window A channel select bits	—
ADCMPANSR1	CMPCHA108 to CMPCHA115	—	Compare window A channel select bits
ADCMPLR0	CMPLCHA009 to CMPLCHA015	Compare window A compare condition select bit	—
ADCMPLR1	CMPLCHA108 to CMPLCHA115	—	Compare window A compare condition select bit
ADCMPLER	CMPLTS (RX660) CMPLTSA (RX261)	Compare window A temperature sensor output compare condition select bit	Compare window A temperature sensor output compare condition select bit
	CMPLOC (RX660) CMPLOCA (RX261)	Compare window A internal reference voltage compare condition select bit	Compare window A internal reference voltage compare condition select bit
ADCMPSR0	CMPSTCHA009 to CMPSTCHA015	Compare window A flag	—
ADCMPSR1	CMPSTCHA108 to CMPSTCHA 115	—	Compare window A flag

Register	Bit	RX660 (S12AH)	RX261 (S12ADE)
ADCMPSER	CMPFTS (RX660) CMPSTTSA (RX261)	Compare window A temperature sensor output compare flag	Compare window A temperature sensor output compare flag
	CMPFOC (RX660) CMPSTOCA (RX261)	Compare window A internal reference voltage compare flag	Compare window A internal reference voltage compare flag
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits Selects a channel to be compared by the compare window B condition. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : : : : : 0 1 0 1 1 0: AN022 0 1 0 1 1 1: AN023 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.	Compare window B channel select bits Selects a channel to be compared by the compare window B condition. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 0 1 0 0 0: AN008 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : : 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADVMONCR	—	A/D internal reference voltage monitoring circuit enable register	—
ADVMONO	—	A/D internal reference voltage monitoring circuit output enable register	—
ADVREFCR	—	A/D reference voltage control register	—
ADBUFn	—	—	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register
ADCCR	—	—	A/D conversion cycle control register

2.28 Temperature Sensor

Table 2.79 shows a Comparison of the Registers for the Temperature Sensor.

Table 2.79 Comparison of the Registers for the Temperature Sensor

Register	Bit	RX660 (TEMPS)	RX261 (TEMPSA)
TSCDR	—	Temperature sensor calibration data register (b0 to b31)	Temperature sensor calibration data register (b0 to b15)

2.29 Data Operation Circuit

Table 2.80 shows a Comparative Overview of the Data Operation Circuit, and Table 2.81 shows a Comparison of the Registers for the Data Operation Circuit.

Table 2.80 Comparative Overview of the Data Operation Circuit

Item	RX660 (DOCA)	RX261 (DOC)
Data operation functions	• Comparison of 16- or 32-bit data (match/mismatch, greater-than/less-than, in-range/out-of-range) • Addition or subtraction of 16- or 32-bit data	• 16-bit data comparison, addition, and subtraction
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Interrupt	• When the data comparison result matches the detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (when an overflow occurs) • When the data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (when an underflow occurs)	• When the data comparison result matches the detection condition • When the result of data addition becomes greater than FFFFh (when an overflow occurs) • When the result of data subtraction becomes less than 0000h (when an underflow occurs)
Event link function (output)	• When the data comparison result matches the detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (when an overflow occurs) • When the data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (when an underflow occurs)	• When the data comparison result matches the detection condition • When the result of data addition becomes greater than FFFFh (when an overflow occurs) • When the result of data subtraction becomes less than 0000h (when an underflow occurs)

Table 2.81 Comparison of the Registers for the Data Operation Circuit

Register	Bit	RX660 (DOCA)	RX261 (DOC)
DOCR	DCSEL (RX660) DCSEL[2:0] (RX261)	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less-than (DODIR < DODSR0) 0 1 1: Greater-than (DODIR > DODSR0) 1 0 0: In-range (DODSR0 < DODIR < DODSR1) 1 0 1: Out-of-range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.	Detection condition select bits b2 0: Detect a mismatch 1: Detect a match
	DOPSZ	Data operation size select bit	—
DOCR	DOPCIE	Data operation circuit interrupt enable bit (b7)	Data operation circuit interrupt enable bit (b4)
	DOPCF	—	Data operation result flag
	DOPCFCL	—	Data operation result clear bit
DOSR	—	DOC status register	—
DOSCR	—	DOC status clear register	—
DODIR	—	DOC data input register (b0 to b31)	DOC data input register (b0 to b15)
DODSR0 (RX660) DODSR (RX261)	—	DOC data setting register 0 (b31 to b0)	DOC data setting register (b15 to b0)
DODSR1	—	DOC data setting register 1	—

2.30 RAM

Table 2.82 shows a Comparative Overview of RAM.

Table 2.82 Comparative Overview of RAM

Item	RX660	RX261
RAM capacity	128 KB	128 KB
RAM address	RAM: 0000 0000h to 0001 FFFFh	RAM: 0000 0000h to 0001 FFFFh
Memory bus	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Data retention function	The data retention function is not available for deep software standby mode.	—
Low power consumption function	Ability to transition to module stop state	Ability to specify module stop state
Error checking function	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.	• Parity error detection • A non-maskable interrupt or an interrupt is generated when an error occurs.

2.31 Flash Memory

Table 2.83 shows a Comparative Overview of Flash Memory, and Table 2.84 shows a Comparison of the Registers for Flash Memory.

Table 2.83 Comparative Overview of Flash Memory

Item	RX660 (FLASH)		RX261 (FLASH)
	Code flash memory	Data flash memory	—
Memory space	• User area: Maximum of 1 MB • User boot area: 32 KB	• Data area: 32 KB	• User area: Maximum of 512 KB • Data area: 8 KB • Extra area: Startup area information, access window information, and unique IDs are stored
Address	1 MB: FFF0 0000h to FFFF FFFFh 512 KB: FFF8 0000h to FFFF FFFFh Data flash memory 0100 0000h to 0100 7FFFh		512 KB: FFF8 0000h to FFFF FFFFh 384 KB: FFFA 0000h to FFFF FFFFh 256 KB: FFFC 0000h to FFFF FFFFh Data flash memory 0010 0000h to 0010 1FFFh
Operating clock	• FCLK: 4 to 60 MHz (during programming or erasure in code flash memory or data flash memory); up to 60 MHz (during a read from data flash memory)		• FCLK: 1 to 64 MHz (in ROM P/E mode or E2 data flash memory P/E mode); up to 64 MHz (during a read from E2 data flash memory) • HOCO clock: 24, 32, 48, or 64 MHz (in ROM P/E mode or E2 data flash memory P/E mode)
Read cycle	One cycle	A single read operation by 16- or 8-bit access requires 8 FCLK clock cycles.	One ICLK clock cycle
Value after erasure	FFh	Undefined	• ROM: FFh • E2 data flash memory: FFh

Item	RX660 (FLASH)		RX261 (FLASH)
	Code flash memory	Data flash memory	—
Programming/erasure method	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).		• Software commands can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface or USB interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).
Security function	Protects against illicit tampering with or reading of data in flash memory.		Protects against illicit tampering with or reading of data in flash memory.
Protection function	Protects against erroneous programming of the flash memory.		In self-programming, rewrite can be enabled for a specified area in the user area and disabled for other areas.
Trusted Memory (TM) function	Protects blocks 8 and 9 of code flash memory against illicit reads.		—
Background operation (BGO) function	Reading from the user area is possible during programming/erasure in the data area.		Programs deployed in ROM can be executed while the content of E2 data flash memory is being reprogrammed.
Units of programming and erasure	Programming in the user area or user boot area: In units of 256 bytes Erasure in the user area: In blocks	Programming in the data area: In units of 4 bytes Erasure in the data area: In blocks	• Programming in ROM: In units of 8 bytes • Programming in E2 data flash memory: In bytes • Erasure in both types of flash memory: In blocks
Other functions	Interrupts can be accepted during self-programming.		—
On-board programming (serial programming and self-programming)	Programming/erasure in boot mode (SCI interface) — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — Programming/erasure is possible in user boot area.		Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. — The user area and data area are programmable.

Item	RX660 (FLASH)		RX261 (FLASH)
	Code flash memory	Data flash memory	—
On-board programming (serial programming and self-programming)	Programming/erasure in boot mode (FINE interface) — FINE is used. Programming/erasure in user boot mode — User's own boot programs can be created. Programming/erasure in single-chip mode — Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.		Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. Boot mode (USB interface) — Channel 0 of the USB 2.0 function (USB0) module is used. — The user area and data area are programmable. — Flash memory can be rewritten in self-powered or bus-powered mode. — Can be connected to a computer using only a USB cable. Self-programming (single-chip mode) — The user area and data area are programmable using a flash programming routine in a user program.
Off-board programming (programming or erasure by using a parallel programmer)	Programming/erasure of the user area and user boot area is possible using a parallel programmer	Programming/erasure of the data area is not possible using a parallel programmer.	—
Start-up program protection function	—		This function enables the safe rewriting of block 0 to block 7.
Area protection	—		In self-programming, rewrite can be enabled for a specified area in the user area and disabled for other areas.
Unique ID	A unique 12-byte ID code is provided for each MCU.		A unique 16-byte ID code is provided for each MCU.

Table 2.84 Comparison of the Registers for Flash Memory

Register	Bit	RX660 (FLASH)	RX261 (FLASH)
FWEPROR	—	Flash P/E protect register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
FSADDR	—	FACI command processing start address register	—
FEADDR	—	FACI command processing end address register	—
DFLCTL	—	—	E2 DataFlash control register
FENTRYR	—	—	Flash P/E mode entry register
MEMWAITR	—	—	Memory wait cycle setting register
FPR	—	—	Protection unlock register
FPSR	—	—	Protection unlock status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial setting register
FRESETR	—	—	Flash reset register
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FWBn	—	—	Flash write buffer register n (n = 0 to 3)
FSTATR (RX660) FSTATR0 (RX261)	—	Flash status register (b31 to b0)	Flash status register 0 (b7 to b0)
	FLWEERR	Flash write/erase protect error flag	—
	PRGSPD	Programming suspend status flag	—
	ERSSPD	Erasure suspend status flag	—
	DBFULL	Data buffer full flag	—
	SUSRDY	Suspend ready flag	—
	PRGERR	Programming error flag (b12)	Programming error flag (b1)

Register	Bit	RX660 (FLASH)	RX261 (FLASH)
FSTATR (RX660) FSTATR0 (RX261)	ERSERR	Erasure error flag (b13)	Erasure error flag (b0)
	ILGLERR	Illegal command error flag (b14)	Illegal command error flag (b4)
	FRDY	Flash ready flag	—
	BCERR	—	Blank check error flag
	EILGLERR	—	Extra area illegal command error flag
FSTATR1	—	—	Flash status register 1
FENTRYR	—	Flash P/E mode entry register	—
FPROTR	—	Flash protection register	—
FSUINITR	—	Flash sequencer set-up initialization register	—
FLKSTAT	—	Lock bit status register	—
FCMDR	—	FACI command register	—
FPESTAT	—	Flash P/E status register	—
FBCCNT	—	Data flash blank check control register	—
FBCSTAT	—	Data flash blank check status register	—
FPSADDR	—	Data flash programming start address register	—
FCPSR	—	Flash sequencer processing switching register	—
FPCKAR	—	Flash sequencer processing clock frequency notification register	—
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash start-up setting monitor register
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register
UIDRn	—	Unique ID register n (n = 0 to 2)	Unique ID register n (n = 0 to 3)

2.32 Package

As indicated in Table 2.85, there are differences in the package drawing codes and availability of some package types. Please bear this in mind at the board design stage.

Table 2.85 Packages

Package type	RENESAS Code	
	RX660	RX261
144-pin LFQFP	○	×
48-pin HWQFN	×	○

○: Package available (RENESAS code omitted); ×: Package not available

3. Comparison of Pin Functions

The following presents a comparison of pin functions, and compares the pins used for the power supply, clocks, and system control. **Blue text** indicates pin functions that are included in only one of the MCU groups, and **red text** indicates pin functions that are present in both groups but differ in some respect. Pin functions whose specifications do not differ between the groups are shown in **black text**.

3.1 100-Pin Package

Table 3.1 shows a Comparison of the Pin Functions for the 100-Pin Package.

Table 3.1 Comparison of the Pin Functions for the 100-Pin Package

100-Pin	RX660 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
1	P06	P06*8
2	EMLE*1/P03*2/IRQ11*2/DA0*2	P03*8/DA0
3	P04	P04*8
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/ RTS0#/SS0#/IRQ11	PJ3/GTIOC6B/GTIOC6B#/CTS6#/RTS6#/SS6#
5	VCL	VCL
6	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
7	MD/FINED/PN6	MD/FINED/PG7
8	XCIN*3/PH7*4	XCIN/PH7
9	XCOUT*3/PH6*4	XCOUT/EXCIN/PH6
10	RES#	RES#
11	XTAL/P37/IRQ4	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36/IRQ5	EXTAL/P36/IRQ2
14	VCC	VCC
15	P35/NMI	UPSEL/P35/NMI
16	TRST#*1/P34/MTIOC0A/TMCI3/POE10#/SCK6/ SCK0/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/ IRQ4
17	P33/MTIOC0D/TMRI3/POE4#/POE11#/RXD6/ SMISO6/SSCL6/RXD0/SMISO0/SSCL0/ CRX0-A/IRQ3-DS	P33/GTIOC1B/GTIOC7B/GTIOC1B#/GTIOC7B#/ TMRI3/RXD6/SMISO6/SSCL6/CRX0*7/IRQ3
18	P32/MTIOC0C/TMO3/RTCIC2*5/RTCOUT*5/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/ SMOSI0/SSDA0/CTX0-A/IRQ2-DS	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*7/USB0_VBUSEN*7/TS0/IRQ2
19	TMS*1/P31/MTIOC4D/TMCI2/RTCIC1*5/ CTS1#/RTS1#/SS1#/IRQ1-DS	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	TDI*1/P30/MTIOC4B/TMRI3/RTCIC0*5/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	TCK*1/P27/CS3#/MTIOC2B/TMCI3/SCK1/IRQ7/ CVREFC3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
22	TDO*1/P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/ CMPC30	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*7/TS4
23	P25/CS1#/MTIOC4C/MTCLKB/RXD3/SMISO3/ SSCL3/IRQ5/ADTRG0#	P25/GTIOC1B/GTIOC6A/GTIOC1B#/GTIOC6A#/ GTETRGB/ADTRG0#
24	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/ IRQ12	P24/GTIOC1A/GTIOC6B/GTIOC1A#/GTIOC6B#/ GTETRGA/TMRI1/USB0_VBUSEN*7
25	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/SSDA3/ CTS0#/RTS0#/SS0#/IRQ3	P23/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/ GTETRGD/CTS000#/RTS000#/SS000#/DE000

100-Pin	RX660 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
26	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15	P22/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/ GTETRGC/TMO0/SCK000/TXDB000/ USB0_OVRCURB*7
27	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/ SSCL0/IRQ9	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/ TMCI0/RXD000/SMISO000/SSCL000/ USB0_EXICEN*7
28	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/ IRQ8	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/ TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/ USB0_ID*7
29	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
30	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*5/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*7/USB0_VBUSEN*7/ USB0_OVRCURB*7/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/SCK3/CRX0-C/IRQ5/CMPC20	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*7/TS5/IRQ5
32	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/CTX0-C/IRQ4/CVREFC2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*7/USB0_OVRCURA*7/TS6/IRQ4
33	P13/MTIOC0B/TMO3/TXD2/SMOSI2/SSDA2/ SDA0/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/ GTIV/TMO3/SDA0/IRQ3
34	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2	P12/TMCI1/SCL0/IRQ2
35	PH3/MTIOC4D/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
36	PH2/MTIOC4C/TMRI0/TOC1/IRQ1	PH2*6/GTIOC1B*6/GTIOC1B#*6/ TMRI0*6/USB0_DM*6/TS8*6/IRQ1*6
37	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0	PH1*6/GTIOC0B*6/GTIOC0B#*6/ GTOULO*6/TMO0*6/USB0_DP*6/TS9*6/ IRQ0*6
38	PH0/MTIOC3B/CACREF/ADTRG0#	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
39	P55/D0[A0/D0]/WAIT#/MTIOC4D/MTIOC4A/ TMO3/CRX0-D/IRQ10	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*7/TS11
40	P54/ALE/D1[A1/D1]/MTIOC4B/TMCI1/CTS2#/ RTS2#/SS2#/CTX0-D/IRQ4	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*7/ TS12
41	P53/BCLK/PMC0/IRQ3	P53/PMC0
42	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2	P52
43	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1	P51/PMC0
44	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/IRQ0	P50
45	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/TXD010-C/ SMOSI010-C/SSDA010-C/MISOA-A/IRQ14	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
46	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/TMCI2/ TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*7TS14

100-Pin	RX660 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
47	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/TXDB008/RSPCKA/USB0_ID*7/PMC0/TS15
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/RTS010#-B/SS010#-B/DE010-B/SSLA0-A/PMC0/IRQ12	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1/SCK5/CTS008#/RTS008#/SS008#/DE008/SSLA0/PMC0/TSCAP
49	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/PMC0/IRQ11	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
50	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/TXDB011-A/SSLA3-A/IRQ10	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/A17/MTIOC3A/SCK5/TXD011-C/SMOSI011-C/SSDA011-C/TXDA011-C/SSLA2-A/IRQ12	PC1/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/SCK5/SSLA2
52	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/RXD011-C/SMISO011-C/SSCL011-C/SSLA1-A/IRQ14	PC0/GTIOC6B/GTIOC6B#/GTETRGC/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/TXD011-B/SMOSI011-B/SSDA011-B/IRQ15	PB7/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
54	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/RXD011-B/SMISO011-B/SSCL011-B/IRQ6	PB6/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
55	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE4#/TOC2/SCK9/SCK11/SCK011-B/IRQ13	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*7/TS20
56	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/CTS011#-B/RTS011#-B/SS011#-B/DE011-B/IRQ4	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
57	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
58	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/IRQ2	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
59	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS/COMP1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/IRQ12	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
62	VSS	VSS
63	PA7/A7/MISOA-B/IRQ7	PA7/GTIOC5B/GTIOC5B#/MISOA
64	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27

100-Pin	RX660 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
66	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/SSLA0-B/ IRQ5-DS/CVREFC1/ADST0	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
68	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/RXD12/ SMISO12/SSCL12/RXDX12/SSLA3-B/IRQ10	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/MTIOC3B/ SCK5/SCK12/SSLA2-B/IRQ11/ADTRG0#	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
70	PA0/BC0#/A0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/ GTOVUP/CACREF/SSLA1/TS32
71	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/TOC1/ IRQ7/AN015	PE7/IRQ7/AN023
72	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/TIC1/ CTS4#/RTS4#/SS4#/IRQ6/AN014	PE6/IRQ6/AN022
73	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/ IRQ5/AN021/CMPOB0
74	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/AN012	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
75	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/POE8#/ MTIOC1B/TOC3/CTS12#/RTS12#/SS12#/IRQ11/ AN011	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/ TS34/AN019
76	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/ CVREFB0
77	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/MTIOC3B/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ IRQ9/AN009/CMPC00	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/AN017/ CMPB0
78	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/SCK12/ IRQ8/AN008	PE0/SCK12/AN016
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023	PD7/IRQ7/AN031
80	PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/IRQ6/ AN022	PD6/IRQ6/AN030
81	PD5/D5[A5/D5]/MTIC5W/POE10#/MTIOC8C/ IRQ5/AN021	PD5/IRQ5/AN029
82	PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/AN020	PD4/IRQ4/AN028
83	PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/IRQ3/ AN019	PD3/IRQ3/AN027
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/CRX0-B/IRQ2/ AN018	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*[7]/IRQ2/ AN026
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/CTX0-B/IRQ1/ AN017	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/ SSCL6/CTX0*[7]/IRQ1/AN025
86	PD0/D0[A0/D0]/POE4#/IRQ0/AN016	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P47/IRQ15-DS/AN007	P47*[8]/AN007
88	P46/IRQ14-DS/AN006	P46*[8]/AN006
89	P45/IRQ13-DS/AN005	P45*[8]/AN005

100-Pin	RX660 (100-Pin LFQFP)	RX261 (100-Pin LFQFP)
90	P44/IRQ12-DS/AN004	P44*8/AN004
91	P43/IRQ11-DS/AN003	P43*8/AN003
92	P42/IRQ10-DS/AN002	P42*8/AN002
93	P41/IRQ9-DS/AN001	P41*8/AN001
94	VREFL0/PJ7	VREFL0/PJ7*8
95	P40/IRQ8-DS/AN000	P40*8/AN000
96	VREFH0/PJ6	VREFH0/PJ6*8
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07*8/ADTRG0#
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05*8/DA1

Notes: 1. Not available for products without the JTAG interface.
2. Not available for products with the JTAG interface.
3. Not available on products that do not have a sub-clock oscillator.
4. Not available on products that have a sub-clock oscillator.
5. Not available on products that do not have a sub-clock oscillator.
6. Not available on the RX261.
7. Not available on the RX260.
8. The power supply to the I/O buffers for these pins is AVCC0.

3.2 80-Pin Package

Table 3.2 shows a Comparison of the Pin Functions for the 80-Pin Package.

Table 3.2 Comparison of the Pin Functions for the 80-Pin Package

80-Pin	RX660 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
1	P06	P06*6
2	P03/IRQ11/DA0	P03*6/DA0
3	P04	P04*6
4	VCL	VCL
5	PJ1/MTIOC3A	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
6	MD/FINED/PN6	MD/FINED/PG7
7	XCIN*1/PH7*2	XCIN/PH7
8	XCOUT*1/PH6*2	XCOUT/EXCIN/PH6
9	RES#	RES#
10	XTAL/P37/IRQ4	XTAL/P37/IRQ4
11	VSS	VSS
12	EXTAL/P36/IRQ5	EXTAL/P36/IRQ2
13	VCC	VCC
14	P35/NMI	UPSEL/P35/NMI
15	P34/MTIOC0A/TMCI3/POE10#/SCK6/SCK0/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/IRQ4
16	P32/MTIOC0C/TMO3/RTCIC2*3/RTCOUT*3/POE0#/POE10#/TXD6/SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/CTX0-A/IRQ2-DS	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/CTX0*5/USB0_VBUSEN*5/TS0/IRQ2
17	P31/MTIOC4D/TMCI2/RTCIC1*3/CTS1#/RTS1#/SS1#/IRQ1-DS	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
18	P30/MTIOC4B/TMRI3/RTCIC0*3/POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
19	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
20	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*5/TS4
21	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/TMCI0/RXD000/SMISO000/SSCL000/USB0_EXICEN*5
22	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/IRQ8	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/USB0_ID*5
23	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/MISOA-C/SDA2/IRQ7/COMP2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
24	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*3/TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/MOSIA-C/SCL2/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0_VBUS*5/USB0_VBUSEN*5/USB0_OVRCURB*5/IRQ6/ADTRG0#
25	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/SCK3/CRX0-C/IRQ5/CMPC20	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/CRX0*5/TS5/IRQ5
26	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/SS1#/CTX0*5/USB0_OVRCURA*5/TS6/IRQ4

80-Pin	RX660 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
27	P13/MTIOC0B/TMO3/SDA0/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/GTIV/TMO3/SDA0/IRQ3
28	P12/MTIC5U/TMCI1/SCL0/IRQ2	P12/TMCI1/SCL0/IRQ2
29	PH3/MTIOC4D/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
30	PH2/MTIOC4C/TMRI0/TOC1/IRQ1	PH2*4/GTIOC1B*4/GTIOC1B#*4/TMRI0*4/USB0_DM*5/TS8*4/IRQ1*4
31	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0	PH1*4/GTIOC0B*4/GTIOC0B#*4/GTOULO*4/TMO0*4/USB0_DP*5/TS9*4/IRQ0*4
32	PH0/MTIOC3B/CACREF/ADTRG0#	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/TS10
33	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/IRQ10	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/TMO3/CRX0*5/TS11
34	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*5/TS12
35	UB/PC7/MTIOC3A/MTCLKB/TMO2/CACREF/TOC0/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/TXD10/TXD010-C/SMOSI010-C/SSDA010-C/MISOA-A/IRQ14	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/GTCPPO0/TMO2/LPTO/CACREF/TXD008/TXDA008/SMOSI008/SSDA008/MISOA/TS13
36	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/SMISO8/SSCL8/SMISO10/SSCL10/RXD10/RXD010-C/SMISO010-C/SSCL010-C/MOSIA-A/IRQ13	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/RXD008/SMISO008/SSCL008/MOSIA/USB0_EXICEN*5/TS14
37	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/TXDB008/RSPCKA/USB0_ID*5/PMC0/TS15
38	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/SS10#/CTS10#/RTS10#/CTS010#-B/RTS010#-B/SS010#-B/DE010-B/SSLA0-A/PMC0/IRQ12	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1/SCK5/CTS008#/RTS008#/SS008#/DE008/SSLA0/PMC0/TSCAP
39	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/PMC0/IRQ11	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
40	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/TXDB011-A/SSLA3-A/IRQ10	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
41	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/SMOSI11/SSDA11/TXD11/TXD011-B/SMOSI011-B/SSDA011-B/IRQ15	PB7/PC1*7/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
42	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/SMISO11/SSCL11/RXD11/RXD011-B/SMISO011-B/SSCL011-B/IRQ6	PB6/PC0*7/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
43	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/TOC2/SCK9/SCK11/SCK011-B/IRQ13	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*5/TS20
44	PB4/CTS9#/RTS9#/SS9#/SS11#/CTS11#/RTS11#/CTS011#-B/RTS011#-B/SS011#-B/DE011-B/IRQ4	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
45	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
46	PB2/CTS4#/RTS4#/SS4#/CTS6#/RTS6#/SS6#/IRQ2	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23

80-Pin	RX660 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
47	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS/COMP1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
48	VCC	VCC
49	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/IRQ12	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
50	VSS	VSS
51	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
52	PA5/MTIOC6B/RSPCKA-B/IRQ5	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
53	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/SSLA0-B/IRQ5-DS/CVREFC1/ADST0	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
54	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
55	PA2/MTIOC7A/RXD5/SMISO5/SSCL5/RXD12/SMISO12/SSCL12/RXDX12/SSLA3-B/IRQ10	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
56	PA1/MTIOC0B/MTCLKC/MTIOC7B/MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ADTRG0#	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
57	PA0/MTIOC4A/CACREF/MTIOC6D/SSLA1-B/IRQ0	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
58	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/COMP0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
59	PE4/MTIOC4D/MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/AN012	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
60	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/SS12#/IRQ11/AN011	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
61	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/RXDX12/IRQ7-DS/AN010/CVREFC0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
62	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ9/AN009/CMPC00	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
63	PE0/MTIOC3D/SCK12/IRQ8/AN008	PE0/SCK12/AN016
64	PD2/MTIOC4D/TIC2/CRX0-B/IRQ2/AN018	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*5/IRQ2/AN026
65	PD1/MTIOC4B/POE0#/CTX0-B/IRQ1/AN017	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/SSCL6/CTX0*5/IRQ1/AN025
66	PD0/POE4#/IRQ0/AN016	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
67	P47/IRQ15-DS/AN007	P47*6/AN007
68	P46/IRQ14-DS/AN006	P46*6/AN006
69	P45/IRQ13-DS/AN005	P45*6/AN005

80-Pin	RX660 (80-Pin LFQFP)	RX261 (80-Pin LFQFP)
70	P44/IRQ12-DS/AN004	P44*6/AN004
71	P43/IRQ11-DS/AN003	P43*6/AN003
72	P42/IRQ10-DS/AN002	P42*6/AN002
73	P41/IRQ9-DS/AN001	P41*6/AN001
74	VREFL0/PJ7	VREFL0/PJ7*6
75	P40/IRQ8-DS/AN000	P40*6/AN000
76	VREFH0/PJ6	VREFH0/PJ6*6
77	AVCC0	AVCC0
78	P07/IRQ15/ADTRG0#	P07*6/ADTRG0#
79	AVSS0	AVSS0
80	P05/IRQ13/DA1	P05*6/DA1

Notes: 1. Not available on products that do not have a sub-clock oscillator.
2. Not available on products that have a sub-clock oscillator.
3. Not available on products that do not have a sub-clock oscillator.
4. Not available on the RX261.
5. Not available on the RX260.
6. The power supply to the I/O buffers for these pins is AVCC0.
7. PC0 and PC1 are effective only when the port switching function is selected.

3.3 64-Pin Package

Table 3.3 shows a Comparison of the Pin Functions for the 64-Pin Package.

Table 3.3 Comparison of the Pin Functions for the 64-Pin Package

64-Pin	RX660 (64-Pin LFQFP)	RX261 (64-Pin LFQFP)
1	P03/IRQ11/DA0	P03*6/DA0
2	VCL	VCL
3	MD/FINED/PN6	MD/FINED/PG7
4	XCIN*1/PH7*2	XCIN/PH7
5	XCOUT*1/PH6*2	XCOUT/EXCIN/PH6
6	RES#	RES#
7	XTAL/P37/IRQ4	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36/IRQ5	EXTAL/P36/IRQ2
10	VCC	VCC
11	P35/NMI	UPSEL/P35/NMI
12	P32/MTIOC0C/TMO3/RTCIC2*3/RTCOUT*3/ POE0#/POE10#/TXD6/SMOSI6/SSDA6/ CTX0-A/IRQ2-DS	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*5/USB0_VBUSEN*5/TS0/IRQ2
13	P31/MTIOC4D/TMCI2/RTCIC1*3/CTS1#/RTS1#/ SS1#/IRQ1-DS	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	P30/MTIOC4B/TMRI3/RTCIC0*3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0-DS/COMP3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1/IRQ7/CVREFC3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*5/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/RTCOUT*3/ TXD1/SMOSI1/SSDA1/RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*5/USB0_VBUSEN*5/ USB0_OVRCURB*5/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/SCK3/CRX0-C/IRQ5/CMPC20	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*5/TS5/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/CTX0-C/IRQ4/CVREFC2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*5/USB0_OVRCURA*5/TS6/IRQ4
21	PH3/MTIOC4D/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
22	PH2/MTIOC4C/TMRI0/TOC1/IRQ1	PH2*4/GTIOC1B*4/GTIOC1B#*4/ TMRI0*4/USB0_DM*5/TS8*4/IRQ1*4
23	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0	PH1*4/GTIOC0B*4/GTIOC0B#*4/ GTOULO*4/TMO0*4/USB0_DP*5/TS9*4/ IRQ0*4
24	PH0/MTIOC3B/CACREF/ADTRG0#	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
25	P55/MTIOC4D/MTIOC4A/TMO3/CRX0-D/IRQ10	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*5/TS11
26	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*5/TS12

64-Pin	RX660 (64-Pin LFQFP)	RX261 (64-Pin LFQFP)
27	UB/PC7/MTIOC3A/MTCLKB/TMO2/CACREF/ TOC0/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/TXD010-C/SMOSI010-C/SSDA010-C/ MISOA-A/IRQ14	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
28	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*5/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/ SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*5/PMC0/TS15
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/SS10#/ CTS10#/RTS10#/CTS010#-B/RTS010#-B/ SS010#-B/DE010-B/SSLA0-A/PMC0/IRQ12	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/PMC0/ IRQ11	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/ SMOSI5/SSDA5/PMC0/TS16
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/ RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/SMOSI11/ SSDA11/TXD11/TXD011-B/SMOSI011-B/ SSDA011-B/IRQ15	PB7/PC1*7/GTIOC0A/GTIOC7B/GTIOC0A#/ GTIOC7B#/TXD009/TXDA009/SMOSI009/ SSDA009/TS18
34	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/SMISO11/ SSCL11/RXD11/RXD011-B/SMISO011-B/ SSCL011-B/IRQ6	PB6/PC0*7/GTIOC0B/GTIOC7A/GTIOC0B#/ GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/TOC2/ SCK9/SCK11/SCK011-B/IRQ13	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/ USB0_VBUS*5/TS20
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/TIC2/ SCK4/SCK6/PMC0/IRQ3	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/ TMO0/LPTO/SCK6/PMC0/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/SMOSI4/ SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS/COMP1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/ TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/ CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/RSPCKA-C/IRQ12	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/ GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1

64-Pin	RX660 (64-Pin LFQFP)	RX261 (64-Pin LFQFP)
44	PA1/MTIOC0B/MTCLKC/MTIOC7B/MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ADTRG0#	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
45	PA0/MTIOC4A/CACREF/MTIOC6D/SSLA1-B/IRQ0	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/COMP0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/MTIOC4A/MTIOC7D/IRQ12/AN012	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
48	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/SS12#/IRQ11/AN011	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
49	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/RXDX12/IRQ7-DS/AN010/CVREFC0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
50	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/IRQ9/AN009/CMPC00	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
51	PE0/MTIOC3D/SCK12/IRQ8/AN008	PE0/SCK12/AN016
52	P47/IRQ15-DS/AN007	P47*6/AN007
53	P46/IRQ14-DS/AN006	P46*6/AN006
54	P45/IRQ13-DS/AN005	P45*6/AN005
55	P44/IRQ12-DS/AN004	P44*6/AN004
56	P43/IRQ11-DS/AN003	P43*6/AN003
57	P42/IRQ10-DS/AN002	P42*6/AN002
58	P41/IRQ9-DS/AN001	P41*6/AN001
59	VREFL0/PJ7	VREFL0/PJ7*6
60	P40/IRQ8-DS/AN000	P40*6/AN000
61	VREFH0/PJ6	VREFH0/PJ6*6
62	AVCC0	AVCC0
63	P07/IRQ15/ADTRG0#	P05*6/DA1
64	AVSS0	AVSS0

Notes: 1. Not available on products that do not have a sub-clock oscillator.
2. Not available on products that have a sub-clock oscillator.
3. Not available on products that do not have a sub-clock oscillator.
4. Not available on the RX261.
5. Not available on the RX260.
6. The power supply to the I/O buffers for these pins is AVCC0.
7. PC0 to PC3 are effective only when the port switching function is selected.

3.4 48-Pin Package

Table 3.4 shows a Comparison of the Pin Functions for the 48-Pin Package.

Table 3.4 Comparison of the Pin Functions for the 48-Pin Package

48-Pin	RX660 (48-Pin LFQFP)	RX261 (48-Pin LFQFP/HWQFN)
1	VCL	VCL
2	MD/FINED/PN6	MD/FINED/PG7
3	RES#	RES#
4	XTAL/P37/IRQ4	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36/IRQ5	EXTAL/P36/IRQ2
7	VCC	VCC
8	P35/NMI	UPSEL/P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ IRQ1-DS	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ CTS1#/RTS1#/SS1#/TS1/IRQ1
10	P30/MTIOC4B/POE8#/RXD1/SMISO1/SSCL1/ IRQ0-DS/COMP3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RXD1/SMISO1/SSCL1/TS2/IRQ0
11	P27/MTIOC2B/SCK1/IRQ7/CVREFC3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ CTS3#/RTS3#/SS3#/IRQ6/CMPC30	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/MOSIA-C/SCL2/ IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/ USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/ SSCL1/SCK3/CRX0-C/IRQ5/CMPC20	P15/GTIOC3B/GTIOC5B/GTIOC3B#/ GTIOC5B#/GTETRGB/GTIV/TMCI2/RXD1/ SMISO1/SSCL1/CRX0*2/TS5/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/ SS1#/CTX0-C/IRQ4/CVREFC2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/ GTIOC7B#/GTETRGA/GTCPPO0/TMRI2/ CTS1#/RTS1#/SS1#/CTX0*2/ USB0_OVRCURA*2/TS6/IRQ4
17	PH3/MTIOC4D/TMCI0	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
18	PH2/MTIOC4C/TMRI0/TOC1/IRQ1	PH2*1/GTIOC1B*1/GTIOC1B#*1/ TMRI0*1/USB0_DM*2/TS8*1/IRQ1*1
19	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/ TS9*1/IRQ0*1
20	PH0/MTIOC3B/CACREF/ADTRG0#	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
21	UB/PC7/MTIOC3A/MTCLKB/TMO2/CACREF/ TOC0/TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/TXD010-C/SMOSI010-C/SSDA010-C/ MISOA-A/IRQ14	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
22	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14

48-Pin	RX660 (48-Pin LFQFP)	RX261 (48-Pin LFQFP/HWQFN)
23	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/PMC0/ IRQ5	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/SS10#/ CTS10#/RTS10#/CTS010#-B/RTS010#-B/ SS010#-B/DE010-B/SSLA0-A/PMC0/IRQ12	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/ GTIOC3A#/GTETRGC/GTIU/GTOULO/TMCI1/ SCK5/CTS008#/RTS008#/SS008#/DE008/ SSLA0/PMC0/TSCAP
25	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/TOC2/ IRQ13	PB5/PC3*4/GTIOC4B/GTIOC5A/GTIOC4B#/ GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/ USB0_VBUS*2/TS20
26	PB3/MTIOC0A/MTIOC4A/TMO0/POE11#/TIC2/ SCK4/SCK6/PMC0/IRQ3	PB3/PC2*4/GTIOC1A/GTIOC3A/GTIOC1A#/ GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/ GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
27	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/SMOSI4/ SSDA4/TXD6/SMOSI6/SSDA6/IRQ4-DS/COMP1	PB1/PC1*4/GTIOC1B/GTIOC2B/GTIOC1B#/ GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/ GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/ TS24/IRQ4/CMPOB1
28	VCC	VCC
29	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/SSCL4/ RXD6/SMISO6/SSCL6/RSPCKA-C/IRQ12	PB0/PC0*4/GTIOC0B/GTIOC2A/GTIOC0B#/ GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/ RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/POE10#/MTIOC3D/ CTS5#/RTS5#/SS5#/CTS12#/RTS12#/SS12#/ MOSIA-B/IRQ14	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/ GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/ RTS5#/SS5#/MOSIA/TS26
32	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/ GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/ SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
33	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/ GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/ GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/ SSCL5/TS29/IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/MTIOC7B/MTIOC3B/ SCK5/SCK12/SSLA2-B/IRQ11/ADTRG0#	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/ GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/ GTIV/GTOUUP/SCK5/SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/MTIOC4A/MTIOC7D/ IRQ12/AN012	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
36	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/CTS12#/ RTS12#/SS12#/IRQ11/AN011	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/TS34/ AN019
37	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/IRQ7-DS/AN010/CVREFC0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/CMPC00	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SSDA12/TXDX12/SIOX12/AN017/CMPB0
39	P47/IRQ15-DS/AN007	P47*3/AN007
40	P46/IRQ14-DS/AN006	P46*3/AN006
41	P45/IRQ13-DS/AN005	P45*3/AN005
42	P42/IRQ10-DS/AN002	P42*3/AN002
43	P41/IRQ9-DS/AN001	P41*3/AN001

48-Pin	RX660 (48-Pin LFQFP)	RX261 (48-Pin LFQFP/HWQFN)
44	VREFL0/PJ7	VREFL0/PJ7*3
45	P40/IRQ8-DS/AN000	P40*3/AN000
46	VREFH0/PJ6	VREFH0/PJ6*3
47	AVCC0	AVCC0
48	AVSS0	AVSS0

Notes: 1. Not available on the RX261.
2. Not available on the RX260.
3. The power supply to the I/O buffers for these pins is AVCC0.
4. PC0 to PC3 are effective only when the port switching function is selected.

4. Important Information when Migrating Between MCUs

This section provides notes on differences between the RX261 Group and RX660 Group MCUs.

4.1 Considerations for Functional Design

Some of the software that runs on the RX660 Group is compatible with the RX261 Group. However, due to differences in aspects such as operation timing and electrical characteristics, you must evaluate your circumstances thoroughly.

The following explains software-related matters to consider in relation to function settings that differ between the RX261 Group and RX660 Group.

Section 1, “Comparison of Built-In Functions of the RX260/RX261 Group and the RX660 Group” explains the differences between modules and functions.

For details, refer to the User’s Manual: Hardware document listed in section 5, “Reference Documents”.

4.1.1 Clock Frequency Settings

The RX261 Group and RX660 Group have different restrictions in relation to clock frequency settings. For details, refer to Table 4.1.

Table 4.1 Comparison of the Restrictions on the Clock Frequency Settings

Item	RX660	RX261
Restrictions on the clock frequency settings	ICLK ≥ BCLK, PCLKA ≥ PCLKB PCLKB ≥ CANFDCLK (when CANFD is used) PCLKB ≥ CANFDMCLK (when CANFD is used)	PCLKA ≥ PCLKB PCLKB ≥ CANFDCLK (when CANFD is used) PCLKB ≥ CANFDMCLK (when CANFD is used)
Restrictions on the clock frequency ratios	ICLK:FCLK = N:1 or 1:N CLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKB:PCLKD = 1:1 or 2:1 or 4:1 or 1:2 PCLKA:PCLKB = 2:1 (when CANFD is used)	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKB = 2:1 (when CANFD is used)

4.1.2 PLL Circuit

The frequency multiplication factors of the PLL circuit that can be set for the RX660 Group and RX261 Group MCUs are different. For the RX660 Group MCU, the settable range is from ×10 to ×30 (in 0.5 increments). For the RX261 Group MCU, the settable range is from ×4 to ×15.5 (in 0.5 increments). To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.3 Initialization of the Voltage Detection Level Select Register (LVDLVLR)

The procedure for initializing the LVDLVLR register is different.

4.1.4 Initialization of the Sub-clock Oscillator Control Register (SOSCCR)

The procedure for initializing the SOSCCR register is different.

5. Reference Documents

User’s Manual: Hardware

RX660 Group User's Manual: Hardware Rev.1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

RX260/RX261 Group User's Manual: Hardware Rev.1.00 (R01UH1045EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This application note reflects the content of the following technical update:

- TN-RX*-A0270A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun. 7, 2024	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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