RX260/RX261 Group, RX230/RX231 Group

Differences Between the RX260/RX261 Group and the RX230/RX231 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX261 Group and RX231 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 100-pin package version of the RX261 Group and the 100-pin package version of the RX231 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware for the products in question.

Target Devices

RX260/RX261 Group and RX230/RX231 Group

Contents

1. Comparison of Built-In Functions of RX260/RX261 Group and RX230/RX231 Group

A comparison of the built-in functions of the RX260/RX261 Group and RX230/RX231 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 shows a Comparison of Built-In Functions of RX230/RX231 Group and RX260/RX261 Group.

Table 1.1 Comparison of Built-In Functions of RX230/RX231 Group and RX260/RX261 Group

Function	RX230/ RX231	RX260/ RX261
CPU	●	
Operating modes	■	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	●/▲	
Voltage detection circuit (LVDAb)	●/▲	
Clock generation circuit	●/▲/■	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	●/■	
Battery backup function	○	×
Register write protection function	●/■	
Exception handling	○	
Interrupt controller (ICUb)	●/■	
Buses	●/▲/■	
Memory-protection unit (MPU)	○	
DMA controller (DMACA)	○	
Data transfer controller (DTCa): RX230/RX231, (DTCb): RX260/RX261	●	
Event link controller (ELC)	●/■	
I/O ports	●/■	
Multi-function pin controller (MPC)	●/▲/■	
Multi-function timer pulse unit 2 (MTU2a)	○	×
General purpose PWM timer (GPTWa)	×	○
Port output enable 2 (POE2a)	○	×
Port output enable for GPTW (POEGc)	×	○
16-bit timer pulse unit (TPUa)	○	×
8-bit timer (TMR): RX230/RX231, (TMRa): RX260/RX261	●	
Compare match timer (CMT)	○	
Realtime clock (RTCe): RX230/RX231, (RTCBa): RX260/RX261	■	
Low-power timer (LPT): RX230/RX231, (LPTa): RX260/RX261	●	
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	

Function	RX230/ RX231	RX260/ RX261
USB 2.0 host/function module (USBd): RX231, *1 USB 2.0 FS host/function module (USBe): RX261*2	●/■	
Serial communications interface (SCIg, SCIh): RX230/RX231, (SCIk, SCIh): RX260/RX261	●/▲/■	
Serial communications interface (RSCI)	×	○
IrDA interface	○	×
I²C bus interface (RIICa)	○	
CAN module (RSCAN): RX231,*1 CAN FD module (CANFD): RX261*2	●/▲/■	
Serial sound interface (SSI)	○	×
Serial peripheral interface (RSPIa):RX230/RX231, (RSPIc):RX260/RX261	●/▲/■	
CRC calculator (CRC)	○	
SD host interface (SDHIa)*1	○	×
Trusted Secure IP (TSIP-Lite)*1	○	×
Renesas Secure IP (RSIP-E11A)*2	×	○
Capacitive touch sensing unit (CTSU): RX230/RX231, (CTSU2SLa): RX260/RX261	●/▲/■	
Remote control signal receiver (REMCa)	×	○
12-bit A/D converter (S12ADE)	●/▲	
12-bit D/A converter (R12DAA): RX230/RX231, D/A converter (DAa): RX260/RX261	▲	
Temperature sensor (TEMPSA)	▲	
Comparator B (CMPBa)	●/■	
Data operation circuit (DOC)	○	
RAM	●/▲	
Flash memory (FLASH)	●/▲/■	
Packages	●/■	

Notes: 1. Not implemented on RX230 Group products.
2. Not implemented on RX260 Group products.

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Items with no differences in register specifications are not listed.

2.1 CPU

Table 2.1 shows a Comparative Overview of CPUs.

Table 2.1 Comparative Overview of CPUs

Item	RX231	RX261
CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 64 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: — 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 111 instructions — Standard provided instructions: 111 Basic instructions: 77, variable-length instruction format Single-precision floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

2.2 Operating Modes

Table 2.2 shows a Comparative Overview of Operating Modes, and Table 2.3 shows a Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX231	RX261
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	Boot mode (USB interface)
	Boot mode (FINE interface)	Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode	—

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX231	RX261
SYSCR0	—	System control register 0	—

2.3 Address Space

Figure 2.1 shows a Comparative Memory Map in Single-Chip Mode.

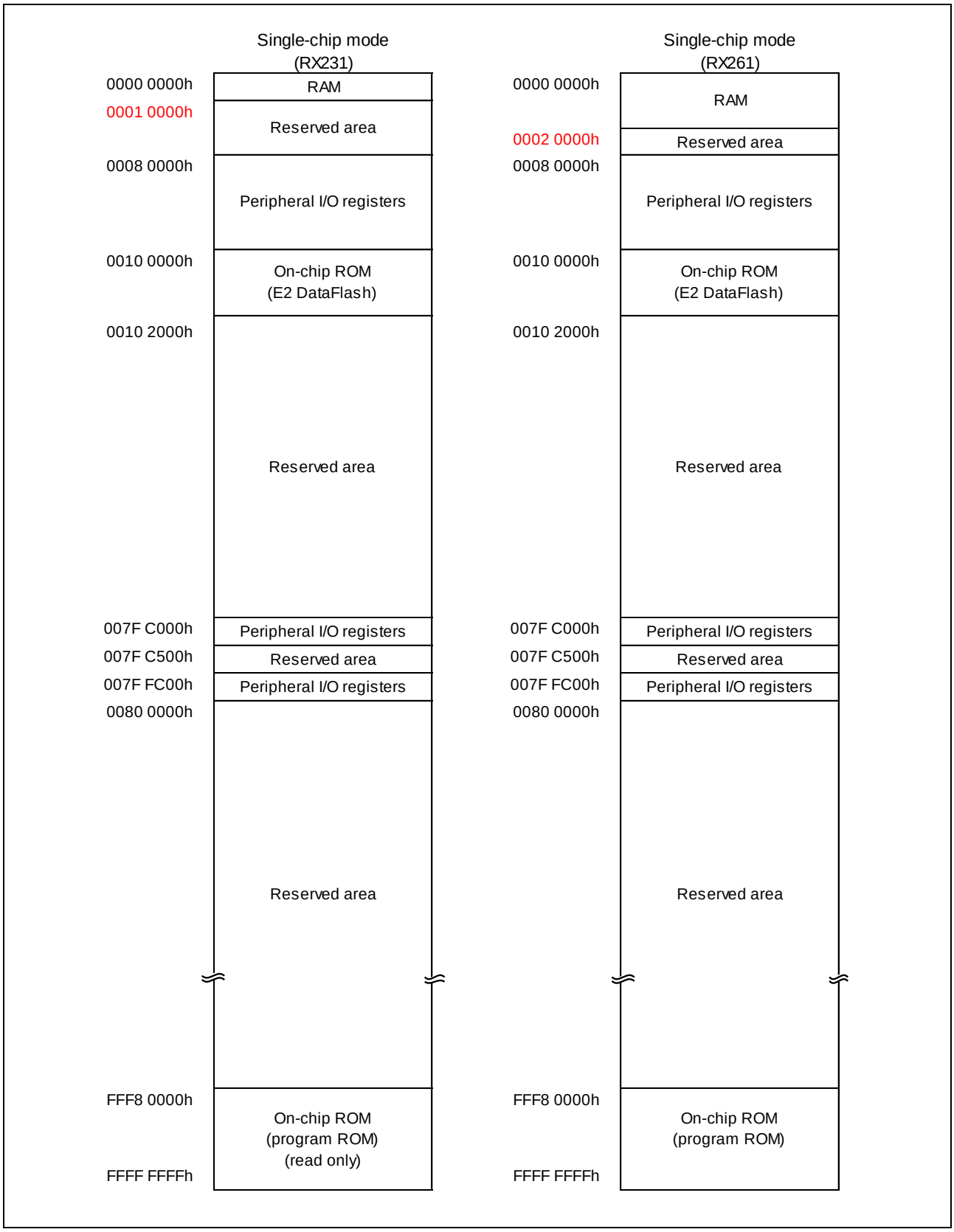

Figure 2.1 Comparative Memory Map in Single-Chip Mode

2.4 Option-Setting Memory

Table 2.4 shows a Comparison of Option-Setting Memory Registers.

Table 2.4 Comparison of Option-Setting Memory Registers

Register	Bit Name	RX231 (OFSM)	RX261(OFSM)
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected. 0 1: 2.82 V is selected. 1 0: 2.51 V is selected. 1 1: 1.90 V is selected.	Voltage detection 0 level select bits b1 b0 0 0: 3.85 V is selected. 0 1: 2.85 V is selected. 1 0: 2.53 V is selected. 1 1: 1.90 V is selected.
	VDSEL2	—	Voltage detection 0 level select bit 2
	HOCOFRQ[1:0]	—	HOCO frequency selection bits

2.5 Voltage Detection Circuit

Table 2.5 shows a Comparative Overview of Voltage Detection Circuits, and Table 2.6 shows a Comparison of Voltage Detection Circuit Registers.

Table 2.5 Comparative Overview of Voltage Detection Circuits

Item		RX231 (LVDAb)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	When voltage drops below Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2
				Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.			Switching between VCC and the voltage input on the CMPA2 pin can be accomplished using the LVCMPCR.EXVCCINP2 bit.
	Detection voltage	Selectable from four levels using the OFS1 register	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits	Selectable from five levels using the OFS1 register	Selectable from 16 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits
	Monitoring flags	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection

Item		RX231 (LVDAb)			RX261 (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Processing upon voltage detection	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or the CMPA2 pin: CPU restart timing selectable: after specified time with VCC or the CMPA2 pin > Vdet2, or after specified time with Vdet2 > VCC or the CMPA2 pin	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or the CMPA2 pin: CPU restart timing selectable: after specified time with VCC or the CMPA2 pin > Vdet2, or after specified time with Vdet2 > VCC or the CMPA2 pin
	Interrupts	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable and maskable interrupt	Selectable between non-maskable and maskable interrupt		Selectable between non-maskable and maskable interrupt	Selectable between non-maskable and maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or the CMPA2 pin, VCC or the CMPA2 pin > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC or the CMPA2 pin, VCC or the CMPA2 pin > Vdet2, or both
Event link function		—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection	—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection

Table 2.6 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX231 (LVDAb)	RX261 (LVDAb)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.16 V 0 0 1 0: 4.03 V 0 0 1 1: 3.86 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.80 V 1 0 0 0: 2.68 V 1 0 0 1: 2.59 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V 1 1 1 0: 1.75 V 1 1 1 1: 1.65 V Settings other than the above are prohibited.
LVDLVLR	LVD2LVL[1:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b5 b4 0 0: 4.32 V 0 1: 4.17 V 1 0: 4.03 V 1 1: 3.84 V

2.6 Clock Generation Circuit

Table 2.7 shows a Comparative Overview of Clock Generation Circuits, and Table 2.8 shows a Comparison of Clock Generation Circuit Registers.

Table 2.7 Comparative Overview of Clock Generation Circuits

Item	RX231	RX261
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKA, PCLKB, and PCLKD) to be supplied to peripheral modules. The peripheral module clock PCLKA is the operating clock for the MTU2, the peripheral module clock PCLKD is for the S12AD, and PCLKB is for modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CAN clock (CANMCLK) to be supplied to the RSCAN. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the SSI clock (SSISCK) to be supplied to the SSI.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the CANFD (message buffer RAM) and GPTW. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the USB clock (UCLK) to be supplied to the USB. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX231	RX261
Operating frequency	• ICLK: 54 MHz (max.) • PCLKA: 54 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 54 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • BCLK: 32 MHz (max.) • BCLK pin output: 16 MHz (max.) • UCLK: 48 MHz • CANMCLK: 20 MHz (max.) • LPTCLK: Same frequency as that of the selected oscillator • CACCLK: Same frequency as that of each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • SSISCK: 20 MHz (max.)	• ICLK: 64 MHz (max.) • PCLKA: 64 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 64 MHz (max.) • FCLK: — 1 MHz to 64 MHz (for programming and erasing the ROM and E2 DataFlash) — 64 MHz (max.) (for reading from the E2 DataFlash) • UCLK: 48 MHz • CANFDCLK: 32 MHz (max.) • CANFDMCLK: 20 MHz (max.) • LPTCLK: — 32.768 kHz (when the sub-clock is selected) — 15 kHz (when the IWDT-dedicated clock (IWDTCLK) is selected) — 1 MHz (when the LOCO clock frequency divided by 4 is selected) • REMCLK: Same frequency as that of the selected oscillator • CACCLK: Same frequency as that of the selected oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz
Main clock oscillator	• Resonator frequency: — 1 MHz to 20 MHz (VCC ≥ 2.4 V) — 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When detecting a main clock oscillation stop, this function switches the system clock source to the LOCO and drives the MTU pin to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When detecting a main clock oscillation stop, this function switches the system clock source to the LOCO and drives the GPTW pin to high-impedance. • Drive capacity switching function

Item	RX231	RX261
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN, XCOUT • Drive capacity switching function	• Resonator frequency: 32.768 kHz • External clock input frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN, XCOUT • Sub-clock external input pin: EXCIN • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 13.5 (increments of 0.5) • Oscillation frequency: 24 MHz to 54 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz
PLL2 circuit	—	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 4 to 15.5 (increments of 0.5) • Oscillation frequency: 24 MHz to 64 MHz
USB-dedicated PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 6 MHz, 8 MHz, and 12 MHz • Frequency multiplication ratio: Selectable from 4, 6, 8, and 12 • Oscillation frequency: 48 MHz (VCC ≥ 2.4 V)	—
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz and 54 MHz	• Oscillation frequency: 24 MHz, 32 MHz, 48 MHz, and 64 MHz
Low-speed on-chip oscillator (LOCO)	• Oscillation frequency: 4 MHz	• Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	• Oscillation frequency: 15 kHz	• Oscillation frequency: 15 kHz

Table 2.8 Comparison of Clock Generation Circuit Registers

Register	Bit	RX231	RX261
SCKCR	BCLK[3:0]	External bus clock (BCLK) select bits	—
	PSTOP1	BCLK pin output control bit	—
PLLCR	STC[5:0]	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13 0 1 1 0 1 0: ×13.5 Settings other than the above are prohibited.	Frequency multiplication factor select bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 0 1 0 0 0 0: ×8.5 0 1 0 0 0 1: ×9 0 1 0 0 1 0: ×9.5 0 1 0 0 1 1: ×10.0 0 1 0 1 0 0: ×10.5 0 1 0 1 0 1: ×11.0 0 1 0 1 1 0: ×11.5 0 1 0 1 1 1: ×12.0 0 1 1 0 0 0: ×12.5 0 1 1 0 0 1: ×13.0 0 1 1 0 1 0: ×13.5 0 1 1 0 1 1: ×14.0 0 1 1 1 0 0: ×14.5 0 1 1 1 0 1: ×15.0 0 1 1 1 1 0: ×15.5 Settings other than the above are prohibited.
PLL2CR	—	—	PLL2 control register
PLL2CR2	—	—	PLL2 control register 2
UPLLCR	—	USB-dedicated PLL control register	—
UPLLCR2	—	USB-dedicated PLL control register 2	—
BCKCR	—	External bus clock control register	—
SOSCCR	SOSTP	Sub-clock oscillator control register	Sub-clock oscillator control register
		Initial value after a reset differs.	
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
OSCOVFSR	PL2OVF	—	PLL2 clock oscillation stabilization flag
	UPLOVF	USB-dedicated PLL clock oscillation stabilization flag	—

Register	Bit	RX231	RX261
CKOCR	CKOSEL [3:0]	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Sub-clock 0 1 0 0: PLL Settings other than the above are prohibited.	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO is selected. 0 0 0 1: HOCO is selected. 0 0 1 0: Main clock oscillator is selected. 0 0 1 1: Sub-clock oscillator is selected. 0 1 0 0: PLL circuit is selected. 1 0 0 0: CTSU observation clock is selected. Settings other than the above are prohibited.
	CKODIV [2:0]	CLKOUT output division ratio select bits b14 b12 0 0 0: No division 0 0 1: x1/2 0 1 0: x1/4 0 1 1: x1/8 1 0 0: x1/16 Settings other than the above are prohibited.	CLKOUT output division ratio select bits b14 b12 0 0 1: x1/1 0 0 1: x1/2 0 1 0: x1/4 0 1 1: x1/8 1 0 0: x1/16 1 0 1 x1/32 1 1 0: x1/64 1 1 1: x1/128
MEMWAIT	—	Memory wait cycle setting register	—

Register	Bit	RX231	RX261
MOSCWTCR	MSTS[4:0]	Main clock oscillator wait b4 b0 0 0 0 0 0: Wait time = 2 cycles (0.5 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)	Main clock oscillator wait b4 b0 0 0 0 0 0: Wait time = 0 cycle (0 µs) 0 0 0 0 1: Wait time = 1,024 cycles (256 µs) 0 0 0 1 0: Wait time = 2,048 cycles (512 µs) 0 0 0 1 1: Wait time = 4,096 cycles (1.024 ms) 0 0 1 0 0: Wait time = 8,192 cycles (2.048 ms) 0 0 1 0 1: Wait time = 16,384 cycles (4.096 ms) 0 0 1 1 0: Wait time = 32,768 cycles (8.192 ms) 0 0 1 1 1: Wait time = 65,536 cycles (16.384 ms) 0 1 0 0 0: Wait time = 131,072 cycles (32.768 ms) Settings other than the above are prohibited. Wait time when LOCO = 4.0 MHz (0.25 µs, TYP.)
MOFCR	MODRV21	Main clock oscillator drive capability switch bit VCC ≥ 2.4 V 0: 1 MHz to less than 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited.	Main clock oscillator drive capability switch bit 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz
LOFCR	—	—	Low-speed on-chip oscillator forced oscillation control register
LOCOTRR	—	Low-speed on-chip oscillator trimming register	—
LOCOTRR2	—	—	Low-speed on-chip oscillator trimming register 2
HOCOTRR3	—	High-speed on-chip oscillator trimming register 3	—
CANFDCKDIVCR	—	—	CANFD clock frequency division control register
USBCKCR	—	—	USB clock control register
CANFDCKCR	—	—	CANFD clock control register
SOMCR	—	—	Sub-clock oscillator mode control register

2.7 Low Power Consumption

Table 2.9 shows a Comparative Overview of Low Power Consumption Functions, Table 2.10 shows a Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 shows a Comparison of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX231	RX261
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), high-speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), external bus clock (BCLK), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKA, PCLKB, or PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode • Snooze mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, deep sleep mode, and snooze mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Four operating power control modes are available: — High-speed operating mode — Middle-speed operating mode — Middle-speed operating mode 2 — Low-speed operating mode

Table 2.10 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX231	RX261
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PLL2	—	Operation possible
	USB-dedicated PLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Operation possible (retained)	Operation possible (retained)
	DMAC	Operation possible	Operation possible
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Deep sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	PLL2	—	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX231	RX261
Deep sleep mode	USB-dedicated PLL	Operation possible	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	PLL2	—	Stopped
	USB-dedicated PLL	Stopped	—
	CPU	Stopped (retained)	Stopped (retained)
	RAM	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Low-power timer (LPT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX231	RX261
Software standby mode	RTCOUT output	Operation possible	Operation possible
	CLKOUT output	Operation possible	Operation possible
	Comparator B	Operation possible	Operation possible
Snooze mode	Transition method	—	When snooze transition conditions are met while in software standby mode
	Method of cancellation other than reset	—	Interrupt or occurrence of snooze end condition
	State after cancellation	—	Program execution state (interrupt processing) or software standby mode
	Main clock oscillator	—	Operation possible
	Sub-clock oscillator	—	Operation possible
	High-speed on-chip oscillator	—	Operation possible
	Low-speed on-chip oscillator	—	Operation possible
	IWDT-dedicated on-chip oscillator	—	Operation possible
	PLL	—	Operation possible
	PLL2	—	Operation possible
	CPU	—	Stopped (retained)
	RAM	—	Operation possible (retained)
	DMAC	—	Stopped (retained)
	DTC	—	Operation possible
	Flash memory	—	Stopped (retained)
	Watchdog timer (WDT)	—	Stopped (retained)
	Independent watchdog timer (IWDT)	—	Operation possible
	Realtime clock (RTC)	—	Operation possible
	Low-power timer (LPT)	—	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	Voltage detection circuit (LVD)	—	Operation possible
	Power-on reset circuit	—	Operation
	Peripheral modules	—	Operation possible
	I/O ports	—	Operation
	RTCOUT output	—	Operation possible
	CLKOUT output	—	Operation possible
	Comparator B	—	Operation possible

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX231	RX261
SBYCR	OPE	Output port enable bit	—
MSTPCRA	MSTPA7	—	General purpose PWM timer module stop bit
	MSTPA9	Multi-function timer pulse unit 2 module stop bit	—
	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop bit	—
MSTPCRB	MSTPB0	RSCAN0 module stop bit	—
MSTPCRC	MSTPC0	RAM module stop bit Target module: RAM (0000 0000h to 0000 FFFFh)	RAM module stop bit Target module: RAM (0000 0000h to 0001 FFFFh)
	MSTPC20	IrDA module stop bit	—
	MSTPC29	—	Remote control signal receiver module stop bit
MSTPCRD	MSTPD9	—	CANFD0 module stop bit
	MSTPD15	Serial sound interface module stop bit	—
	MSTPD19	SD host interface (SDHI) module stop bit	—
	MSTPD31	Trusted Secure IP function module stop bit*1, *2, *3	RSIP module stop bit
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than the above are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1 0 0: Middle-speed operating mode 2 Settings other than the above are prohibited.
SOPCCR	SOPCM	Sub operating power control mode select bit 0: High-speed or middle-speed operating mode 1: Low-speed operating mode	Sub operating power control mode select bit 0: High-speed or middle-speed operating mode, or middle-speed operating mode 2 1: Low-speed operating mode
SNZCR	—	—	Snooze control register
SNZCR2	—	—	Snooze control register 2
RPSCR	—	—	RAM power-saving control register

Notes: 1. This bit is reserved on chip version A of the RX231 Group. To initialize unused circuits, once set it to 0 at the beginning of the program.
2. Even if the Trusted Secure IP function is not used on chip version B of the RX231 Group, it should be set to 0 at the beginning of the program to initialize any unused circuits.
3. This bit is reserved on chip version C of the RX231 Group and in the RX230 Group. It is read as 1. The write value should be 1.

2.8 Register Write Protection Function

Table 2.12 shows a Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX231	RX261
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, BCKCR, HOCOCR2, MEMWAIT, LOCOTRR, ILOCOTRR, HOCOTRR0, HOCOTRR3	• Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, PLL2CR, PLL2CR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, LOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR2, ILOCOTRR, HOCOTRR0, SOMCR, CANFDCKCR, CANFDCKDIVCR, USBCKCR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR, RPSCR, SNZCR, SNZCR2 • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	• Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	• Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPCMR1, LPWUCR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR • Registers related to the battery backup function: VBATTCR, VBATTSR, VBTLVDICR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Interrupt Controller

Table 2.13 shows a Comparative Overview of Interrupt Controllers, and Table 2.14 shows a Comparison of Interrupt Controller Registers.

Table 2.13 Comparative Overview of Interrupt Controllers

Item		RX231 (ICUb)	RX261 (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection — The detection method is fixed for each connected peripheral module source.	• Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source)
Interrupts	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each interrupt source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each interrupt source. • Digital filter function: Supported
	Software interrupts	• Interrupt generated by writing to a register • Number of sources: 1	• Interrupt generated by writing to a register • Number of sources: 1
	Event link interrupts	An ELSR8l, ELSR18l, or ELSR19l interrupt can be generated by an ELC event.	An ELSR8l, ELSR18l, or ELSR19l interrupt can be generated by an ELC event.
	Interrupt priority	Specified by registers.	Specified by registers.
	Fast interrupt function	Faster interrupt handling by the CPU can be specified for a single interrupt source only.	Faster interrupt handling by the CPU can be specified for a single interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.

Item		RX231 (ICUb)	RX261 (ICUb)
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: — Falling edge — Rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	WDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	IWDT underflow/refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage detection circuit 1 (LVD1)	Interrupt from voltage detection circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage detection circuit 2 (LVD2)	Interrupt from voltage detection circuit 2 (LVD2)
	VBATT voltage monitoring interrupt	Voltage monitoring interrupt of the VBATT	—
	RAM error interrupt	—	Interrupt on detection of a parity check error in RAM
Return from low power consumption state	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by any non-maskable interrupt or any other interrupt source.
	Deep sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by any non-maskable interrupt or any other interrupt source.
	Software standby mode	Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or an RTC alarm/periodic interrupt.	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC interval, REMC, or USB0 resume), or ELSR8I interrupt (LPT-dedicated interrupt).
	Snooze mode	—	Return is initiated by an NMI pin interrupt, external pin interrupt (IRQ0 to IRQ7), peripheral interrupt (IWDT, voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC interval, REMC, or USB0 resume), or SNZI interrupt (snooze cancellation interrupt).

Table 2.14 Comparison of Interrupt Controller Registers

Register	Bit	RX231 (ICUb)	RX261 (ICUb)
NMISR	VBATST	VBATT voltage monitoring interrupt status flag	—
	RAMST	—	RAM error interrupt status flag
NMIER	VBATST	VBATT voltage monitoring interrupt status flag	—
	RAMEN	—	RAM error interrupt enable bit
NMICLR	VBATCLR	VBAT clear bit	—

2.10 Buses

Table 2.15 shows a Comparative Overview of Buses.

Table 2.15 Comparative Overview of Buses

Item		RX231	RX261
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	• Connected to RAM	• Connected to RAM
	Memory bus 2	• Connected to ROM	• Connected to ROM
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	• Connected to peripheral modules (USB0, RSCAN, and CTSU) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (USB0, CANFD, CTSU, REMC, and RSCI) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (GPTW) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	—	• Connected to peripheral modules (CANFD (message buffer RAM)) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX231	RX261
Internal peripheral buses	Internal peripheral bus 6	• Connected to the flash control module and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to the external devices • Operates in synchronization with the external bus clock (BCLK)	—

2.11 Data Transfer Controller

Table 2.16 shows a Comparative Overview of Data Transfer Controllers, and Table 2.17 shows a Comparison of Data Transfer Controller Registers.

Table 2.16 Comparative Overview of Data Transfer Controllers

Item	RX231 (DTCa)	RX261 (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either "performed only when the transfer counter becomes 0" or "every time" can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either "performed only when the transfer counter becomes 0" or "every time" can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX231 (DTCa)	RX261 (DTCb)
Transfer space	• 16 MB in short-address mode (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • 4 GB in full-address mode (Area from 0000 0000h to FFFF FFFFh except reserved areas)	• 16 MB in short-address mode (Areas from 0000 0000h to 007F FFFFh and FF80 0000h to FFFF FFFFh except reserved areas) • 4 GB in full-address mode (Area from 0000 0000h to FFFF FFFFh except reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	An event link request is generated after one data transfer (for block transfers, after one block).
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of the transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to the module-stop state	Ability to transition to the module-stop state

Table 2.17 Comparison of Data Transfer Controller Registers

Register	Bit	RX231 (DTCa)	RX261 (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.12 Event Link Controller

Table 2.18 shows a Comparative Overview of Event Link Controllers, Table 2.19 shows a Comparison of Event Link Controller Registers, Table 2.20 lists Correspondences between ELSRn Registers and Peripheral Modules, and Table 2.21 lists Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers.

Table 2.18 Comparative Overview of Event Link Controllers

Item	RX231 (ELC)	RX261 (ELC)
Event link function	• 63 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event signal input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be set by grouping multiple specified ports among total of eight ports.	• 116 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event signal input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be set by grouping multiple specified ports among total of eight ports.
Low power consumption function	Ability to transition to the module-stop state	Ability to transition to the module-stop state

Table 2.19 Comparison of Event Link Controller Registers

Register	Bit	RX231 (ELC)	RX261 (ELC)
ELSRn	—	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 14 to 16, 18 to 29)	Event link setting register n (n = 7, 8, 10, 12, 14 to 16, 18 to 28, 48 to 56)
	ELS[7:0]	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 08h to 6Ah: Specifies the number for the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 1Fh to C6h: Specifies the number for the event signal to be linked. Settings other than the above are prohibited.
ELOPA	—	Event link option setting register A	—
ELOPB	—	Event link option setting register B	—

Table 2.20 Correspondences between ELSRn Registers and Peripheral Modules

Register	RX231 (ELC)	RX261 (ELC)
ELSR1	MTU1	—
ELSR2	MTU2	—
ELSR3	MTU3	—
ELSR4	MTU4	—
ELSR7	CMT1	CMT1
ELSR8	ICU (LPT-dedicated interrupt)	ICU (LPT-dedicated interrupt)
ELSR10	TMR0	TMR0
ELSR12	TMR2	TMR2
ELSR14	CTSU	CTSU
ELSR15	S12AD	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR29	POE	—
ELSR48	—	GPTW event source A (common to all channels)
ELSR49	—	GPTW event source B (common to all channels)
ELSR50	—	GPTW event source C (common to all channels)
ELSR51	—	GPTW event source D (common to all channels)
ELSR52	—	GPTW event source E (common to all channels)
ELSR53	—	GPTW event source F (common to all channels)
ELSR54	—	GPTW event source G (common to all channels)
ELSR55	—	GPTW event source H (common to all channels)
ELSR56	—	S12AD (ELCTRG01N)

Table 2.21 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	RX231 (ELC)	RX261 (ELC)
08h	MTU1 compare match 1A	—
09h	MTU1 compare match 1B	—
0Ah	MTU1 overflow	—
0Bh	MTU1 underflow	—
0Ch	MTU2 compare match 2A	—
0Dh	MTU2 compare match 2B	—
0Eh	MTU2 overflow	—
0Fh	MTU2 underflow	—
10h	MTU3 compare match 3A	—
11h	MTU3 compare match 3B	—
12h	MTU3 compare match 3C	—
13h	MTU3 compare match 3D	—
14h	MTU3 overflow	—
15h	MTU4 compare match 4A	—
16h	MTU4 compare match 4B	—
17h	MTU4 compare match 4C	—
18h	MTU4 compare match 4D	—
19h	MTU4 overflow	—
1Ah	MTU4 underflow	—
1Fh	CMT1 compare match 1	CMT1 compare match 1
22h	TMR0 compare match A0	TMR0 compare match A0
23h	TMR0 compare match B0	TMR0 compare match B0
24h	TMR0 overflow	TMR0 overflow
28h	TMR2 compare match A2	TMR2 compare match A2
29h	TMR2 compare match B2	TMR2 compare match B2
2Ah	TMR2 overflow	TMR2 overflow
2Eh	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
31h	IWDT underflow or refresh error	IWDT underflow or refresh error
32h	LPT compare match	LPT compare match 0
33h	—	LPT compare match 1
34h	S12AD comparison conditions met	S12AD comparison conditions met
35h	S12AD comparison conditions not met	S12AD comparison conditions not met
3Ah	SCI5 error (receive error or error signal detection)	SCI5 error (receive error or error signal detection)
3Bh	SCI5 receive data full	SCI5 receive data full
3Ch	SCI5 transmit data empty	SCI5 transmit data empty
3Dh	SCI5 transmit end	SCI5 transmit end
4Eh	RIIC0 communication error or event generation	RIIC0 communication error or event generation
4Fh	RIIC0 receive data full	RIIC0 receive data full
50h	RIIC0 transmit data empty	RIIC0 transmit data empty
51h	RIIC0 transmit end	RIIC0 transmit end

Value of ELS[7:0] Bits	RX231 (ELC)	RX261 (ELC)
52h	RSPI0 error (mode fault, overrun, or parity error)	RSPI0 error (mode fault, overrun, underrun, or parity error)
53h	RSPI0 idle	RSPI0 idle
54h	RSPI0 receive data full	RSPI0 receive data full
55h	RSPI0 transmit data empty	RSPI0 transmit data empty
56h	RSPI0 transmit end	RSPI0 transmit end
58h	S12AD A/D conversion end	S12AD A/D conversion end
59h	Comparator B0 comparison result change	Comparator B0 comparison result change
5Ah	Comparator B0/B1 common comparison result change	Comparator B0/B1 common comparison result change
5Bh	LVD1 voltage detection	LVD1 voltage detection
5Ch	LVD2 voltage detection	LVD2 voltage detection
5Dh	DMAC0 transfer end	DMAC0 transfer end
5Eh	DMAC1 transfer end	DMAC1 transfer end
5Fh	DMAC2 transfer end	DMAC2 transfer end
60h	DMAC3 transfer end	DMAC3 transfer end
61h	DTC transfer end	DTC transfer end
62h	Oscillation stop detection of the clock generation circuit	Oscillation stop detection of the clock generation circuit
63h	Input port group 1 input edge detection	Input port group 1 input edge detection
64h	Input port group 2 input edge detection	Input port group 2 input edge detection
65h	Single input port 0 input edge detection	Single input port 0 input edge detection
66h	Single input port 1 input edge detection	Single input port 1 input edge detection
67h	Single input port 2 input edge detection	Single input port 2 input edge detection
68h	Single input port 3 input edge detection	Single input port 3 input edge detection
69h	Software event	Software event
6Ah	DOC data operation condition met	DOC data operation condition met
80h	—	GPTW0 compare match A
81h	—	GPTW0 compare match B
82h	—	GPTW0 compare match C
83h	—	GPTW0 compare match D
84h	—	GPTW0 compare match E
85h	—	GPTW0 compare match F
86h	—	GPTW0 overflow
87h	—	GPTW0 underflow
88h	—	GPTW0 A/D conversion start request A
89h	—	GPTW0 A/D conversion start request B
8Ah	—	GPTW1 compare match A
8Bh	—	GPTW1 compare match B
8Ch	—	GPTW1 compare match C
8Dh	—	GPTW1 compare match D
8Eh	—	GPTW1 compare match E
8Fh	—	GPTW1 compare match F
90h	—	GPTW1 overflow
91h	—	GPTW1 underflow

Value of ELS[7:0] Bits	RX231 (ELC)	RX261 (ELC)
92h	—	GPTW1 A/D conversion start request A
93h	—	GPTW1 A/D conversion start request B
94h	—	GPTW2 compare match A
95h	—	GPTW2 compare match B
96h	—	GPTW2 compare match C
97h	—	GPTW2 compare match D
98h	—	GPTW2 compare match E
99h	—	GPTW2 compare match F
9Ah	—	GPTW2 overflow
9Bh	—	GPTW2 underflow
9Ch	—	GPTW2 A/D conversion start request A
9Dh	—	GPTW2 A/D conversion start request B
9Eh	—	GPTW3 compare match A
9Fh	—	GPTW3 compare match B
A0h	—	GPTW3 compare match C
A1h	—	GPTW3 compare match D
A2h	—	GPTW3 compare match E
A3h	—	GPTW3 compare match F
A4h	—	GPTW3 overflow
A5h	—	GPTW3 underflow
A6h	—	GPTW4 compare match A
A7h	—	GPTW4 compare match B
A8h	—	GPTW4 compare match C
A9h	—	GPTW4 compare match D
AAh	—	GPTW4 compare match E
ABh	—	GPTW4 compare match F
ACh	—	GPTW4 overflow
ADh	—	GPTW4 underflow
AEh	—	GPTW5 compare match A
AFh	—	GPTW5 compare match B
B0h	—	GPTW5 compare match C
B1h	—	GPTW5 compare match D
B2h	—	GPTW5 compare match E
B3h	—	GPTW5 compare match F
B4h	—	GPTW5 overflow
B5h	—	GPTW5 underflow
B6h	—	GPTW6 compare match A
B7h	—	GPTW6 compare match B
B8h	—	GPTW6 compare match C
B9h	—	GPTW6 compare match D
BAh	—	GPTW6 compare match E
BBh	—	GPTW6 compare match F
BCh	—	GPTW6 overflow
BDh	—	GPTW6 underflow
BEh	—	GPTW7 compare match A

Value of ELS[7:0] Bits	RX231 (ELC)	RX261 (ELC)
BFh	—	GPTW7 compare match B
C0h	—	GPTW7 compare match C
C1h	—	GPTW7 compare match D
C2h	—	GPTW7 compare match E
C3h	—	GPTW7 compare match F
C4h	—	GPTW7 overflow
C5h	—	GPTW7 underflow
C6h	—	GPTW (OPS) UVW-phase input edge detection

2.13 I/O Ports

Table 2.22 to Table 2.24 show a comparative overview of I/O ports, Table 2.25 shows a Comparison of I/O Port Functions, and Table 2.27 shows a Comparison of I/O Port Registers.

Table 2.22 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX231 (100-Pin)	RX261 (100-Pin)
PORT0	P03, P05, P07	P03 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTG	—	PG7
PORTH[*1]	—	PH0, PH3, PH6, PH7
PORTJ	PJ3	PJ1, PJ3, PJ6, PJ7

Note: 1. There are PH0 to PH3 ports on the RX230, and PH1 and PH2 ports on the RX260.

Table 2.23 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX231 (64-Pin)	RX261 (64-Pin)
PORT0	P03, P05	P03, P05
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P47
PORT5	P54, P55	P54, P55
PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC2 to PC7	PC0 to PC7
PORTE	PE0 to PE5	PE0 to PE5
PORTG	—	PG7
PORTH[*1]	—	PH0, PH3, PH6, PH7
PORTJ	—	PJ6, PJ7

Note: 1. There are PH0 to PH3 ports on the RX230, and PH1 and PH2 ports on the RX260.

Table 2.24 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX231 (48-Pin)	RX261 (48-Pin)
PORT1	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40 to P42, P46	P40 to P42, P45 to P47
PORTA	PA1, PA3, PA4, PA6	PA1, PA3, PA4, PA6
PORTB	PB0, PB1, PB3, PB5	PB0, PB1, PB3, PB5
PORTC	PC4 to PC7	PC0 to PC7
PORTE	PE1 to PE4	PE1 to PE4
PORTG	—	PG7
PORTH[*1]	—	PH0, PH3
PORTJ	—	PJ6, PJ7

Note: 1. There are PH0 to PH3 ports on the RX230, and PH1 and PH2 ports on the RX260.

Table 2.25 Comparison of I/O Port Functions

Item	Port Symbol	RX231	RX261
Input pull-up function	PORT0	P03, P05, P07	P03 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	P50 to P55
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTG	—	PG7
	PORTH[*1]	—	PH0, PH3
	PORTJ	PJ3	PJ1, PJ3, PJ6, PJ7
Open drain output function	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT5	P50 to P52, P54	P50 to P52, P54
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE7
	PORTG	—	PG7
	PORTJ	PJ3	—
5 V tolerant	PORT1	P12, P13, P16, P17	P12, P13, P16, P17
	PORTB	PB5	—

Note: 1. There are PH0 to PH3 ports on the RX230, and PH1 and PH2 ports on the RX260.

Table 2.26 Comparison of Drive Capacity Switching on I/O Ports

Port Symbol	Drive Capacity Switching	RX231	RX261
PORT0	Fixed to normal	P03, P05, P07	P03 to P07
	Normal/high	—	—
PORT1	Fixed to normal	—	P12 to P17
	Normal/high	P12 to P17	—
PORT2	Fixed to normal	—	P20 to P27
	Normal/high	P20 to P27	—
PORT3	Fixed to normal	P36, P37	P30 to P34, P36, P37
	Normal/high	P30 to P34	—
PORT4	Fixed to normal	P40 to P47	P40 to P47
	Normal/high	—	—
PORT5	Fixed to normal	—	P50 to P55
	Normal/high	P50 to P55	—
PORTA	Fixed to normal	—	PA0 to PA7
	Normal/high	PA0 to PA7	—
PORTB	Fixed to normal	—	PB0 to PB7
	Normal/high	PB0 to PB7	—
PORTC	Fixed to normal	—	PC0 to PC7
	Normal/high	PC0 to PC7	—
PORTD	Fixed to normal	—	PD0 to PD7
	Normal/high	PD0 to PD7	—
PORTE	Fixed to normal	—	PE0 to PE7
	Normal/high	PE0 to PE7	—
PORTG	Fixed to normal	—	PG7
	Normal/high	—	—
PORTH[*1]	Fixed to normal	—	PH0, PH3, PH6, PH7
	Normal/high	—	—
PORTJ	Fixed to normal	—	PJ1, PJ3, PJ6, PJ7
	Normal/high	PJ3	—

Note: 1. There are PH0 to PH3 ports for normal/high drive capacity switching on the RX230, and PH1 and PH2 ports for fixed-to-normal drive capacity on the RX260.

Table 2.27 Comparison of I/O Port Registers

Register	Bit Name	RX231*1	RX261*1
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, J)	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, G, H, J)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, J)	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, G, H, J)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to E, J)	Pm0 to Pm7 bits (m = 0 to 5, A to E, G, H, J)
PMR	B0 to B7	Pm0 to Pm7 pin mode control bits (m = 0 to 5, A to E, J)	Pm0 to Pm7 pin mode control bits (m = 0 to 5, A to E, G, H, J)
ODR0	B2, B3,	Pm1 output type select bits (m =1 to 3, 5, A to C, E, J) • P21, P31, P51, PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 output type select bits (m = 1 to 3, 5, A to E) • P21, P31, P51, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Setting prohibited.
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m =1 to 3, 5, A to C, E)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, 5, A to C, E, G)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, G, H, J)
DSCR	—	Drive capacity control register (m =1 to 3, 5, A to E, J)	—
PRWCNTR	—	—	Port read wait control register

Note: 1. There are PH0 to PH3 ports on the RX230, and PH1 and PH2 ports on the RX260.

2.14 Multi-Function Pin Controller

Table 2.28 shows a Comparison of Multiplexed Pin Assignments, and Table 2.29 to Table 2.40 show Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, **orange** text designates pins that exist on the RX230/RX231 Group only and **blue** text designates pins that exist on the RX260/RX261 Group only. A circle (○) indicates that a function is assigned, a cross (×) indicates that the pin does not exist or that no function is assigned, and grayed out indicates that the function is not implemented.

Table 2.28 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Interrupt	NMI (input)	P35	○	○	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○	○	○
		PD0	○	×	×	○	×	×
		PH1*3	○	○	○	○	○	○
	IRQ1 (input)	P31	○	○	○	○	○	○
		PD1	○	×	×	○	×	×
		PH2*3	○	○	○	○	○	○
	IRQ2 (input)	P32	○	×	×	○	○	×
		P12	○	×	×	○	×	×
		PD2	○	×	×	○	×	×
		P36				○	○	○
	IRQ3 (input)	P33	○	×	×	○	×	×
		P13	○	×	×	○	×	×
		PD3	○	×	×	○	×	×
	IRQ4 (input)	PB1	○	○	○	○	○	○
		P14	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PD4	○	×	×	○	×	×
		P37				○	○	○
	IRQ5 (input)	PA4	○	○	○	○	○	○
		P15	○	○	○	○	○	○
		PD5	○	×	×	○	×	×
		PE5	○	○	×	○	○	×
	IRQ6 (input)	PA3	○	○	○	○	○	○
		P16	○	○	○	○	○	○
		PD6	○	×	×	○	×	×
		PE6	○	×	×	○	×	×
	IRQ7 (input)	PE2	○	○	○	○	○	○
		P17	○	○	○	○	○	○
		PD7	○	×	×	○	×	×
		PE7	○	×	×	○	×	×
Clock generation circuit	CLKOUT (output)	PE3	○	○	○	○	○	○
		PE4	○	○	○	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	P34	○	×	×			
		PB3	○	○	○			
	MTIOC0B (input/output)	P13	○	×	×			
		P15	○	○	○			
		PA1	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC0C (input/output)	P32	○	×	×			
		PB1	○	○	○			
	MTIOC0D (input/output)	P33	○	×	×			
		PA3	○	○	○			
	MTIOC1A (input/output)	P20	○	×	×			
		PE4	○	○	○			
	MTIOC1B (input/output)	P21	○	×	×			
		PB5	○	○	○			
	MTIOC2A (input/output)	P26	○	○	○			
		PB5	○	○	○			
	MTIOC2B (input/output)	P27	○	○	○			
		PE5	○	○	×			
	MTIOC3A (input/output)	P14	○	○	○			
		P17	○	○	○			
		PC1	○	×	×			
		PC7	○	○	○			
	MTIOC3B (input/output)	P17	○	○	○			
		P22	○	×	×			
		PB7	○	○	×			
		PC5	○	○	○			
	MTIOC3C (input/output)	P16	○	○	○			
		PC0	○	×	×			
		PC6	○	○	○			
		PJ3	○	×	×			
	MTIOC3D (input/output)	P16	○	○	○			
		P23	○	×	×			
		PB6	○	○	×			
		PC4	○	○	○			
	MTIOC4A (input/output)	P24	○	×	×			
		PA0	○	○	×			
		PB3	○	○	○			
		PE2	○	○	○			
	MTIOC4B (input/output)	P30	○	○	○			
		P54	○	○	×			
		PC2	○	○	×			
		PD1	○	×	×			
		PE3	○	○	○			
	MTIOC4C (input/output)	P25	○	×	×			
		PB1	○	○	○			
		PE1	○	○	○			
		PE5	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Multi-function timer unit 2	MTIOC4D (input/output)	P31	○	○	○			
		P55	○	○	×			
		PC3	○	○	×			
		PD2	○	×	×			
		PE4	○	○	○			
	MTIC5U (input)	PA4	○	○	○			
		PD7	○	×	×			
	MTIC5V (input)	PA6	○	○	○			
		PD6	○	×	×			
	MTIC5W (input)	PB0	○	○	○			
		PD5	○	×	×			
	MTCLKA (input)	P14	○	○	○			
		P24	○	×	×			
		PA4	○	○	○			
		PC6	○	○	○			
	MTCLKB (input)	P15	○	○	○			
		P25	○	×	×			
		PA6	○	○	○			
		PC7	○	○	○			
	MTCLKC (input)	P22	○	×	×			
		PA1	○	○	○			
		PC4	○	○	○			
	MTCLKD (input)	P23	○	×	×			
		PA3	○	○	○			
		PC5	○	○	○			
Port output enable 2	POE0# (input)	PC4	○	○	○			
		PD7	○	×	×			
	POE1# (input)	PB5	○	○	○			
		PD6	○	×	×			
	POE2# (input)	P34	○	×	×			
		PA6	○	○	○			
		PD5	○	×	×			
	POE3# (input)	P33	○	×	×			
		PB3	○	○	○			
		PD4	○	×	×			
	POE8# (input)	P17	○	○	○			
		P30	○	○	○			
		PD3	○	×	×			
		PE3	○	○	○			
16-bit timer pulse unit	TIOCA0 (input/output)	PA0	○	○	×			
	TIOCB0 (input/output)	P17	○	○	○			
		PA1	○	○	○			
	TIOCC0 (input/output)	P32	○	×	×			
	TIOCD0 (input/output)	P33	○	×	×			
		PA3	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
16-bit timer pulse unit	TIOCA1 (input/output)	PA4	○	○	○			
	TIOCB1 (input/output)	P16	○	○	○			
		PA5	○	×	×			
	TIOCA2 (input/output)	PA6	○	○	○			
	TIOCB2 (input/output)	P15	○	○	○			
		PA7	○	×	×			
	TIOCA3 (input/output)	P21	○	×	×			
		PB0	○	○	○			
	TIOCB3 (input/output)	P20	○	×	×			
		PB1	○	○	○			
	TIOCC3 (input/output)	P22	○	×	×			
		PB2	○	×	×			
	TIOCD3 (input/output)	P23	○	×	×			
		PB3	○	○	○			
	TIOCA4 (input/output)	P25	○	×	×			
		PB4	○	×	×			
	TIOCB4 (input/output)	P24	○	×	×			
		PB5	○	○	○			
	TIOCA5 (input/output)	P13	○	×	×			
		PB6	○	○	×			
	TIOCB5 (input/output)	P14	○	○	○			
		PB7	○	○	×			
	TCLKA (input)	P14	○	○	○			
		PC2	○	○	×			
	TCLKB (input)	P15	○	○	○			
		PA3	○	○	○			
		PC3	○	○	×			
	TCLKC (input)	P16	○	○	○			
		PB2	○	×	×			
		PC0	○	×	×			
	TCLKD (input)	P17	○	○	○			
		PB3	○	○	○			
		PC1	○	×	×			
8-bit timer	TMO0 (output)	P22	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PH1*3	○	○	○	○	○	○
	TMCI0 (input)	P21	○	×	×	○	×	×
		PB1	○	○	○	○	○	○
		PH3*3	○	○	○	○	○	○
	TMRI0 (input)	P20	○	×	×	○	×	×
		PA4	○	○	○	○	○	○
		PH2*3	○	○	○	○	○	○
	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
8-bit timer	TMCI1 (input)	P12	○	×	×	○	×	×
		P54	○	○	×	○	○	×
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	×	×	○	×	×
		P32	○	×	×	○	○	×
		P55	○	○	×	○	○	×
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	×	×	○	×	×
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○
		P33	○	×	×	○	×	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	×	×			
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	×	×			
	SCK0 (input/output)	P22	○	×	×			
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	×	×			
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○	○	○
		P31	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Serial communications interface	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	×	×	○	×	×
		PA3	○	○	○	○	○	○
		PC2	○	○	×	○	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	×
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
		PC4	○	○	○	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	×	×	○	×	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P33	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PD1				○	×	×
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P32	○	×	×	○	○	×
		PB1	○	○	○	○	○	○
		PD0				○	×	×
	SCK6 (input/output)	P34	○	×	×	○	×	×
		PB3	○	○	○	○	○	○
		PD2				○	×	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	×	×	○	×	×
		PJ3	○	×	×	○	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○			
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○			
	SCK8 (input/output)	PC5	○	○	○			
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○			
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	×			
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	×			
	SCK9 (input/output)	PB5	○	○	×			
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	×	×			
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○ (SMISO12 function not implemented.)	○	○	○ (SMISO12 function not implemented.)

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Serial communications interface	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○ (SMOSI12 function not implemented.)	○	○	○ (SMOSI12 function not implemented.)
	SCK12 (input/output)	PE0	○	○	×	○	○	×
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○ (SS12# function not implemented.)	○	○	○ (SS12# function not implemented.)
	RXD000 (input)/ SMISO000 (input/output)/ SSCL000 (input/output)	P21				○	×	×
	TXD000 (output)/ TXDA000 (output)/ SMOSI000 (input/output)/ SSDA000 (input/output)	P20				○	×	×
	SCK000 (input/output)	P22				○	×	×
	TXDB000 (output)	P22				○	×	×
	CTS000# (input)/ RTS000# (output)/ SS000# (input)	P23				○	×	×
	DE000 (output)	P23				○	×	×
	RXD008 (input)/ SMISO008 (input/output)/ SSCL008 (input/output)	PC6				○	○	○
	TXD008 (output)/ TXDA008 (output)/ SMOSI008 (input/output)/ SSDA008 (input/output)	PC7				○	○	○
	SCK008 (input/output)	PC5				○	○	○
	TXDB008 (output)	PC5				○	○	○
	CTS008# (input)/ RTS008# (output)/ SS008# (input)	PC4				○	○	○
	DE008 (output)	PC4				○	○	○
	RXD009 (input)/ SMISO009 (input/output)/ SSCL009 (input/output)	PB6				○	○	×
	TXD009 (output)/ TXDA009 (output)/ SMOSI009 (input/output)/ SSDA009 (input/output)	PB7				○	○	×
	SCK009 (input/output)	PB5				○	○	×
	TXDB009 (output)	PB5				○	○	×

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Serial communications interface	CTS009# (input)/ RTS009# (output)/ SS009# (input)	PB4				○	×	×
	DE009 (output)	PB4				○	×	×
I²C bus interface	SCL (input/output)	P16	○	○	○			
		P12	○	×	×			
	SDA (input/output)	P17	○	○	○			
		P13	○	×	×			
	SCL0 (input/output)	P12				○	×	×
		P16				○	○	○
	SDA0 (input/output)	P13				○	×	×
		P17				○	○	○
Serial peripheral interface	RSPCKA (input/output)	PA5	○	×	×	○	×	×
		PB0	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
	MOSIA (input/output)	P16	○	○	○	○	○	○
		PA6	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	P17	○	○	○	○	○	○
		PA7	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	×
		PC0	○	×	×	○	×	×
	SSLA2 (output)	PA1	○	○	○	○	○	○
		PC1	○	×	×	○	×	×
	SSLA3 (output)	PA2	○	×	×	○	×	×
		PC2	○	○	×	○	○	×
Realtime clock	RTCOUT (output)	P16	○	○	×	○	○	×
		P32	○	×	×	○	○	×
	RTCIC0 (input)	P30	○	○	×	○	○	×
	RTCIC1 (input)	P31	○	○	×	○	○	×
	RTCIC2 (input)	P32	○	×	×	○	○	×
IrDA interface	IRTXD5 (output)	PA4	○	○	○			
		PC3	○	○	×			
	IRRXD5 (input)	PA2	○	×	×			
		PA3	○	○	○			
	RRXD5 (input)	PC2	○	○	×			
CAN module	CRXD0 (input)	P15	○	○	○			
		P55	○	○	×			
	CTXD0 (output)	P14	○	○	○			
		P54	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Serial sound interface	SSISCK0 (input/output)	P23	○	×	×			
		P31	○	○	○			
		PA1	○	○	○			
	SSIWS0 (input/output)	P21	○	×	×			
		P27	○	○	○			
		PA6	○	○	○			
	SSITXD0 (output)	P17	○	○	○			
		PA4	○	○	○			
	SSIRXD0 (input)	P20	○	×	×			
		P26	○	○	○			
		PA3	○	○	○			
	AUDIO_MCLK (input)	P22	○	×	×			
		P30	○	○	○			
		PE3	○	○	○			
SD host interface	SDHI_CLK (output)	PB1	○	○	×			
	SDHI_CMD (input/output)	PB0	○	○	×			
	SDHI_D0 (input/output)	PC3	○	○	×			
	SDHI_D1 (input/output)	PB6	○	○	×			
		PC4	○	○	×			
	SDHI_D2 (input/output)	PB7	○	○	×			
	SDHI_D3 (input/output)	PC2	○	○	×			
	SDHI_CD (input)	PB5	○	○	×			
	SDHI_WP (input)	PB3	○	○	×			
USB 2.0 host/function module	USB0_DP (input/output)	PH1 *2 *3				○	○	○
	USB0_DM (input/output)	PH2 *2 *3				○	○	○
	USB0_VBUS (input)	P16	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	USB0_EXICEN (output)	P21	○	×	×	○	×	×
		PC6	×	○	○	○	○	○
	USB0_VBUSEN (output)	P16	○	○	○	○	○	○
		P24	○	×	×	○	×	×
		P26	×	○	○	○	○	○
		P32	○	×	×	○	○	×
	USB0_OVRCURA (input)	P14	○	○	○	○	○	○
	USB0_OVRCURB (input)	P16	○	○	○	○	○	○
		P22	○	×	×	○	×	×
	USB0_ID (input)	P20	○	×	×	○	×	×
		PC5	×	○	○	○	○	○
12-bit A/D converter	AN000 (input)	P40	○	○	○	○	○	○
	AN001 (input)	P41	○	○	○	○	○	○
	AN002 (input)	P42	○	○	○	○	○	○
	AN003 (input)	P43	○	○	×	○	○	×
	AN004 (input)	P44	○	○	×	○	○	×
	AN005 (input)	P45	○	×	×	○	○	○
	AN006 (input)	P46	○	○	○	○	○	○
	AN007 (input)	P47	○	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
12-bit A/D converter	AN016 (input)	PE0	○	○	×	○	○	×
	AN017 (input)	PE1	○	○	○	○	○	○
	AN018 (input)	PE2	○	○	○	○	○	○
	AN019 (input)	PE3	○	○	○	○	○	○
	AN020 (input)	PE4	○	○	○	○	○	○
	AN021 (input)	PE5	○	○	×	○	○	×
	AN022 (input)	PE6	○	×	×	○	×	×
	AN023 (input)	PE7	○	×	×	○	×	×
	AN024 (input)	PD0	○	×	×	○	×	×
	AN025 (input)	PD1	○	×	×	○	×	×
	AN026 (input)	PD2	○	×	×	○	×	×
	AN027 (input)	PD3	○	×	×	○	×	×
	AN028 (input)	PD4	○	×	×	○	×	×
	AN029 (input)	PD5	○	×	×	○	×	×
	AN030 (input)	PD6	○	×	×	○	×	×
	AN031 (input)	PD7	○	×	×	○	×	×
	ADTRG0# (input)	P07	○	×	×	○	×	×
		P16	○	○	○	○	○	○
		P25	○	×	×	○	×	×
D/A converter	DA0 (output)	P03	○	○	×	○	○	×
	DA1 (output)	P05	○	○	×	○	○	×
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	○	×	○	○	×
		PC7	○	○	○	○	○	○
		PH0*3	○	○	○	○	○	○
LVD voltage detection input	CMPA2 (input)	PE4	○	○	○	○	○	○
Comparator B	CMPB0 (input)	PE1	○	○	○	○	○	○
	CVREFB0 (input)	PE2	○	○	○	○	○	○
	CMPB1 (input)	PA3	○	○	○	○	○	○
	CVREFB1 (input)	PA4	○	○	○	○	○	○
	CMPB2 (input)	P15	○	○	○			
	CVREFB2 (input)	P14	○	○	○			
	CMPB3 (input)	P26	○	○	○			
	CVREFB3 (input)	P27	○	○	○			
	CMPOB0 (output)	PE5	○	○	×	○	○	×
	CMPOB1 (output)	PB1	○	○	○	○	○	○
	CMPOB2 (output)	P17	○	○	○			
	CMPOB3 (output)	P30	○	○	○			
Capacitive touch sensing unit (CTSU)	TSCAP (output)(—) *4	PC4	○	○	○	○	○	○
	TS0 (output)(input/output) *5	P34	○	×	×			
		P32				○	○	×
	TS1 (output)(input/output) *5	P33	○	×	×			
		P31				○	○	○
	TS2 (output)(input/output) *5	P27	○	○	○			
		P30				○	○	○
		P26	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Capacitive touch sensing unit (CTSU)	TS3 (output)(input/output) *5	P27				○	○	○
	TS4 (output)(input/output) *5	P25	○	×	×			
		P26				○	○	○
	TS5 (output)(input/output) *5	P24	○	×	×			
	TS5 (output)(input/output) *5	P15				○	○	○
	TS6 (output)(input/output) *5	P23	○	×	×			
		P14				○	○	○
	TS7 (output)(input/output) *5	P22	○	×	×			
		PH3*3				○	○	○
	TS8 (output)(input/output) *5	P21	○	×	×			
		PH2*3				○	○	○
	TS9 (output)(input/output) *5	P20	○	×	×			
		PH1*3				○	○	○
	TS10 (input/output)	PH0*3				○	○	○
	TS11 (input/output)	P55				○	○	×
	TS12 (output)(input/output) *5	P15	○	○	○			
		P54				○	○	×
	TS13 (output)(input/output) *5	P14	○	○	○			
		PC7				○	○	○
	TS14 (input/output) *5	PC6				○	○	○
	TS15 (output)(input/output) *5	P55	○	○	×			
		PC5				○	○	○
	TS16 (output)(input/output) *5	P54	○	○	×			
		PC3				○	○	×
	TS17 (output)(input/output) *5	P53	○	×	×			
		PC2				○	○	×
	TS18 (output)(input/output) *5	P52	○	×	×			
		PB7				○	○	×
	TS19 (output)(input/output) *5	P51	○	×	×			
		PB6				○	○	×
	TS20 (output)(input/output) *5	P50	○	×	×			
		PB5				○	○	○
	TS21 (input/output)	PB4				○	×	×
	TS22 (output)(input/output) *5	PC6	○	○	○			
		PB3				○	○	○
	TS23 (output)(input/output) *5	PC5	○	○	○			
		PB2				○	×	×
	TS24 (input/output)	PB1				○	○	○
	TS25 (input/output)	PB0				○	○	○
	TS26 (input/output)	PA6				○	○	○
	TS27 (output)(input/output) *5	PC3	○	○	×			
		PA5				○	×	×
	TS28 (input/output) *5	PA4				○	○	○
	TS29 (input/output) *5	PA3				○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
Capacitive touch sensing unit (CTSU)	TS30 (output)(input/output) *5	PC2	○	○	×			
		PA2				○	×	×
	TS31 (input/output)	PA1				○	○	○
	TS32 (input/output)	PA0				○	○	×
	TS33 (output)(input/output) *5	PC1	○	×	×			
		PE4				○	○	○
	TS34 (input/output)	PE3				○	○	○
	TS35 (output)(input/output) *5	PC0	○	×	×			
		PE2				○	○	○
External bus	CS0# (output)	P24	○	×	×			
	CS0# (output)	PC7	○	×	×			
	CS1# (output)	P25	○	×	×			
		PC6	○	×	×			
	CS2# (output)	P26	○	×	×			
		PC5	○	×	×			
	CS3# (output)	P27	○	×	×			
		PC4	○	×	×			
	A0 to A7 (output)	PA0 to PA7	○	×	×			
	A8 to A15 (output)	PB0 to PB7	○	×	×			
	A16 to A23 (output)	PC0 to PC7	○	×	×			
	D0 to D7 (input/output)	PD0 to PD7	○	×	×			
	D8 to D15 (input/output)	PE0 to PE7	○	×	×			
	BCLK (output)	P53	○	×	×			
	RD# (output)	P52	○	×	×			
	WR# (output)	P50	○	×	×			
	WR0# (output)	P50	○	×	×			
	WR1# (output)	P51	○	×	×			
	BC0# (output)	PA0	○	×	×			
	BC1# (output)	P51	○	×	×			
	WAIT# (input)	P51	○	×	×			
		P55	○	×	×			
		PC5	○	×	×			
	ALE (output)	P54	○	×	×			
General purpose PWM timer	GTIOC0A (input/output)/ GTIOC0A# (input/output)	P17				○	○	○
		P22				○	×	×
		PA0				○	○	×
		PA1				○	○	○
		PB7				○	○	×
		PC5				○	○	○
		PH0*3				○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC0B (input/output)/ GTIOC0B# (input/output)	P16				○	○	○
		P17				○	○	○
		P23				○	×	×
		PA1				○	○	○
		PA6				○	○	○
		PB0				○	○	○
		PB6				○	○	×
		PC4				○	○	○
		PH1*3				○	○	○
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	P24				○	×	×
		P32				○	○	×
		P55				○	○	×
	GTIOC1A (input/output)/ GTIOC1A# (input/output)	PA0				○	○	×
		PB3				○	○	○
		PE2				○	○	○
		PE4				○	○	○
	GTIOC1B (input/output)/ GTIOC1B# (input/output)	P25				○	×	×
		P33				○	×	×
		PA3				○	○	○
		PA4				○	○	○
		PB1				○	○	○
		PE1				○	○	○
		PE5				○	○	×
		PH2*3				○	○	○
	GTIOC2A (input/output)/ GTIOC2A# (input/output)	P21				○	×	×
		P30				○	○	○
		P54				○	○	×
		PB0				○	○	○
		PC2				○	○	×
		PD1				○	×	×
		PE3				○	○	○
	GTIOC2B (input/output)/ GTIOC2B# (input/output)	P20				○	×	×
		P31				○	○	○
		P55				○	○	×
		PA3				○	○	○
		PB1				○	○	○
		PC3				○	○	×
		PD2				○	×	×
		PE4				○	○	○
		PH3*3				○	○	○
	GTIOC3A (input/output)/ GTIOC3A# (input/output)	P22				○	×	×
		P34				○	×	×
		PB2				○	×	×
		PB3				○	○	○
		PC4				○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
General purpose PWM timer	GTIOC3B (input/output)/ GTIOC3B# (input/output)	P13				○	×	×
		P15				○	○	○
		P23				○	×	×
		PA1				○	○	○
		PB3				○	○	○
	GTIOC4A (input/output)/ GTIOC4A# (input/output)	P20				○	×	×
		PA4				○	○	○
		PE4				○	○	○
	GTIOC4B (input/output)/ GTIOC4B# (input/output)	P16				○	○	○
		P21				○	×	×
		PA5				○	×	×
		PB5				○	○	○
		PE3				○	○	○
	GTIOC5A (input/output)/ GTIOC5A# (input/output)	P26				○	○	○
		PA6				○	○	○
		PB5				○	○	○
	GTIOC5B (input/output)/ GTIOC5B# (input/output)	P15				○	○	○
		P27				○	○	○
		PA7				○	×	×
		PE5				○	○	×
	GTIOC6A (input/output)/ GTIOC6A# (input/output)	P14				○	○	○
		P17				○	○	○
		P25				○	×	×
		PB4				○	×	×
		PC1				○	×	×
		PC7				○	○	○
		PJ1				○	×	×
	GTIOC6B (input/output)/ GTIOC6B# (input/output)	P16				○	○	○
		P24				○	×	×
		PB5				○	○	○
		PC0				○	×	×
		PC6				○	○	○
		PJ3				○	×	×
	GTIOC7A (input/output)/ GTIOC7A# (input/output)	P13				○	×	×
		P32				○	○	×
		PB1				○	○	○
		PB6				○	○	×
		PC5				○	○	○
	GTIOC7B (input/output)/ GTIOC7B# (input/output)	P14				○	○	○
		P33				○	×	×
		PA3				○	○	○
		PB7				○	○	×

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
General purpose PWM timer	GTETRGA (input)	P14				○	○	○
		P24				○	×	×
		PA4				○	○	○
		PC2				○	○	×
		PC6				○	○	○
	GTETRGB (input)	P15				○	○	○
		P25				○	×	×
		PA3				○	○	○
		PA6				○	○	○
		PC3				○	○	×
		PC7				○	○	○
	GTETRGC (input)	P16				○	○	○
		P22				○	×	×
		PA1				○	○	○
		PB2				○	×	×
		PC0				○	×	×
		PC4				○	○	○
	GTETRGD (input)	P17				○	○	○
		P23				○	×	×
		PA3				○	○	○
		PB3				○	○	○
		PC1				○	×	×
		PC5				○	○	○
	GTCPPO0 (output)	P14				○	○	○
		P17				○	○	○
		PC1				○	×	×
		PC7				○	○	○
		PJ1				○	×	×
	GTIU (input)	P34				○	×	×
		PB3				○	○	○
		PC4				○	○	○
	GTIV (input)	P13				○	×	×
		P15				○	○	○
		PA1				○	○	○
	GTIW (input)	P32				○	○	×
		PB1				○	○	○
		PC5				○	○	○
	GTOULO (output)	P16				○	○	○
		PA6				○	○	○
		PC4				○	○	○
		PH1*3				○	○	○
	GTOUUP (output)	P17				○	○	○
		PA1				○	○	○
		PC5				○	○	○
		PH0*3				○	○	○

Module/ Function	Pin Function	Port Allocation	RX230/231 (MPC)			RX260/261 (MPC)		
			100-Pin	64-Pin	48-Pin	100-Pin	64-Pin	48-Pin
General purpose PWM timer	GTOVLO (output)	PA3				○	○	○
		PA4				○	○	○
		PB1				○	○	○
		PE1				○	○	○
	GTOVUP (output)	PA0				○	○	×
		PB3				○	○	○
		PE2				○	○	○
		PE4				○	○	○
	GTOWLO (output)	P31				○	○	○
		PA3				○	○	○
		PB1				○	○	○
		PE4				○	○	○
	GTOWUP (output)	P30				○	○	○
		PB0				○	○	○
		PC2				○	○	×
		PE3				○	○	○
Low-power timer	LPTO (output)	P26				○	○	○
		PB3				○	○	○
		PC7				○	○	○
CAN FD module	CTX0 (output)	P14				○	○	○
		P32				○	○	×
		P54				○	○	×
		PD1				○	×	×
	CRX0 (input)	P15				○	○	○
		P33				○	×	×
		P55				○	○	×
		PD2				○	×	×
Remote control signal receiver	PMC0 (input)	P51				○	×	×
	PMC0 (input)	P53				○	×	×
		PB3				○	○	○
		PC3				○	○	×
		PC4				○	○	○
		PC5				○	○	○

Notes: 1. To use this pin function, set the corresponding pin as general input (clear the PORT.PDR.Bm and PORT.PMR.Bm bits to 0).
2. PH1 and PH2 pins for the RX260; USB0_DP and USB0_DM pins for the RX261.
3. The RX231 does not have PH0 to PH3 pins, and the RX261 does not have PH1 and PH2 pins.
4. LPF connection pin for the RX231; secondary power (capacitor) connection pin for measurement for the RX261.
5. Output pin for the RX231; input/output pin for the RX261.

Table 2.29 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX231 (n = 2 to 7)	RX261 (n = 2 to 7)
P12PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 01111b: SCL	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 01111b: SCL0
P13PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00011b: TIOCA5 00101b: TMO3 01111b: SDA	Pin function select bits 00000b: Hi-Z 00011b: GTIV 00101b: TMO3 01111b: SDA0 10100b: GTIOC3B 10101b: GTIOC7A 10110b: GTIOC3B# 10111b: GTIOC7A#
P14PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00011b: TIOCB5 00100b: TCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTXD0 10001b: USB0_OVRCURA 11001b: TS13	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 10000b: CTX0 10001b: USB0_OVRCURA 10100b: GTIOC6A 10101b: GTIOC7B 10110b: GTIOC6A# 10111b: GTIOC7B# 11000b: GTETRGA 11001b: TS6
P15PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00011b: TIOCB2 00100b: TCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRXD0 11001b: TS12	Pin function select bits 00000b: Hi-Z 00011b: GTIV 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 10000b: CRX0 10100b: GTIOC3B 10101b: GTIOC5B 10110b: GTIOC3B# 10111b: GTIOC5B# 11000b: GTETRGB 11001b: TS5

Register	Bit	RX231 (n = 2 to 7)	RX261 (n = 2 to 7)
P16PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00011b: TIOCB1 00100b: TCLKC 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6B# 00010b: GTETRGC 00011b: GTOULO 00101b: TMO2 00111b: RTCOUT 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL0 10001b: USB0_VBUS 10010b: USB0_VBUSEN 10011b: USB0_OVRCURB 10100b: GTIOC0B 10101b: GTIOC4B 10110b: GTIOC0B# 10111b: GTIOC4B# 11000b: GTIOC6B
P17PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00011b: TIOCB0 00100b: TCLKD 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA 10000b: CMPOB2 10111b: SSITXD0	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6A# 00010b: GTETRGD 00011b: GTCPPO0 00100b: GTOUUP 00101b: TMO1 01010b: SCK1 01101b: MISOA 01111b: SDA0 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC6A
P1nPFS	ASEL	Analog function select bit	—

Table 2.30 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
P20PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00011b: TIOCB3 00101b: TMRI0 01010b: TXD0/SMOSI0/SSDA0 10001b: USB0_ID 10111b: SSIRXD0 11001b: TS9	Pin function select bits 00000b: Hi-Z 00001b: TMRI0 01010b: TXD000/TXDA000/ SMOSI000/SSDA000 10001b: USB0_ID 10100b: GTIOC2B 10101b: GTIOC4A 10110b: GTIOC2B# 10111b: GTIOC4A#
P21PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: TIOCA3 00101b: TMCI0 01010b: RXD0/SMISO0/SSCL0 10001b: USB0_EXICEN 10111b: SSIWS0 11001b: TS8	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 01010b: RXD000/SMISO000/ SSCL000 10001b: USB0_EXICEN 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B#
P22PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00011b: TIOCC3 00101b: TMO0 01010b: SCK0 10001b: USB0_OVRCURB 10111b: AUDIO_MCLK 11001b: TS7	Pin function select bits 00000b: Hi-Z 00101b: TMO0 01010b: SCK000 01100b: TXDB000 10001b: USB0_OVRCURB 10100b: GTIOC0A 10101b: GTIOC3A 10110b: GTIOC0A# 10111b: GTIOC3A# 11000b: GTETRGC

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
P23PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKD 00011b: TIOCD3 01011b: CTS0#/RTS0#/SS0# 10111b: SSISCK0 11001b: TS6	Pin function select bits 00000b: Hi-Z 01011b: CTS000#/RTS000#/ SS000# 01100b: DE000 10100b: GTIOC0B 10101b: GTIOC3B 10110b: GTIOC0B# 10111b: GTIOC3B# 11000b: GTETRGD
P24PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00010b: MTCLKA 00011b: TIOCB4 00101b: TMRI1 10001b: USB0_VBUSEN 11001b: TS5	Pin function select bits 00000b: Hi-Z 00101b: TMRI1 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC6B 10110b: GTIOC1A# 10111b: GTIOC6B# 11000b: GTETRGA
P25PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTCLKB 00011b: TIOCA4 01001b: ADTRG0# 11001b: TS4	Pin function select bits 00000b: Hi-Z 01001b: ADTRG0# 10100b: GTIOC1B 10101b: GTIOC6A 10110b: GTIOC1B# 10111b: GTIOC6A# 11000b: GTETRGB

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
P26PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10111b: SSIRXD0 11001b: TS3	Pin function select bits 00000b: Hi-Z 00101b: TMO1 01010b: TXD1/SMOSI1/SSDA1 10001b: USB0_VBUSEN 10100b: GTIOC5A 10110b: GTIOC5A# 11001b: TS4 11011b: LPTO
P27PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2B 00101b: TMCI3 01010b: SCK1 10111b: SSIWS0 11001b: TS2	Pin function select bits 00000b: Hi-Z 00101b: TMCI3 01010b: SCK1 10100b: GTIOC5B 10110b: GTIOC5B# 11001b: TS3
P2nPFS	ASEL	Analog function select bit	—

Table 2.31 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX231 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P30PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMRI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1 10000b: CMPOB3 10111b: AUDIO_MCLK	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 00101b: TMRI3 01010b: RXD1/SMISO1/SSCL1 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS2
P31PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 10111b: SSISCK0	Pin function select bits 00000b: Hi-Z 00011b: GTOWLO 00101b: TMCI2 01011b: CTS1#/RTS1#/SS1# 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS1

Register	Bit	RX231 (n = 0 to 4)	RX261 (n = 0 to 4, 6, 7)
P32PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00011b: TIOCC0 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 10001b: USB0_VBUSEN	Pin function select bits 00000b: Hi-Z 00011b: GTIW 00101b: TMO3 00111b: RTCOUT 01011b: TXD6/SMOSI6/SSDA6 10000b: CTX0 10001b: USB0_VBUSEN 10100b: GTIOC1A 10101b: GTIOC7A 10110b: GTIOC1A# 10111b: GTIOC7A# 11001b: TS0
P33PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00011b: TIOCD0 00101b: TMRI3 00111b: POE3# 01011b: RXD6/SMISO6/SSCL6 11001b: TS1	Pin function select bits 00000b: Hi-Z 00101b: TMRI3 01011b: RXD6/SMISO6/SSCL6 10000b: CRX0 10100b: GTIOC1B 10101b: GTIOC7B 10110b: GTIOC1B# 10111b: GTIOC7B#
P34PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00101b: TMCI3 00111b: POE2# 01011b: SCK6 11001b: TS0	Pin function select bits 00000b: Hi-Z 00001b: GTIU 00101b: TMCI3 01011b: SCK6 10100b: GTIOC3A 10110b: GTIOC3A#
P36PFS	PSEL[4:0]	—	Pin function select bits
P37PFS	PSEL[4:0]	—	Pin function select bits
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/64/48-pin) P31: IRQ1 (100/64/48-pin) P32: IRQ2 (100-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 (100/80/64/48-pin) P31: IRQ1 (100/80/64/48-pin) P32: IRQ2 (100/80/64-pin) P33: IRQ3 (100-pin) P34: IRQ4 (100/80-pin) P36: IRQ2 (80/64/48-pin) P37: IRQ4 (80/64/48-pin)

Table 2.32 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX231 (n = 0 to 5)	RX261 (n = 1, 3 to 5)
P50PFS	PSEL[4:0]	Pin function select bits	—
P51PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 11001b: TS19	Pin function select bits 00000b: Hi-Z 11100b: PMC0
P52PFS	PSEL[4:0]	Pin function select bits	—
P53PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 11001b: TS17	Pin function select bits 00000b: Hi-Z 11100b: PMC0
P54PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00101b: TMCI1 10000b: CTXD0 11001b: TS16	Pin function select bits 00000b: Hi-Z 00101b: TMCI1 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A# 11001b: TS12
P55PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00101b: TMO3 10000b: CRXD0 11001b: TS15	Pin function select bits 00000b: Hi-Z 00101b: TMO3 10000b: CRX0 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11001b: TS11

Table 2.33 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PA0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00011b: TIOCA0 00111b: CACREF 01101b: SSLA1	Pin function select bits 00000b: Hi-Z 00010b: GTOVUP 00111b: CACREF 01101b: SSLA1 10100b: GTIOC0A 10101b: GTIOC1A 10110b: GTIOC0A# 10111b: GTIOC1A# 11001b: TS32

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PA1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: TIOCB0 01010b: SCK5 01101b: SSLA2 10111b: SSISCK0	Pin function select bits 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGC 00011b: GTIV 00100b: GTOUUP 01010b: SCK5 01101b: SSLA2 10100b: GTIOC0A 10101b: GTIOC0B 10110b: GTIOC0A# 10111b: GTIOC0B# 11000b: GTIOC3B 11001b: TS31
PA2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 00011b: TIOCD0 00100b: TCLKB 01010b: RXD5/SMISO5/SSCL5 10111b: SSIRXD0	Pin function select bits 00000b: Hi-Z 00001b: GTIOC7B# 00010b: GTETRGB 00011b: GTETRGD 00100b: GTOVLO 01000b: GTOWLO 01010b: RXD5/SMISO5/SSCL5 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B# 11000b: GTIOC7B 11001b: TS29
PA4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKA 00011b: TIOCA1 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10111b: SSITXD0	Pin function select bits 00000b: Hi-Z 00010b: GTOVLO 00101b: TMRI0 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0 10100b: GTIOC1B 10101b: GTIOC4A 10110b: GTIOC1B# 10111b: GTIOC4A# 11000b: GTETRGA 11001b: TS28

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PA5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00011b: TIOCB1 01101b: RSPCKA	Pin function select bits 00000b: Hi-Z 01101b: RSPCKA 10100b: GTIOC4B 10110b: GTIOC4B# 11001b: TS27
PA6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKB 00011b: TIOCA2 00101b: TMCI3 00111b: POE2# 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10111b: SSIWS0	Pin function select bits 00000b: Hi-Z 00011b: GTOULO 00101b: TMCI3 01011b: CTS5#/RTS5#/SS5# 01101b: MOSIA 10100b: GTIOC0B 10101b: GTIOC5A 10110b: GTIOC0B# 10111b: GTIOC5A# 11000b: GTETRGB 11001b: TS26
PA7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00011b: TIOCB2 01101b: MISOA	Pin function select bits 00000b: Hi-Z 01101b: MISOA 10100b: GTIOC5B 10110b: GTIOC5B#

Table 2.34 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00011b: TIOCA3 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11010b: SDHI_CMD	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 10100b: GTIOC0B 10101b: GTIOC2A 10110b: GTIOC0B# 10111b: GTIOC2A# 11001b: TS25

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PB1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00011b: TIOCB3 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11010b: SDHI_CLK	Pin function select bits 00000b: Hi-Z 00001b: GTIOC7A# 00010b: GTOVLO 00011b: GTIW 00100b: GTOWLO 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 10100b: GTIOC1B 10101b: GTIOC2B 10110b: GTIOC1B# 10111b: GTIOC2B 11000b: GTIOC7A 11001b: TS24
PB2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00011b: TIOCC3 00100b: TCLKC 01011b: CTS6#/RTS6#/SS6#	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC7A 10110b: GTIOC7A# 11000b: GTETRGC 11001b: TS23
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00011b: TIOCD3 00100b: TCLKD 00101b: TMO0 00111b: POE3# 01011b: SCK6 11010b: SDHI_WP	Pin function select bits 00000b: Hi-Z 00001b: GTIOC3B# 00010b: GTETRGD 00011b: GTIU 00100b: GTOVUP 00101b: TMO0 01011b: SCK6 10100b: GTIOC1A 10101b: GTIOC3A 10110b: GTIOC1A# 10111b: GTIOC3A# 11000b: GTIOC3B 11001b: TS22 11011b: LPTO 11100b: PMC0

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PB4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00011b: TIOCA4 01011b: CTS9#/RTS9#/SS9#	Pin function select bits 00000b: Hi-Z 01011b: CTS009#/RTS009#/ SS009# 01100b: DE009 10100b: GTIOC6A 11100b: GTIOC6A# 11001b: TS21
PB5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00011b: TIOCB4 00101b: TMRI1 00111b: POE1# 01010b: SCK9 10001b: USB0_VBUS 11010b: SDHI_CD	Pin function select bits 00000b: Hi-Z 00001b: GTIOC6B# 00101b: TMRI1 01010b: SCK009 01100b: TXDB009 10001b: USB0_VBUS 10100b: GTIOC4B 10101b: GTIOC5A 10110b: GTIOC4B# 10111b: GTIOC5A# 11000b: GTIOC6B 11001b: TS20
PB6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00011b: TIOCA5 01010b: RXD9/SMISO9/SSCL9 11010b: SDHI_D1	Pin function select bits 00000b: Hi-Z 01010b: RXD009/SMISO009/ SSCL009 10100b: GTIOC0B 10101b: GTIOC7A 10110b: GTIOC0B# 10111b: GTIOC7A# 11001b: TS19

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PB7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00011b: TIOCB5 01010b: TXD9/SMOSI9/SSDA9 11010b: SDHI_D2	Pin function select bits 00000b: Hi-Z 01010b: TXD009/TXDA009/ SMOSI009/SSDA009 10100b: GTIOC0A 10101b: GTIOC7B 10110b: GTIOC0A# 10111b: GTIOC7B# 11100b: TS18

Table 2.35 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PC0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00011b: TCLKC 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 11001b: TS35	Pin function select bits 00000b: Hi-Z 01011b: CTS5#/RTS5#/SS5# 01101b: SSLA1 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGC
PC1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00011b: TCLKD 01010b: SCK5 01101b: SSLA2 11001b: TS33	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 01010b: SCK5 01101b: SSLA2 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGD
PC2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00011b: TCLKA 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30 11010b: SDHI_D3	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 10100b: GTIOC2A 10110b: GTIOC2A# 11000b: GTETRGA 11001b: TS17

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PC3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00011b: TCLKB 01010b: TXD5/SMOSI5/SSDA5 11001b: TS27 11010b: SDHI_D0	Pin function select bits 00000b: Hi-Z 01010b: TXD5/SMOSI5/SSDA5 10100b: GTIOC2B 10110b: GTIOC2B# 11000b: GTETRGB 11001b: TS16 11100b: PMC0
PC4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00101b: TMCI1 00111b: POE0# 01010b: SCK5 01011b: CTS8#/RTS8#/SS8# 01101b: SSLA0 11001b: TSCAP 11010b: SDHI_D1	Pin function select bits 00000b: Hi-Z 00001b: GTIU 00100b: GTOULO 00101b: TMCI1 01010b: SCK5 01011b: CTS008#/RTS008#/ SS008# 01100b: DE008 01101b: SSLA0 10100b: GTIOC0B 10101b: GTIOC3A 10110b: GTIOC0B# 10111b: GTIOC3A# 11000b: GTETRGC 11001b: TSCAP 11100b: PMC0
PC5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK8 01101b: RSPCKA 11001b: TS23	Pin function select bits 00000b: Hi-Z 00010b: GTOUUP 00011b: GTIW 00101b: TMRI2 01010b: SCK008 01100b: TXDB008 01101b: RSPCKA 10001b: USB0_ID 10100b: GTIOC0A 10101b: GTIOC7A 10110b: GTIOC0A# 10111b: GTIOC7A# 11000b: GTETRGD 11001b: TS15 11100b: PMC0

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PC6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01010b: RXD8/SMISO8/SSCL8 01101b: MOSIA 11001b: TS22	Pin function select bits 00000b: Hi-Z 00101b: TMCI2 01010b: RXD008/SMISO008/ SSCL008 01101b: MOSIA 10001b: USB0_EXICEN 10100b: GTIOC6B 10110b: GTIOC6B# 11000b: GTETRGA 11001b: TS14
PC7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01010b: TXD8/SMOSI8/SSDA8 01101b: MISOA	Pin function select bits 00000b: Hi-Z 00001b: GTCPPO0 00101b: TMO2 00111b: CACREF 01010b: TXD008/TXDA008/ SMOSI008/SSDA008 01101b: MISOA 10100b: GTIOC6A 10110b: GTIOC6A# 11000b: GTETRGB 11001b: TS13 11011b: LPTO

Table 2.36 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PD0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z	Pin function select bits 00000b: Hi-Z 01011b: TXD6/SMOSI6/SSDA6
PD1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B	Pin function select bits 00000b: Hi-Z 01011b: RXD6/SMISO6/SSCL6 10000b: CTX0 10100b: GTIOC2A 10110b: GTIOC2A#
PD2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D	Pin function select bits 00000b: Hi-Z 01011b: SCK6 10000b: CRX0 10100b: GTIOC2B 10110b: GTIOC2B#

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PD3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE8#	Pin function select bits 00000b: Hi-Z
PD4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE3#	Pin function select bits 00000b: Hi-Z
PD5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00111b: POE2#	Pin function select bits 00000b: Hi-Z
PD6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: POE1#	Pin function select bits 00000b: Hi-Z
PD7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 00111b: POE0#	Pin function select bits 00000b: Hi-Z

Table 2.37 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PE1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 01100b: TXD12/TXDX12/SIOX12 SMOSI12/SSDA12	Pin function select bits 00000b: Hi-Z 00010b: GTOVLO 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12 10100b: GTIOC1B 10110b: GTIOC1B#
PE2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 01100b: RXD12/RXDX12/ SMISO12/SSCL12	Pin function select bits 00000b: Hi-Z 00010b: GTOVUP 01100b: RXD12/RXDX12/ SMISO12/SSCL12 10100b: GTIOC1A 10110b: GTIOC1A# 11001b: TS35

Register	Bit	RX231 (n = 0 to 7)	RX261 (n = 0 to 7)
PE3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4B 00111b: POE8# 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 10111b: AUDIO_MCLK	Pin function select bits 00000b: Hi-Z 00011b: GTOWUP 01001b: CLKOUT 01100b: CTS12#/RTS12#/SS12# 10100b: GTIOC2A 10101b: GTIOC4B 10110b: GTIOC2A# 10111b: GTIOC4B# 11001b: TS34
PE4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 01001b: CLKOUT	Pin function select bits 00000b: Hi-Z 00001b: GTIOC4A# 00010b: GTOVUP 00011b: GTOWLO 01001b: CLKOUT 10100b: GTIOC1A 10101b: GTIOC2B 10110b: GTIOC1A# 10111b: GTIOC2B# 11000b: GTIOC4A 11001b: TS33
PE5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4C 00010b: MTIOC2B 10000b: CMPOB0	Pin function select bits 00000b: Hi-Z 10000b: CMPOB0 10100b: GTIOC1B 10101b: GTIOC5B 10110b: GTIOC1B# 10111b: GTIOC5B#

Table 2.38 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX230/RX231 (n = 0 to 3)*1	RX260/RX261 (n = 0 to 3)*2
PH0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: CACREF	Pin function select bits 00000b: Hi-Z 00010b: GTOUUP 00111b: CACREF 10100b: GTIOC0A 10110b: GTIOC0A# 11001b: TS10

Register	Bit	RX230/RX231 (n = 0 to 3)*1	RX260/RX261 (n = 0 to 3)*2
PH1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMO0	Pin function select bits 00000b: Hi-Z 00011b: GTOULO 00101b: TMO0 10100b: GTIOC0B 10110b: GTIOC0B# 11001b: TS9
PH2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMRI0	Pin function select bits 00000b: Hi-Z 00101b: TMRI0 10100b: GTIOC1B 10110b: GTIOC1B# 11001b: TS8
PH3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00101b: TMCI0	Pin function select bits 00000b: Hi-Z 00101b: TMCI0 10100b: GTIOC2B 10110b: GTIOC2B# 11001b: TS7

Notes: 1. Only the RX230 has the PH0 to PH3 registers. The RX231 does not have the PHnPFS register.
2. Only the RX260 has the PH1 and PH2 registers.

Table 2.39 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX231 (n = 3)	RX261 (n = 1, 3, 6, 7)
PJ1PFS	PSEL[4:0]	—	PJ1 pin function select bits
PJ3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 01011b: CTS6#/RTS6#/SS6#	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 10100b: GTIOC6B 10110b: GTIOC6B#
PJ6PFS	PSEL[4:0]	—	PJ6 pin function select bits
PJ7PFS	PSEL[4:0]	—	PJ7 pin function select bits
PJnPFS	ASEL	—	Analog function select bit

Table 2.40 Comparisons of Multi-Function Pin Controller Registers

Register	Bit Name	RX231	RX261
PFCSE	—	CS output enable register	—
PFAOE0	—	Address output enable register 0	—
PFAOE1	—	Address output enable register 1	—
PFBCR0	—	External bus control register 0	—
PFBCR1	—	External bus control register 1	—

2.15 8-Bit Timer

Table 2.41 shows a Comparative Overview of 8-Bit Timers.

Table 2.41 Comparative Overview of 8-Bit Timers

Item	RX231 (TMR)	RX261 (TMRa)
Count clock	• Frequency dividing clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selected by compare match A or B, or an external counter reset signal.	Selected by compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0, TMR2)	Compare match A, compare match B, and overflow (TMR0, TMR2)
Event link function (input)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)	One of the following three operations proceeds in response to an event reception: (1) Counting start operation (TMR0, TMR2) (2) Event counting operation (TMR0, TMR2) (3) Counting restart operation (TMR0, TMR2)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of SCI basic clock	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Ability to transition each unit to the module stop state	Ability to transition each unit to the module stop state

2.16 Realtime Cock

Table 2.42 shows a Comparative Overview of Realtime Clocks and Table 2.43 shows a Comparison of Realtime Clock Registers.

Table 2.42 Comparative Overview of Realtime Clocks

Item	RX231 (RTCe)	RX261 (RTCBa)
Count mode	Calendar count mode/ binary count mode	Calendar count mode/ binary count mode
Count source	Sub-clock (XCIN)	Sub-clock (crystal resonator or external clock), or main clock (EXTAL)
Clock and calendar functions	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (less than 30 seconds is rounded down to 00 seconds, and 30 seconds or more is rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output	• Calendar count mode — Year, month, date, day-of-week, hour, minute, second are counted, BCD display — 12 hours/24 hours mode switching function — 30 seconds adjustment function (less than 30 seconds is rounded down to 00 seconds, and 30 seconds or more is rounded up to one minute) — Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Common to both modes — Start/stop function — The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz). — Clock error correction function — Clock (1 Hz/64 Hz) output

Item	RX231 (RTCe)	RX261 (RTCBa)
Interrupts	• Alarm interrupt (ALM) As an alarm interrupt condition, the following comparison targets can be selected: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected. — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt.	• Alarm interrupt (ALM) As an alarm interrupt condition, the following comparison targets can be selected: — Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected. — Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt is generated at either of the following timings: — When a carry from the 64-Hz counter to the second counter is generated. — When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode can be performed by an alarm interrupt or periodic interrupt.
Time capture function	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, the month, date, hour, minute, and second are captured or the 32-bit binary counter value is captured.	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, the month, date, hour, minute, and second are captured or the 32-bit binary counter value is captured.
Event link function	Periodic event output	Periodic event output

Table 2.43 Comparison of Realtime Clock Registers

Register	Bit	RX231 (RTCe)	RX261 (RTCBa)
RCR3	—	RTC control register 3	—
RTCCRn	TCEN *1	Time capture event input pin enable bit	Time capture event input pin enable bit
		The initial values of the registers are different.	

Note: 1. This bit is not initialized by reset sources other than a power-on reset.

2.17 Low-Power Timer

Table 2.44 shows a Comparative Overview of Low-Power Timers, and Table 2.45 shows a Comparison of Low-Power Timer Registers.

Table 2.44 Comparative Overview of Low-Power Timers

Item	RX231 (LPT)	RX261 (LPTa)
Clock source	Sub-clock oscillator or IWDT-dedicated on-chip oscillator	Sub-clock, LOCO clock (divided by 4), or IWDT-dedicated clock
Clock division ratio	Divided by 2, 4, 8, 16, or 32	No division, or divided by 2, 4, 8, 16, or 32
Count operation	• Count up using the 16-bit up-counter • Count operation can be continued even in software standby mode	• Count up using the 16-bit up-counter • Count operation can be continued even in software standby mode
Compare match	• Compare match 0 (A compare match signal is generated only in software standby mode)	• Compare match 0 (A compare match signal is generated only in software standby mode) • Compare match 1
PWM waveform generation	—	A PWM waveform can be output on the LPTO pin.
Interrupt	—	Compare match 1
Event link function (output)	• Compare match 0 An event signal is output (a compare match signal is generated only in software standby mode).	• Compare match 0 (A compare match signal is generated only in software standby mode) • Compare match 1

Table 2.45 Comparison of Low-Power Timer Registers

Register	Bit	RX231 (LPT)	RX261 (LPTa)
LPTCR1	LPCNTPSSEL [2:0]	Low-power timer clock division ratio select bits b2 b0 0 0 1: Source clock divided by 2 0 1 0: Source clock divided by 4 0 1 1: Source clock divided by 8 1 0 0: Source clock divided by 16 1 0 1: Source clock divided by 32 Settings other than the above are prohibited.	Clock division ratio select bits b2 b0 0 0 0: No division 0 0 1: Divided by 2 0 1 0: Divided by 4 0 1 1: Divided by 8 1 0 0: Divided by 16 1 0 1: Divided by 32 Settings other than the above are prohibited.

Register	Bit	RX231 (LPT)	RX261 (LPTa)
LPTCR1	LPCNTCKSEL (RX231) LPCNTCKSEL, LPCNTCKSEL2 (RX261)	Low-power timer clock source select bit 0: Sub-clock oscillator is selected. 1: IWDT-dedicated on-chip oscillator is selected.	Low-power timer clock source select bit Low-power timer clock source select bit 2 LPCNTCKSEL LPCNTCKSEL2 0 0: Sub-clock 0 1: LOCO clock divided by 4 0 0: IWDT-dedicated clock (IWDTCLK) 1 1: LOCO clock divided by 4
	LPCMRE1	—	Compare match 1 enable bit
LPTCR2	OPOL	—	Output polarity select bit
	OLVL	—	Output level select bit
	PWME	—	PWM mode enable bit
LPCMR1	—	—	Low-power timer compare register 1

2.18 USB 2.0 Host/Function Module and USB 2.0 FS Host/Function Module

Table 2.46 shows a Comparative Overview of USB 2.0 Host/Function Module and USB 2.0 FS Host/Function Module, and Table 2.47 shows a Comparison of USB 2.0 Host/Function Module Registers and USB 2.0 FS Host/Function Module Registers.

Table 2.46 Comparative Overview of USB 2.0 Host/Function Module and USB 2.0 FS Host/Function Module

Item	RX231 (USBd)	RX261 (USBe)
Features	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host controller, function controller, and On-The-Go (OTG) are supported (one channel). • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected. • BC1.2 (Battery Charging Specification Revision 1.2) is supported.	• USB Device Controller (UDC) and transceiver for USB 2.0 are incorporated. • Host controller, function controller, and On-The-Go (OTG) are supported (one channel). • The host controller and the function controller can be switched by software. • Self-power mode or bus power mode can be selected.
	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers	When the host controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Connects and communicates with multiple peripheral devices via a single hub
	When the function controller is selected: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) are supported. • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function	When the function controller is selected: • Full-speed transfer (12 Mbps) is supported. • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF interpolation function
Communication data transfer type	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer

Item	RX231 (USBd)	RX261 (USBe)
Pipe configuration	• Buffer memory for USB communication is provided. • Up to 10 pipes selectable (including the default control pipe) • PIPE1 to PIPE9 can be assigned any endpoint number.	• Buffer memory for USB communication is provided. • Up to 10 pipes selectable (including the default control pipe) • PIPE1 to PIPE9 can be assigned any endpoint number.
	Transfer conditions that can be set for each pipe: • PIPE0: — Control transfer, 64-byte single buffer • PIPE1 and PIPE2: — 64-byte double buffer can be specified for bulk transfer. — 256-byte double buffer can be specified for isochronous transfer. • PIPE3 to PIPE5: — Bulk transfer; 64-byte double buffer can be specified • PIPE6 to PIPE9: — Interrupt transfer; 64-byte single buffer	Transfer conditions that can be set for each pipe: • PIPE0: — Control transfer, 64-byte single buffer • PIPE1 and PIPE2: — 64-byte double buffer can be specified for bulk transfer. — 256-byte double buffer can be specified for isochronous transfer. • PIPE3 to PIPE5: — Bulk transfer; 64-byte double buffer can be specified • PIPE6 to PIPE9: — Interrupt transfer; 64-byte single buffer
Other functions	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/D–	• Reception ending function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0, 1) port has been read (DCLRM) • NAK setting function for response PID generated by end of transfer (SHTNAK) • On-chip pull-up and pull-down resistors of D+/D–
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.47 Comparison of USB 2.0 Host/Function Module Registers and USB 2.0 FS Host/Function Module Registers

Register	Bit	RX231 (USBd)	RX261 (USBe)
SYSCFG	DMRPU	D- line resistor control bit	—
	CNEN	Single-ended receiver enable bit	—
DVSTCTR0	RHST[2:0]	USB bus reset status flag When the host controller function is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection When the function controller function is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection	USB bus reset status flag When the host controller function is selected b2 b0 0 0 0: Communication speed not determined (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection When the function controller function is selected b2 b0 0 0 0: Communication speed not determined 0 0 1: USB bus reset in progress 0 1 0: USB bus reset in progress or full-speed connection
INTENB1	PDDETINTE0	PDDETINT0 detection interrupt enable bit	—
INTSTS1	PDDETINT0	PDDET0 detection interrupt status flag	—
USBMC	—	USB module control register	—
USBBCCTRL0	—	BC control register 0	—

2.19 Serial Communications Interface

Table 2.48 shows a Comparative Overview of Serial Communications Interfaces, Table 2.49 shows a Comparison of Serial Communications Interface Channel Specifications, and Table 2.50 shows a Comparison of Serial Communications Interface Registers.

Table 2.48 Comparative Overview of Serial Communications Interfaces

Item		RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Number of channels		• SCIg: 6 channels • SCIh: 1 channel	• SCIk: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, and receive error • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Individual channels can be transitioned to the module stop state.	Individual channels can be transitioned to the module stop state.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.

Item		RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	Data match detection	—	Compares receive data and comparison data, and generates interrupt when they match
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include control field 0 • Function for measuring bit rates

Item		RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Extended serial mode (supported by SCI12 only)	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is turned off.	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.49 Comparison of Serial Communications Interface Channel Specifications

Item	RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
Asynchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI6, SCI12
Data match detection	—	SCI1, SCI5, SCI6
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKB: SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	PCLKB: SCI1, SCI5, SCI6, SCI12

Table 2.50 Comparison of Serial Communications Interface Registers

Register	Bit	RX231 (SCIg, SCIh)	RX261 (SCIk, SCIh)
SCR	MPIE	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags ORER and FER in the SSR register to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.	Multi-processor interrupt enable bit (Valid in asynchronous mode when the SMR.MP bit is set to 1.) 0: Normal reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in the SSR register to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and normal reception resumes.
SEMR	ITE	—	Immediate transmission enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
SPMR	MSS	Master/slave select bit 0: TXDn pin: Transmit, RXDn pin: Receive (master mode) 1: TXDn pin: Receive, RXDn pin: Transmit (slave mode)	Master/slave select bit 0: SMOSIn pin: Transmit, SMISOn pin: Receive (master mode) 1: SMOSIn pin: Receive, SMISOn pin: Transmit (slave mode)
CDR	—	—	Comparison data register
DCCR	—	—	Data comparison control register
SPTR	—	—	Serial port register
TMGR	—	—	Transmit/receive timing select register

2.20 CAN Module and CAN FD Module

Table 2.51 shows a Comparative Overview of CAN Module and CAN FD Module, and Table 2.52 shows a Comparison Between the CAN Module Registers and the CAN FD Module Registers.

Table 2.51 Comparative Overview of CAN Module and CAN FD Module

Item	RX231 (RSCAN)	RX261 (CANFD)
Protocol	Conforming to the ISO 11898-1 standard	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX231) Data transfer rate (RX261)	1 Mbps, max.	Arbitration phase: 1 Mbps, max. Data phase: TBD, max.*1
Operating frequency	PCLKB: 32 MHz (max.) CANMCLK: 20 MHz (max.)	Register block: 32 MHz, max. (PCLKB) Message buffer RAM: 64 MHz, max. (PCLKA)
Operating clock for data link layer (DLL clock)	—	32 MHz, max. (either CANFDMCLK or CANFDCLK can be selected)
Buffer (RX231) Message buffer (RX261)	A total of 20 buffers • Channel-specific buffer: 4 buffers (4 buffers × 1 channel) Transmit buffer: 4 buffers per channel • Channel-shared buffer: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per channel (up to 16 buffers allocatable to each)	• Transmit message buffer: 4 buffers • Transmit queue: 1 queue Automatic transfer of messages to the transmit queue is supported. • Receive message buffer: 32 buffers
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD *1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Interrupts can be enabled or disabled for each FIFO buffer. • Mirror function (to receive messages transmitted from the own CAN node)	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes*1

Item	RX231 (RSCAN)	RX261 (CANFD)
Receive filter function (RX231) Acceptance filter (RX261)	• Receive messages can be selected according to 16 receive rules. • The number of receive rules (0 to 16) can be set for each channel. • Acceptance filter processing: ID and mask can be set for each receive rule. • DLC filter processing: A DLC check value can be set for each receive rule.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Receive message transfer function	• Routing function A function that transfers received messages to arbitrary destination buffers (maximum number of destination buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Label information can be stored together when storing a message in a receive buffer and FIFO buffer.	—
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or transmit buffer number priority transmission mode can be selected. • Transmission can be aborted. (Completion of abort can be confirmed with a flag.) • Interrupt can be enabled or disabled individually for each transmit buffer and for each transmit/receive FIFO buffer.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Channel transmission interrupts can be enabled or disabled.
FIFO	• Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) • Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)	The FIFO size is programmable. • Receive FIFO buffer: 2 FIFO buffers • Common FIFO buffer: 1 FIFO buffer (Whether to use the FIFO buffer as a receive FIFO buffer or transmit FIFO buffer can be selected.)
Interval transmission function (RX231) Automatic transmission interval adjustment (RX261)	The message transmission interval time can be set. (transmit mode of transmit/receive FIFO buffers)	Available when the common FIFO queue is configured as a transmit FIFO queue The interval between messages sent from the FIFO can be adjusted.
Transmit history function	Stores the history information of transmitted messages.	—

Item	RX231 (RSCAN)	RX261 (CANFD)
Method of recovery from the bus-off state	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to channel halt mode when the bus-off state starts. • The mode automatically changes to channel halt mode when the bus-off state ends. • A program causes a transition to channel halt mode. • A program causes a transition to error active state (forcible return from the bus-off state).	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when the bus-off state starts. • Automatically enters CH_HALT mode when the bus-off state ends. • Enters CH_HALT mode by software (during the period of recovery from the bus-off state). • A program causes a transition to error active state.
Timer	Time stamp function (recording of 16-bit timer value for the message reception time)	Transmission and reception timestamp function
Interrupt function	• Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) — Channel transmission interrupt Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Channel error interrupt — Transmit/receive FIFO receive interrupt	• Global — Receive FIFO interrupt — Global error interrupt — Receive message buffer interrupt • Channel — Channel transmission interrupt Transmit success interrupt Transmit abort interrupt Transmit queue interrupt Common FIFO transmission interrupt Transmit history interrupt — Channel error interrupt — Common FIFO receive interrupt
Software support	—	Label information is automatically added to received messages.
Test modes	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)	• Basic test mode • Listen-only mode • Self-test mode 0 (external loopback mode) • Self-test mode 1 (internal loopback mode)
Low power consumption function (RX231) Power down function (RX261)	Ability to specify module stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to module stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

Table 2.52 Comparison Between the CAN Module Registers and the CAN FD Module Registers

Register	Bit	RX231 (RSCAN)	RX261 (CANFD)
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFOn configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFOn status register (n = 0, 1)
RFPCRn	—	—	Receive FIFOn pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)

Register	Bit	RX231 (RSCAN)	RX261 (CANFD)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	Transmit message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register
CFGL	—	Bit configuration register L	—
CFGH	—	Bit configuration register H	—
CTRL	—	Control register L	—
CTRH	—	Control register H	—
STSL	—	Status register L	—
STSH	—	Status register H	—
ERFLL	—	Error flag register L	—
ERFLH	—	Error flag register H	—
GCFGL	—	Global configuration register L	—

Register	Bit	RX231 (RSCAN)	RX261 (CANFD)
GCFGH	—	Global configuration register H	—
GCTRL	—	Global control register L	—
GCTRH	—	Global control register H	—
GSTS	—	Global status register	—
GERFLL	—	Global error flag register	—
GTINTSTS	—	Global transmission interrupt status register	—
GTSC	—	Timestamp register	—
GAFLCFG	—	Receive rule number configuration register	—
GAFLIDLj	—	Receive rule entry register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive rule entry register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive rule entry register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive rule entry register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive rule entry register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive rule entry register jCH (j = 0 to 15)	—
RMNB	—	Receive buffer number configuration register	—
RMND0	—	Receive buffer receive complete flag register	—
RMIDLn	—	Receive buffer register nAL (n = 0 to 15)	—
RMIDHn	—	Receive buffer register nAH (n = 0 to 15)	—
RMTSn	—	Receive buffer register nBL (n = 0 to 15)	—
RMPTRn	—	Receive buffer register nBH (n = 0 to 15)	—
RMDF0n	—	Receive buffer register nCL (n = 0 to 15)	—
RMDF1n	—	Receive buffer register nCH (n = 0 to 15)	—
RMDF2n	—	Receive buffer register nDL (n = 0 to 15)	—
RMDF3n	—	Receive buffer register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO control register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO status register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO pointer control register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO access register mAL (m = 0, 1)	—
RFIDHm	—	Receive FIFO access register mAH (m = 0, 1)	—

Register	Bit	RX231 (RSCAN)	RX261 (CANFD)
RFTSm	—	Receive FIFO access register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO access register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO access register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO access register mCH (m = 0, 1)	—
RFDF2m	—	Receive FIFO access register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO access register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/receive FIFO control register 0L	—
CFCCH0	—	Transmit/receive FIFO control register 0H	—
CFSTS0	—	Transmit/receive FIFO status register 0	—
CFPCTR0	—	Transmit/receive FIFO pointer control register 0	—
CFIDL0	—	Transmit/receive FIFO access register 0AL	—
CFIDH0	—	Transmit/receive FIFO access register 0AH	—
CFTS0	—	Transmit/receive FIFO access register 0BL	—
CFPTR0	—	Transmit/receive FIFO access register 0BH	—
CFDF00	—	Transmit/receive FIFO access register 0CL	—
CFDF10	—	Transmit/receive FIFO access register 0CH	—
CFDF20	—	Transmit/receive FIFO access register 0DL	—
CFDF30	—	Transmit/receive FIFO access register 0DH	—
RFMSTS	—	Receive FIFO message lost status register	—
CFMSTS	—	Transmit/receive FIFO message lost status register	—
RFISTS	—	Receive FIFO interrupt status register	—
CFISTS	—	Transmit/receive FIFO receive interrupt status register	—
TMCp	—	Transmit buffer control register p (p = 0 to 3)	—
TMSTSp	—	Transmit buffer status register p (p = 0 to 3)	—
TMTRSTS	—	Transmit buffer transmit request status register	—
TMTCSTS	—	Transmit buffer transmit complete status register	—
TMTASTS	—	Transmit buffer transmit abort status register	—

Register	Bit	RX231 (RSCAN)	RX261 (CANFD)
TMIEC	—	Transmit buffer interrupt enable register	—
TMIDLp	—	Transmit buffer register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit buffer register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit buffer register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit buffer register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit buffer register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit buffer register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit buffer register pDH (p = 0 to 3)	—
THLCC0	—	Transmit history buffer control register	—
THLSTS0	—	Transmit history buffer status register	—
THLACC0	—	Transmit history buffer access register	—
THLPCTR0	—	Transmit history buffer pointer control register	—
GRWCR	—	Global RAM window control register	—
GTSTCFG	—	Global test configuration register	—
GTSTCTRL	—	Global test control register	—
GLOCKK	—	Global test protection unlock register	—
RPGACCr	—	RAM test register r (r = 0 to 127)	—

2.21 Serial Peripheral Interface

Table 2.53 shows a Comparative Overview of Serial Peripheral Interfaces, and Table 2.54 shows a Comparison of Serial Peripheral Interface Registers.

Table 2.53 Comparative Overview of Serial Peripheral Interfaces

Item	RX231 (RSPIa)	RX261 (RSPIc)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication mode: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 8). — Width at high level: 4 cycles of PCLK — Width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from division by 2 to division by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK

Item	RX231 (RSPIa)	RX261 (RSPIc)
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function

Item	RX231 (RSPIa)	RX261 (RSPIc)
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — RSPI error interrupt (mode fault, overrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt
Event link function (output)	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full signal — Transmit buffer empty signal — Mode fault, overrun, or parity error signal — RSPI idle signal — Transmission-completed signal	• The following events can be output to the event link controller. (RSPI0) — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, or parity error) — Idle events — Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	• Ability to specify module stop state	• Ability to specify module stop state

Table 2.54 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX231 (RSPIa)	RX261 (RSPId)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurs 1: A mode fault error occurs	Mode fault error flag 0: Neither a mode fault error nor an underrun error occurs. 1: A mode fault error or an underrun error occurs.
	UDRF	—	Underrun error flag
SPDR	—	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1) • Word access (SPDCR.SPLW = 0)	RSPI data register Supported access sizes • Longword access (SPDCR.SPLW = 1, SPBYTE = 0) • Word access (SPDCR.SPLW = 0, SPBYTE = 0) • Byte access (SPDCR.SPBYT = 1)
SPDCR	SPBYT	—	RSPI byte access specification bit
SPDCR2	—	—	RSPI data control register 2

2.22 Capacitive Touch Sensing Unit

Table 2.55 shows a Comparative Overview of Capacitive Touch Sensing Units, and Table 2.56 shows a Comparison of Capacitive Touch Sensing Unit Registers.

Table 2.55 Comparative Overview of Capacitive Touch Sensing Units

Item		RX231 (CTSU)	RX261 (CTSU2SLa)
Operating clock		PCLK, PCLK/2, or PCLK/4	Selectable among PCLKB (1 MHz and above), PCLKB/2, PCLKB/4, and PCLKB/8
I/O pins	Electrostatic capacitance measurement pins	TS0 to TS9, TS12, TS13, TS15 to TS20, TS22, TS23, TS27, TS30, TS33, TS35 (24 channels)	Pins TS0 to TS35 (36 channels)
	TSCAP pin	LPF (low-pass filter) connection pin	Measurement power supply capacitor connection pin (0.01 µF)
Measurement modes	Self-capacitance method	Measured from charging/discharging current against electrode capacitance	Measured from charging/discharging current against electrode capacitance
	Mutual capacitance method	Measured from charging/discharging current against the capacitance between transmission electrode and reception electrode	Measured from charging/discharging current against the capacitance between transmission electrode and reception electrode
	Current measurement mode	—	Direct reading of current flowing to pin
Scan modes	Single-scan mode	Electrostatic capacitance is measured on a user-defined channel.	Electrostatic capacitance is measured on one channel.
	Multi-scan mode	Electrostatic capacitance is measured on multiple user-defined channels successively.	Electrostatic capacitance is measured on multiple channels successively.
Noise prevention		Synchronous noise prevention, high-range noise prevention	• Sensor drive pulse spectrum diffusion function • Sensor drive pulse random phase shift function • Noise hopping function using multiple-frequency sensor drive pulses
Individual pin adjustments		• Offset current adjustment function • Specification of sensor drive pulse frequency • Specification of measurement duration	• Offset current adjustment function • Specification of sensor drive pulse frequency • Specification of measurement duration
Measurement start conditions		• Software trigger • External trigger (event input from event link controller (ELC))	• Software trigger • External trigger (event input from event link controller (ELC))

Item	RX231 (CTSU)	RX261 (CTSU2SLa)
Automatic processing functions	—	• Automatic correction function • Automatic determination function
Low-power functions	—	Ability to perform measurement in snooze mode • Measurement start by external trigger input via ELC • Ability to end snooze mode by contactless determination using automatic determination function • Ability to cancel snooze mode by measurement end interrupt
Interrupt sources	• Channel-specific setting register write request interrupt (CTSUWR) • Measurement data transfer request interrupt (CTSURD) • Measurement end interrupt (CTSUFN)	• Register setting request interrupt (CTSUWR) • Measurement result read request interrupt (CTSURD) • Measurement end interrupt (CTSUFN)
Event link function	Measurement start trigger input	Measurement start trigger input
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.56 Comparison of Capacitive Touch Sensing Unit Registers

Register	Bit	RX231 (CTSU)	RX261 (CTSU2SLa)
CTSUCRA	—	—	CTSU control register A
CTSUCRB	—	—	CTSU control register B
CTSUMCH	—	—	CTSU measurement channel register
CTSUCHACA	—	—	CTSU channel enable control register A
CTSUCHACB	—	—	CTSU channel enable control register B
CTSUCHTRCA	—	—	CTSU channel transmit/receive control register A
CTSUCHTRCB	—	—	CTSU channel transmit/receive control register B
CTSUSR	—	—	CTSU status register
CTSUSO	—	—	CTSU sensor offset register
CTSUSCNT	—	—	CTSU sensor counter
CTSUCALIB	—	—	CTSU calibration register
CTSUSUCLKA	—	—	CTSU sensor unit clock control register A
CTSUSUCLKB	—	—	CTSU sensor unit clock control register B
CTSUTRIMA	—	—	CTSU trimming register A
CTSUTRIMB	—	—	CTSU trimming register B
CTSUOPT	—	—	CTSU option setting register
CTSUSCNTACT	—	—	CTSU sensor counter automatic correction table access register
CTSUMCACTn	—	—	CTSU multi-clock automatic

Register	Bit	RX231 (CTSU)	RX261 (CTSU2SLa)
			correction table n (n = 1 to 3)
CTSUAJCR	—	—	CTSU automatic judgment control register
CTSUAJTHR	—	—	CTSU threshold register
CTSUAJMMAR	—	—	CTSU moving average result register
CTSUAJBLACT	—	—	CTSU baseline average intermediate result register
CTSUAJBLAR	—	—	CTSU baseline average result register
CTSUAJRR	—	—	CTSU automatic judgment result register
CTSUADCC	—	—	CTSU A/D converter connection control register
CTSUCR0	—	CTSU control register 0	—
CTSUCR1	—	CTSU control register 1	—
CTSUSDPRS	—	CTSU synchronous noise reduction setting register	—
CTSUSST	—	CTSU sensor stabilization wait control register	—
CTSUMCH0	—	CTSU measurement channel register 0	—
CTSUMCH1	—	CTSU measurement channel register 1	—
CTSUCHACn	—	CTSU channel enable control register n (n = 0 to 3)	—
CTSUCHAC4	—	CTSU channel enable control register 4	—
CTSUCHTRCn	—	CTSU channel transmit/receive control register n (n = 0 to 3)	—
CTSUCHTRC4	—	CTSU channel transmit/receive control register 4	—
CTSUDCLKC	—	CTSU high-pass noise reduction control register	—
CTSUST	—	CTSU status register	—
CTSUSSC	—	CTSU high-pass noise reduction spectrum diffusion control register	—
CTSUSO0	—	CTSU sensor offset register 0	—
CTSUSO1	—	CTSU sensor offset register 1	—
CTSUSC	—	CTSU sensor counter	—
CTSURC	—	CTSU reference counter	—
CTSUERRS	—	CTSU error status register	—

2.23 12-Bit A/D Converter

Table 2.57 shows a Comparative Overview of 12-Bit A/D Converters, and Table 2.58 shows a Comparison of 12-Bit A/D Converter Registers.

Table 2.57 Comparative Overview of 12-Bit A/D Converters

Item	RX231 (S12ADE)	RX261 (S12ADE)
Number of units	1 unit	1 unit
Input channels	24 channels	25 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.83 µs per channel (when A/D conversion clock (ADCLK) = 54 MHz)	0.7 µs (ADCCR.CCS bit = 0) or 0.5 µs (ADCCR.CCS bit = 1) per channel (when A/D conversion clock (ADCLK) = 64 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock ADCLK can be set so that the frequency division ratio should be one of the following. — PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data registers	• 24 registers for analog input • One register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • In A/D-converted value addition mode, the sum of all A/D-converted results is stored in the A/D data registers as a value with the number of bits for conversion accuracy + 2 bits/4 bits. • Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 25 registers for analog input • One register for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • In A/D-converted value addition mode, the sum of all A/D-converted results is stored in the A/D data registers as a value with the number of bits for conversion accuracy + 2 bits/4 bits. • Double trigger mode (selectable in single scan and group scan modes) — The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX231 (S12ADE)	RX261 (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 arbitrarily selected channels. • Group scan mode: — Analog inputs of up to 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 25 arbitrarily selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 25 arbitrarily selected channels. • Group scan mode: — Analog inputs of up to 25 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be specified.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU), the event link controller (ELC), or the 16-bit timer pulse unit (TPU). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the general purpose PWM timer (GPTW) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX231 (S12ADE)	RX261 (S12ADE)
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode or average mode can be selected. • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • A/D-converted value addition mode or average mode can be selected. • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).

Item	RX231 (S12ADE)	RX261 (S12ADE)
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.58 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX231 (S12ADE)	RX261 (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 7, 16 to 31)	A/D data register y (y = 0 to 8, 16 to 31)
ADANSA0	ANSA008	—	A/D conversion channel select bit
ADANSB0	ANSB008	—	A/D conversion channel select bit
ADADS0	ADS008	—	A/D-converted value addition/average channel select bit
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 8, L, T, O)
ADCMPANSR0	CMPCHA008	—	Compare window A channel select bit
ADCMPLR0	CMPLCHA008	—	Compare window A comparison condition select bit
ADCMPSR0	CMPSTCHA008	—	Compare window A flag

Register	Bit	RX231 (S12ADE)	RX261 (S12ADE)
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 0 0 1 0 0 0: AN008 0 1 0 0 0 0: AN016 0 1 0 0 0 1: AN017 : 0 1 1 1 0 1: AN029 0 1 1 1 1 0: AN030 0 1 1 1 1 1: AN031 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADCCR	—	—	A/D conversion cycle control register

2.24 12-Bit D/A Converter and D/A Converter

Table 2.59 shows a Comparative Overview of 12-bit D/A Converter and D/A Converter, and Table 2.60 shows a Comparison of 12-Bit D/A Converter Registers and D/A Converter Registers.

Table 2.59 Comparative Overview of 12-bit D/A Converter and D/A Converter

Item	RX231 (R12DAA)	RX261 (DAa)
Resolution	12 bits	8 bits
Output channels	2 channels	2 channels
Measure against interference between analog modules	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.	Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 8-bit D/A converter inrush current with the enable signal.
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	Ability to start D/A conversion on channel 0 when an event signal is input	Ability to start D/A conversion on channel 0 when an event signal is input

Table 2.60 Comparison of 12-Bit D/A Converter Registers and D/A Converter Registers

Register	Bit	RX231 (R12DAA)	RX261 (DAa)
DAADSCR	DAADST	D/A A/D synchronous conversion bit 0: The 12-bit D/A converter does not perform conversion in synchronization with the 12-bit A/D converter (to disable the measure against interference between D/A and A/D conversion). 1: The 12-bit D/A converter performs conversion in synchronization with the 12-bit A/D converter (to enable the measure against interference between D/A and A/D conversion).	D/A enable bit 0: The 8-bit D/A converter does not perform conversion in synchronization with the 12-bit A/D converter (to disable the measure against interference between D/A and A/D conversion). 1: The 8-bit D/A converter performs conversion in synchronization with the 12-bit A/D converter (to enable the measure against interference between D/A and A/D conversion).
DAVREFCR	—	D/A VREF control register	—

2.25 Temperature Sensor

Table 2.61 shows a Comparison of Temperature Sensor Registers.

Table 2.61 Comparison of Temperature Sensor Registers

Register	Bit	RX231 (TEMPSA)	RX261 (TEMPSA)
TSCDRH, TSCDRL (RX231) TSCDR (RX261)	—	Temperature sensor calibration data register	Temperature sensor calibration data register

2.26 Comparator B

Table 2.62 shows a Comparative Overview of Comparator B Modules, and Table 2.63 shows a Comparison of Comparator B Registers.

Table 2.62 Comparative Overview of Comparator B Modules

Item	RX231 (CMPBa)	RX261 (CMPBa)
Number of channels	4 channels (comparator B0 to comparator B3)	2 channels (comparator B0, comparator B1)
Analog input voltage	Voltage input to CMPBn pin (n = 0 to 3)	Voltage input to CMPBn pin
Reference input voltage	Voltage input to CVREFBn pin (n = 0 to 3) or internal reference voltage	Voltage input to CVREFBn pin or internal reference voltage
Comparison result	Read from the CPBFLG.CPBnOUT flag (n = 0 to 3) Ability to output comparison result to CMPOBn pin (n = 0 to 3).	Read from the CPBFLG.CPBnOUT flag Ability to output comparison result to CMPOBn pin
Interrupt request	• When the comparator B0 comparison result changes • When the comparator B1 comparison result changes • When the comparator B2 comparison result changes • When the comparator B3 comparison result changes	• When the comparator B0 comparison result changes • When the comparator B1 comparison result changes
Timing of event generation to ELC	• When the comparator B0 comparison result changes • When the comparator B0 or B1 comparison result changes	• When the comparator B0 comparison result changes • When the comparator B0 or B1 comparison result changes
POE source output timing	—	• When the comparator B0 comparison result changes • When the comparator B1 comparison result changes
Selectable functions	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency, can be selected. • Window function Ability to specify whether the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0 to 3) < high-side reference (VRFH)) • Reference input voltage Ability to select CVREFBn pin (n = 0 to 3) input or internal reference voltage (generated internally) • Comparator B response speed Ability to select high-speed or low-speed mode	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency, can be selected. • Window function Ability to specify whether the window function is enabled or disabled (VRFL < CMPBn < VRFH) • Reference input voltage Ability to select CVREFBn pin input or internal reference voltage (generated internally) • Comparator B response speed Ability to select high-speed or low-speed mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.63 Comparison of Comparator B Registers

Register	Bit	RX231 (CMPBa)	RX261 (CMPBa)
CPB1CNT1	—	Comparator B1 control register 1	—
CPB1CNT2	—	Comparator B1 control register 2	—
CPB1FLG	—	Comparator B1 flag register	—
CPB1INT	—	Comparator B1 interrupt control register	—
CPB1F	—	Comparator B1 filter select register	—
CPB1MD	—	Comparator B1 mode select register	—
CPB1REF	—	Comparator B1 reference input voltage select register	—
CPB1OCR	—	Comparator B1 output control register	—

2.27 RAM

Table 2.64 shows a Comparative Overview of RAM.

Table 2.64 Comparative Overview of RAM

Item	RX231	RX261
RAM capacity	Up to 64 KB	128 KB
RAM address	• RAM capacity 64 KB RAM0: 0000 0000h to 0000 FFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh	• RAM: 0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 1
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing.*1 • The RAM can be enabled or disabled.
Low power consumption function	Ability to transition to module stop state	Ability to specify module stop state
Error checking	—	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Note: 1. An access across an 8-byte boundary doubles the number of cycles.

Table 2.65 Comparison of RAM Registers

Register	Bit	RX231	RX261
RAMMODE	—	—	RAM operating mode control register
RAMSTS	—	—	RAM error status register
RAMECAD	—	—	RAM error address capture register
RAMPRCR	—	—	RAM protection register

2.28 Flash Memory

Table 2.66 shows a Comparative Overview of Flash Memory, and Table 2.67 shows a Comparison of Flash Memory Registers.

Table 2.66 Comparative Overview of Flash Memory

Item	RX231	RX261
Memory capacity	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores start-up area information, access window information, and unique ID.	• User area: Up to 512 KB • User boot area: 8 KB • Extra area: Stores start-up area information, access window information, and unique ID.
Addresses	• 512 KB — FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: — FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB: — FFFE 0000h to FFFF FFFFh • Data area: — 0100 0000h to 0010 1FFFh	• 512 KB — FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB: — FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB: — FFFC 0000h to FFFF FFFFh • Data area: — 0100 0000h to 0010 1FFFh
Operating clock	• FCLK: 1 to 32 MHz (when ROM in P/E mode or E2 data flash in P/E mode) 32 MHz (max.) (when E2 data flash in read mode)	• FCLK: 1 to 64 MHz (when ROM in P/E mode or E2 data flash in P/E mode) 64 MHz (max.) (when E2 data flash in read mode) • HOCO clock: 24 MHz, 32 MHz, 48 MHz, or 64 MHz (when ROM in P/E mode or E2 data flash in P/E mode)
Software commands	• The following software commands are implemented: — Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: — Start-up area information program and access window information program	• The following software commands are implemented: — Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: — Start-up area information program, access window protect, and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.

Item	RX231	RX261
On-board programming (serial programming and self-programming)	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous mode. — The user area and data area are programmable. • Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. • Boot mode (USB interface) — Channel 0 (USB0) of the USB 2.0 function module is used. — The user area and data area are programmable. — The flash memory can be programmed in self-powered or bus-powered mode. — A personal computer can be connected using only a USB cable. • Self-programming (single-chip mode) — The user area and data area are programmable using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous mode. — The user area and data area are programmable. • Boot mode (FINE interface) — FINE is used. — The user area and data area are programmable. • Boot mode (USB interface) — Channel 0 (USB0) of the USB 2.0 function module is used. — The user area and data area are programmable. — The flash memory can be programmed in self-powered or bus-powered mode. — A personal computer can be connected using only a USB cable. • Self-programming (single-chip mode) — The user area and data area are programmable using a flash programming routine in a user program.
Off-board programming	The user area and data area can be programmed using a flash programmer (serial programmer or parallel programmer) compatible with the MCU.	—
ID code protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes. • Connection with a parallel programmer can be controlled using ROM codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 7.	This function is used to safely program blocks 0 to 7.
Area protection	It is possible to designate a specific range within the user area that may be programmed and prohibit programming outside that range during self-programming.	It is possible to designate a specific range within the user area that may be programmed and prohibit programming outside that range during self-programming.
Background operation (BGO) function	Programs in a ROM area can run while the E2 DataFlash is being programmed.	Programs in a ROM area can run while the E2 DataFlash is being programmed.

Table 2.67 Comparison of Flash Memory Registers

Register	Bit	RX231	RX261
MEMWAITR	—	—	Memory wait cycle setting register
FPMCR	FMS0, FMS1, FMS2 (RX231) FMS0, FMS1 (RX261)	Flash operating mode select bits FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than the above are prohibited.	Flash operating mode select bits FMS1 FMS0 0 0: ROM/E2 DataFlash read mode 0 1: ROM P/E mode 1 0: E2 DataFlash P/E mode 1 1: Setting prohibited.
	LVPE	Low-voltage P/E mode enable bit	—
FISR	PCKA[4:0] (RX231) PCKA[5:0] (RX261)	Peripheral clock notification bits Bits for setting the FlashIF clock (FCLK) frequency	Peripheral clock notification bits Bits for setting the FlashIF clock (FCLK) frequency
FSCMR	AWPR	—	Access window protect flag

2.29 Packages

As indicated in Table 2.68, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.68 Packages

Package Type	RENESAS Code	
	RX231	**RX261**
100-pin TFLGA	○	×
80-pin LFQFP	×	○
64-pin WFLGA	○	×
64-pin HWQFN	○	×
48-pin HWQFN	PWQN0048KB-A	PWQN0048KC-A

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exist on both groups with different specifications are indicated by **red text**. **Black text** indicates there are no differences in item specifications between groups.

3.1 100-Pin Package

Table 3.1 shows a Comparative Listing of 100-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 100-Pin Package Pin Functions

100-Pin	RX230/231 (100-pin LFQFP)	RX260/261 (100-pin LFQFP)
1	VREFH	P06*3
2	P03/DA0	P03*3/DA0
3	VREFL	P04*3
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#	PJ3/GTIOC6B/GTIOC6B#/CTS6#/RTS6#/SS6#
5	VCL	VCL
6	VBATT	PJ1/GTIOC6A/GTIOC6A#/GTCPPO0
7	MD/FINED	MD/FINED/PG7
8	XCIN	XCIN/PH7
9	XCOUT	XCOUT/EXCIN/PH6
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ2
14	VCC	VCC
15	UPSEL/P35/NMI	UPSEL/P35/NMI
16	P34/MTIOC0A/TMCI3/POE2#/SCK6/TS0/IRQ4	P34/GTIOC3A/GTIOC3A#/GTIU/TMCI3/SCK6/IRQ4
17	P33/MTIOC0D/TMRI3/POE3#/TIOCD0/RXD6/SMISO6/SSCL6/TS1/IRQ3	P33/GTIOC1B/GTIOC7B/GTIOC1B#/GTIOC7B#/TMRI3/RXD6/SMISO6/SSCL6/CRX0*2/IRQ3
18	P32/MTIOC0C/TMO3/TIOCC0/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/USB0_VBUSEN/IRQ2	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
19	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/SSISCK0/IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	P27/CS3#/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/CVREFB3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
22	P26/CS2#/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/SSIRXD0/TS3/CMPB3	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
23	P25/CS1#/MTIOC4C/MTCLKB/TIOCA4/TS4/ADTRG0#	P25/GTIOC1B/GTIOC6A/GTIOC1B#/GTIOC6A#/GTETRGB/ADTRG0#
24	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/TIOCB4/USB0_VBUSEN/TS5	P24/GTIOC1A/GTIOC6B/GTIOC1A#/GTIOC6B#/GTETRGA/TMRI1/USB0_VBUSEN*2
25	P23/MTIOC3D/MTCLKD/TIOCD3/CTS0#/RTS0#/SS0#/SSISCK0/TS6	P23/GTIOC0B/GTIOC3B/GTIOC0B#/GTIOC3B#/GTETRGD/CTS000#/RTS000#/SS000#/DE000
26	P22/MTIOC3B/MTCLKC/TMO0/TIOCC3/SCK0/USB0_OVRCURB/AUDIO_MCLK/TS7	P22/GTIOC0A/GTIOC3A/GTIOC0A#/GTIOC3A#/GTETRGC/TMO0/SCK000/TXDB000/USB0_OVRCURB*2

100-Pin	RX230/231 (100-pin LFQFP)	RX260/261 (100-pin LFQFP)
27	P21/MTIOC1B/TMCI0/TIOCA3/RXD0/SMISO0/ SSCL0/USB0_EXICEN/SSIWS0/TS8	P21/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/ TMCI0/RXD000/SMISO000/SSCL000/ USB0_EXICEN*2
28	P20/MTIOC1A/TMRI0/TIOCB3/TXD0/SMOSI0/ SSDA0/USB0_ID/SSIRXD0/TS9	P20/GTIOC2B/GTIOC4A/GTIOC2B#/GTIOC4A#/ TMRI0/TXD000/TXDA000/SMOSI000/SSDA000/ USB0_ID*2
29	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/ TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/ CMPOB2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
30	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/ RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL/USB0_VBUS/USB0_VBUSEN/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/ RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/ CMPB2	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
32	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/ CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/ TS13/IRQ4/CVREFB2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
33	P13/MTIOC0B/TMO3/TIOCA5/SDA/IRQ3	P13/GTIOC3B/GTIOC7A/GTIOC3B#/GTIOC7A#/ GTIV/TMO3/SDA0/IRQ3
34	P12/TMCI1/SCL/IRQ2	P12/TMCI1/SCL0/IRQ2
35	VCC_USB*4/PH3*4/TMCI0*4	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
36	PH2*4/TMRI0*4/USB0_DM*4/IRQ1*4	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/ USB0_DM*2/TS8*1/IRQ1*1
37	PH1*4/TMO0*4/USB0_DP*4/IRQ0*4	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
38	VSS_USB*4/PH0*4/CACREF*4	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
39	P55/WAIT#/MTIOC4D/TMO3/CRXD0/TS15	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11
40	P54/ALE/MTIOC4B/TMCI1/CTXD0/TS16	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
41	BCLK/P53/TS17	P53/PMC0
42	P52/RD#/TS18	P52
43	P51/WR1#/BC1#/WAIT#/TS19	P51/PMC0
44	P50/WR0#/WR#/TS20	P50
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/TMO2/ TXD8/SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
46	PC6/A22/CS1#/MTIOC3C/MTCLKA/TMCI2/ RXD8/SMISO8/SSCL8/MOSIA/TS22	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
47	PC5/A21/CS2#/WAIT#/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA/TS23	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/SCK5/CTS8#/RTS8#/SS8#/SSLA0/ SDHI_D1/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP

100-Pin	RX230/231 (100-pin LFQFP)	RX260/261 (100-pin LFQFP)
49	PC3/A19/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/IRTXD5/SDHI_D0/TS27	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/SMOSI5/SSDA5/PMC0/TS16
50	PC2/A18/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/SDHI_D3/TS30	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/A17/MTIOC3A/TCLKD/SCK5/SSLA2/TS33	PC1/GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/SCK5/SSLA2
52	PC0/A16/MTIOC3C/TCLKC/CTS5#/RTS5#/SS5#/SSLA1/TS35	PC0/GTIOC6B/GTIOC6B#/GTETRGC/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/A15/MTIOC3B/TIOCB5/TXD9/SMOSI9/SSDA9/SDHI_D2	PB7/GTIOC0A/GTIOC7B/GTIOC0A#/GTIOC7B#/TXD009/TXDA009/SMOSI009/SSDA009/TS18
54	PB6/A14/MTIOC3D/TIOCA5/RXD9/SMISO9/SSCL9/SDHI_D1	PB6/GTIOC0B/GTIOC7A/GTIOC0B#/GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
55	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/SCK9/USB0_VBUS/SDHI_CD	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/USB0_VBUS*2/TS20
56	PB4/A12/TIOCA4/CTS9#/RTS9#/SS9#	PB4/GTIOC6A/GTIOC6A#/CTS009#/RTS009#/SS009#/DE009/TS21
57	PB3/A11/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/TCLKD/SCK6/SDHI_WP	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
58	PB2/A10/TIOCC3/TCLKC/CTS6#/RTS6#/SS6#	PB2/GTIOC3A/GTIOC3A#/GTETRGC/CTS6#/RTS6#/SS6#/TS23
59	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/RSPCKA/SDHI_CM D	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
62	VSS	VSS
63	PA7/A7/TIOCB2/MISOA	PA7/GTIOC5B/GTIOC5B#/MISOA
64	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/A5/TIOCB1/RSPCKA	PA5/GTIOC4B/GTIOC4B#/RSPCKA/TS27
66	PA4/A4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
68	PA2/A2/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/A1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/SSISCK0	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/SCK5/SSLA2/TS31
70	PA0/A0/BC0#/MTIOC4A/TIOCA0/SSLA1/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
71	PE7/D15[A15/D15]/IRQ7/AN023	PE7/IRQ7/AN023
72	PE6/D14[A14/D14]/IRQ6/AN022	PE6/IRQ6/AN022

100-Pin	RX230/231 (100-pin LFQFP)	RX260/261 (100-pin LFQFP)
73	PE5/D13[A13/D13]/MTIOC4C/MTIOC2B/IRQ5/ AN021/CMPOB0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/ IRQ5/AN021/CMPOB0
74	PE4/D12[A12/D12]/MTIOC4D/MTIOC1A/AN020/ CMPA2/CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
75	PE3/D11[A11/D11]/MTIOC4B/POE8#/CTS12#/ RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/ TS34/AN019
76	PE2/D10[A10/D10]/MTIOC4A/RXD12/RXDX12/ SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/ CVREFB0
77	PE1/D9[A9/D9]/MTIOC4C/TXD12/TXDX12/ SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/AN017/ CMPB0
78	PE0/D8[A8/D8]/SCK12/AN016	PE0/SCK12/AN016
79	PD7/D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN031	PD7/IRQ7/AN031
80	PD6/D6[A6/D6]/MTIC5V/POE1#/IRQ6/AN030	PD6/IRQ6/AN030
81	PD5/D5[A5/D5]/MTIC5W/POE2#/IRQ5/AN029	PD5/IRQ5/AN029
82	PD4/D4[A4/D4]/POE3#/IRQ4/AN028	PD4/IRQ4/AN028
83	PD3/D3[A3/D3]/POE8#/IRQ3/AN027	PD3/IRQ3/AN027
84	PD2/D2[A2/D2]/MTIOC4D/IRQ2/AN026	PD2/GTIOC2B/GTIOC2B#/SCK6/CRX0*2/IRQ2/ AN026
85	PD1/D1[A1/D1]/MTIOC4B/IRQ1/AN025	PD1/GTIOC2A/GTIOC2A#/RXD6/SMISO6/ SSCL6/CTX0*2/IRQ1/AN025
86	PD0/D0[A0/D0]/IRQ0/AN024	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P47/AN007	P47*3/AN007
88	P46/AN006	P46*3/AN006
89	P45/AN005	P45*3/AN005
90	P44/AN004	P44*3/AN004
91	P43/AN003	P43*3/AN003
92	P42/AN002	P42*3/AN002
93	P41/AN001	P41*3/AN001
94	VREFL0	VREFL0/PJ7*3
95	P40/AN000	P40*3/AN000
96	VREFH0	VREFH0/PJ6*3
97	AVCC0	AVCC0
98	P07/ADTRG0#	P07*3/ADTRG0#
99	AVSS0	AVSS0
100	P05/DA1	P05*3/DA1

Notes: 1. Not implemented in the RX261.
2. Not implemented in the RX260.
3. The power supply of the I/O buffer for these pins is AVCC0.
4. PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, and PH3/TMCI0 on the RX230. VSS_USB, USB0_DP, USB0_DM, and VCC_USB on the RX231.

3.2 64-Pin Package

Table 3.2 shows a Comparative Listing of 64-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 64-Pin Package Pin Functions

64-Pin	RX230/231 (64-Pin LFQFP, 64-Pin HWQFN)	RX260/261 (64-pin LFQFP)
1	P03/DA0	P03*3/DA0
2	VCL	VCL
3	MD/FINED	MD/FINED/PG7
4	XCIN	XCIN/PH7
5	XCOUT	XCOUT/EXCIN/PH6
6	RES#	RES#
7	XTAL/P37	XTAL/P37/IRQ4
8	VSS	VSS
9	EXTAL/P36	EXTAL/P36/IRQ2
10	VCC	VCC
11	UPSEL/P35/NMI	UPSEL/P35/NMI
12	VBATT	P32/GTIOC1A/GTIOC7A/GTIOC1A#/GTIOC7A#/ GTIW/TMO3/RTCOUT/RTCIC2/TXD6/SMOSI6/ SSDA6/CTX0*2/USB0_VBUSEN*2/TS0/IRQ2
13	P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/RTS1#/ SS1#/SSISCK0/IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ RTCIC1/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	P30/MTIOC4B/TMRI3/POE8#/RTCIC0/RXD1/ SMISO1/SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RTCIC0/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/ CVREFB3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
16	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0/TS3/CMPB3	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
17	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/ TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/ CMPOB2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/ RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/SCL/ USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/ IRQ6/ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/MOSIA/ SCL0/USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/ RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/ CMPB2	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
20	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/ CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/ TS13/IRQ4/CVREFB2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
21	VCC_USB*4/PH3*4/TMCI0*4	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
22	PH2*4/TMRI0*4/USB0_DM*4/IRQ1*4	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/ USB0_DM*2/TS8*1/IRQ1*1
23	PH1*4/TMO0*4/USB0_DP*4/IRQ0*4	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
24	VSS_USB*4/PH0*4/CACREF*4	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
25	P55/MTIOC4D/TMO3/CRXD0/TS15	P55/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/ TMO3/CRX0*2/TS11

64-Pin	RX230/231 (64-Pin LFQFP, 64-Pin HWQFN)	RX260/261 (64-pin LFQFP)
26	P54/MTIOC4B/TMCI1/CTXD0/TS16	P54/GTIOC2A/GTIOC2A#/TMCI1/CTX0*2/TS12
27	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/ SSCL8/MOSIA/USB0_EXICEN/TS22	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/ USB0_ID/TS23	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
30	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/SSLA0/SDHI_D1/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
31	PC3/MTIOC4D/TCLKB/TXD5/SMOSI5/SSDA5/ IRTXD5/SDHI_D0/TS27	PC3/GTIOC2B/GTIOC2B#/GTETRGB/TXD5/ SMOSI5/SSDA5/PMC0/TS16
32	PC2/MTIOC4B/TCLKA/RXD5/SMISO5/SSCL5/ SSLA3/IRRXD5/SDHI_D3/TS30	PC2/GTIOC2A/GTIOC2A#/GTETRGA/GTOWUP/ RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/PC1/MTIOC3B/TIOCB5/TXD9/SMOSI9/ SSDA9/SDHI_D2	PB7/PC1*5/GTIOC0A/GTIOC7B/GTIOC0A#/ GTIOC7B#/TXD009/TXDA009/SMOSI009/ SSDA009/TS18
34	PB6/PC0/MTIOC3D/TIOCA5/RXD9/SMISO9/ SSCL9/SDHI_D1	PB6/PC0*5/GTIOC0B/GTIOC7A/GTIOC0B#/ GTIOC7A#/RXD009/SMISO009/SSCL009/TS19
35	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TIOCB4/ SCK9/USB0_VBUS/SDHI_CD	PB5/GTIOC4B/GTIOC5A/GTIOC4B#/GTIOC5A#/ GTIOC6B/GTIOC6B#/TMRI1/SCK009/TXDB009/ USB0_VBUS*2/TS20
36	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/TIOCD3/ TCLKD/SCK6/SDHI_WP	PB3/GTIOC1A/GTIOC3A/GTIOC1A#/GTIOC3A#/ GTIOC3B/GTIOC3B#/GTETRGD/GTIU/GTOVUP/ TMO0/LPTO/SCK6/PMC0/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TIOCB3/TXD6/ SMOSI6/SSDA6/SDHI_CLK/IRQ4/CMPOB1	PB1/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7A/GTIOC7A#/GTOVLO/GTIW/GTOWLO/ TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/ CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/TIOCA3/RXD6/SMISO6/SSCL6/ RSPCKA/SDHI_CM D	PB0/GTIOC0B/GTIOC2A/GTIOC0B#/GTIOC2A#/ GTOWUP/RXD6/SMISO6/SSCL6/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/ CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/ SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/ CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/ SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/ SSISCK0	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31

64-Pin	RX230/231 (64-Pin LFQFP, 64-Pin HWQFN)	RX260/261 (64-pin LFQFP)
45	PA0/MTIOC4A/TIOCA0/SSLA1/CACREF	PA0/GTIOC0A/GTIOC1A/GTIOC0A#/GTIOC1A#/GTOVUP/CACREF/SSLA1/TS32
46	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0	PE5/GTIOC1B/GTIOC5B/GTIOC1B#/GTIOC5B#/IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/GTOWLO/TS33/AN020/CMPA2
48	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/AUDIO_MCLK/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/GTIOC4B#/GTOWUP/CTS12#/RTS12#/SS12#/TS34/AN019
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/IRQ7/AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/SMISO12/SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/AN017/CMPB0
51	PE0/SCK12/AN016	PE0/SCK12/AN016
52	VREFL	P47*3/AN007
53	P46/AN006	P46*3/AN006
54	VREFH	P45*3/AN005
55	P44/AN004	P44*3/AN004
56	P43/AN003	P43*3/AN003
57	P42/AN002	P42*3/AN002
58	P41/AN001	P41*3/AN001
59	VREFL0	VREFL0/PJ7*3
60	P40/AN000	P40*3/AN000
61	VREFH0	VREFH0/PJ6*3
62	AVCC0	AVCC0
63	P05/DA1	P05*3/DA1
64	AVSS0	AVSS0

Notes: 1. Not implemented in the RX261.
2. Not implemented in the RX260.
3. The power supply of the I/O buffer for these pins is AVCC0.
4. PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, and PH3/TMCI0 on the RX230. VSS_USB, USB0_DP, USB0_DM, and VCC_USB on the RX231.
5. PC0 and PC1 are valid only when the port switching function is selected.

3.3 48-Pin Package

Table 3.3 shows a Comparative Listing of 48-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX230/RX231 (48-Pin LFQFP, 48-Pin HWQFN)	RX260/RX261 (48-Pin LFQFP, 48-Pin HWQFN)
1	VCL	VCL
2	MD/FINED	MD/FINED/PG7
3	RES#	RES#
4	XTAL/P37	XTAL/P37/IRQ4
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36/IRQ2
7	VCC	VCC
8	UPSEL/P35/NMI	UPSEL/P35/NMI
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/ SSISCK0/IRQ1	P31/GTIOC2B/GTIOC2B#/GTOWLO/TMCI2/ CTS1#/RTS1#/SS1#/TS1/IRQ1
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/ SSCL1/AUDIO_MCLK/IRQ0/CMPOB3	P30/GTIOC2A/GTIOC2A#/GTOWUP/TMRI3/ RXD1/SMISO1/SSCL1/TS2/IRQ0
11	P27/MTIOC2B/TMCI3/SCK1/SSIWS0/TS2/ CVREFB3	P27/GTIOC5B/GTIOC5B#/TMCI3/SCK1/TS3
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/ USB0_VBUSEN/SSIRXD0/TS3/CMPB3	P26/GTIOC5A/GTIOC5A#/TMO1/LPTO/TXD1/ SMOSI1/SSDA1/USB0_VBUSEN*2/TS4
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/TIOCB0/ TCLKD/SCK1/MISOA/SDA/SSITXD0/IRQ7/ CMPOB2	P17/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC6A/GTIOC6A#/GTETRGD/GTCPPO0/ GTOUUP/TMO1/SCK1/MISOA/SDA0/IRQ7
14	P16/MTIOC3C/MTIOC3D/TMO2/TIOCB1/TCLKC/ TXD1/SMOSI1/SSDA1/MOSIA/SCL/USB0_VBUS/ USB0_VBUSEN/USB0_OVRCURB/IRQ6/ ADTRG0#	P16/GTIOC0B/GTIOC4B/GTIOC0B#/GTIOC4B#/ GTIOC6B/GTIOC6B#/GTETRGC/GTOULO/ TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/ USB0_VBUS*2/USB0_VBUSEN*2/ USB0_OVRCURB*2/IRQ6/ADTRG0#
15	P15/MTIOC0B/MTCLKB/TMCI2/TIOCB2/TCLKB/ RXD1/SMISO1/SSCL1/CRXD0/TS12/IRQ5/ CMPB2	P15/GTIOC3B/GTIOC5B/GTIOC3B#/GTIOC5B#/ GTETRGB/GTIV/TMCI2/RXD1/SMISO1/SSCL1/ CRX0*2/TS5/IRQ5
16	P14/MTIOC3A/MTCLKA/TMRI2/TIOCB5/TCLKA/ CTS1#/RTS1#/SS1#/CTXD0/USB0_OVRCURA/ TS13/IRQ4/CVREFB2	P14/GTIOC6A/GTIOC7B/GTIOC6A#/GTIOC7B#/ GTETRGA/GTCPPO0/TMRI2/CTS1#/RTS1#/ SS1#/CTX0*2/USB0_OVRCURA*2/TS6/IRQ4
17	VCC_USB*4/PH3*4/TMCI0*4	PH3/GTIOC2B/GTIOC2B#/TMCI0/TS7
18	PH2*4/TMRI0*4/USB0_DM*4/IRQ1*4	PH2*1/GTIOC1B*1/GTIOC1B#*1/TMRI0*1/ USB0_DM*2/TS8*1/IRQ1*1
19	PH1*4/TMO0*4/USB0_DP*4/IRQ0*4	PH1*1/GTIOC0B*1/GTIOC0B#*1/ GTOULO*1/TMO0*1/USB0_DP*2/TS9*1/ IRQ0*1
20	VSS_USB*4/PH0*4/CACREF*4	PH0/GTIOC0A/GTIOC0A#/GTOUUP/CACREF/ TS10
21	UB/PC7/MTIOC3A/MTCLKB/TMO2/TXD8/ SMOSI8/SSDA8/MISOA/CACREF	UB/PC7/GTIOC6A/GTIOC6A#/GTETRGB/ GTCPPO0/TMO2/LPTO/CACREF/TXD008/ TXDA008/SMOSI008/SSDA008/MISOA/TS13
22	PC6/MTIOC3C/MTCLKA/TMCI2/RXD8/SMISO8/ SSCL8/MOSIA/USB0_EXICEN/TS22	PC6/GTIOC6B/GTIOC6B#/GTETRGA/TMCI2/ RXD008/SMISO008/SSCL008/MOSIA/ USB0_EXICEN*2/TS14

48-Pin	RX230/RX231 (48-Pin LFQFP, 48-Pin HWQFN)	RX260/RX261 (48-Pin LFQFP, 48-Pin HWQFN)
23	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/RSPCKA/ USB0_ID/TS23	PC5/GTIOC0A/GTIOC7A/GTIOC0A#/GTIOC7A#/ GTETRGD/GTOUUP/GTIW/TMRI2/SCK008/ TXDB008/RSPCKA/USB0_ID*2/PMC0/TS15
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/SSLA0/TSCAP	PC4/GTIOC0B/GTIOC3A/GTIOC0B#/GTIOC3A#/ GTETRGC/GTIU/GTOULO/TMCI1/SCK5/ CTS008#/RTS008#/SS008#/DE008/SSLA0/ PMC0/TSCAP
25	PB5/PC3/MTIOC2A/MTIOC1B/TMRI1/POE1#/ TIOCB4/USB0_VBUS	PB5/PC3*5/GTIOC4B/GTIOC5A/GTIOC4B#/ GTIOC5A#/GTIOC6B/GTIOC6B#/TMRI1/ USB0_VBUS*2/TS20
26	PB3/PC2/MTIOC0A/MTIOC4A/TMO0/POE3#/ TIOCD3/TCLKD/SCK6	PB3/PC2*5/GTIOC1A/GTIOC3A/GTIOC1A#/ GTIOC3A#/GTIOC3B/GTIOC3B#/GTETRGD/ GTIU/GTOVUP/TMO0/LPTO/SCK6/PMC0/TS22
27	PB1/PC1/MTIOC0C/MTIOC4C/TMCI0/ TIOCB3/TXD6/SMOSI6/SSDA6/IRQ4/CMPOB1	PB1/PC1*5/GTIOC1B/GTIOC2B/GTIOC1B#/ GTIOC2B#/GTIOC7A/GTIOC7A#/GTOVLO/ GTIW/GTOWLO/TMCI0/TXD6/SMOSI6/SSDA6/ TS24/IRQ4/CMPOB1
28	VCC	VCC
29	PB0/PC0/MTIC5W/TIOCA3/RXD6/SMISO6/ SSCL6/RSPCKA	PB0/PC0*5/GTIOC0B/GTIOC2A/GTIOC0B#/ GTIOC2A#/GTOWUP/RXD6/SMISO6/SSCL6/ RSPCKA/TS25
30	VSS	VSS
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/TIOCA2/ CTS5#/RTS5#/SS5#/MOSIA/SSIWS0	PA6/GTIOC0B/GTIOC5A/GTIOC0B#/GTIOC5A#/ GTETRGB/GTOULO/TMCI3/CTS5#/RTS5#/ SS5#/MOSIA/TS26
32	PA4/MTIC5U/MTCLKA/TMRI0/TIOCA1/TXD5/ SMOSI5/SSDA5/SSLA0/SSITXD0/IRTXD5/IRQ5/ CVREFB1	PA4/GTIOC1B/GTIOC4A/GTIOC1B#/GTIOC4A#/ GTETRGA/GTOVLO/TMRI0/TXD5/SMOSI5/ SSDA5/SSLA0/TS28/IRQ5/CVREFB1
33	PA3/MTIOC0D/MTCLKD/TIOCD0/TCLKB/RXD5/ SMISO5/SSCL5/SSIRXD0/IRRXD5/IRQ6/CMPB1	PA3/GTIOC1B/GTIOC2B/GTIOC1B#/GTIOC2B#/ GTIOC7B/GTIOC7B#/GTETRGB/GTETRGD/ GTOVLO/GTOWLO/RXD5/SMISO5/SSCL5/TS29/ IRQ6/CMPB1
34	PA1/MTIOC0B/MTCLKC/TIOCB0/SCK5/SSLA2/ SSISCK0	PA1/GTIOC0A/GTIOC0B/GTIOC0A#/GTIOC0B#/ GTIOC3B/GTIOC3B#/GTETRGC/GTIV/GTOUUP/ SCK5/SSLA2/TS31
35	PE4/MTIOC4D/MTIOC1A/AN020/CMPA2/ CLKOUT	CLKOUT/PE4/GTIOC1A/GTIOC2B/GTIOC1A#/ GTIOC2B#/GTIOC4A/GTIOC4A#/GTOVUP/ GTOWLO/TS33/AN020/CMPA2
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/ AUDIO_MCLK/AN019/CLKOUT	CLKOUT/PE3/GTIOC2A/GTIOC4B/GTIOC2A#/ GTIOC4B#/GTOWUP/CTS12#/RTS12#/TS34/ AN019
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/IRQ7/ AN018/CVREFB0	PE2/GTIOC1A/GTIOC1A#/GTOVUP/RXD12/ SSCL12/RXDX12/TS35/IRQ7/AN018/CVREFB0
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/ AN017/CMPB0	PE1/GTIOC1B/GTIOC1B#/GTOVLO/TXD12/ SSDA12/TXDX12/SIOX12/AN017/CMPB0
39	VREFL	P47*3/AN007
40	P46/AN006	P46*3/AN006
41	VREFH	P45*3/AN005
42	P42/AN002	P42*3/AN002
43	P41/AN001	P41*3/AN001
44	VREFL0	VREFL0/PJ7*3

48-Pin	RX230/RX231 (48-Pin LFQFP, 48-Pin HWQFN)	RX260/RX261 (48-Pin LFQFP, 48-Pin HWQFN)
45	P40/AN000	P40*3/AN000
46	VREFH0	VREFH0/PJ6*3
47	AVCC0	AVCC0
48	AVSS0	AVSS0

Notes: 1. Not implemented in the RX261.
2. Not implemented in the RX260.
3. The power supply of the I/O buffer for these pins is AVCC0.
4. PH0/CACREF, PH1/IRQ0/TMO0, PH2/IRQ1/TMRI0, and PH3/TMCI0 on the RX230. VSS_USB, USB0_DP, USB0_DM, and VCC_USB on the RX231.
5. PC0 to PC3 are valid only when the port switching function is selected.

4. Important Information When Migrating Between MCUs

This section presents important information on differences between the RX261 Group and the RX231 Group.

Section 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX231 Group is compatible with the RX261 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX261 Group and the RX231 Group are as follows:

For differences between modules and functions, refer to section 2, Comparative Overview of Specifications.

For further information, refer to the User's Manual: Hardware of each MCU group, which is listed in section 5, Reference Documents.

4.1.1 Clock Frequency Settings

The clock frequency setting restrictions differ between the RX261 Group and the RX231 Group. For details, see Table 4.1.

Table 4.1 Comparison of Clock Frequency Setting Restrictions

Item	RX231	RX261
Clock frequency setting restrictions	ICLK ≥ BCLK	PCLKA ≥ PCLKB PCLKB ≥ CANFDCLK (when CANFD is used) PCLKB ≥ CANFDMCLK (when CANFD is used)
Clock frequency ratio restrictions	ICLK:FCLK = N:1 or 1:N ICLK:BCLK = N:1 ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N	ICLK:FCLK = N:1 or 1:N ICLK:PCLKA = N:1 or 1:N ICLK:PCLKB = N:1 or 1:N ICLK:PCLKD = N:1 or 1:N PCLKA:PCLKB = 2:1 (when CANFD is used)

4.1.2 PLL Circuit

The frequency multiplication factor of the PLL circuit can be set to ×4 to ×13.5 (in ×0.5 increments) on the RX231 Group and to ×4 or ×15.5 (in ×0.5 increments) on the RX261 Group. To use the PLL circuit, change the setting of the PLLCR.STC bits to an appropriate value.

4.1.3 Initialization of the Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX261 Group and the RX231 Group, even on products with the same pin count.

4.1.4 Note in High-Speed Operating Mode

The maximum operating frequency for reading flash memory in high-speed operation mode differs between the RX261 Group and the RX231 Group. For details, see Table 4.2, Comparison of Maximum Operating Frequency for Reading Flash Memory in High-Speed Operation Mode.

Table 4.2 Comparison of Maximum Operating Frequency for Reading Flash Memory in High-Speed Operation Mode

Item	RX231	RX261
ICLK	54 MHz	64 MHz
FCLK	32 MHz	64 MHz
PCLKD	54 MHz	64 MHz
PCLKB	32 MHz	32 MHz
PCLKA	54 MHz	64 MHz
BCLK	32 MHz	—

5. Reference Documents

User's Manual: Hardware

RX230 Group, RX231 Group User's Manual: Hardware Rev.1.20 (R01UH0496EJ0120)
(The latest version can be downloaded from the Renesas Electronics website.)

RX260 Group, RX261 Group User's Manual: Hardware Rev.1.00 (R01UH1045EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A0147B/E

TN-RX*-A0214A/E

TN-RX*-A0198B/E

TN-RX*-A0217A/E

TN-RX*-A0227A/E

TN-RX*-A0224B/E

TN-RX*-A0237B/E

TN-RX*-A0264A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.7.24	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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