Renesas RA Family

Differences Between Products of the RA6T1 and RA6T2 Groups

Introduction

This application note summarizes the differences in peripheral functions and pin assignments between products of the RA6T1 and RA6T2 groups. This application note is a reference designed to allow the sharing of software resources and to enhance efficiency during development for devices of the two groups. Unless otherwise specified, the information in this application note applies to products of the RA6T1 and RA6T2 groups with the maximum specifications in the 100-pin package with the greatest number of pins. For details of differences in the specifications such as electrical characteristics, usage notes, and setting procedures, refer to the User's Manual for the products of the relevant group.

Target Device

Products of the RA6T1 and RA6T2 groups

Contents

1. Comparison of Built-In Functions of Products of the RA6T1 and RA6T2 Groups

Table 1 describes a comparison of built-in functions of products of the RA6T1 and RA6T2 groups. For details of the functions, see 2. Comparative Overview of Specifications and 6. References.
Note: "-" indicates "Not implemented".

Table 1. Comparison of Built-in Functions of RA6T1 and RA6T2 Groups

Product name		**RA6T1**		**RA6T2**			**Function difference**
Package		LQFP64	LQFP100	LQFP48 QFN48	LQFP64 QFN64	LQFP100	Yes
CPU		Arm Cortex-M4		Arm Cortex-M33			Yes
Code flash memory		512 KB, 256 KB		512 KB, 256 KB			No
Data flash memory		8 KB		16 KB			Yes
SRAM		Parity: 64 KB		ECC: 64 KB			Yes
Standby SRAM		—		Parity: 1 KB			Yes
System	CPU clock	120 MHz (max.)		240 MHz (max.)			Yes
	CPU clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL		MOSC, HOCO, MOCO, LOCO, PLL			Yes
	CAC	Yes		Yes			Yes
	Backup registers	512 B		—			Yes
	ICU	Yes		Yes			Yes
	WDT/IWDT	Yes		Yes			Yes
	KINT	8 ch		8 ch			No
Event link	ELC	Yes		Yes			Yes
DMA	DTC	1 ch		1 ch			Yes
	DMAC	8 ch		8 ch			Yes
Timer	GPT	32bit x 13 ch (Hi-res output x 4 ch) *1		32bit x 10 ch (Hi-res output x 4 ch) *1			Yes
	AGT	16bit x 2 ch		32bit x 2 ch			Yes
Communication	SCI	7 ch		6 ch			Yes
	IIC	2 ch		2 ch			Yes
	SPI	2 ch		2 ch			Yes
	CAN/CANFD	1 ch (CAN)		1 ch (CANFD)			Yes

Product name			**RA6T1**		**RA6T2**			**Function difference**
Analog	ADC12	Unit 0	7 ch*2	11 ch*2	6 ch	10 ch	12 ch + 9 ch*3	Yes
		Unit 1	3 ch*2	8 ch*2	4 ch	8 ch	8 ch + 9 ch*3	
	3ch-S/H	Unit 0	1 (3 ch)	1 (3 ch)	1 (3 ch)	1 (3 ch)	1 (3 ch)	Yes
		Unit 1	—	1 (3 ch)	1 (2 ch)	1 (3 ch)	1 (3 ch)	
	DAC12		2 ch		2 ch	4 ch		Yes
	ACMPHS		6 ch		3 ch	4 ch		Yes
	PGA	Unit 0	3 ch	3 ch	3 ch	3 ch		Yes
		Unit 1	—	3 ch	—	1 ch		
	TSN		Yes		Yes			Yes
Data processing	CRC		Yes		Yes			Yes
	DOC		Yes		Yes			Yes
Accelerator	TFU		—		Yes			Yes
	IIRFA		—		Yes			Yes
Security			SCE7		SCE5, TrustZone, and Lifecycle management			Yes

Note 1. Available pins depend on the pin count. For details, see the MCU User's Manual associated with each product.

Note 2. Some input channels (AN005/AN105 and AN006/AN106) of the ADC units share the same port pin, and the two units cannot use the shared pin at the same time.

Note 3. Shared terminal for UNIT0 and UNIT1.

2. Comparative Overview of Specifications

This section provides a comparative overview of specifications. In the comparative overview, red text indicates functions that are only included in one of the two groups or functions for which the specifications differ between the two groups. Note that the descriptions in the comparative overview are in accord with the user's manuals for each of the groups. Therefore, expressions might differ for the same overview of functions.

Note: "-" indicates "Not implemented".

2.1 CPU

Table 2 shows a comparative overview of the CPUs.

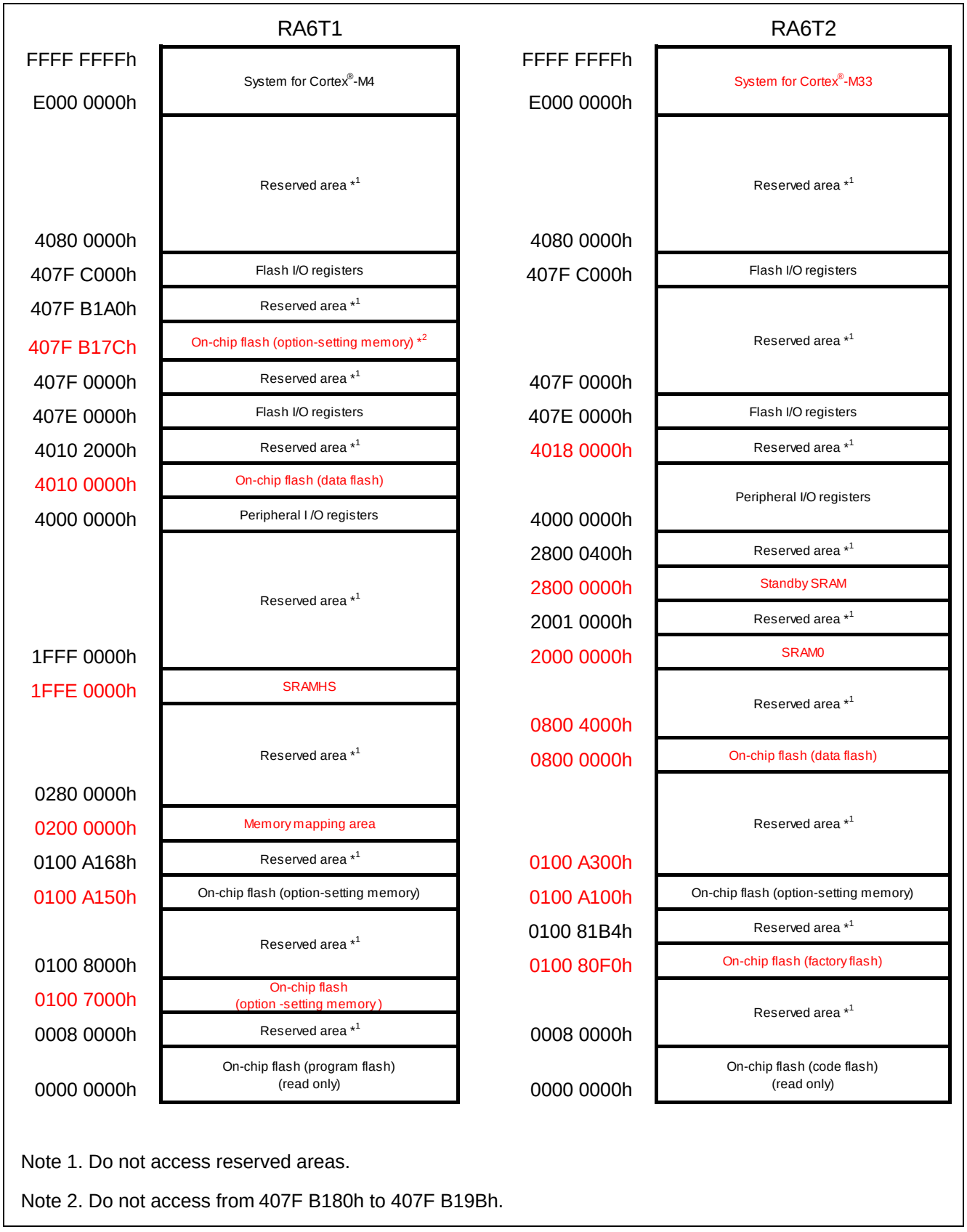
Table 2. Comparative Overview of the CPUs

Item	RA6T1	RA6T2
CPU	• Arm Cortex-M4 — Revision: r0p1-01rel0 — Armv7E-M architecture profile — Single Precision Floating-Point Unit (Compliant with the ANSI/IEEE Std 754-2008)	• Arm Cortex-M33 — Revision: r0p4-00rel1 — Armv8-M architecture profile — Single Precision Floating-Point Unit compliant with the ANSI/IEEE Std 754-2008 • SAU (Security Attribution Unit): 0 region • IDAU (Implementation Defined Attribution Unit): 8 regions — Code flash (secure, non-secure callable, and non-secure) — Data flash (secure and non-secure) — SRAM0 (secure, non-secure callable, and non-secure)
	• Memory Protection Unit (MPU) — Armv7 Protected Memory System Architecture — Eight protected regions	• Memory Protection Unit (MPU) — Armv8 Protected Memory System Architecture (PMSAv8) — Secure MPU (MPU_S): 8 regions — Non-secure MPU (MPU_NS): 8 regions
	• SysTick timer — Driven by SYSTICCLK (LOCO) or ICLK	• SysTick timer — Two SysTick timers: Secure and non-secure instances — Driven by SysTick timer clock (SYSTICCLK) or system clock (ICLK)

Item	RA6T1	RA6T2
Debug	• Arm CoreSight™ ETM-M4 — Revision: r0p1-00rel0 — Arm ETM architecture version 3.5 • CoreSight Instrumentation Trace Macrocell (ITM) • Data Watchpoint and Trace Unit (DWT) — 4 comparators for watchpoints and triggers • Flash Patch and Breakpoint Unit (FPB) — The Flash Patch (remap) function is not available, and only the breakpoint function is available. — 6 instruction comparators — 2 literal comparators • CoreSight Time Stamp Generator (TSG) — Time stamp for ETM and ITM — Driven by CPU clock • Debug Register Module (DBGREG) — Reset control — Halt control • CoreSight Debug Access Port (DAP) — JTAG Debug Port (JTAG-DP) — Serial Wire Debug Port (SW-DP) • Cortex-M4 Trace Port Interface Unit (TPIU) — 4-bit TPIU formatter output — Serial Wire Output • CoreSight Embedded Trace Buffer (ETB) — CoreSight Trace Memory Controller with ETB configuration — Buffer size: 2 KB	• Arm® CoreSight™ ETM-M33 — Revision: r0p2-00rel0 — ARM ETM architecture version 4.2 • Instrumentation Trace Macrocell (ITM) • Data Watchpoint and Trace Unit (DWT) — 4 comparators for watchpoints and triggers • Breakpoint Unit (BPU) — The breakpoint function is available — 8 instruction comparators — No literal comparator • Time Stamp Generator (TSG) — Time stamp for ETM and ITM — Driven by CPU clock • Debug Register Module (DBGREG) — Reset control — Halt control • Debug Access Port (DAP) — JTAG Debug Port (JTAG-DP) — Serial Wire Debug Port (SW-DP) • Cortex-M33 Trace Port Interface Unit (TPIU) — 4-bit TPIU formatter output — Serial Wire Output • Cross Trigger Interface (CTI) • Embedded Trace Buffer (ETB) — CoreSight Trace Memory Controller with ETB configuration — Buffer size: 2 KB
Operating frequency	• CPU: Maximum 120 MHz • 4-bit TPIU trace interface: Maximum 60 MHz • Serial Wire Output (SWO) trace interface: Maximum 60 MHz • Joint Test Action Group (JTAG) interface: Maximum 25 MHz • Serial Wire Debug (SWD) interface: Maximum 25 MHz	• CPU: Maximum 240 MHz • 4-bit TPIU trace interface: Maximum 60 MHz • Serial Write Output (SWO) trace interface: Maximum 60 MHz • Joint Test Action Group (JTAG) interface: Maximum 25 MHz • Serial Wire Data (SWD) interface: Maximum 25 MHz

2.2 Address Space

Figure 1 shows a comparison of memory maps.



Note 1. Do not access reserved areas.

Note 2. Do not access from 407F B180h to 407F B19Bh.

Figure 1. Comparison of Memory Maps

2.3 Resets

Table 3 shows a comparison of reset names and sources, Table 4 shows a comparison of reset detect flags to be initialized by each reset source, Table 5 shows a comparison of clock states when a reset occurs, and Table 6 shows a comparison of programming conditions of the option-setting memory area.

Table 3. Comparison of Reset Names and Sources

Item	RA6T1	RA6T2
RES pin reset	Voltage input to the RES pin is driven low.	Voltage input to the RES pin is driven low.
Power-on reset	VCC rise (voltage detection: V_{POR})	VCC rise (voltage detection: V_{POR})
Independent watchdog timer reset	IWDT underflow or refresh error	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection: V_{det0})	VCC fall (voltage detection: V_{det0})
Voltage monitor 1 reset	VCC fall (voltage detection: V_{det1})	VCC fall (voltage detection: V_{det1})
Voltage monitor 2 reset	VCC fall (voltage detection: V_{det2})	VCC fall (voltage detection: V_{det2})
SRAM parity error reset	SRAM parity error detection	SRAM parity error detection
SRAM ECC error reset	—	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection	—
Stack pointer error reset	Stack pointer error detection	—
TrustZone error reset	—	TrustZone error detection
Cache parity error reset	—	Cache parity error detection
Deep software standby reset	Canceling of Deep Software Standby mode by an interrupt	Deep Software Standby mode is canceled by an interrupt
Software reset	Register setting (by using the Arm® software reset bit AIRCR.SYSRESETREQ)	Register setting (by using the software reset bit AIRCR.SYSRESETREQ)

Table 4. Comparison of Reset Detect Flags to be Initialized by each Reset Source

Item	RA6T1	RA6T2
RES pin reset	• Power-on Reset Detect Flag (RSTSR0.PORF) • Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF) • Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF) • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	• Power-on Reset Detect Flag (RSTSR0.PORF) • Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF) • Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • SRAM ECC Error Reset Detect Flag (RSTSR1.REERF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • TrustZone Error Reset Detect Flag (RSTSR1.TZERF) • Cache Parity Error Reset Detect Flag (RSTSR1.CPERF) • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)

Item	RA6T1	RA6T2
Power-on reset	• Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF) • Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF), • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF) • Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	• Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF) • Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • SRAM ECC Error Reset Detect Flag (RSTSR1.REERF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • TrustZone Error Reset Detect Flag (RSTSR1.TZERF) • Cache Parity Error Reset Detect Flag (RSTSR1.CPERF) • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF) • Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)
Independent watchdog timer reset	• No flags are to be initialized.	• No flags are to be initialized.
Watchdog timer reset	• No flags are to be initialized.	• No flags are to be initialized.

Item	RA6T1	RA6T2
Voltage monitor 0 reset	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF) • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF) • Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • SRAM ECC Error Reset Detect Flag (RSTSR1.REERF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • TrustZone Error Reset Detect Flag (RSTSR1.TZERF) • Cache Parity Error Reset Detect Flag (RSTSR1.CPERF) • Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)
Voltage monitor 1 reset	• No flags are to be initialized.	• No flags are to be initialized.
Voltage monitor 2 reset	• No flags are to be initialized.	• No flags are to be initialized.
SRAM parity error reset	• No flags are to be initialized.	• No flags are to be initialized.
SRAM ECC error reset	—	• No flags are to be initialized.
Bus master MPU error reset	• No flags are to be initialized.	• No flags are to be initialized.
Bus slave MPU error reset	• No flags are to be initialized.	—
Stack Pointer error reset	• No flags are to be initialized.	—
TrustZone error reset	—	• No flags are to be initialized.
Cache parity error reset	—	• No flags are to be initialized.

Item	RA6T1	RA6T2
Deep Software Standby reset (DEEPCUT[0] = 0)	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Software Reset Detect Flag (RSTSR1.SWRF) • SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • SRAM ECC Error Reset Detect Flag (RSTSR1.REERF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • TrustZone Error Reset Detect Flag (RSTSR1.TZERF) • Cache Parity Error Reset Detect Flag (RSTSR1.CPERF)
Deep Software Standby reset (DEEPCUT[0] = 1)	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Software Reset Detect Flag (RSTSR1.SWRF)	• Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF) • Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF) • Software Reset Detect Flag (RSTSR1.SWRF)
	• SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	• SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF) • SRAM ECC Error Reset Detect Flag (RSTSR1.REERF) • Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF) • TrustZone Error Reset Detect Flag (RSTSR1.TZERF) • Cache Parity Error Reset Detect Flag (RSTSR1.CPERF)
Software reset	• No flags are to be initialized.	• No flags are to be initialized.

Item	RA6T1	RA6T2
RES pin reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, and LVD1CR1/LVD1SR) • Voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, and LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • MPU register • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, and LVD1CR1/LVD1SR) • Voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, and LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register, BUS_ERROR_STATUS register)*4 • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Power-on reset		• Independent watchdog timer registers (IWDTRR, IWDTSR)
	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR)
	• Voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, LVD1CR1/LVD1SR)	• Voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, LVD1CR1/LVD1SR)
	• Voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, LVD2CR1/LVD2SR)	• Voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, LVD2CR1/LVD2SR)
	• SOSC register (SOSCCR)	
	• LOCO registers (LOCOCR and LOCOUTCR)	• LOCO registers (LOCOCR and LOCOUTCR)
	• MOSC register (MOMCR)	• MOSC register (MOMCR)
	• AGT register	
	• MPU register	• Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS registers and BUS_ERROR_STATUS registers)*4
	• Pin state (except XCIN/XCOUT pin)	• Pin state
	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2)	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2, and SYOCDCR)
		• Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, and MSSAR, TZFSAR)
	• Registers other than those shown*1, CPU, and internal state	• Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Independent watchdog timer reset	• Watchdog time registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, and LVD1CR1/LVD1SR) • Voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, and LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • MPU register • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, and LVD1CR1/LVD1SR) • Voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, and LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS registers, and BUS_ERROR_STATUS registers)*4 • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Watchdog timer reset		• Independent watchdog timer registers (IWDTRR and IWDTSR)
	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)
	• Voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, and LVD1CR1/LVD1SR)	• Voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, and LVD1CR1/LVD1SR)
	• Voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, and LVD2CR1/LVD2SR)	• Voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, and LVD2CR1/LVD2SR)
	• LOCO register (LOCOCR)	• LOCO register (LOCOCR)
	• MOSC register (MOMCR)	• MOSC register (MOMCR)
	• MPU register	• Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4
	• Pin state (except XCIN/XCOUT pin)	• Pin state
	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2)	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2)
		• Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR)
	• Registers other than those shown*1, CPU, and internal state	• Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Voltage monitor 0 reset		• Independent watchdog timer registers (IWDTRR, IWDTSR)
	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)
	• Voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, and LVD1CR1/LVD1SR)	• Voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, and LVD1CR1/LVD1SR)
	• Voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, and LVD2CR1/LVD2SR)	• Voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, and LVD2CR1/LVD2SR)
	• LOCO registers (LOCOCR and LOCOUTCR)	• LOCO registers (LOCOCR and LOCOUTCR)
	• MOSC register (MOMCR)	• MOSC register (MOMCR)
	• AGT register	
	• MPU register	• Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4
	• Pin state (except XCIN/XCOUT pin)	• Pin state
	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2)	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2)
		• Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR)
	• Registers other than those shown*1, CPU, and internal state	• Registers other than those shown*2, CPU, and internal state
Voltage monitor 1 reset		• Independent watchdog timer registers (IWDTRR and IWDTSR)
	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)
	• LOCO registers (LOCOCR and LOCOUTCR)	• LOCO registers (LOCOCR and LOCOUTCR)
	• MOSC register (MOMCR)	• MOSC register (MOMCR)
	• AGT register	
	• MPU register	• Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4
	• Pin state (except XCIN/XCOUT pin)	• Pin state

Item	RA6T1	RA6T2
Voltage monitor 1 reset	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, TZFSAR) • Registers other than those shown*2, CPU, and internal state
Voltage monitor 2 reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO registers (LOCOCR and LOCOUTCR) • MOSC register (MOMCR) • AGT register • MPU register • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO registers (LOCOCR and LOCOUTCR) • MOSC register (MOMCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4 • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
SRAM parity error reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • MPU register • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4 • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
SRAM ECC error reset	—	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4 • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state
Bus master MPU error reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Bus slave MPU error reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	—
Stack pointer error reset	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state (except XCIN/XCOUT pin) • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2) • Registers other than those shown*1, CPU, and internal state	—
TrustZone error reset	— —	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Cache parity error reset	—	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • LOCO register (LOCOCR) • MOSC register (MOMCR) • Pin state • Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2) • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state
Deep Software Standby reset (DEEPCUT[0] = 0)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 register (LVD1CR1/LVD1SR) • Voltage monitor function 2 register (LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • MPU register • Pin state (except XCIN/XCOUT pin)*3 • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR and IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 register (LVD1CR1/LVD1SR) • Voltage monitor function 2 register (LVD2CR1/LVD2SR) • LOCO register (LOCOCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4 • Pin state*3 • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Deep Software Standby reset (DEEPCUT[0] = 1)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 register (LVD1CR1/LVD1SR) • Voltage monitor function 2 register (LVD2CR1/LVD2SR) • LOCO registers (LOCOCR and LOCOUTCR) • AGT register • MPU register • Pin state (except XCIN/XCOUT pin)*3 • Registers other than those shown*1, CPU, and internal state	• Independent watchdog timer registers (IWDTRR, IWDTSR) • Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR) • Voltage monitor function 1 register (LVD1CR1/LVD1SR) • Voltage monitor function 2 register (LVD2CR1/LVD2SR) • LOCO registers (LOCOCR and LOCOUTCR) • Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4 • Pin state*3 • Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR) • Registers other than those shown*2, CPU, and internal state

Item	RA6T1	RA6T2
Software reset		• Independent watchdog timer registers (IWDTRR and IWDTSR)
	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)	• Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR)
	• LOCO register (LOCOCR)	• LOCO register (LOCOCR)
	• MOSC register (MOMCR)	• MOSC register (MOMCR)
	• MPU register	• Bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register)*4
	• Pin state (except XCIN/XCOUT pin)	• Pin state
	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2)	• Low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, and DPSIEGR0 to DPSIEGR2)
		• Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR)
	• Registers other than those shown*1, CPU, and internal state	• Registers other than those shown*2, CPU, and internal state

Note 1. Registers other than the following registers: Watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR), voltage monitor function 1 registers (LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL, and LVD1CR1/LVD1SR), voltage monitor function 2 registers (LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL, and LVD2CR1/LVD2SR), SOSC registers (SOSCCR and SOMCR), LOCO registers (LOCOCR and LOCOUTCR), MOSC register (MOMCR), AGT register, MPU register, pin state (except XCIN/XCOUT pin), pin state (XCIN/XCOUT pin), and low-power function registers (DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, and DPSIEGR0 to DPSIEGR2)

Note 2. Registers other than the following registers: Independent watchdog timer registers (IWDTRR and IWDTSR), watchdog timer registers (WDTRR, WDTCR, WDTSR, WDTRCR, and WDTCSTPR), voltage monitor function 1 registers (LVD1CR0, LVD1CMPCR, and LVD1CR1/LVD1SR), voltage monitor function 2 registers (LVD2CR0, LVD2CMPCR, and LVD2CR1/LVD2SR), LOCO registers (LOCOCR and LOCOUTCR), MOSC register (MOMCR), bus, MPU, and TrustZone error registers (BUS_ERROR_ADDRESS register and BUS_ERROR_STATUS register), pin state, low-power function registers (DPSBYCR, DPSIER0 to DPSIER2, DPSIFR0 to DPSIFR2, DPSIEGR0 to DPSIEGR2, and SYOCDCR), Security Attribute Registers (CPUDSAR, RSTSAR, LVDSAR, CGFSAR, LPMSAR, DPFSAR, ICUSARx, BUSSARA, BUSSARB, CSAR, MMPUSARA, MMPUSARB, DMACSAR, DTCSAR, ELCSARA, ELCSARB, PmSAR, SRAMSAR, STBRAMSAR, FSAR, PSARB, PSARC, PSARD, PSARE, MSSAR, and TZFSAR)

Note 3. This depends on the setting of DPSBYCR.IOKEEP.

Note 4. Some control bits are not initialized by any types of reset.

Table 5. Comparison of Clock States when a Reset Occurs

Item		RA6T1	RA6T2
SOSC	Enable or disable	• POR Initialized to enable • Others Continue with the state that was selected before the reset occurred.	—
	Drive capability	• Continue with the state that was selected before the reset occurred	—
LOCO	Enable or disable	• Initialized to enable	• Initialized to enable
	Oscillation accuracy	• POR, LVD0, LVD1, LVD2, or Deep Software Standby (DEEPCUT[0] = 1): • Initialized to accuracy before trimming by LOCOUTCR (accuracy: ±15%) • Others Continue with the accuracy that was trimmed by LOCOUTCR	• POR, LVD0, LVD1, LVD2, or Deep Software Standby (DEEPCUT[0] = 1): Initialized to accuracy before trimming by power-on (accuracy: ±10%) • Others Continue with the accuracy that was trimmed by LOCOUTCR

2.4 Option-Setting Memory

Figure 2 shows a comparison of option-setting memory areas, and Table 6 shows a comparison of programming conditions of the option-setting memory area.

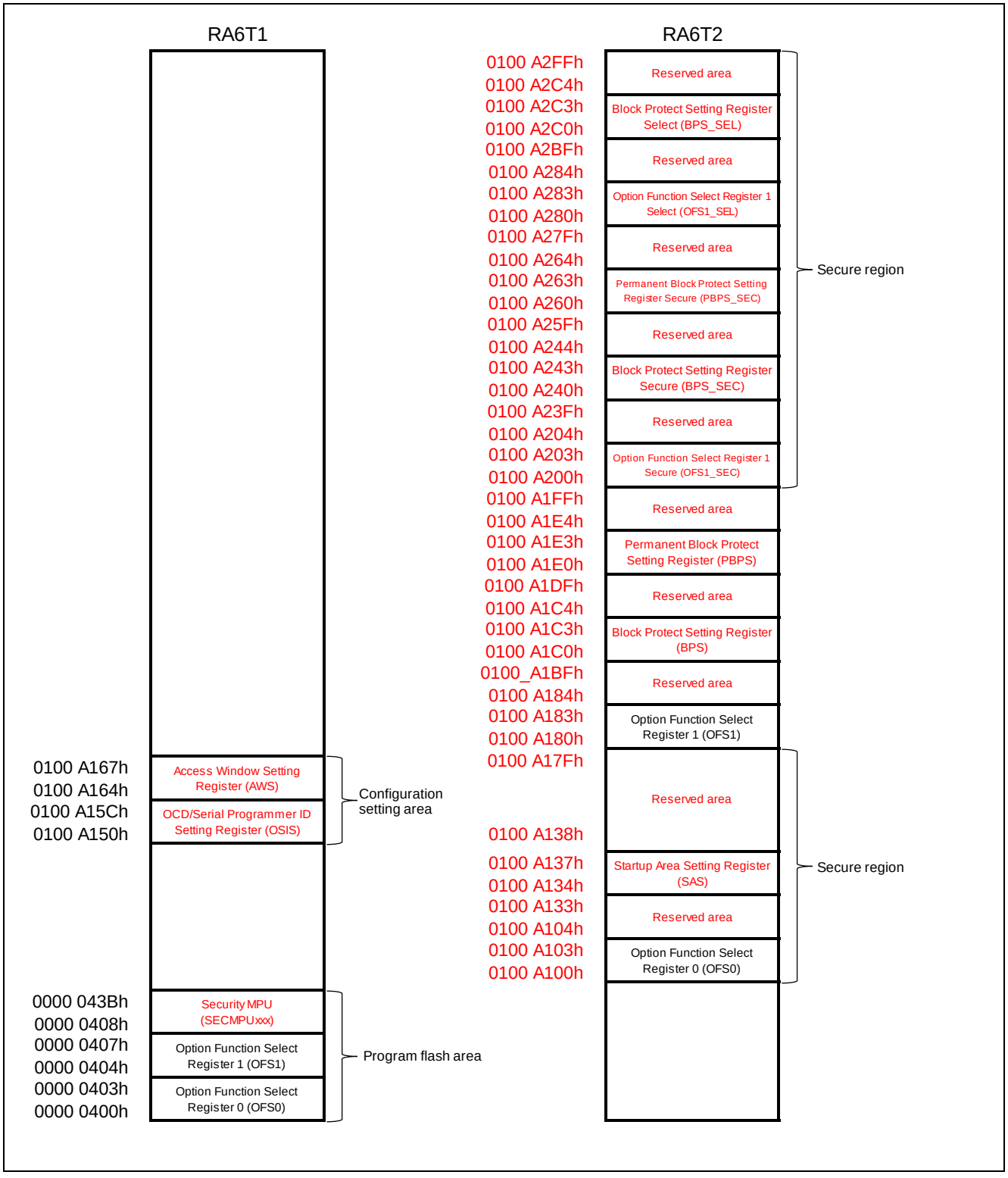


Figure 2. Comparison of Option-setting Memory Areas

Table 6. Comparison of Programming Conditions of the Option-setting Memory Area

Item		RA6T1	RA6T2
Self-programming	Secure region	—	Programming commands issued by secure access
	Other region	—	Programming commands issued by secure or non-secure access
Serial programming	Secure region	—	Programming commands issued when the device life cycle is SSD
	Other region	—	Programming commands issued when the device life cycle is SSD or NSECSD
Programming by the on-chip debugger	Secure region	—	Programming commands issued when the debug level is DBG2
	Other region	—	Programming commands issued when the debug level is DBG2 or DBG1

2.5 Low Voltage Detection

Table 7 to Table 9 provide comparative overviews of Low Voltage Detection.

Table 7. Comparative Overview of Low Voltage Detection (voltage monitor 0)

Item		RA6T1 (LVD)	RA6T2 (LVD)
Means for setting up operation		OFS1 register	OFS1 register
Target for monitoring		VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det0}	V_{det0}
Detected event		Voltage falls past V_{det0}.	Voltage falls past V_{det0}.
Detection voltage		Selectable from three different levels in the OFS1.VDSEL0[1:0] bits	Selectable from 3 different levels in the OFS1.VDSEL[1:0] bits
Monitoring flag		None	None
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 0 reset
		Reset when V_{det0} > VCC The CPU restarts after the specified time with VCC > V_{det0}.	Reset when V_{det0} > VCC The CPU restarts after the specified time with VCC > V_{det0}.
	Interrupt	No interrupt	No interrupt
Digital filter	Switching between enable and disable	No digital filter function	No digital filter function
	Sampling time	—	—
Event link function		None	None
TrustZone Filter		—	—

Table 8. Comparative Overview of Low Voltage Detection (voltage monitor 1)

Item		RA6T1 (LVD)	RA6T2 (LVD)
Means for setting up operation		LVD registers	LVD registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det1}	V_{det1}
Detected event		Voltage rises or falls past V_{det1}.	Voltage rises or falls past V_{det1}.
Detection voltage		Selectable from three different levels in the LVDLVLR.LVD1LVL[4:0] bit	Selectable from 3 different levels in the LVD1CMPCR.LVD1LVL[4:0] bits
Monitoring flag		LVD1SR.MON flag: Monitors whether the voltage is higher or lower than V_{det1}	LVD1SR.MON flag: Monitors whether the voltage is higher or lower than V_{det1}
		LVD1SR.DET flag: V_{det1} passage detection	LVD1SR.DET flag: V_{det1} passage detection
Process on voltage detection	Reset	Voltage monitor 1 reset	Voltage monitor 1 reset
		Reset when V_{det1} > VCC CPU restart timing selectable: After the specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det1} > VCC CPU restart timing selectable: After the specified time with VCC > V_{det1} or V_{det1} > VCC
	Interrupt	Voltage monitor 1 interrupt	Voltage monitor 1 interrupt
		Non-maskable or maskable interrupt is selectable.	Non-maskable or maskable interrupt is selectable.
		Interrupt request issued when V_{det1} > VCC or VCC > V_{det1}	Interrupt request issued when V_{det1} > VCC and VCC > V_{det1}, or either
Digital filter	Switching between enable and disable	Available	Available
	Sampling time	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)
Event link function		Available. Output of event signals on detection of V_{det1} crossings	Available. Output of event signals on detection of V_{det1} crossings
TrustZone Filter		—	The security attribution can be set for each register.

Table 9. Comparative Overview of Low Voltage Detection (voltage monitor 2)

Item		RA6T1 (LVD)	RA6T2 (LVD)
Means for setting up operation		LVD registers	LVD registers
Target for monitoring		VCC pin input voltage	VCC pin input voltage
Monitored voltage		V_{det2}	V_{det2}
Detected event		Voltage rises or falls past V_{det2}.	Voltage rises or falls past V_{det2}.
Detection voltage		Selectable from three different levels in the LVDLVLR.LVD2LVL[2:0] bit	Selectable from 3 different levels in the LVD2CMPCR.LVD2LVL[2:0] bits
Monitoring flag		LVD2SR.MON flag: Monitors whether the voltage is higher or lower than V_{det2}	LVD2SR.MON flag: Monitors whether the voltage is higher or lower than V_{det2}
		LVD2SR.DET flag: V_{det2} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 2 reset	Voltage monitor 2 reset
		Reset when V_{det2} > VCC CPU restart timing selectable: After the specified time with VCC > V_{det2} or V_{det2} VCC	Reset when V_{det2} > VCC CPU restart timing selectable: After the specified time with either VCC > V_{det2} or V_{det2} > VCC
	Interrupt	Voltage monitor 2 interrupt	Voltage monitor 2 interrupt
		Non-maskable or maskable interrupt is selectable.	Non-maskable or maskable interrupt is selectable.
		Interrupt request issued when V_{det2} > VCC or VCC > V_{det2}	Interrupt request issued when V_{det2} > VCC and VCC > V_{det2}, or either
Digital filter	Switching between enable and disable	Available	Available
	Sampling time	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)	1/n LOCO frequency x 2 (n: 2, 4, 8, 16)
Event link function		Available. Output of event signals on detection of V_{det2} crossings	Available. Output of event signals on detection of V_{det2} crossings
TrustZone Filter		—	The security attribution can be set for each register.

2.6 Clock Generation Circuits

Table 10 shows a comparative overview of clock and generation circuits (clock sources), and Table 11 shows a comparative overview of clock generation circuits (internal clocks).

Table 10. Comparative Overview of Clock Generation Circuits (clock sources)

Item		RA6T1	RA6T2
Main clock oscillator (MOSC)	Resonator frequency	8 MHz to 24 MHz	8 MHz to 24 MHz
	External clock input frequency	Up to 24 MHz	Up to 24 MHz
	External resonator or additional circuit	Ceramic resonator, crystal	Ceramic resonator, crystal
	Connection pins	EXTAL, XTAL	EXTAL, XTAL
	Drive capability switching	Available	Available
	Oscillation stop detection function	Available	Available

Item		RA6T1	RA6T2
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz	—
	External resonator or additional circuit	Crystal	—
	Connection pins	XCIN, XCOUT	—
	Drive capability switching	Available	—
PLL circuit	Input clock source	MOSC, HOCO	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3	Selectable from 1, 2, and 3
	Input frequency	8 MHz to 24 MHz	8 MHz to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps)	Selectable from 10 to 30 (0.5 steps)
	PLL output frequency	120 MHz to 240 MHz	120 MHz to 240 MHz
PLL2 circuit	Input clock source	—	MOSC, HOCO
	Input pulse frequency division ratio	—	Selectable from 1, 2, and 3
	Input frequency	—	8 MHz to 24 MHz
	Frequency multiplication ratio	—	Selectable from 10 to 30 (0.5 steps)
	PLL output frequency	—	120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16/18/20 MHz	16/18/20 MHz
	User trimming	Available	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz	8 MHz
	User trimming	Available	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz	32.768 kHz
	User trimming	Available	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz	15 kHz
External clock input for JTAG (TCK)	Input clock frequency	Up to 25 MHz	Up to 25 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz	Up to 25 MHz

Table 11. Comparative Overview of Clock Generation Circuits (internal clocks)

Item		RA6T1*1,*3	RA6T2*2,*4
System clock (ICLK)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	CPU, DTC, DMAC, Flash, SRAM	CPU, DTC, DMAC, Flash, RAM, I/O ports, TFU, IIRFA
	Oscillation frequency	Up to 120 MHz	Up to 240 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
Peripheral module clock A (PCLKA)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	Peripheral modules (SPI, SCI, SCE7, CRC, IrDA, and GPT bus clock)	Peripheral modules (SCI, CANFD-RAM, CNECC, SPI, CRC, DOC, ADC, DAC12, SCE5, GPT bus clock, PDG, and IIC)
	Oscillation frequency	Up to 120 MHz	Up to 120 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
Peripheral module clock B (PCLKB)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	Peripheral modules (IIC, DOC, CAC, CAN, DAC12, POEG, AGT, ELC, I/O ports, WDT, IWDT, ADC12, KINT, ACMPHS, and TSN)	Peripheral modules (CAC, ELC, POEG, WDT, IWDT, AGT, CANFD, TSN, Standby SRAM, KINT, and ACMPHS)
	Oscillation frequency	Up to 60 MHz	Up to 60 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
Peripheral module clock C (PCLKC)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	Peripheral module (ADC12 conversion clock)	Peripheral module (ADC)
	Oscillation frequency	Up to 60 MHz	Up to 60 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
Peripheral module clock D (PCLKD)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	Peripheral module (GPT count clock)	Peripheral modules (GPT)
	Oscillation frequency	Up to 120 MHz	Up to 120 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
Flash interface clock (FCLK)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	Flash interface	FlashIF
	Oscillation frequency	4 to 60 MHz (P/E) Up to 60 MHz (read)	4 MHz to 60 MHz (P/E) Up to 60 MHz (read)
	Division ratio	1, 2, 4, 8, 16, 32, 64	1/2/4/8/16/32/64
CANFD clock (CANFDCLK)	Clock source	—	PLL/PLL2
	Clock supply	—	CAN-FD
	Oscillation frequency	—	Up to 40 MHz
	Division ratio	—	1/2/4/6/8
CAN clock (CANMCLK)	Clock source	MOSC	MOSC
	Clock supply	CAN	CAN-FD
	Oscillation frequency	8 to 24 MHz	8 MHz to 24 MHz
Peripheral module asynchronous	Clock source	—	MOSC/HOCO/MOCO/LOCO/PLL/PLL2

Item		RA6T1*1,*3	RA6T2*2,*4
clock for GPT (GPTCLK)	Clock supply	—	GPT
	Oscillation frequency	—	Up to 200 MHz
	Division ratio	—	1/2/4/6/8
Peripheral module asynchronous clock for IIC (IICCLK)	Clock source	—	MOSC/HOCO/MOCO/LOCO/PLL/PLL2
	Clock supply	—	IIC
	Oscillation frequency	—	Up to 200 MHz
	Division ratio	—	1/2/4/6/8
Peripheral module asynchronous clock for SCI/SPI (SCISPICLK)	Clock source	—	MOSC/HOCO/MOCO/LOCO/PLL/PLL2
	Clock supply	—	SCI, SPI
	Oscillation frequency	—	Up to 120 MHz
	Division ratio	—	1/2/4/6/8
AGT clock (AGTSCLK, AGTLCLK)	Clock source	SOSC, LOCO	LOCO
	Clock supply	AGT	AGT
	Oscillation frequency	32.768 kHz	32.768 kHz
CAC main clock (CACMCLK)	Clock source	MOSC	MOSC
	Clock supply	CAC	CAC
	Oscillation frequency	Up to 24 MHz	Up to 24 MHz
CAC sub-clock (CACSCLK)	Clock source	SOSC	—
	Clock supply	CAC	—
	Oscillation frequency	32.768 kHz	—
CAC LOCO clock (CACLCLK)	Clock source	LOCO	LOCO
	Clock supply	CAC	CAC
	Oscillation frequency	32.768 kHz	32.768 kHz
CAC MOCO clock (CACMOCLK)	Clock source	MOCO	MOCO
	Clock supply	CAC	CAC
	Oscillation frequency	8 MHz	8 MHz
CAC HOCO clock (CACHCLK)	Clock source	HOCO	HOCO
	Clock supply	CAC	CAC
	Oscillation frequency	16, 18, 20 MHz	16/18/20 MHz
CAC IWDTLOCO clock (CACILCLK)	Clock source	IWDTLOCO	IWDTLOCO
	Clock supply	CAC	CAC
	Oscillation frequency	15 kHz	15 kHz
IWDT clock (IWDTCLK)	Clock source	IWDTLOCO	IWDTLOCO
	Clock supply	IWDT	IWDT
	Oscillation frequency	15 kHz	15 kHz
SysTick timer clock (SYSTICCLK)	Clock source	LOCO	LOCO
	Clock supply	SysTick timer	SysTick timer
	Oscillation frequency	32.768 kHz	32.768 kHz
JTAG clock (JTAGTCK)	Clock source	TCK pin	TCK pin
	Clock supply	JTAG	JTAG
	Oscillation frequency	Up to 25 MHz	Up to 25 MHz
Clock and buzzer output (CLKOUT)	Clock source	MOSC, SOSC, LOCO, MOCO, HOCO	MOSC/LOCO/MOCO/HOCO
	Clock supply	CLKOUT pin	CLKOUT pin
	Oscillation frequency	Up to 24 MHz	Up to 24 MHz
	Division ratio	1, 2, 4, 8, 16, 32, 64, 128	1/2/4/8/16/32/64/128
Serial wire clock (SWCLK)	Clock source	SWCLK pin	SWCLK
	Clock supply	OCD	OCD
	Oscillation frequency	Up to 25 MHz	Up to 25 MHz

Item		RA6T1*1,*3	RA6T2*2,*4
Trace clock (TRCLK)	Clock source	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	MOSC/HOCO/MOCO/LOCO/PLL
	Clock supply	CPU-OCD	CPU-OCD
	Oscillation frequency	Up to 60 MHz	Up to 120 MHz
	Division ratio	1, 2, 4	1, 2, 4
TCLK pin output (TCLK)	Clock source	1/2 TRCLK	1/2 TRCLK
	Clock supply	TCLK pin	TCLK pin
	Oscillation frequency	Up to 30 MHz	Up to 60 MHz

Note 1. Restrictions on setting the clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
Restrictions on the clock frequency ratio (N: integer of up to 64): ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N

If the A/D converter is enabled, the clock frequency ratio is constrained as follows:

PCLKB:PCLKC = 1:1, 1:2, 1:4, 2:1, 4:1, or 8:1

Note 2. Restrictions on setting the clock frequency: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB, GPTCLK ≥ PCLKA, ICLK ≥ FCLK
Restrictions on the clock frequency ratio: (N: integer of up to 64):

ICLK:FCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1, ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N, ICLK:TRCLK = N:1 or 1:N

If the CANFD is used, the clock frequency ratio is constrained to be PCLKA:PCLKB = 2:1.

Note 3. If the PLL reference clock source is HOCO, the PLL multiplication setting must be set to 120 MHz - 240 MHz in consideration of the HOCO frequency (minimum/maximum).

Note 4. The multiplication of PLL and PLL2 should be set to be within the output frequency range of PLL and PLL2, taking the frequency of HOCO into consideration. The division of PLL and PLL2 input should also be set to be within the input frequency range of PLL and PLL2, taking the frequency of HOCO into consideration.

2.7 Clock Frequency Accuracy Measurement Circuits

Table 12 shows a comparative overview of clock frequency accuracy measurement circuits.

Table 12. Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RA6T1 (CAC)	RA6T2 (CAC)
Measurement target clock	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).	Frequency can be measured for: • Main clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDT-dedicated clock • Peripheral module clock B (PCLKB).
Measurement reference clock	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB).	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDT-dedicated clock • Peripheral module clock B (PCLKB).
Selectable function	Digital filter	Digital filter
Interrupt source	• Measurement end • Frequency error • Overflow	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
TrustZone Filter	—	The security attribution can be set.

2.8 Low Power Modes

Table 13 shows a comparative overview of low power modes. Table 14 to Table 17 provide comparisons of operating conditions for each low power mode, and Table 18 to Table 20 provide comparisons of interrupt sources for canceling each low power mode.

Table 13. Comparative Overview of Low Power Modes

Item	RA6T1	RA6T2
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), and flash interface clock (FCLK).	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), and flash interface clock (FCLK).
Module stop	Peripheral module functions can be stopped independently.	Functions can be stopped independently for each peripheral module.
Lowe power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode
Power control mode	Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency and voltage. Three operating power control modes are available: • High-speed mode • Low-speed mode • Subosc-speed mode	• Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency. • The following two operating power control modes are available: High-speed mode Low-speed mode
TrustZone Filter	—	The security attribution can be set for each register.

Table 14. Comparison of Operating Conditions of Sleep Mode

Item	RA6T1	RA6T2
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 0
Canceling method	All interrupts. Any reset available in the mode	All interrupts. Any reset available in the mode
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state
Main clock oscillator	Selectable	Selectable
Sub-clock oscillator	Selectable	—
High-speed on-chip oscillator	Selectable	Selectable
Middle-speed on-chip oscillator	Selectable	Selectable
Low-speed on-chip oscillator	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1
PLL	Selectable	Selectable
PLL2	—	Selectable
Oscillation stop detection function	Selectable	Selectable
Clock/buzzer output function	Selectable	Selectable
CPU	Stop (Retained)	Stop (Retained)
RA6T1: SRAMHS RA6T2: SRAMn (n = 0)	Selectable	Selectable

Item	RA6T1	RA6T2
Standby SRAM	—	Selectable
Flash memory	Operating	Operating
DMA Controller (DMAC)	Selectable	Selectable
Data Transfer Controller (DTC)	Selectable	Selectable
Watchdog timer (WDT)	Selectable*1	Selectable*1
Independent watchdog timer (IWDT)	Selectable*1	Selectable*1
RA6T1: Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1) RA6T2: Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable
12-Bit A/D Converter RA6T1: (ADC12) RA6T2: (ADC)	Selectable	Selectable
Programmable Gain Amplifiers (PGAs)	Selectable*2	Selectable*3
12-Bit D/A Converter (DAC12)	Selectable	Selectable
Data Operation Circuit (DOC)	Selectable	Selectable
Serial Communications Interface (SCI0)	Selectable	Selectable
Serial Communications Interface RA6T1: (SCIn, n = 1 to 4, 8, 9) RA6T2: (SCIn, n = 1 to 4, 9)	Selectable	Selectable
I^2C Bus Interface (IIC0)	Selectable	Selectable
I^2C Bus Interface (IIC1)	Selectable	Selectable
Event Link Controller (ELC)	Selectable	Selectable
High-Speed Analog Comparator (ACMPHS0)	Selectable	Selectable
High-Speed Analog Comparator RA6T1: (ACMPHSn, n = 1 to 3, 4, 5) RA6T2: (ACMPHSn, n = 1 to 3)	Selectable	Selectable
IRQn pin interrupt RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Selectable	Selectable
NMI, IRQn-DS pin interrupt RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable
Power-on reset circuit	Operating	Operating
Other peripheral modules	Selectable	Selectable
I/O Ports	Operating	Operating

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in the Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in the Option Function Select Register 0 (OFS0) in WDT auto start mode.

Note 2. When using the Programmable Gain Amplifiers, MSTPDn (n = 15 or 16) must be set to 0.

Note 3. When using the Programmable Gain Amplifiers, MSTPD16 must be set to 0.

Table 15. Comparison of Operating Conditions of Software Standby Mode

Item	RA6T1	RA6T2
Transition condition	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0
Canceling method	Interrupts shown in Table 18. Any reset available in the mode	Interrupts shown in Table 18. Any reset available in the mode
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state
Main clock oscillator	Stop	Stop
Sub-clock oscillator	Selectable	—
High-speed on-chip oscillator	Stop	Stop
Middle-speed on-chip oscillator	Stop	Stop
Low-speed on-chip oscillator	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*1	Selectable*1
PLL	Stop	Stop
PLL2	—	Stop
Oscillation stop detection function	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable*2	Selectable*3
CPU	Stop (Retained)	Stop (Retained)
RA6T1: SRAMHS RA6T2: SRAMn (n = 0)	Stop (Retained)	Stop (Retained)
Standby SRAM	—	Stop (Retained)
Flash memory	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Stop (Retained)	Stop (Retained)
Data Transfer Controller (DTC)	Stop (Retained)	Stop (Retained)
Watchdog timer (WDT)	Stop (Retained)	Stop (Retained)
Independent watchdog timer (IWDT)	Selectable*1	Selectable*1
RA6T1: Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1) RA6T2: Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable*4	Selectable*5
12-Bit A/D Converter RA6T1: (ADC12) RA6T2: (ADC)	Stop (Retained)	Stop (Retained)
Programmable Gain Amplifiers (PGAs)	Selectable*6	Stop (Retained)
12-Bit D/A Converter (DAC12)	Stop (Retained)	Stop (Retained)
Data Operation Circuit (DOC)	Stop (Retained)	Stop (Retained)
Serial Communications Interface (SCI0)	Stop (Retained)	Stop (Retained)
Serial Communications Interface RA6T1: (SCIn, n = 1 to 4, 8, 9) RA6T2: (SCIn, n = 1 to 4, 9)	Stop (Retained)	Stop (Retained)
I^2C Bus Interface (IIC0)	Selectable*7	Selectable*7
I^2C Bus Interface (IIC1)	Stop (Retained)	Stop (Retained)
Event Link Controller (ELC)	Stop (Retained)	Stop (Retained)
High-Speed Analog Comparator (ACMPHS0)	Selectable*8	Stop (Retained)

Item	RA6T1	RA6T2
High-Speed Analog Comparator RA6T1: (ACMPHSn, n = 1 to 3, 4, 5) RA6T2: (ACMPHSn, n = 1 to 3)	Selectable*9	Stop (Retained)
IRQn pin interrupt RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Selectable	Selectable
NMI, IRQn-DS pin interrupt RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable
Power-on reset circuit	Operating	Operating
Other peripheral modules	Stop (Retained)	Stop (Retained)
I/O Ports	Retained*10	Retained

Note 1. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in the Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in the Option Function Select Register 0 (OFS0) in WDT auto start mode.

Note 2. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).

Note3. Stopped when the Clock Output Source Select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO).

Note 4. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK), or 101b (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

When 100b (AGTLCLK) is selected in AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must be set to 00b before entering Deep Software Standby mode.

Note 5. AGT0 operation is possible when 100b (AGTLCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK) or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

Note 6. When using the Programmable Gain Amplifiers, MSTPDn (n = 15 or 16) must be set to 0.

Note 7. IIC0 wakeup interrupt is available.

Note 8. When the CMPCTL.CSTEN bit is 1, canceling Software Standby Mode or entering Snooze mode by the comparator detection is possible.

Note 9. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter.

Note 10. For the address bus and bus control signals (for CSC: CS0, CS1, CS4 to CS7, RD, WR0, and ALE), keeping the output state or changing to the high-impedance state can be selected in the SBYCR.OPE bit.

Table 16. Comparison of Operating Conditions of Snooze Mode

Item	RA6T1	RA6T2
Transition condition	Snooze request trigger SNZCR.SNZE = 1 in Software Standby mode	Snooze request trigger SNZCR.SNZE = 1 in Software Standby mode
Canceling method	Interrupts shown in Table 19. Any reset available in the mode	Interrupts shown in Table 19. Any reset available in the mode
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)
State after cancellation by a reset	Reset state	Reset state
Main clock oscillator	Selectable*1	Selectable*2
Sub-clock oscillator	Selectable	—
High-speed on-chip oscillator	Selectable	Selectable
Middle-speed on-chip oscillator	Selectable	Selectable
Low-speed on-chip oscillator	Selectable	Selectable
IWDT-dedicated on-chip oscillator	Selectable*3	Selectable*3
PLL	Selectable*1	Selectable*2
PLL2	—	Selectable*2
Oscillation stop detection function	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable
CPU	Stop (Retained)	Stop (Retained)
RA6T1: SRAMHS RA6T2: SRAMn (n = 0)	Selectable	Selectable
Standby SRAM	—	Selectable
Flash memory	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Operation prohibited	Operation prohibited
Data Transfer Controller (DTC)	Selectable	Selectable
Watchdog timer (WDT)	Stop (Retained)	Stop (Retained)
Independent watchdog timer (IWDT)	Selectable*3	Selectable*3
RA6T1: Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1) RA6T2: Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable*4	Selectable*5
12-Bit A/D Converter RA6T1: (ADC12) RA6T2: (ADC)	Selectable*6	Selectable*7
Programmable Gain Amplifiers (PGAs)	Selectable*8	Selectable*9
12-Bit D/A Converter (DAC12)	Selectable	Selectable
Data Operation Circuit (DOC)	Selectable	Selectable
Serial Communications Interface (SCI0)	Selectable (RXD0 falling edge can be used to transition to snooze mode) (only in asynchronous mode)*10	Selectable (RXD0 falling edge can be used to transition to snooze mode) (only in asynchronous mode)*10
Serial Communications Interface RA6T1: (SCIn, n = 1 to 4, 8, 9) RA6T2: (SCIn, n = 1 to 4, 9)	Operation prohibited	Operation prohibited
I^2C Bus Interface (IIC0)	Selectable*11	Selectable Only wakeup interrupt is available*11
I^2C Bus Interface (IIC1)	Operation prohibited	Operation prohibited

Item	RA6T1	RA6T2
Event Link Controller (ELC)	Selectable*12	Selectable*12
High-Speed Analog Comparator (ACMPHS0)	Selectable VCOUT function only*13	Selectable VCOUT function only*14
High-Speed Analog Comparator RA6T1: (ACMPHSn, n = 1 to 3, 4, 5) RA6T2: (ACMPHSn, n = 1 to 3)	Selectable VCOUT function only*14	Selectable VCOUT function only*14
IRQn pin interrupt RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Selectable	Selectable
NMI, IRQn-DS pin interrupt RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable
Low voltage detection (LVD)	Selectable	Selectable
Power-on reset circuit	Operating	Operating
Other peripheral modules	Operation prohibited	Operation prohibited
I/O Ports	Operating	Operating

Note 1. When using SCI0 in Snooze mode, MOSCCR.MOSTP and PLLCR.PLLSTP bits must be 1.

Note 2. When using SCI0 in Snooze mode, MOSCCR.MOSTP, PLLCR.PLLSTP, and PLL2CR.PLL2STP bits must be 1.

Note 3. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in the Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in the Option Function Select Register 0 (OFS0) in WDT auto start mode.

Note 4. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when100b (AGTLCLK), 110b (AGTSCLK), or 101b (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

When 100b (AGTLCLK) is selected in AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must be set to 00b before entering Deep Software Standby mode.

Note 5. AGT0 operation is possible when 100b (AGTLCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK) or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

Note 6. When using the 12-Bit A/D Converter in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits must be 1.

Note 7. When using the 12-Bit A/D Converter in Snooze mode, the ADCMPENR.CMPENn bits must be set to 1.

Note 8. When using the Programmable Gain Amplifiers, MSTPDn (n = 15 or 16) must be set to 0.

Note 9. When using the Programmable Gain Amplifiers, MSTPD16 must be set to 0.

Note 10. Serial communication mode of SCI0 is asynchronous mode.

Note 11. IIC0 wakeup interrupt is available.

Note 12. Available events are restricted.

Note 13. When the CMPCTL0.CSTEN bit is 1, canceling Software Standby Mode or entering Snooze mode by the comparator detection is possible.

Note 14. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter.

Table 17. Comparison of Operating Conditions of Deep Software Standby Mode

Item	RA6T1	RA6T2
Transition condition	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	Interrupts shown in Table 20. Any reset available in the mode	Interrupts shown in Table 20. Any reset available in the mode
State after cancellation by an interrupt	Reset state	Reset state
State after cancellation by a reset	Reset state	Reset state
Main clock oscillator	Stop	Stop
Sub-clock oscillator	Selectable	—
High-speed on-chip oscillator	Stop	Stop
Middle-speed on-chip oscillator	Stop	Stop
Low-speed on-chip oscillator	Selectable*1	Selectable*1
IWDT-dedicated on-chip oscillator	Stop	Stop
PLL	Stop	Stop
PLL2	—	Stop
Oscillation stop detection function	Operation prohibited	Operation prohibited
Clock/buzzer output function	Stop (Undefined)	Stop (Undefined)
CPU	Stop (Undefined)	Stop (Undefined)
RA6T1: SRAMHS RA6T2: SRAMn (n = 0)	Stop (Undefined)	Stop (Undefined)
Standby SRAM	—	Stop (Retained or Undefined)*2
Flash memory	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Stop (Undefined)	Stop (Undefined)
Data Transfer Controller (DTC)	Stop (Undefined)	Stop (Undefined)
Watchdog timer (WDT)	Stop (Undefined)	Stop (Undefined)
Independent watchdog timer (IWDT)	Stop (Undefined)	Stop (Undefined)
RA6T1: Low Power Asynchronous General Purpose Timer (AGTn, n = 0, 1) RA6T2: Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable*3	Stop (Undefined)
12-Bit A/D Converter RA6T1: (ADC12) RA6T2: (ADC)	Stop (Undefined)	Stop (Undefined)
Programmable Gain Amplifiers (PGAs)	Stop (Undefined)	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Stop (Undefined)	Stop (Undefined)
Data Operation Circuit (DOC)	Stop (Undefined)	Stop (Undefined)
Serial Communications Interface (SCI0)	Stop (Undefined)	Stop (Undefined)
Serial Communications Interface RA6T1: (SCIn, n = 1 to 4, 8, 9) RA6T2: (SCIn, n = 1 to 4, 9)	Stop (Undefined)	Stop (Undefined)
I^2C Bus Interface (IIC0)	Stop (Undefined)	Stop (Undefined)
I^2C Bus Interface (IIC1)	Stop (Undefined)	Stop (Undefined)
Event Link Controller (ELC)	Stop (Undefined)	Stop (Undefined)
High-Speed Analog Comparator (ACMPHS0)	Stop (Undefined)	Stop (Undefined)
High-Speed Analog Comparator RA6T1: (ACMPHSn, n = 1 to 3, 4, 5) RA6T2: (ACMPHSn, n = 1 to 3)	Stop (Undefined)	Stop (Undefined)

Item	RA6T1	RA6T2
IRQn pin interrupt RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Stop (Undefined)	Stop (Undefined)
NMI, IRQn-DS pin interrupt RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Selectable	Selectable
Key Interrupt Function (KINT)	Stop (Undefined)	Stop (Undefined)
Low voltage detection (LVD)	Selectable*4	Selectable*4
Power-on reset circuit	Operating*5	Operating*5
Other peripheral modules	Stop (Undefined)	Stop (Undefined)
I/O Ports	Retained*6	Retained

Note 1. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode.
If the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.

Note 2. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. If the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is undefined in Deep Software Standby mode.

Note 3. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK), or 101b (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.

When 100b (AGTLCLK) is selected in AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must be set to 00b before entering Deep Software Standby mode.

Note 4. When using LVD in Deep Software Standby mode, the DPSBYCR.DEEPCUT[1:0] bits must be set to 00b or 01b before entering Deep Software Standby mode.

Note 5. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.

Note 6. For the address bus and bus control signals (for CSC: CS0, CS1, CS4 to CS7, RD, WR0, and ALE), keeping the output state or changing to the high-impedance state can be selected in the SBYCR.OPE bit.

Table 18. Comparison of Interrupt Sources for Canceling Software Standby Mode

Item		RA6T1	RA6T2
NMI		Yes	Yes
Port	PORT_IRQn RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Yes	Yes
	PORT_IRQn-DS RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes	Yes
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPHS	ACMP_HS0	Yes	—
IIC0	RA6T1: IIC0_WUI RA6T2: IIC0_WU	Yes	Yes
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	—
	ADC12n_WCMPUM	No	—
ADC	ADC_CCMPM0	—	No
	ADC_CCMPM1	—	No
SCI0	SCI0_AM	No	No
	SCI0_RXI_OR_ERI	No	—
DTC	DTC_COMPLETE	No	No
DOC	DOC_DOPCI	No	No

Table 19. Comparison of Interrupt Sources for Canceling Snooze Mode

Item		RA6T1	RA6T2
NMI		Yes	Yes
Port	PORT_IRQn RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	Yes	Yes
	PORT_IRQn-DS RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes
KINT	KEY_INTKR	Yes	Yes
AGT1	AGT1_AGTI	Yes*1	Yes*1
	AGT1_AGTCMAI	Yes	Yes
	AGT1_AGTCMBI	Yes	Yes
ACMPHS	ACMP_HS0	Yes	—
IIC0	RA6T1: IIC0_WUI RA6T2: IIC0_WU	Yes	Yes
ADC12n (n = 0, 1)	ADC12n_WCMPM	Yes with SELSR0*1	—
	ADC12n_WCMPUM	Yes with SELSR0*1	—

Item		RA6T1	RA6T2
ADC	ADC_CCMPM0	—	Yes with SELSR0*1
	ADC_CCMPM1	—	Yes with SELSR0*1
SCI0	SCI0_AM	Yes with SELSR0*2	Yes with SELSR0
	SCI0_RXI_OR_ERI	Yes with SELSR0*2	—
DTC	DTC_COMPLETE	Yes with SELSR0*1	Yes with SELSR0*1
DOC	DOC_DOPCI	Yes with SELSR0	Yes with SELSR0

Note 1. The event that is enabled by the SNZEDCR register must not be used.
Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be selected.

Table 20. Comparison of Interrupt Sources for Canceling Deep Software Standby Mode

Item		RA6T1	RA6T2
NMI		Yes	Yes
Port	PORT_IRQn RA6T1: (n = 0 to 13) RA6T2: (n = 0 to 13, 14, 15)	No	No
	PORT_IRQn-DS RA6T1: (n = 0, 1, 4 to 12) RA6T2: (n = 0, 1, 2, 3, 4 to 12, 13 to 15)	Yes	Yes
LVD	LVD_LVD1	Yes	Yes
	LVD_LVD2	Yes	Yes
IWDT	IWDT_NMIUNDF	No	No
KINT	KEY_INTKR	No	No
AGT1	AGT1_AGTI	Yes	No
	AGT1_AGTCMAI	No	No
	AGT1_AGTCMBI	No	No
ACMPHS	ACMP_HS0	No	—
IIC0	RA6T1: IIC0_WUI RA6T2: IIC0_WU	No	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	—
	ADC12n_WCMPUM	No	—
ADC	ADC_CCMPM0	—	No
	ADC_CCMPM1	—	No
SCI0	SCI0_AM	No	No
	SCI0_RXI_OR_ERI	No	—
DTC	DTC_COMPLETE	No	No
DOC	DOC_DOPCI	No	No

2.9 Register Write Protection

Table 21 shows a comparative overview of register write protection.

Table 21. Comparative Overview of Register Write Protection

Item	RA6T1	RA6T2
PRC0	• Registers related to the clock generation circuit SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, and FLLCR2	• Registers related to the clock generation circuit SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, OSTDCR, OSTDSR, PLL2CCR, PLL2CR, MOCOUTCR, HOCOUTCR, SCISPICKDIVCR, CANFDCKDIVCR, GPTCKDIVCR, IICCKDIVCR, SCISPICKCR, CANFDCKCR, GPTCKCR, IICCKCR, MOSCWTCR, MOMCR, LOCOCR, and LOCOUTCR
PRC1	• Registers related to the low power modes SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIER0 to 3, DPSIFR0 to 3, DPSIEGR0 to 2, SYOCDCR, and STCONR • Register related to the AGT function VBTICTLR	• Registers related to the low power modes SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIER0 to 2, DPSIFR0 to 2, DPSIEGR0 to 2, and SYOCDCR
PRC3	• Registers related to the LVD LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, and LVD2CR0	• Registers related to the LVD LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVD1CMPCR, LVD2CMPCR, LVD1CR0, and LVD2CR0
PRC4	—	• Registers related to the security function CGFSAR, RSTSAR, LPMSAR, LVDSAR, DPFSAR, CSAR, SRAMSAR, STBRAMSAR, DTCSAR, DMACSAR, ICUSARx, BUSSARx, MMPUSARx, TZFSAR, CPUDSAR, FSAR, PSARx, MSSAR, PmSAR, and ELCSARx

2.10 Interrupt Controller Unit

Table 22 shows a comparative overview of interrupt controller unit.

Table 22. Comparative Overview of Interrupt Controller Unit

Item		RA6T1 (ICU)	RA6T2 (ICU)
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 268 (select factors with event list numbers 64 to 511.)	• Interrupts from peripheral modules Number of sources: 265 (select factors with event list numbers 17 to 511)
	External pin interrupts	• Interrupt detection on low level, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter function supported • 14 sources, with interrupts from IRQ0 to IRQ13 pins	• Interrupt detection on low level, falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source. • Digital filter function supported • 16 sources, with interrupts from IRQi (i = 0 to 15) pins
	Interrupt requests to CPU (NVIC)	96 sources	• 96 interrupt requests are output to NVIC.
	DMAC control	The DTC and DMAC can be activated using interrupt sources.	• The DMAC can be activated using interrupt sources.

Item		RA6T1 (ICU)	RA6T2 (ICU)
			• The target interrupt source can be selected individually for every DMAC channels.
	DTC control		• The DTC can be activated using interrupt sources. • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported
	Oscillation stop detection interrupt	Interrupt on detecting that the main oscillator has stopped	Interrupt on detecting that the main oscillator has stopped
	WDT underflow/refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1	Voltage monitor interrupt of low voltage detection detector 1 (LVD1)	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	Low voltage detection 2	Voltage monitor interrupt of low voltage detection detector 2 (LVD2)	Voltage monitor 2 interrupt of the voltage monitor 2 circuit (LVD_LVD2)
	RPEST	Interrupt on SRAM parity error	Interrupt on SRAM parity error
	RECCST	—	Interrupt on SRAM ECC error
Non-maskable interrupts	TZFST	—	Interrupt on TrustZone Filter error
	CPEST	—	Interrupt on cache RAM parity error
	BUSSST	Interrupt on MPU bus slave error	—
	BUSMST	Interrupt on MPU bus master error	Interrupt on bus master MPU error
	SPEST	Interrupt on CPU stack pointer monitor	—
Low power mode		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software Standby mode: Return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register.	• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source. • Software Standby mode: Return is initiated by non-maskable interrupts. Interrupt can be selected in the WUPEN register.
		• Snooze mode: Return is initiated by non-maskable interrupts. Interrupts can be selected in the SELSR0 and WUPEN registers.	• Snooze mode: Return is initiated by non-maskable interrupts. Interrupts can be selected in the SELSR0 and WUPEN registers.
TrustZone Filter		—	Available

2.11 Buses

Table 23 shows a comparative overview of buses.

Table 23. Comparative Overview of Buses

Item		RA6T1	RA6T2
Main bus	ICode bus (CPU)	• Connected to the CPU • Connected to on-chip memory (code flash memory and SRAMHS)	—
	DCode bus (CPU)	• Connected to the CPU • Connected to on-chip memory (code flash memory and SRAMHS)	
	System bus (CPU)	• Connected to the CPU • Connected to the on-chip memory and internal peripheral buses	
	DMA bus	• Connected to the DMAC and DTC • Connected to the on-chip memory and internal peripheral buses	
Slave interface	Memory bus 1	• Connected to code flash memory	
	Memory bus 2	• Connected to SRAMHS	
	Memory bus 3	• Connected to code flash memory and SRAMHS through the DMA bus	
	Internal peripheral bus 1	• Connected to system control related to peripheral modules	
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O ports, POEG, WDT, IWDT, IIC, CAN, ADC12, DAC12, TSN, and DOC)	
	Internal peripheral bus 4	• Connected to peripheral modules (GPT, SCI, IrDA, SPI, and CRC)	
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, AGT, and ACMPHS)	
	Internal peripheral bus 7	• Connected to Secure IPs (SCE7)	
	Internal peripheral bus 9	• Connected to flash memory (in P/E), data flash memory, and TSN	
Bus master	Code bus (Cortex-M33)	—	• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to the CPU Instruction Cache for instructions and operands
	System bus (Cortex-M33)		• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to the CPU Data Cache for system
	DMAC/DTC		• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to the DMAC/DTC

Item		RA6T1	RA6T2
Bus slave	FHBIU	—	• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to Code Flash Memory and Configuration area
	FLBIU		• Bus I/F maximum frequency: 60 MHz • Sync clock: FCLK • Connected to Data Flash Memory and FACI
	S0BIU		• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to SRAM0 (Standby RAM)
	PSBIU		• Bus I/F maximum frequency: 240 MHz • Sync clock: ICLK • Connected to peripheral system modules (DTC, DMAC, ICU, Flash, MPU, SRAM, Debug/Trace module, System controller, and BUS controller) • Connected to peripheral modules (IIRFA, TFU, and IO ports)
	PLBIU		• Bus I/F maximum frequency: 60 MHz • Sync clock: PCLKB • Connected to peripheral modules (CAC, ELC, POEG, WDT, IWDT, AGT, CANFD, TSN, ACMPHS, and KINT)
	PHBIU		• Bus I/F maximum frequency: 120 MHz • Sync clock: PCLKA • Connected to peripheral modules (GPT, SCI, SPI, CRC, DOC, ADC, DAC12, CNECC, IIC, SCE5, and PDG)

Note: FHBIU: Flash High speed Bus Interface Unit

FLBIU: Flash Low speed Bus Interface Unit

S0BIU: SRAM0 Bus Interface Unit

PSBIU: Peripheral System Bus Interface Unit

PLBIU: Peripheral Low speed Bus Interface Unit

PHBIU: Peripheral High speed Bus Interface Unit

2.12 Memory Protection Units

Table 24 shows a comparative overview of memory protection units, and Table 25 shows a comparison of behavior on MPU error detection.

Table 24. Comparative Overview of Memory Protection Units

Item		RA6T1 (MPU)	RA6T2 (MPU)
Illegal memory access	RA6T1: Arm® Cortex®-M4 CPU RA6T2: Arm® Cortex®-M33 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs. • The MPU can change a default memory map.	• Arm® CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs. • The MPU can change a default memory map.
	CPU stack pointer monitor	2 regions • Main Stack Pointer (MSP) • Process Stack Pointer (PSP)	—
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with subregions and background region	Memory protection function for the CPU: • (8+8) region MPU with sub regions and background region for secure and non-secure
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 32 regions	Memory protection function for each master except for the CPU: • DMAC/DTC: 8 regions
	Bus slave MPU	Memory protection function for each bus slave	—
Security	Security MPU	Protect accesses from non-secure programs to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, and two security functions)	—

Table 25. Comparison of Behavior on MPU Error Detection

Item		RA6T1 (MPU)	RA6T2 (MPU)
CPU stack pointer monitor	Notification type	Reset or non-maskable interrupt	—
	Error response by HRESP signal of AHB I/F	—	
	Bus Access on error detection	Don't care	
	Storing of error access information	Not stored	
Arm MPU	Notification type	Hard fault	• Hard fault
	Error response by HRESP signal of AHB I/F	—	Not supported
	Bus Access on error detection	• Does not correctly have write access • Does not correctly have read access	• Does not correctly have write access • Does not correctly have read access
	Storing of error access information	Stored in the Cortex-M4 processor	Stored in the Cortex-M33 processor

Item		RA6T1 (MPU)	RA6T2 (MPU)
Bus master MPU	Notification type	Reset or non-maskable interrupts	• Reset or non-maskable interrupts • Hard fault
	Error response by HRESP signal of AHB I/F	—	Supported
	Bus Access on error detection	• Write access to the protected region • Read access to the protected region	• Write access is ignored. • Read access is read as 0.
	Storing of error access information	Stored	Stored
Bus slave MPU	Notification type	• Reset or non-maskable interrupts • Hard fault	—
	Error response by HRESP signal of AHB I/F	—	
	Bus Access on error detection	• Write access is ignored. • Read access is read as 0.	
	Storing of error access information	Stored	
Security MPU	Notification type	Not notified	—
	Error response by HRESP signal of AHB I/F	—	
	Bus Access on error detection	Does not correctly have write access	
	Storing of error access information	Does not correctly have read access Not stored	

2.13 DMA Controllers

Table 26 shows a comparative overview of DMA controllers.

Table 26. Comparative overview of DMA Controllers

Item	RA6T1 (DMAC)	RA6T2 (DMAC)
Number of channels	8 channels (DMACm, m = 0 to 7)	8 channels (DMACn (n = 0 to 7))
Transfer space	4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)	4 GB (0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas)
Maximum transfer volume	64 M data units (maximum number of transfers in block transfer mode: 1,024 data units x 65,536 blocks)	64 M data (maximum number of transfers in block transfer mode: 1,024 data/block x 65,536 blocks)
DMA activation source	Selectable for each channel: • Software trigger	Selectable for each channel: • Software trigger
	• Interrupt requests from peripheral modules or trigger from external interrupt input pins	• Interrupt requests from peripheral modules or trigger from external interrupt input pins
Channel priority	Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: Highest)	Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: Highest)

Item		RA6T1 (DMAC)	RA6T2 (DMAC)
Transfer data	Single data	Bit length: 8, 16, or 32 bits	Bit length: 8, 16, or 32 bits
	Block size	Number of data: 1 to 1,024	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Selectable free running mode (total number of data transfers is not specified)	• One data transfer by one DMA transfer request • Free-running function (setting in which total number of data transfers is not specified) selectable
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination. • Maximum settable repeat size: 1,024 • Selectable free-running function
	Repeat-block transfer mode	—	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 • Block transfer can be repeated. • Maximum settable repeat size: 64 K • Selectable free-running function
Transfer mode	Block transfer mode	• One data block transfer by one DMA transfer request • Maximum settable block size: 1,024 data	• One block data transfer by one DMA transfer request • Maximum settable block size: 1,024 data • Selectable free-running function
Selective functions	Extended repeat area function	• Allow data to be transferred by repeating the address values in the specified range, with the upper bit values in the transfer address register fixed • Area of 2 bytes to 128 Mbytes individually selectable as the extended repeat area for transfer source and destination.	• Function in which data can be transferred by repeating the address values in the specified range with the upper bit values in the transfer address register fixed. • Area of 2 bytes to 128 Mbytes can be separately set as the extended repeat area for transfer source and destination.
Processing on DMA transfer error		—	• When a DMAC transfer error occurs, the transfer on the channel that caused the error stops. • A request to clear the register for activation request of DMAC error channel is sent to ICU.

Item		RA6T1 (DMAC)	RA6T2 (DMAC)
Interrupt (DMACn_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified in the transfer counter	Generated on completion of transferring data volume specified in the transfer counter
	Transfer escape end interrupt	Generated when: • The repeat size of data transfer is complete • The source address of the extended repeat area overflows • The destination address of the extended repeat area overflows	• Generated when the repeat size of data transfer is completed • Generated when the source address of the extended repeat area overflows • Generated when the destination address of the extended repeat area overflows
Interrupt (DMA_TRANSERR)	Error response detection interrupt	—	Generated when a DMAC transfer error occurs
Event link activation (DMACn_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred).	An event link request is generated after each data transfer (for block transfer, after each block is transferred).
Master TrustZone Filter		—	TrustZone violation area of Flash or SRAM is detected before a non-secure channel accesses the bus.
Module-stop function		Module-stop state can be set to reduce power consumption.	Module-stop state can be set.
TrustZone Filter		—	The security attribution can be set for each channel.

2.14 Data Transfer Controller

Table 27 shows a Comparative overview of Data Transfer Controller.

Table 27. Comparative Overview of Data Transfer Controller

Item	RA6T1 (DTC)	RA6T2 (DTC)
Transfer mode	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 x 32 bits (1024 bytes). • Block transfer mode A single activation leads to a single block transfer. The maximum block size is 256 x 32 bits = 1024 bytes.	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 x 32 bits (1024 bytes). • Block transfer mode A single activation leads to a single block transfer. The maximum block size is 256 x 32 bits = 1024 bytes.

Item	RA6T1 (DTC)	RA6T2 (DTC)
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU). • Multiple data units can be transferred on a single activation source (chain transfer). • Chain transfers can be set to either execute when the counter is 0, or always execute.	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU). • Multiple data units can be transferred on a single activation source (chain transfer). • Chain transfers can be set to either execute when the counter is 0, or always execute.
Transfer space	• 4 GB (0000 0000h to FFFF FFFF, excluding reserved areas)	• 4 GB area from 0x0000_0000 to 0xFFFF_FFFF, excluding reserved areas
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), 1 word (32 bits) • Single block size: 1 to 256 data units
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after a data transfer of a specified volume.	• An interrupt request can be generated to the CPU on a DTC activation interrupt or DTC_COMPLETE interrupt. • An interrupt request can be generated to the CPU after a single data transfer. • An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Processing on DTC transfer error	—	• When a DTC transfer error occurs, the transfer that caused the error stops. • A request to clear the register is issued for the activation request of DTC error number to ICU.
Error response detection interrupt	—	Generated when a DTC transfer error occurs
Event link function	An event link request is generated after one data transfer (for block, after one block transfer).	An event link request is generated after one data transfer (for block, after one block transfer).
Read skip	Read of transfer information can be skipped.	Read of transfer information can be skipped.
Write-back skip	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped.	When the transfer source or destination address is specified as fixed, a write-back of transfer information can be skipped.
TrustZone	—	TrustZone violation area of Flash or SRAM is detected before a bus is accessed.
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
TrustZone filter	—	The security attribution can be set for each activation source.

2.15 Event Link Controllers

Table 28 shows a comparative overview of event link controllers.

Table 28. Comparative Overview of Event Link Controllers

Item	RA6T1 (ELC)	RA6T2 (ELC_B)
Event link function	229 types of event signals can be directly connected to modules. The ELC can generate an ELC event signal, and events that activate the DTC.	215 types of event signals can be directly connected to modules. The ELC generates an ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set.	Module-stop state can be set.
TrustZone Filter	—	The security attribution can be set for each register.

2.16 I/O Ports

Table 29 and Table 30 provide comparative overviews of I/O ports. Table 31 shows a comparison of I/O port functions.

Table 29. Comparative Overview of I/O Ports (100 pins)

Item	RA6T1		RA6T2	
	100 pins	Number of pins	100 pins	Number of pins
PORT0	P000 to P002, P003 to P008, P014, P015	11	P000 to P002	3
PORT1	P100 to P115	16	—	0
PORT2	P200, P201, P205 to P211, P212, P213, P214	12	P201, P212, P213	3
PORT3	P300 to P307	8	—	0
PORT4	P400 to P415	16	—	0
PORT5	P500 to P504, P508	6	—	0
PORT6	P600 to P602, P608 to P610	6	—	0
PORT7	P708	1	—	0
PORTA	—	0	PA00 to PA15	16
PORTB	—	0	PB00 to PB10, PB12 to PB15	15
PORTC	—	0	PC00 to PC15	16
PORTD	—	0	PD00 to PD15	16
PORTE	—	0	PE00 to PE06, PE08 to PE15	15

Table 30. Comparative Overview of I/O Ports (64 pins)

Item	RA6T1		RA6T2	
	64 pins	Number of pins	64 pins	Number of pins
PORT0	P000, P001, P002, P003, P014, P015	6	P002	1
PORT1	P100 to P112	13	—	0
PORT2	P200, P201, P205 to P207, P210, P212, P213	8	P201, P212, P213	3
PORT3	P300 to P302	3	—	0
PORT4	P400 to P402, P407 to P411	8	—	0
PORT5	P500, P501	2	—	0
PORT6	—	0	—	0
PORT7	—	0	—	0
PORTA	—	0	PA00 to PA15	16

Item	RA6T1		RA6T2	
	64 pins	Number of pins	64 pins	Number of pins
PORTB	—	0	PB00 to PB09, PB12 to PB15	14
PORTC	—	0	PC00 to PC15	16
PORTD	—	0	PD02	1
PORTE	—	0	—	0

Table 31. Comparison of I/O Port Functions

Item		RA6T1	RA6T2
Input pull-up	PORT0	P000, P001, P002 to P008, P014, P015	P000, P001
	PORT1	P100 to P115	—
	PORT2	P200, P201, P205 to P211, P212, P213, P214	P201, P212, P213
	PORT3	P300 to P307	—
	PORT4	P400 to P415	—
	PORT5	P500 to P504, P508	—
	PORT6	P600 to P602, P608 to P610	—
	PORT7	P708	—
	PORTA	—	PA06 to PA15
	PORTB	—	PB00, PB01, PB03 to PB010, PB12 to PB15
	PORTC	—	PC00 to PC15
	PORTD	—	PD00 to PD15
	PORTE	—	PE00 to PE06, PE08 to PE15
Open-drain output	PORT0	P008, P014, P015	—
	PORT1	P100 to P115	—
	PORT2	P201, P205 to P211, P212, P213, P214	P201, P212, P213
	PORT3	P300 to P307	—
	PORT4	P400 to P415	—
	PORT5	P500 to P504, P508	—
	PORT6	P600 to P602, P608 to P610	—
	PORT7	P708	—
	PORTA	—	PA08 to PA15
	PORTB	—	PB03 to PB10, PB12 to PB15
	PORTC	—	PC06 to PC12, PC14, PC15
	PORTD	—	PD00 to PD15
	PORTE	—	PE00 to PE06, PE08 to PE15

Item		RA6T1	RA6T2
Drive capability switching	PORT0	—	—
	PORT1	P100 to P115: Low, middle, high	—
	PORT2	P205 to P211, P212, P213, P214: Low, middle, high	P201: Low
			P212, P213: Low, middle, high
	PORT3	P300 to P307: Low, middle, high	—
	PORT4	P400 to P415: Low, middle, high	—
	PORT5	P500 to P504, P508: Low, middle, high	—
	PORT6	P600 to P602, P608 to P610: Low, middle, high	—
	PORT7	P708: Low, middle, high	—
	PORTA	—	PA08 to PA11: Low, middle, high, High current drive
			PA12 to PA15: Low, middle, high
	PORTB	—	PB03 to PB10: Low, middle, high
			PB12 to PB15: Low, middle, high, High current drive
	PORTC	—	PC06 to PC09: Low, middle, high, High current drive
			PC10 to PC12: Low, middle, high
			PC14, PC15: Low
Drive capability switching	PORTD	—	PD00 to PD07: Low, middle, high
			PD08 to PD15: Low, middle, high, High current drive
	PORTE	—	PE00, PE01: Low, middle, high
			PE02 to PE06: Low, middle, high, high-speed high-drive
			PE08, PE09: Low, middle, high
			PE10 to PE15: Low, middle, high, High current drive
5 V tolerant	PORT0	—	—
	PORT1	—	—
	PORT2	P205, P206	—
	PORT3	—	—
	PORT4	P400, P401, P407 to P415	—
	PORT5	—	—
	PORT6	—	—
	PORT7	P708	—
	PORTA	—	PA12 to PA15
	PORTB	—	PB03, PB05 to PB09
	PORTC	—	PC10 to PC12, PC14, PC15
	PORTD	—	PD00 to PD07
	PORTE	—	PE00, PE01

Item		RA6T1	RA6T2
I/O	PORT0	P000 to P002, P003 to P007: Input	P000 to P002: Input
		P008, P014, P015: Input/Output	
	PORT1	P100 to P115: Input/Output	—
	PORT2	P200: Input	P201, P212, P213: Input/Output
		P201, P205 to P211, P212, P213, P214: Input/Output	
	PORT3	P300 to P307: Input/Output	—
	PORT4	P400 to P415: Input/Output	—
	PORT5	P500 to P504, P508: Input/Output	—
	PORT6	P600 to P602, P608 to P610: Input/Output	—
	PORT7	P708: Input/Output	—
	PORTA	—	PA00 to PA07: Input
			PA08 to PA15: Input/Output
	PORTB	—	PB00 to PB02: Input
			PB03 to PB10, PB12 to PB15: Input/Output
	PORTC	—	PC00 to PC05: Input
			PC06 to PC12: Input/Output
			PC13: Input
			PC14, PC15: Input/Output
	PORTD	—	PD00 to PD15: Input/Output
	PORTE	—	PE00 to PE06, PE08 to PE15: Input/Output

2.17 Port Output Enable for GPT

Table 32 shows a comparative overview of port output enable for GPT.

Table 32. Comparative Overview of Port Output Enable for GPT

Item	RA6T1 (POEG)	RA6T2 (POEG)
Request of output stopping in response to input level detection	The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection.	• The request to stop output is issued to the GPT when a POEGGn.PIDF flag is set in response to the detection of input of the selected level on the corresponding GTETRGn pin (n = A to D). • The request to stop output is issued to the GPT immediately upon detection of input of the selected level on the corresponding GTETRGn pin.
Requests to stop output in the form of an output stopping signal from the GPT	• When the GTIOCA and the GTIOCB pins are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG. Through reception of these requests, the POEG can control whether the GTIOCA and GTIOCB pins are output-disabled. • GPT output pins can be disabled when the GPT output pins detect a dead time error.	• The request to stop output is issued to the GPT when the GPT detects the active level (high or low) on the GTIOCA and GTIOCB pins at the same time while the corresponding POEGGn.IOCF flag is set. • The request to stop output is issued to the GPT when the GPT detects a deadtime error while the corresponding POEGGn.IOCF flag is set.

Item	RA6T1 (POEG)	RA6T2 (POEG)
Requests to stop output in response to detection by a comparator	The GPT output pins can be disabled when an interrupt request is generated by a change in the output results of any of the comparators.	• The request to stop output is issued to the GPT when a POEGGn.IOCF flag is set in response to edge-detection by a comparator. • The request to stop output is issued directly to the GPT upon detecting level on a comparator.
Requests to stop output in response to detecting the stopping of oscillation	The GPT output pins can be disabled when oscillation of the clock generation circuit stops.	A request to stop output is issued to the GPT when the oscillation stop detection circuit for the main clock detects the stopping of oscillation while the corresponding POEGGn.OSTPF flag is set.
Requests by software to stop output	The GPT output pins can be disabled by modifying the register settings.	The request to stop output is issued to the GPT when the software sets the POEGGn.SSF flag.
Interrupt	• Allows output-disable control by the input level detection • Allows output-disable requests from the GPT or ACMPHS	• An interrupt is generated in response to the request to stop output in the form of the POEGGn.PIDF flag. • An interrupt is generated in response to the request to stop output in the form of the POEGGn.IOCF flag.
External trigger output to the GPT	The GTETRGn signals can be output to the GPT after polarity and filter selection.	The GTETRGn pin is used for output as external triggers.
Noise removal	• Three times sampling for every PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be set for any of the input pins GTETRGn. • Positive or negative polarity can be selected for any of the input pins GTETRGn. • Signal state after polarity and filter selection can be monitored.	• Each GTETRGn pin has a digital noise filter. • Four types of sampling clock are selectable for the filter.
TrustZone Filter	—	• The security attribution can be set for each group.

2.18 General PWM Timers

Table 33 shows a comparative overview of General PWM Timers, and Table 34 shows a Comparison of General PWM Timer Functions.

Table 33. Comparative Overview of General PWM Timers

Item	RA6T1 (GPT)	RA6T2 (GPT)
Functions	• 32 bits × 13 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation	• 32 bits x 10 channels (GPT32n (n = 0 to 9)) • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms. • Registers for setting up frame cycles in each channel with capability for generating interrupts at overflow or underflow • Generation of dead times in PWM operation
		• Generation of high accuracy duty in the vicinity of duty 0% and 100% PWM waveform • In output compare operation, the setting compare register is immediately used to generate PWM waveform with dead times.
	• Synchronous starting, stopping, and clearing counters for arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight ELC events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D converter start triggers can be generated.	• Synchronous starting, stopping, and clearing counters for arbitrary channels • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of eight ELC events • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to the status of two input pins • Count start, count stop, count clear, up-count, down-count, or input capture operation in response to a maximum of four external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D conversion start request generation function

Item	RA6T1 (GPT)	RA6T2 (GPT)
Functions	• PWM waveform for controlling brushless DC motors can be generated. • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC. • Enables the noise filter for input capture and input UVW • Bus clock: PCLKA • Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64).	• PWM waveform for controlling brushless DC motors can be generated. • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC. • Enables the noise filter for input capture and input UVW. • Period count function • External pulse width measuring function • Logical operation between the channel output • Synchronous counter clearing, counter setting, and input capture among channels • Bus clock: PCLKA, Core clock: GTCLK*1 • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64) (when using synchronous clock), PCLKA ≤ GTCLK (when using asynchronous clock)

Note 1. The GPT core clock (GTCLK) is PCLKD when synchronous clock is selected, and is GPTCLK when asynchronous clock is selected.

Table 34. Comparison of General PWM Timer Functions (GPT32EH and GPT32E)

Item	RA6T1	RA6T2
Count clock	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024	GTCLK GTCLK/2 GTCLK/4 GTCLK/8 GTCLK/16 GTCLK/32 GTCLK/64 GTCLK/128 GTCLK/256 GTCLK/512 GTCLK/1024 GTETRGA, GTETRGB, GTETRGC, GTETRGD
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR	GTPR
Cycle setting buffer registers	GTPBR GTPDBR*1	GTPBR GTPDBR
I/O pins	GTIOCA GTIOCB	GTIOCnA GTIOCnB (n = 0 to 9)
External trigger input pins	GTETRGA*2 GTETRGB*2 GTETRGC*2 GTETRGD*2	GTETRGA*3 GTETRGB*3 GTETRGC*3 GTETRGD*3

Item		RA6T1	RA6T2
Counter clear sources		GTPR register compare match Input capture Input pin state ELC event input GTETRGn (n = A, B, C, D) pin input	GTPR register compare match Input capture Input pin status ELC event input GTETRGn (n = A to D) pin input GTCCR register compare match Other channel's counter clear sources
Period count function		—	Available (GPT32n (n = 0 to 3))
Compare match output	Low output	Available	Available
	High output	Available	Available
	Toggle output	Available	Available
Input capture function		Available	Available
Automatic addition of dead time		Available*4	Available
PWM mode		Available	Available
High accuracy PWM waveform		—	Available (GPT32n (n = 0 to 3))
Phase count function		Available	Available (GPT32n (n = 0 to 3))
External pulse width measuring function		—	Available (GPT32n (n = 0 to 3))
Buffer operation		Double buffer	Double buffer Simultaneous operation disable control for multiple channels Buffer operation by counter clearing/compare match
Item		RA6T1	RA6T2
One-shot operation		Available	Available
DMAC/DTC activation		All interrupt sources	All interrupt sources
A/D converter start trigger		Compare match of GTADTRA or GTADTRB*1	Compare match of GTADTRA or GTADTRB register
Brushless DC motor control function		Available	Available
Interrupt sources		10 sources*5 GTCCRA compare match/input capture (GPTn_CCMPA) GTCCRB compare match/input capture (GPTn_CCMPB) GTCCRC compare match (GPTn_CMPC) GTCCRD compare match (GPTn_CMPD) GTCCRE compare match (GPTn_CMPCE) GTCCRF compare match (GPTn_CMPF) GTADTRA compare match*1 (GPTn_ADTRGA) GTADTRB compare match*1 (GPTn_ADTRGB) GTCNT overflow (GTPR compare match) (GPTn_OVF) GTCNT underflow (GPTn_UDF)	11 sources GTCCRA compare match/input capture (GPTn_CCMPA) GTCCRB compare match/input capture (GPTn_CCMPB) GTCCRC compare match (GPTn_CMPC) GTCCRD compare match (GPTn_CMPD) GTCCRE compare match (GPTn_CMPE) GTCCRF compare match (GPTn_CMPF) GTADTRA compare match (GPTn_ADTRGA) GTADTRB compare match (GPTn_ADTRGB) GTCNT overflow (GTPR compare match) (GPTn_OVF) GTCNT underflow (GPTn_UDF) GTPC count stop (GPTx_PC) (x = 0 to 3)

Item	RA6T1	RA6T2
Interrupt skipping function	Skipping of GTCNT overflows (GTPR compare match) (GPTn_OVF)/GTCNT underflow (GPTn_UDF) interrupts (with interlocking function for other interrupts or A/D conversion requests)	Skipping of interrupts of GTCNT counter overflow (GTPR register compare match) (GTPn_OVF) and GTCNT counter underflow (GTPn_UDF) (interlocked with other interrupts and A/D conversion start requests) Skipping of GTADTRA and GTADTRB register compare match (GPT32y (y = 4 to 9)) Buffer operation skipping function
Event linking (ELC) function	Available	Available
Noise filtering function	Available	Available
Logical operation between the channel output	—	Available
Synchronous counter clearing/counter setting/input capture	—	Available

Note 1. Supported GPT32EH and GPT32E of RA6T1.
Note 2. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPD14 bit.
Note 3. GTETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPCRD.MSTPDn (n = 11 to 14) bit.
Note 4. GPT32 of RA6T1 does not support the dead-time buffer.
Note 5. RA6T1 interrupt sources: GPT32EH and GPT32E are 10 sources. GPT32 is 8 sources.

2.19 PWM Delay Generation Circuits

Table 35 shows a comparative overview of PWM Delay Generation Circuits.

Table 35. Comparative Overview of PWM Delay Generation Circuits

Item	RA6T1	RA6T2
Function	The circuit can control the timing with which signals on the two PWM output pins for channel 0/1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT clock (PCLKD).	The circuit can control the timing with which signals on the two PWM output pins for channel 0/1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT core clock (GTCLK). The GPT core clock (GTCLK) can be selected from PCLKD or GPTCLK.

2.20 Low Power Asynchronous General-Purpose Timer and Asynchronous General-Purpose Timer

Table 36 shows a comparative overview of Low Power Asynchronous General-Purpose Timer and Asynchronous General-Purpose Timer.

Table 36. Comparative overview of Low Power Asynchronous General-Purpose Timer and Asynchronous General-Purpose Timer

Item		RA6T1 (Low Power Asynchronous General- Purpose Timer: AGT)	RA6T2 (Asynchronous General-Purpose Timer: AGTW_B)
Operating modes	Timer mode	The count source is counted.	The count source is counted.
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow.	The count source is counted and the output is inverted at each timer underflow.

Item		RA6T1 (Low Power Asynchronous General- Purpose Timer: AGT)	RA6T2 (Asynchronous General-Purpose Timer: AGTW_B)
	Event counter mode	An external event is counted.	An external event is counted.
	Pulse width measurement mode	An external pulse width is measured.	An external pulse width is measured.
	Pulse period measurement mode	An external pulse period is measured.	An external pulse period is measured.
Number of channels		16 bits x 2 channels (AGTn (n = 0, 1))	32 bits × 2 channels (AGTWn (n = 0, 1))
Count source (operating clock)	Timer mode	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK, AGTLCLK/2, AGTLCLK/4, AGTLCLK/8, AGTLCLK/16, AGTLCLK/32, AGTLCLK/64, AGTLCLK/128, AGTSCLK, AGTSCLK/2, AGTSCLK/4, AGTSCLK/8, AGTSCLK/16, AGTSCLK/32, AGTSCLK/64, AGTSCLK/128, or underflow signal of AGT0 is selectable.	PCLKB, PCLKB/2, PCLKB/8, AGTLCLK/d (d = 1, 2, 4, 8, 16, 32, 64, or 128), or underflow signal of AGTW0 is selectable.
	Pulse output mode		
	Pulse width measurement mode		
	Pulse period measurement mode		
	Event counter mode	External event input	External event input
Interrupt and Event Link function		• Underflow event signal or measurement complete event signal — When the counter underflows — When the measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode — When the set edge of the external input (AGTIO) is input in pulse period measurement mode	• Underflow event signal or measurement complete event signal — When the counter underflows — When the measurement of the active width of the external input pin (AGTWIOn) is complete in pulse width measurement mode — When the set edge of the external input pin (AGTWIOn) is input in pulse period measurement mode
Interrupt and Event Link function		• Compare match A event signal — When the values of AGT and AGTCMA matched (compare match A function enabled) • Compare match B event signal — When the values of AGT and AGTCMB matched (compare match B function enabled) Return from Snooze mode or Software Standby mode can be performed with AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI.	• Compare match A event signal — When the values of AGT register and AGTCMA register matched (compare match A function enabled) • Compare match B event signal — When the values of AGT and AGTCMB matched (compare match B function enabled) • Return from Snooze mode or Software Standby mode can be performed with AGT1_AGTI, AGT1_AGTCMAI, or AGT1_AGTCMBI.

Item	RA6T1 (Low Power Asynchronous General- Purpose Timer: AGT)	RA6T2 (Asynchronous General-Purpose Timer: AGTW_B)
Selectable functions	• Compare match function Either or both of the compare match A and B registers are selectable.	• Compare match function Either or both of the AGT Compare Match A register and AGT Compare Match B register are selectable.
TrustZone Filter	—	The security attribution can be set for each channel.

2.21 Watchdog Timer

Table 37 is comparative overview of Watchdog Timer.

Table 37. Comparative overview of Watchdog Timer

Item	RA6T1 (WDT)	RA6T2 (WDT)
Count source	Peripheral clock (PCLKB)	Peripheral clock (PCLKB)*1
Clock division ratio	Division by 4, 64, 128, 512, 2,048, or 8,192	Division by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto start mode: Counting automatically starts after a reset, or after an underflow or refresh error occurs.	• Auto start mode: Counting automatically starts after a reset, or after an underflow or refresh error occurs.
	• Register start mode: Counting is started with a refresh by writing to the WDTRR register.	• Register start mode: Counting is started with a refresh by writing to the WDTRR register. • Only the secure developer can select Auto-start mode or Register-start mode.
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
WDT reset sources	• Down counter-underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down counter-underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the WDTSR register.	The down-counter value can be read by the WDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output
TrustZone Filter	—	The security attribution can be set.

Note 1: Specify the settings so that the frequency of the peripheral module clock (PCLKB) is equal to or greater than 4 times the frequency of the count clock source after division.

2.22 Independent Watchdog Timer

Table 38 show a comparative overview of Independent Watchdog Timer.

Table 38. Comparative Overview of Independent Watchdog Timer

Item	RA6T1 (IWDT)	RA6T2 (IWDT)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	Counting automatically starts after a reset.	• Counting automatically starts after a reset. • Only the secure developer can start the IWDT.
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically)	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (counting restarts automatically)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods).
IWDT reset sources	• The down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)	• The down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• The down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)	• The down-counter underflows. • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the IWDTSR register.	The down-counter value can be read by the IWDTSR register.
Event link function (output)	• Down-counter underflow event output • Refresh error event output	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the IWDT (OFS0.IWDTTOPS[1:0] bits) • Window start position in the IWDT (OFS0.IWDTRPSS[1:0] bits) • Window end position in the IWDT (OFS0.IWDTRPES[1:0] bits)	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the Independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Window start position in the Independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Window end position in the Independent watchdog timer (OFS0.IWDTRPES[1:0] bits)
Auto start mode	• Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit)	• Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function at transition to Sleep, Software Standby, or Snooze mode (OFS0.IWDTSTPCTL bit)
TrustZone Filter	—	The security attribution can be set.

2.23 Serial Communications Interfaces

Table 39 shows a comparative overview of Serial Communications Interfaces.

Table 39. Comparative Overview of Serial Communications Interfaces

Item		RA6T1 (SCI)	RA6T2 (SCI_B)
Number of modules		7 (SCIn (n = 0 to 4, 8, 9))	6 (SCIn (n = 0 to 4, 9))
Serial communication modes		• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Smart card interface	• Asynchronous • Clock synchronous • Simple IIC • Simple SPI • Simple LIN • Smart card interface • Manchester interface
Transfer speed		Bit rate specifiable with the on-chip baud rate generator	Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications		• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering	• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
Half-duplex communications		—	Half-duplex communication is possible by using only TXDn pins.
Data transfer		Selectable as LSB-first or MSB-first transfer	Selectable as LSB-first or MSB-first transfer
Inverter for communication pins (RXDn, TXDn)		—	Selectable inverter for each pin (RXDn, TXDn)
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match • Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match • Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode) • Break Field detection/output, Bus collision detection, and Active edge detection
Loop Back function		—	Self-diagnosis of communication function by IP internal transmission/reception is possible.
Synchronizer Bypass function		—	Ability to bypass synchronization circuit between bus clock and operation clock (TCLK)
Module-stop function		Module-stop state can be set for each channel.	Module-stop state can be set for each channel.
Snooze end request		SCI0 address mismatch (SCI0_DCUF)	SCI0 address mismatch (SCI0_DCUF)
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits	1 or 2 bits
	Adjustment of receive sampling timing	—	Adjustable receive sampling timing before/after the default timing

Item		RA6T1 (SCI)	RA6T2 (SCI_B)
Asynchronous mode	Adjustment of transmit timing	—	Adjustable edge timing of transmit waveform controlled by the setting value of registers
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	• Parity error • Overrun error • Framing error
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins	Transmission and reception controllable with CTSn_RTSn pin and CTSn pin
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO	Selectable to 1-stage register or 16-stage FIFO
	Address match	An interrupt request or event output can be issued on detecting a match between received data and the value in the compare match register.	An interrupt request or event output can be issued upon detecting a match between received data and the value in the compare match register.
	Address mismatch (SCI0 only) receive data	Snooze end request can be issued on detecting a mismatch between the received data and the value in the compare match register.	Snooze end request can be issued when detecting a mismatch between the received data and the value in the compare match register.
	Start-bit detection	Selectable to low level or falling edge detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by reading the SPTR register	Breaks from framing errors detectable by read from the CSR register
	Clock source	Selectable to internal or external clock	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication enabled among multiple processors	Serial communication enabled among multiple processors
	RS-485 driver control function	—	Output DEn signal to enable external transceiver transmit mode
	Noise cancellation	Digital noise filters included on signal paths from RXDn pin inputs	Digital noise filters included on signal paths from the RXDn pin inputs
Clock synchronous mode	Data length	8 bits	8 bits
	Adjustment of receive sampling timing	—	Adjustable receive sampling timing after the default timing in master mode only when using internal clock
	Receive error detection	Overrun error	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)	Selectable to internal clock (master mode) or external clock (slave mode)
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO	Selectable to 1-stage register or 16-stage FIFO

Item		RA6T1 (SCI)	RA6T2 (SCI_B)
Smart card interface mode	Error processing	Error signal can be automatically transmitted on detecting a parity error during reception.	Error signal can be automatically transmitted upon detecting a parity error during reception.
		Data can be automatically retransmitted on receiving an error signal during transmission.	Data can be automatically retransmitted upon receiving an error signal during transmission.
	Data type	Both direct and inverse convention supported	Both direct and inverse convention supported
Manchester mode	Communication format	—	Manchester code with the preface and the Start Bit added
	Data length		7, 8, or 9 bits
	Transmission stop bit		1 or 2 bits
	Parity function		Even parity, odd parity, or no parity
	Receive error detection		Parity, overrun, framing, Manchester errors
	Hardware flow control		Transmission and reception controllable with CTSn_RTSn and CTSn pins
	Clock source		Only internal clock can be used.
	Double-speed mode		Baud rate generator double-speed mode is selectable.
	Multi-processor communications function		Serial communication enabled among multiple processors
	Manchester encoding/ decoding function		Function to perform Manchester encoding/decoding of transmission/reception data and communicate using Manchester code
	Noise cancellation		The signal paths from input on the RXDn pins incorporate digital noise filters.
	Preface setting/ detection function		The function outputs the configured preface pattern and detects it.
	Start bit setting/ detection function		The function outputs the configured Start Bit pattern and detects it.
	Reception retiming function		Timing correction is performed for each bit of the received signal.
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Up to 400 kbps	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation.	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters and provide an adjustable interval for noise cancellation.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)	Selectable to internal clock (master mode) or external clock (slave mode)

Item		RA6T1 (SCI)	RA6T2 (SCI_B)
Simple SPI mode	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Transmission and reception	—	Selectable to 1-stage register or 16-stage FIFO
	Adjustment of receive sampling timing	—	Adjustable receive sampling timing after the default timing in master mode only when using internal clock
	SSn input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high.	High impedance state can be invoked on the output pins by driving the SSn pin high.
	Clock settings	Configurable among four clock phase and clock polarity settings	Configurable among four clock phase and clock polarity settings
Simple LIN	Start Frame Transmission	—	• Break Field output possible, and Break Field output complete interrupt output possible • Bus collision detection possible, and bus collision detection interrupt output possible
	Start Frame Reception		• Break Field detectable, and Break Field detected interrupt output possible • Control Field 0/1 data comparison function • Control Field 1 can set two types of comparison data of primary and secondary. • Priority interrupt bit can be set in Control Field 1. • Handling of Start Frames that do not include a Break Field • Handling of Start Frames that do not include a Control Field 0 • Bit rate measurement function
	Input/Output control function		• Selectable polarity for TXDn and RXDn signals • Selection of a digital filter for the RXDn signal • Half-duplex operation employing RXDn and TXDn signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDn
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator	Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI) (n = 0 to 4, 8, 9)	Error event output for receive error or error signal detection (SCIn_ERI) (n = 0 to 4, 9)
		Receive data full event output (SCIn_RXI) (n = 0 to 4, 8, 9) *1	Receive data full event output (SCIn_RXI) (n = 0 to 4, 9)

Item	RA6T1 (SCI)	RA6T2 (SCI_B)
Event link function	Transmit data empty event output (SCIn_TXI) (n = 0 to 4, 8, 9) *1	Transmit data empty event output (SCIn_TXI) (n = 0 to 4, 9)
	Address match event output (SCIn_AM) (n = 0 to 4, 8, 9)	Address match event output (SCIn_AM) (n = 0 to 4, 9)
	—	Active edge detection event output (SCIn_AED) (n = 0 to 4, 9)
	Transmit end event output (SCIn_TEI) (n = 0 to 4, 8, 9)*1	Transmit end event output (SCIn_TEI) (n = 0 to 4, 9)
TrustZone Filter	—	The security attribution can be set for each channel.

Note 1. Using this event link function is prohibited when FIFO operation is selected in asynchronous mode.

2.24 I²C Bus Interfaces

Table 40 shows a comparative overview of I2C bus interfaces.

Table 40. Comparative Overview of I2C Bus Interfaces

Item	RA6T1 (IIC)	RA6T2 (IIC_B)
Operating modes	Master mode and slave mode selectable	Master mode and slave mode selectable
Data handler	Double buffer transfer	Single buffer transfer
Communication protocol	Communications format: • I²C bus format or SMBus format	• I²C bus format — Standard-mode (Sm): 0 to 100 kbps — Fast-mode (Fm): 0 to 400 kbps — Fast-mode Plus (Fm+): 0 to 1 Mbps*1 — High-speed mode (Hs-mode): 0 to 3.2 Mbps*1
	Transfer rate: • Fast-mode Plus supported (up to 1 Mbps)	• SMBus format:10 to 100 kbps
Address format	• 7-bit and 10-bit address formats supported, including simultaneous use	• 7-bit address • 10-bit address
Address detection	• Configurable for up to three different slave addresses • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Slave address (static address) (max 3 addresses) • General call address • HS-mode master code*1 • Device ID • Host address • 10-bit slave addressing

Item	RA6T1 (IIC)	RA6T2 (IIC_B)
Clock stretching	Acknowledgment: • For transmission, automatic loading of the acknowledge bit: Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatic transmission of the acknowledge bit: If a wait between the 8th and 9th clock cycles is selected, software can control the value in the acknowledge field in response to the received value.	Clock stretching capability
	Wait function: During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the 8th and 9th clock cycles • Waiting between the 9th clock cycle and the 1st clock cycle of the next transfer	
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed.	Output timing of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation: — SCL clock synchronization is possible when conflict occurs with the SCL signal from another master. — When issuing the start condition causes a conflict on the bus, loss of arbitration is detected by testing for mismatching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for mismatching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to generation of the start condition while the bus is busy is detectable, to prevent the issuing of double start conditions. • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match. • Loss of arbitration due to mismatching of internal and line levels for data is detectable in slave transmission.	• For multi-master operation: — SCL clock synchronization is possible when conflict occurs with the SCL signal from another master. — When issuing the start condition causes a conflict on the bus, loss of arbitration is detected by testing for mismatching between the internal signal for the SDA line and the level on the SDA line. — In master operation, loss of arbitration is detected by testing for mismatching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration due to generation of the start condition while the bus is busy is detectable, to prevent the issuing of double start conditions. • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match. • Loss of arbitration due to mismatching of internal and line levels for data is detectable in slave transmission.
Timeout function	Internal detection of long-interval stops of the SCL clock	Internal detection of long-interval stops of the SCL clock
Noise-filter	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters.	• Analog noise-filter • Digital noise-filter

Item	RA6T1 (IIC)	RA6T2 (IIC_B)
Interrupt sources	• Transfer error or event occurrence (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full • Transmit data empty • Transmit end	• START condition detection • STOP condition detection • NACK detection • Arbitration lost • Timeout detection • Rx data buffer full • Tx data buffer empty • Transmit end • Wake-up condition detection
Error detection	• NACK • Arbitration detection • Timeout	• NACK received • Arbitration lost error • Timeout error
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Event link function	• Transfer error or event occurrence (arbitration detection, NACK, timeout, start or restart condition, or stop condition) • Receive data full • Transmit data empty • Transmit end	• Communication event • Rx data buffer full event • Tx data buffer empty event • Transmit end event
Wake-up function	CPU can return from Software Standby mode using a wakeup event.	Wake-up source: Address detection of slave address

Note 1. Fast-mode Plus and High-speed mode are supported by IIC0 (SCL0_A, SDA0_A).

2.25 CAN Module and CAN with Flexible Data-rate

Table 41 shows a comparative overview of CAN Module and CAN with Flexible Data-rate.

Table 41. Comparative overview of CAN Module and CAN with Flexible Data-rate

Item		RA6T1 (CAN)	RA6T2 (CANFD_B)
Communication		ISO11898-1-compliant for standard and extended frames	CAN functionality conforming to CANFD ISO 11898-1 (2015)
Protocol engine version		—	RS-CANFD_PE V3.0
Data transfer rate	CANFD	—	Up to 1 Mbps for arbitration phase and up to 5 Mbps for data phase
	Classical CAN	Programmable up to 1 Mbps	Up to 1 Mbps
Operation frequency and Peripheral clock		fCAN ≥ 8 MHz (PCLKB or CANMCLK)	60 MHz (PCLKB) RAM clock: 120 MHz (PCLKA)
Data Link Layer (DLL) clock		—	Max ≤ 40 MHz
Input/Output pins		CTX0/CRX0	CTX0/CRX0
CAN channels		1 channel	1 channel
Selectable ID type		• Reception ID format selectable to only standard ID, only extended ID, or mixed IDs • Transmission ID format selectable to only standard ID, only extended ID, or mixed IDs	11-bit Standard ID 11-bit Standard ID +18-bit Extended ID
Selectable frame type		• Support for data frame and remote frame reception • Support for data frame and remote frame transmission	Data frame (RTR = 0) (CAN and CANFD frames) Remote frame (RTR = 1) (only CAN frames)
Variable data byte count for data frames		DLC range: 0 to 8	DLC range: 0 to F

Item	RA6T1 (CAN)	RA6T2 (CANFD_B)
Message buffer	32 mailboxes, with the following two selectable mailbox modes: • Normal mode: 32 mailboxes independently configurable for transmission or reception • FIFO mode: 24 mailboxes independently configurable for either transmission or reception, with remaining mailboxes used for receive (RX) and transmit (TX) 4-stage FIFOs	Up to 32 reception message buffers 4 transmit message buffers 1 transmission queue Automatic message transfer into transmission queues supported
FIFO number		2 reception FIFO buffers 1 COMMON FIFO individually configurable as: • Reception FIFO • Transmission FIFO
Automatic delay interval timer for transmission	—	The delay timer can be applied to: • Transmission FIFO
Enhanced reception filtering	• Eight acceptance masks (one for every four mailboxes) • Masks independently enabled or disabled for each mailbox	Support of 11 bits and 29 bits CAN identifier Programmable 29 bits CAN identifier acceptance filter mask for each entry Programmable routing capability for each FIFO and reception message buffers (up to 2 routing destinations)
Enhanced reception filtering		RTR and IDE masking Data Length Code (DLC) filter Message buffer payload overload protection Updating Acceptance Filter List (AFL) entry during communication
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification-compliant • Automatic invoking of CAN halt mode on bus-off entry • Automatic invoking of CAN halt mode on bus-off end • Transition to CAN halt mode through software • Transition to error-active state through software.	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification-compliant • Automatic invoking of CAN halt mode on bus-off entry • Automatic invoking of CAN halt mode on bus-off end • Transition to CAN halt mode through software • Transition to error-active state through software.
Error status monitoring	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states, including error-warning, error-passive, bus-off entry, and bus-off recovery • Support for reading of error counters	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states, including error-warning, error-passive, bus-off entry, and bus-off recovery • Support for reading of error counters
General software support	Three software support units: • Acceptance filter support • Mailbox search support, including receive mailbox search, transmit mailbox search, and message lost search • Channel search support	Automatic label information added to receive message (for upper software layer support)

Item	RA6T1 (CAN)	RA6T2 (CANFD_B)
Timer	• Time stamp function using a 16-bit counter • Reference clock selectable to 1-bit, 2-bit, 4-bit, and 8-bit time periods	TX and RX Time Stamp function
Interrupt function	Support for five interrupt sources: • Reception complete • Transmission complete • Receive FIFO • Transmit FIFO • Error interrupts.	• Global interrupts — Global interrupt for successful reception into the two RX FIFO buffers — Global error interrupt — Global interrupt for successful reception into the 32 RX message buffers • Channel interrupts — Channel transmission — Channel error interrupt — Successful reception in a Common FIFO in RX mode for a channel
Test mode	Three test modes available for evaluation purposes: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	• Channel specific test modes — Basic test mode — Listen-only mode — Self-test mode 0 (External loop back mode) — Self-test mode 1 (Internal loop back mode) — Restricted operation mode • Global test modes — RAM test mode — Bit Flip Test
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Power down function	CAN sleep mode: CAN clock can be stopped to reduce power consumption.	Module start stop function for CAN node (Channel and Global Sleep mode)
RAM	—	RAM ECC protected (2 bits error detection and 1-bit error correction)
TrustZone Filter	—	One security attribution can be set.

2.26 Serial Peripheral Interfaces

Table 42 shows a comparative overview of Serial Peripheral Interfaces.

Table 42. Comparative Overview of Serial Peripheral Interfaces

Item	RA6T1 (SPI)	RA6T2 (SPI_B)
Number of channels	Two channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method).	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method).
	• Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching	• Transmit-only operation available • Receive-only operation is available. • Communication mode selectable to full-duplex, transmit-only, or receive-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 128-bit transmit and receive buffers • Up to four frames transferrable in one round of transmission or reception (each frame consisting of up to 32 bits) • Byte swap operating function	• MSB-first or LS.B-first selectable • Transfer bit length selectable from 4 to 32 bits • 32 bits × 4 stages FIFO is available as transmit buffer or receive buffer. • Byte swap operating function • Transmit/receive data can be inverted.
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKA (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLKA clock divided by 4 can be input as RSPCK (the maximum RSPCK frequency is that of PCLKA divided by 4). Width at high level: 2 PCLKA cycles width at low level: 2 PCLKA cycles	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing TCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum TCLK clock divided by 2 can be input as RSPCK (TCLK divided by 2 is the maximum RSPCK frequency). Width at high level: 1 TCLK cycle; width at low level: 1 TCLK cycle
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers	• Double buffer configuration for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Underrun error detection • Overrun error detection • Parity error detection • Receive data ready detection

Item	RA6T1 (SPI)	RA6T2 (SPI_B)
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity	[Common to Motorola SPI and TI SSP modes] • Four SSL pins (SSLni: SSLn0 to SSLn3) (n = A or B) for each channel • In single-master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity • Delay between frames in burst transfer is settable.y [Only Motorola mode] • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) [Slave and TI SSP modes] • Controllable delay from OE output assertion to RSPCK operation (RSPCK delay) Range: 0 to 8 RSPCK cycles (set in RSPCK-cycle units)
Communication protocol	—	• Motorola SPI • TI SSP (Synchronous Serial Protocol)

Item	RA6T1 (SPI)	RA6T2 (SPI_B)
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in a loop. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• Transfers of up to eight commands can be performed sequentially in a loop. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	• Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode-fault, overrun, or parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt	Interrupt sources: • Receive buffer full or receive data ready interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault error, underrun error, overrun error, parity error, or receive data ready) • SPI idle interrupt (SPI idle) • Communication end interrupt
Event link function	The following events can be output to the Event Link Controller (ELC): • Receive buffer full signal • Transmit buffer empty signal • Mode-fault, underrun, overrun, or parity error signal • SPI idle signal • Transmission-completed signal	The following events can be output to the Event Link Controller (ELC): • Receive buffer full or receive data ready signal • Transmit buffer empty signal • Mode fault, underrun, overrun, parity error, or receive data ready signal • SPI idle signal • Communication end signal
Other functions	• Switching between CMOS output and open-drain output • SPI initialization function • Loopback mode	• Switching between CMOS output and open-drain output • SPI initialization function • Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
TrustZone Filter	—	The security attribution can be set.

2.27 Cyclic Redundancy Check Calculator

Table 43 shows a Comparative overview of Cyclic Redundancy Check calculator.

Table 43. Comparative Overview of Cyclic Redundancy Check Calculator

Item		RA6T1 (CRC)	RA6T2 (CRC)
Data size	8-bit	8-bit	8-bit
	32-bit	32-bit	32-bit
Data for CRC calculation	8-bit	CRC code generated for data in 8n-bit units (where n is a natural number)	CRC code generated for user-defined data in 8n-bit units (where n is a natural number)
	32-bit	CRC code generated for data in 32n-bit units (where n is a natural number)	CRC code generated for user-defined data in 32n-bit units (where n is a natural number)
CRC processor unit	8-bit	Operation executed on 8 bits in parallel	Operation executed on 8 bits in parallel
	32-bit	Operation executed on 32 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	8-bit	One of three generating polynomials is selectable. [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)	One of three generating polynomials is selectable. [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)
	32-bit	One of two generating polynomials is selectable. [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C)	One of two generating polynomials is selectable. [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C)
CRC calculation switching		The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication.	The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication.
Module-stop function		Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
CRC snoop	8-bit	The monitor reads from and writes to a certain register address.	The monitor reads from and writes to a certain register address.
	32-bit	—	The monitor reads from and writes to a certain register address.
TrustZone Filter		—	The security attribution can be set.

2.28 Secure Cryptographic Engine

Table 44 shows a comparative overview of Secure Cryptographic Engine.

Table 44. Comparative Overview of Secure Cryptographic Engine

Item	RA6T1 (SCE7)	RA6T2 (SCE5_B)
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent accesses and stops the output of data from the SCE7.	Access management circuit • In case of irregular access to the SCE5 due to a tampered program or CPU runaway, this circuit blocks all subsequent accesses and stops data output from the SCE5.
Encryption engine	Advanced Encryption Standard (AES): Compliant with NIST FIPS PUB 197 algorithm • Key sizes: 128, 192, or 256 bits • Block size: 128 bits • Chaining modes ECB, CBC, and CTR: Compliant with NIST SP 800-38A GCM: Compliant with NIST SP 800-38D XTS: Compliant with NIST SP 800-38E GCTR • Throughput for 128-bit data 11 PCLKB cycles for 128-bit key 15 PCLKB cycles for 256-bit key AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Triple Data Encryption Standard (3DES) • 192-bit key length • Operates on a fixed 8-byte block of data • Used in legacy Secure Socket Layer (SSL) and Transport Layer Security (TLS) protocols • Throughput for 64-bit data 16 PCLKB cycles for 56-bit key Alleged RC4 (ARC4) • 2048-bit key length • Throughput for 128-bit data 16 PCLKB cycles for 2048-bit key	AES: Compliant with NIST FIPS PUB 197 • Key length: 128 or 256 bits • Data block size: 128 bits • Encryption usage modes ECB, CBC, and CTR: Compliant with NIST SP 800-38A CMAC: Compliant with NIST SP 800-38B GCM: Compliant with NIST SP 800-38D XTS: Compliant with NIST SP 800-38E GCTR • Throughput for 128-bit data 44 PCLKA cycles for 128-bit key 61 PCLKA cycles for 256-bit key*1 AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Key management • Wrapped keys are only valid within the SCE5.
Generation of random numbers	128-bit true random number generator	32-bit true random number generation circuit

Item	RA6T1 (SCE7)	RA6T2 (SCE5_B)
Signature generation and verification	RSA • Support for 1024-bit and 2048-bit key sizes • Signature generation, signature verification, public-key encryption, and private-key decryption DSA • Support for the following DSA key sizes: — (1024-bit, 160-bit) — (2048-bit, 224-bit) — (2048-bit, 256-bit) • Signature generation, signature verification ECC • Support for curve P-192, P-224, P-256, and P-384 • Signature generation, signature verification • Scalar multiplication	— — —
Message digest computation	HASH • SHA1, SHA224, SHA256, and MD5	—
Hardware Unique Key	—	• A read-only, 128-bit Hardware Unique Key (HUK) • Key derivation functions (KDFs) combine the Hardware Unique Key with the key generation information. The derived keys implement the key wrapping for user key secure storage. • The HUK uniqueness prevents the illicit cloning and copying of keys to another MCU of the MCU group. • The HUK itself is stored in wrapped (encrypted, non-plain) format in an isolated memory area. Therefore it is protected from illicit access and copy.
Unique ID	• An ID unique to the MCU (unique ID) is accessible from the access management circuit through the dedicated bus. • Combining the unique ID with the key generation information prevents illicit copying of data to another MCU.	• A read-only, 128-bit ID unique to an MCU (Unique ID) is accessible from the access management circuit. • Key derivation functions (KDFs) combine the Unique ID with the key generation information. Such derived keys are used to unwrap the HUK within the SCE boundary.
Supervisor mode	• Supervisor mode signals are connected to the access management circuit, and they are used to allow the SCE7 to be controlled only in supervisor mode.	—
Low power consumption	Setting of the module-stop state is possible.	Setting of the module-stop state is possible.

Note 1. This does not include the overhead of calling SCE5 library functions.

2.29 12-Bit A/D Converters

Table 45 shows a comparative overview of 12-Bit A/D Converters.

Table 45. Comparative Overview of 12-Bit A/D Converters

Item	RA6T1 (ADC12)	RA6T2 (ADC_B)
Number of units	Two units (0 and 1)	Two units (unit 0 and unit 1)
Input channels	• Unit 0: Up to 11 channels • Unit 1: Up to 8 channels (two channels share the same port pin)	• Up to 29 analog input channels — A/D Converter Unit 0: Up to 21 analog input channels — A/D Converter Unit 1: Up to 17 analog input channels — 9 analog input channels are shared by A/D Converter Unit 0 and Unit 1.
Extended analog function	Temperature sensor output, internal reference voltage	Self-diagnosis, temperature sensor, internal reference voltage, and D/A converters (DA0 to DA3)
A/D conversion method	Successive approximation method	Successive approximation method
Resolution of A/D converter	12 bits (selectable to 12-bit, 10-bit, or 8-bit conversion)	12 bits
Conversion time	0.4 µs/channel, when A/D conversion clock PCLKC (ADCLK) is operating at 60 MHz.	0.16 µs per channel (when A/D conversion clock ADCLK = 50 MHz)
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock PCLKC (ADCLK)*1 can be set with the following division ratios: PCLKB to PCLKC (ADCLK) division ratios = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4	The A/D conversion clock (ADCLK) can be set by selecting the clock source and the division ratio as follows: • Clock source: Peripheral module clock PCLKC, peripheral module clock PCLKA, and GPT clock GPTCLK • Division ratio: 1/2/3/4/5/6/7/8 A/D conversion clock (ADCLK) can operate between 25 MHz at a minimum and 60 MHz at a maximum.
A/D conversion data	• 19 registers for analog input (11 for unit 0, 8 for unit 1), one for A/D-converted data duplication in double trigger mode in each unit, and two for A/D-converted data duplication in extended operation in double trigger mode in each unit • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • A/D conversion results are stored in A/D data registers. • 8-, 10-, and 12-bit accuracy output for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D conversion results are stored in the A/D data registers as the conversion accuracy bit count + 2 bits.*3	• A/D conversion results are stored in data register or FIFO. • A/D conversion results are available in 16-, 14-, 12-, and 10-bit data formats.

Item	RA6T1 (ADC12)	RA6T2 (ADC_B)
A/D conversion data	• Double trigger mode (selectable in single scan and group scan modes): The first unit of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplication register provided for the associated trigger.	
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, the temperature sensor output, and the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, the temperature sensor output, and the internal reference voltage. • Group scan mode: — A/D conversion is performed only once on the analog inputs of arbitrarily selected channels divided into group A and group B, the temperature sensor output, and the internal reference voltage. — The scan start conditions can be independently selected for group A and group B, allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B stops and A/D conversion is processed on group A. — Restart (rescan) of group B conversion after completion of group A conversion can be set.	• Single scan mode: — Assign any selected analog input or analog channel of the extended analog function to any scan group*4, and convert the selected analog input only once per scan group for A/D conversion. — By selecting the scan start conditions for each scan group individually, A/D conversion for each scan group can be started at different times. • Continuous Scan Mode: — Assign any selected analog input or analog channel of the extended analog function to any scan group*4 and repeat A/D conversion in scan group units.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger from the Event Link Controller (ELC) • Asynchronous trigger from the external trigger pins, ADTRG0 (unit 0) and ADTRG1 (unit 1)	• Software trigger (for simultaneous activation of scan group: max. 9 triggers) • Software trigger (for individual scan group activation: up to 9 triggers) • Trigger from Event Link Controller: 6 triggers • Triggers from GPT: 20 triggers • External trigger input: 2 triggers (ADTRGn input (n = 0, 1))

Item	RA6T1 (ADC12)	RA6T2 (ADC_B)
Functions		• Virtual Channel function (37 virtual channels) • Scan Group function (up to 9 scan groups)
	• Dedicated sample-and-hold function with optional constant sampling and 3 channels in units 0 and 1	• Channel-dedicated sample-and-hold circuit (SH) (3 SH units for A/D Converter Unit 0, and 3 SH units for A/D Converter Unit 1)
	• Variable sampling state count	• Variable sampling time (selected from 16 tables per virtual channel)
	• Self-diagnosis of ADC12	• Self-diagnosis function for A/D Converter
	• Selectable A/D-converted value addition mode or average mode	• Selectable A/D-converted value addition mode or average mode
	• Analog input disconnection detection function (discharge and precharge functions)	• Analog input disconnection detection assist function (discharge function/precharge function)
	• Double trigger mode (duplication of A/D conversion data)	
	• Switching function for 8-, 10-, and 12-bit conversion*2	• The data format selectable from 16-/14-/12-/10-bit • Limiter Clip Function (Up to 8 tables)
	• Automatic clear function for A/D data registers	
	• Digital comparison of values in the comparison and data registers, and between values in the data registers	• Compare Match Function (Up to 8 tables)
		• Self-calibration function • User's Gain adjustment function • User's Offset adjustment function • Built-in FIFO (8 stages per each scan group) • Multiple A/D converters Unit-to-unit synchronous operation function
Programmable gain amplifier	• Amplification of analog input signals to enable A/D conversion, with three channels in units 0 and 1	• Analog input signals can be amplified by programmable gain amplifier (PGA), and A/D conversion can be performed (three PGAs for A/D Converter Unit 0, and one PGA for A/D Converter Unit 1).
	• Compatible with single-ended input and pseudo-differential input	• Support the single-ended input or the pseudo-differential input • Monitor function via pin for PGA output

Item	RA6T1 (ADC12)	RA6T2 (ADC_B)
Interrupt sources and ELC events	• ADC12i_ADI: A/D scan end interrupt • ADC12i_GBADI: A/D scan end interrupt for group B • ADC12i_CMPAI: Window A compare match • ADC12i_CMPBI: Window B compare match • ADC12i_WCMPM: Compare match • ADC12i_WCMPUM: Compare mismatch	• A/D scan end interrupt — Generates the interrupt requests and the ELC events at the end of A/D scan operation for the scan group i (ADC_ADIi (i = 0 to 4)). The interrupt requests are independent for each scan group. — Generates the interrupt request and the ELC event at the end of A/D scan operation for any of the scan groups 5 to 8 (ADC_ADI5678). The interrupt request is shared by scan groups 5 to 8. • FIFO data read request interrupt — Generates the interrupt requests when the number of vacant stages of FIFO for the scan group i becomes less than or equal to the specified value (ADC_FIFOREQi (i = 0 to 4)). The interrupt requests are independent for each scan group. — Generates the interrupt request or the ELC event when the number of vacant stages of FIFO for any of the scan groups 5 to 8 becomes less than or equal to the specified value (ADC_FIFOREQ5678). The interrupt request is shared by scan groups 5 to 8. • FIFO data overflow interrupt — Generates the interrupt request when the overflow occurs in any of the FIFO for the scan groups 0 to 8 (ADC_FIFOOVF). • Limiter Clip interrupt — Generates the interrupt request when the limiter clip using the limiter tables 0 to 7 occurs for A/D conversion results (ADC_LIMCLPI). • Compare Match interrupt — Generates the interrupt requests when a compare match using the compare match tables j occurs for A/D conversion results (ADC_CMPIj (j = 0 to 3)).The interrupt requests are independent for each compare match table. • Composite Compare Match interrupt — Generates the interrupt requests and the ELC events when the compare match of the composite condition using compare match tables 0 to 7 occurs (ADC_CCMPMm (m = 0, 1)). • A/D Converter Error interrupt — Generates the interrupt requests when the operational error is detected in A/D converter Unit j (ADC_ERRj (j = 0, 1)). • A/D Conversion Overflow interrupt

Item	RA6T1 (ADC12)	RA6T2 (ADC_B)
		— Generates the interrupt request when an A/D conversion result overflow occurs (ADC_RESOVFj (j = 0, 1)). The interrupt requests are independent for A/D converter unit j. • A/D Converter calibration end interrupt — Generates the interrupt requests at the end of calibration operation of A/D converter unit j (ADC_CALENDj (j = 0, 1)). • Event Generation — An event is generated at the end of each scan operation for the scan groups 0 to 4. — An event is generated at the end of scan operation for any of the scan groups 5 to 8. — An event is generated when a Complex Compare Match occurs.
ELC interface	Scan can be started by a trigger from the ELC.	• Trigger input — Scan can be started by the trigger from the ELC.
Bus interface	Bus clock synchronized with peripheral clock (PCLKB), maximum frequency = 60 MHz	—
Reference voltage	• Unit 0: — VREFH0 is the high potential reference voltage. — VREFL0 is the low potential reference voltage. • Unit 1: — VREFH is the high potential reference voltage. — VREFL is the low potential reference voltage.	VREFH0 is the analog reference voltage. VREFL0 is the analog reference ground.
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.

Note 1. Peripheral module clock PCLKB is specified in the SCKDIVCR.PCKB[2:0] bits, and A/D conversion clock ADCLK is specified in the SCKDIVCR.PCKC[2:0] bits in units 0 and 1.

Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time.

Note 3. The number of extended bits for addition varies with the A/D conversion accuracy and the number of addition times. A 2-bit extension is up to 4 times conversion (3 times addition) when the A/D conversion accuracy is 8, 10, or 12 bits. A 4-bit extension is 16 times conversion (15 times addition) when the A/D conversion accuracy is 12 bits.

Note 4. Up to 8 channels can be assigned per scan group.

2.30 12-Bit D/A Converters

Table 46 shows a comparative overview of 12-bit D/A Converters.

Table 46. Comparative Overview of 12-Bit D/A Converters

Item	RA6T1 (DAC12)	RA6T2 (DAC12)
Resolution	12 bits	12 bits
Output channels	2 channels	4 channels
Interference reduction between analog modules	Methods provided to minimize interference between D/A and A/D conversion: • D/A converted data update timing is controlled by the ADC12 synchronous D/A conversion enable input signal from the ADC12 (unit 1). • Degradation of A/D conversion accuracy caused by interference is reduced by controlling the DAC12 inrush current generation timing with the enable signal.	—
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Event link function (input)	DA0 and DA1 conversion can be started when an event signal is input.	DA0, DA1, DA2, and DA3 conversion can be started when an event signal is input.
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used
Destination of D/A output control function	Controls whether the output to the external pin or to the internal modules (ACMPHS) is used	Controls whether the output to the external pin or to the internal modules (ACMPHS) is used
TrustZone Filter	—	The security attribution can be set.

2.31 Temperature Sensor

Table 47 shows a comparative overview of temperature sensor.

Table 47. Comparative Overview of Temperature Sensor

Item	RA6T1 (TSN)	RA6T2 (TSN)
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-bit A/D Converter (ADC12).	Temperature sensor outputs a voltage to the 12-bit A/D converter.
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Temperature sensor calibration data	Reference data measured for each MCU at factory shipment is stored.	Reference data measured for each chip at factory shipment is stored in a register.
TrustZone Filter	—	The security attribution can be set.

2.32 High-Speed Analog Comparators

Table 48 shows a comparative overview of High-Speed Analog Comparators, and Table 49 shows a comparison of the input source configurations of High-Speed Analog Comparators.

Table 48. Comparative Overview of High-Speed Analog Comparators

Item	RA6T1 (ACMPHS)	RA6T2 (ACMPHS)
Number of channels	6 channels: ACMPHS0 to ACMPHS3, ACMPHS4, ACMPHS5	4 channels: ACMPHSn (n = 0 to 3)
Analog input voltage	• Output from internal PGA • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)	• Output from internal PGA • Input from internal A/D converter input pin (one selectable)
Reference voltage	• Internal reference voltage (Vref) • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)	• Output from internal D/A converter • Input from internal A/D converter input pin (one selectable)
ACMPHS output	• Comparison result • Generation of ELC event output • Monitoring of output from register	• Comparison result • Generation of ELC event output • Monitoring of output from register
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Rising edge, falling edge, or both edges can be selected.	• Interrupt request generated on valid edge detection from comparison result • Rising edge, falling edge, or both edges can be selected.
Digital filter function	• One of three sampling frequencies can be selected. • Not using the filter function can be selected.	• One of three sampling frequencies can be selected. • Not using the filter function can be selected.

Table 49. Comparison of the Input Source Configurations of High-Speed Analog Comparators

Item		RA6T1 (ACMPHS)	RA6T2 (ACMPHS)
ACMPHS0	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	IVREF3: DA0 IVREF2: DA3 IVREF1: AN017 IVREF0: AN016
	Analog voltage input source	IVCMP3: PGA0 output*5 IVCMP2: AN000*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	IVCMP3: PGA0 output IVCMP2: AN000 IVCMP1: — IVCMP0: AN012
	Output pin	VCOUT*6	VCOUT*6, CMPOUT012*7, CMPOUT0
ACMPHS1	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	IVREF3: DA1 IVREF2: DA3 IVREF1: AN017 IVREF0: AN016
	Analog voltage input source	IVCMP3: PGA1 output*5 IVCMP2: AN001*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	IVCMP3: PGA1 output IVCMP2: AN002 IVCMP1: — IVCMP0: AN013
	Output pin	VCOUT*6	VCOUT*6, CMPOUT012*7, CMPOUT1

Item		RA6T1 (ACMPHS)	RA6T2 (ACMPHS)
ACMPHS2	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	IVREF3: DA2 IVREF2: DA3 IVREF1: AN017 IVREF0: AN016
	Analog voltage input source	IVCMP3: PGA2 output*5 IVCMP2: AN002*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	IVCMP3: PGA2 output IVCMP2: AN004 IVCMP1: — IVCMP0: AN014
	Output pin	VCOUT*6	VCOUT*6, CMPOUT012*7, CMPOUT2
ACMPHS3	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	IVREF3: DA3 IVREF2: DA2 IVREF1: AN017 IVREF0: AN016
	Analog voltage input source	IVCMP3: PGA3 output*5 IVCMP2: AN100*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	IVCMP3: PGA3 output IVCMP2: AN018 IVCMP1: — IVCMP0: AN015
	Output pin	VCOUT*6	VCOUT*6, CMPOUT3
ACMPHS4	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	—
	Analog voltage input source	IVCMP3: PGA4 output*5 IVCMP2: AN101*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	
	Output pin	VCOUT*6	
ACMPHS5	Reference voltage input source	IVREF3: DA0*1 IVREF2: Vref*2 IVREF1: AN116 IVREF0: AN016	—
	Analog voltage input source	IVCMP3: PGA5 output*5 IVCMP2: AN102*3,*5 IVCMP1: DA1*4 IVCMP0: AN017	
	Output pin	VCOUT*6	

Note 1. When D/A converter 0 output is not used, the signal can be used as AN005/AN105 analog input.
Note 2. Internal voltage reference
Note 3. Because input is through PGA, the corresponding module-stop bit MSTPCRD.MSTPD16 (unit 0), or MSTPCRD.MSTPD15 (unit 1) must be set to 0.
Note 4. When D/A converter 1 output is not used, the signal can be used as AN006/AN106 analog input.
Note 5. Setting of ADC12 is required.
Note 6. Compare outputs are bundled with the VCOUT pin.
Note 7. Compare outputs are bundled with the CMPOUT012 pin.

2.33 Data Operation Circuit

Table 50 shows a Comparative overview of Data Operation Circuit.

Table 50. Comparative Overview of Data Operation Circuit

Item	RA6T1 (DOC)	RA6T2 (DOC)
Data operation function	16-bit data comparison, addition, and subtraction	16- or 32-bit data comparison, comparison to detect data above or below thresholds, and window comparison 16- or 32-bit data addition, and subtraction
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Interrupts and event link function	An interrupt is generated on the following conditions: • Compared values either match or mismatch. • The result of data addition is greater than FFFFh. • The result of data subtraction is less than 0000h.	Interrupts: • The compared values match the detection condition. • The result of data addition is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1). • The result of data subtraction is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000h (DOCR.DOBW = 1). Event link function (output): • The compared values match the detection condition. • The result of data addition is greater than 0xFFFF (DOCR.DOBW = 0) or 0xFFFF_FFFF (DOCR.DOBW = 1). • The result of data subtraction is less than 0x0000 (DOCR.DOBW = 0) or 0x0000_0000 (DOCR.DOBW = 1).
TrustZone Filter	—	The security attribution can be set.

2.34 SRAM

Table 51 shows a Comparative overview of SRAM.

Table 51. Comparative Overview of SRAM

Item	RA6T1	RA6T2
SRAM capacity	SRAMHS: 64 KB	SRAM0: 64 KB
SRAM address	SRAMHS: 1FFE 0000h to 1FFE FFFFh	SRAM0: 0x2000_0000 to 0x2000_FFFF
Access	Access to the SRAMHS always requires no wait state.	No wait states are inserted into the read cycle.
Data retention function	Not available in Deep Software Standby mode	Not available in Deep Software Standby mode
Module-stop function	Module-stop state can be set to reduce power consumption.	Module-stop state can be set to reduce power consumption.
Parity	Even-parity (data: 8 bits, parity: 1 bit)	—
Error checking	Even-parity error check	SEC-DED (Single-Error Correction and Double-Error Detection Code)
Security	—	TrustZone Filter is integrated for memory access and SFR access. Access to the memory space is controlled by setting the memory Security Attribution (SA), and access to I/O space (SFR) is controlled by setting the register SA.

2.35 Flash Memory

Table 52 and Table 53 provide comparative overviews of flash memory.

Table 52. Comparative Overview of Flash Memory (code flash memory specifications)

Item	RA6T1	RA6T2
Memory capacity	Up to 512 KB of user area	User area: 512 KB max
Read cycle	• 80 MHz < ICLK frequency ≤ 120 MHz Cache hit: 1 cycle Cache miss: 3 cycles • 40 MHz < ICLK frequency ≤ 80 MHz Cache hit: 1 cycle Cache miss: 2 cycles • ICLK frequency ≤ 40 MHz Cache hit: 1 cycle Cache miss: 1 cycle	• CPU cache hit: 1 cycle • CPU cache disabled or missed: Flash cache hit: 3 cycles Flash cache disabled or missed: — (FLWT = 0x00) 3 cycles — (FLWT = 0x01) 4 cycles
Value after erasure	FFh	0xFF
Programming/erasing methods	• Programming and erasure of code and data flash memory through the FACI commands specified in the FACI command issuing area (407E 0000h) • Programming by dedicated flash-memory programmer transfer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming)	• Programming and erasing the code flash memory and data flash memory, and programming the option-setting memory are handled by the FACI commands specified in the FACI command issuing area (0x407E_0000) (self-programming). • Programming/erasure through transfer by a serial-programmer via a serial interface (serial programming)
Protection	Protection against erroneous overwriting of flash memory	Protects against erroneous rewriting of the flash memory
Background operations (BGOs)	• Data flash memory can be read during code flash memory programming. • Code flash memory can be read during data flash memory programming.	• The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.
Units of programming and erasure	• 128-byte units for programming in user area • Block units for erasure in user area	• Units of programming for the user area: 128 bytes • Units of erasure for the user area: Block units
Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings.	In the initial settings of this MCU, an expansion area of the option-setting memory can be set.

Item	RA6T1	RA6T2
On-board programming (three types)	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically Programming in on-chip debug mode: • JTAG or SWD interface used • Dedicated hardware not required Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system.	Programming/erasure in boot mode (for the SCI interface) • The asynchronous serial interface (SCI9) is used. • The transfer rate is adjusted automatically. Programming/erasure in On-chip debug mode • JTAG or SWD interface is used. Programming and erasure by self-programming • This allows code flash memory programming/erasure without resetting the system.
Unique ID	—	A 16-byte ID code provided for each MCU
FACI command	—	Program: 128 bytes Block erase: 1 block (8 KB or 32 KB) P/E suspend P/E resume Forced Stop Status Clear Configuration set (16 bytes)
Security function	Protection against illicit tampering or reading of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory **Startup area select setting protection** • BTFLG and FSUACR registers are protected by the FSPR bit. Permanent block protect setting protection • Code flash memory is permanently protected from programming/erasure operation by the permanent block protect function. Flash memory protection for TrustZone • Protection for flash memory area (P/E) • Protection for flash memory area (read) • Protection for register • Protection during FACI command operation • Code flash P/E mode entry protection

Item	RA6T1	RA6T2
Safety function	Software protection Error protection Boot program protection • The start-up area select function allows the user to safely update the boot firmware. The size of the start-up area is 8 KB.	Software protection • FACI command protection by FENTRYR register • Flash memory is protected by FWEPROR register. • The user area is protected by the block protect setting. Error protection • Error is detected when unintended commands or prohibited settings occur. The FACI command is not accepted after an error detection. Boot area protection • The start-up area select function allows the user to safely update the boot firmware. The size of the start-up area is 8 KB.
Interrupt request	• FCU_FRDYI • FCU_FIFERR	• FRDYI (flash sequencer ready (processing end)): Enabled by the FRDYIE bit • FIFERR (flash sequencer error): Enabled by the CFAEIE/CMDLKIE/DFAEIE bits
Address conversion	• Start-up area select function is supported.	• Start-up area select function is supported.

Table 53. Comparative Overview of Flash Memory (data flash memory specifications)

Item	RA6T1	RA6T2
Memory capacity	8 KB of data area	Data area: 16 Kbytes
Read cycles	A read operation takes 7 FCLK cycles in words or bytes (FCLK frequency is up to 60 MHz).	• CPU cache hit: 1 cycle • CPU cache disabled or missed: — (FCKMHZ = 0x00 to 0x09) Min: 2 ICLK + 3 FCLK Max: (n + 1) ICLK + 3 FCLK — (FCKMHZ = 0x0A to 0x13) Min: 2 ICLK + 4 FCLK Max: (n + 1) ICLK + 4 FCLK — (FCKMHZ = 0x14 to 0x1D) Min: 2 ICLK+ 5 FCLK Max: (n + 1) ICLK + 5 FCLK — (FCKMHZ = 0x1E to 0x27) Min: 2 ICLK+ 6 FCLK Max: (n + 1) ICLK + 6 FCLK — (FCKMHZ = 0x28 to 0x31) Min: 2 ICLK+ 7 FCLK Max: (n + 1) ICLK + 7 FCLK — (FCKMHZ = 0x32 to 0x3B) Min: 2 ICLK+ 8 FCLK Max: (n + 1) ICLK + 8 FCLK — (FCKMHZ = 0x3C) Min: 2 ICLK+ 9 FCLK Max: (n + 1) ICLK + 9 FCLK

Item	RA6T1	RA6T2
Value after erasure	Undefined	Undefined
Programming/erasing methods	• Programming and erasure of code flash memory and data flash memory through the FACI commands specified in the FACI command issuing area (407E 0000h) • Programming by dedicated flash-memory programmer transfer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming)	• Programming and erasing of the code flash memory and data flash memory, and programming of the option-setting memory are handled by the FACI commands specified in the FACI command issuing area (0x407E_0000) (self-programming). • Programming/erasure through transfer by a serial-programmer via a serial interface (serial programming)
Protection	Protection against erroneous overwriting of flash memory	Protects against erroneous rewriting of the flash memory

Note : When the frequency ratio of ICLK : FCLK is n : 1

Item	RA6T1	RA6T2
Background operations (BGOs)	• Data flash memory can be read during code flash memory programming. • Code flash memory can be read during data flash memory programming.	• The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.
Units of programming and erasure	• 4/8/16-byte units for programming in data area • 64/128/256-byte units for erasure in data area	• Unit of programming for the data area: 4/8/16 bytes • Unit of erasure for the data area: 64/128/256 bytes
Other functions	Interrupts can be accepted during self-programming.	Interrupts can be accepted during self-programming.
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings.	In the initial settings of this MCU, an expansion area of the option-setting memory can be set.
On-board programming (three types)	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically Programming in on-chip debug mode: • JTAG or SWD interface used • Dedicated hardware not required Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system.	Programming/erasure in boot mode (for the SCI interface) • The asynchronous serial interface (SCI9) is used. • The transfer rate is adjusted automatically. Programming/erasure in On-chip debug mode: • JTAG or SWD interface is used. Programming and erasure by self-programming • This allows code flash memory programming/erasure without resetting the system.
Unique ID	—	A 16-byte ID code provided for each MCU

Item	RA6T1	RA6T2
FACI command	—	Program: 4/8/16 bytes Block Erase: 1 block (64 bytes) Multi Block Erase: 64/128/256 bytes P/E suspend P/E resume Forced Stop Blank Check: 4 bytes to data flash memory capacity Status Clear
Security function	Protection against illicit tampering or reading of data in flash memory	Protects against illicit tampering with or reading out of data in flash memory **Startup area select setting protection** • BTFLG and FSUACR registers are protected by the FSPR bit. **Permanent block protect setting protection** • Code flash memory is permanently protected from programming/erasure operation by the permanent block protect function.
		Flash memory protection for TrustZone • Protection for flash memory area (P/E) • Protection for flash memory area (read) • Protection for register • Protection during FACI command operation
		• Code flash P/E mode entry protection
Safety function	Software protection Error protection Boot program protection • The start-up area select function allows the user to safely update the boot firmware. The size of the start-up area is 8 KB.	Software protection • FACI commands are protected by the FENTRYR register. • Flash memory is protected by the FWEPROR register. • The user area is protected by the block protect setting. Error protection • Error is detected when unintended commands or prohibited settings occur. The FACI command is not accepted after an error detection. Boot area protection • The start-up area select function allows the user to safely update the boot firmware. The size of the start-up area is 8 KB.
Interrupt request	• FCU_FRDYI: Enabled by the FRDYIE bit*1 • FCU_FIFERR: Enabled by the CFAEIE/CMDLKIE/DFAEIE bits*1	• FRDYI (flash sequencer ready (processing end)): Enabled by the FRDYIE bit • FIFERR (flash sequencer error): Enabled by the CFAEIE/CMDLKIE/DFAEIE bits
Address conversion	• Start-up area select function is supported.	• Start-up area select function is supported.

Note 1. This information is found in the APN "R01AN5367EU120 Rev1.20".

2.36 Internal Voltage Regulator

Table 54 shows a comparative overview of internal voltage regulator.

Table 54. Comparative Overview of Internal Voltage Regulator

Item	RA6T1	RA6T2
All VCC pins	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL and VCL0 pins	Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.	100-pin product: Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin. 64- or 48-pin product: Connect the pin to VSS through a 0.22-µF multilayer ceramic capacitor. Place the capacitor close to the pin.

3. Comparison of Pin Assignments

The following shows comparison of pin assignments. Red text indicates pins that are different between the two groups.

3.1 100-Pin Package

Figure 3 shows a Comparison of pin assignment for the 100-pin package.

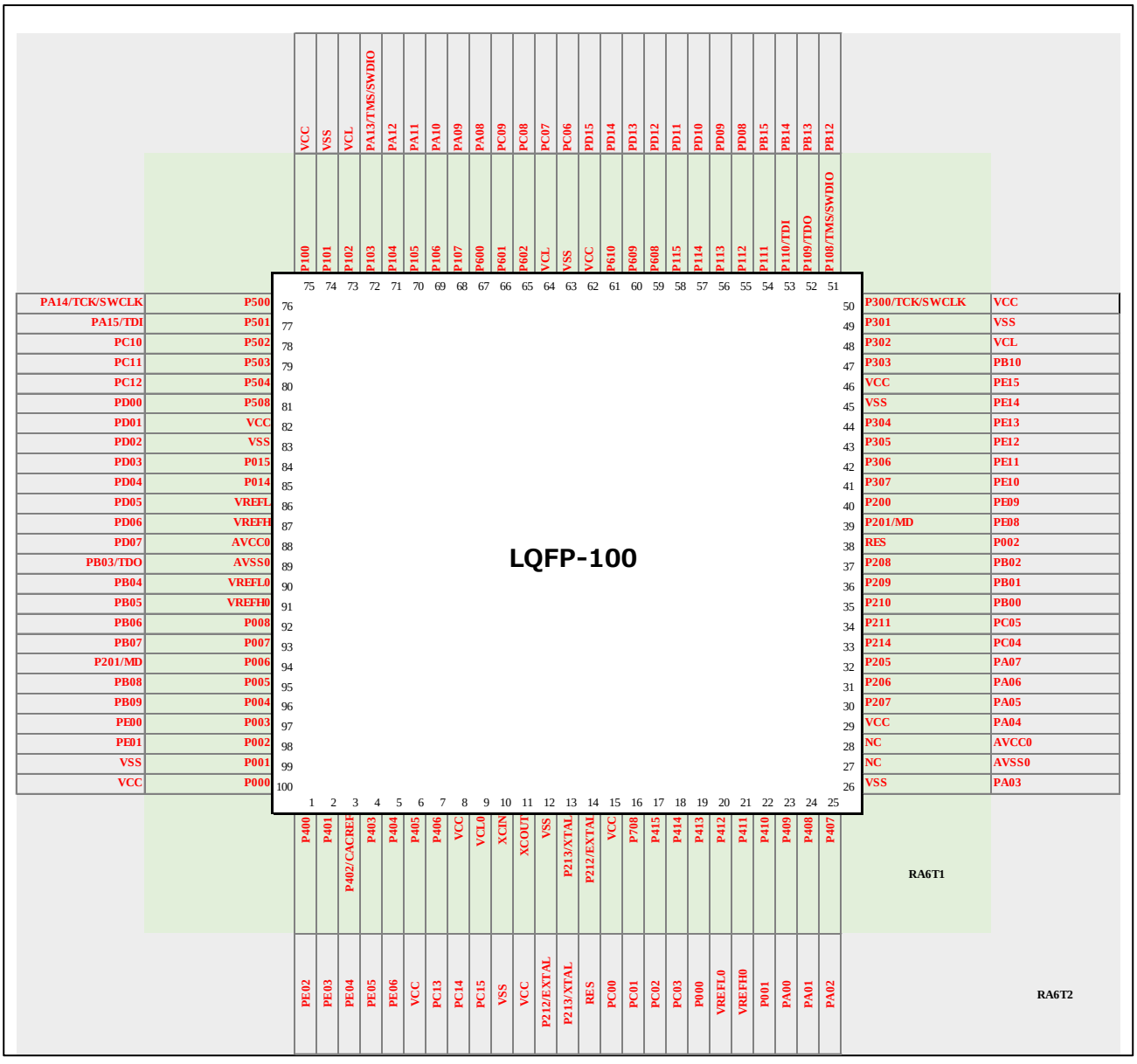


Figure 3. Comparison of Pin Assignment for the 100-pin Package

3.2 64-Pin Package

Figure 4 shows a Comparison of pin assignment for the 64-pin package.

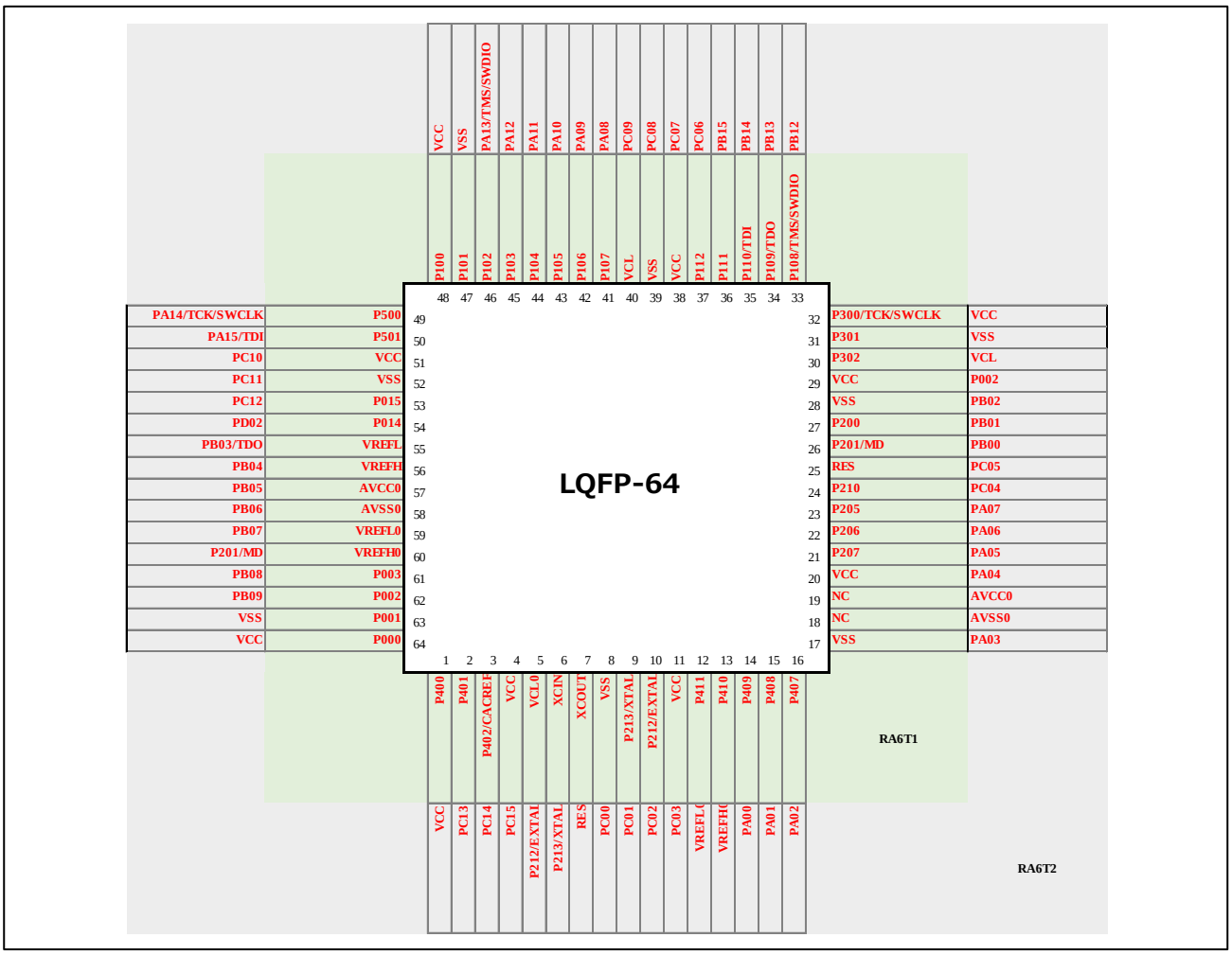


Figure 4. Comparison of Pin Assignment for the 64-pin Package

4. Notes on Porting Programs between MCUs

Some points to note regarding differences in programs between products of the RA6T1 and RA6T2 groups should be observed. Section 4.1, Notes on Functional Design gives details regarding the software.

4.1 Notes on Functional Design

Software for products of the RA6T1 group or RA6T2 group has a high degree of cross-compatibility between the groups. Nevertheless, sufficient evaluation is required due to differences in aspects such as the timing of operations and electrical characteristics. This section describes software-related points to note regarding differences between products of the RA6T1 and RA6T2 groups in terms of peripheral-module settings, functionality, timing, and other items. For differences between modules and functions, see 2.Comparative Overview of Specifications. For details, refer to the User's Manuals Hardware listed in 6. References.

4.1.1 Main Clock Oscillator Drive Capability Auto Switching Function

In the RA6T1 group products, the drive capability of the auto switching function automatically reduces the drive capability of the main clock oscillator and suppresses the EMI associated with the main clock oscillator. In the RA6T2 group products, you must manually switch the drive capacity as required.

4.1.2 Register Access

(1) Invalid register write accesses during specific modes or transitions

The conditions for writing to registers differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

[Registers]

- All registers with a peripheral name of SYSTEM

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- When FENTRYR.FENTRYi = 1 (i = 0 to 3) (flash P/E mode) or FENTRYR.FENTRYD = 1 (data flash P/E mode)
- RA6T2:

[Registers]

- All registers with a peripheral name of SYSTEM

[Conditions]

- OPCCR.OPCMTSF = 1 (during transition of the operating power control mode)
- During the time period from executing a WFI instruction to returning to Normal mode
- FENTRYR.FENTRYC = 1 or FENTRYR.FENTRYD = 1 (flash P/E mode, data flash P/E mode)

(2) Valid settings for the clock-related registers

The valid settings of the clock-related registers in each operating power control mode differ between products of the RA6T1 and RA6T2 groups. For details, see Table 55 and Table 56.

Table 55. Valid Settings for the Clock-related Registers (1)

Item		RA6T1	RA6T2
SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock) 101b (PLL)*1	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 101b (PLL)*1
	Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock)	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock)
	Subosc-speed	010b (LOCO) 100b (Sub-clock)	—
SCKDIVCR.FCK[2:0], ICK[2:0]	High-speed	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)
	Low-speed		
	Subosc-speed	000b (1/1)	—
PLLCR.PLLSTP	High-speed	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
	Low-speed	1 (stopped)	1 (stopped)
	Subosc-speed	1 (stopped)	—
PLL2CR.PLL2STP	High-speed	—	0 (operating) 1 (stopped)
	Low-speed		1 (stopped)
	Subosc-speed		—
HOCOCR.HCSTP	High-speed	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
	Low-speed		
	Subosc-speed	1 (stopped)	—
MOCOCR.MCSTP	High-speed	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
	Low-speed		
	Subosc-speed	1 (stopped)	—
LOCOCR.LCSTP	High-speed	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
	Low-speed		
	Subosc-speed	0 (operating) 1 (stopped)	—
MOSCCR.MOSTP	High-speed	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
	Low-speed		
	Subosc-speed	1 (stopped)	—
SOSCCR.SOSTP	High-speed	0 (operating) 1 (stopped)	—
	Low-speed		
	Subosc-speed	0 (operating) 1 (stopped)	

Note 1. SCKSCR.CKSEL[2:0] only

Table 56. Valid Settings for the Clock-related Registers (2)

Item		RA6T1	RA6T2
OPCCR.OPCM[1:0]	PLL	00b	00b
	PLL2	—	00b
	High-speed on-chip oscillator	00b, 11b	00b, 11b
	Middle-speed on-chip oscillator		
	Main clock oscillator		
	Low-speed on-chip oscillator	00b, 11b	00b, 11b
	Sub-clock oscillator	00b, 11b	—
	IWDT-dedicated on-chip oscillator	00b, 11b	00b, 11b
SOPCCR.SOPCM	PLL	0	—
	PLL2	—	—
	High-speed on-chip oscillator	0	—
	Middle-speed on-chip oscillator		—
	Main clock oscillator		—
	Low-speed on-chip oscillator	0, 1	—
	Sub-clock oscillator		—
	IWDT-dedicated on-chip oscillator		—

(3) Invalid register write accesses by the DTC or DMAC

The registers that cannot be written to by the DTC or DMAC differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

[Register]

- MSTPCRA

RA6T2:

[Registers]

- MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, and MSTPCRE

(4) Invalid register write accesses in Snooze mode

The registers that cannot be written to in Snooze mode differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

[Registers]

- SNZCR, SNZEDCR, and SNZREQCR

RA6T2:

[Registers]

- SNZCR, SNZEDCR0, and SNZREQCR0

(5) Invalid register write accesses to FLWT.FLWT[2:0]

In the RA6T1 group products, do not write any value other than 000b to the FLWT.FLWT[2:0] bits under the following condition.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(6) Invalid register write accesses when the PRCR.PRC1 bit is 0

The registers that cannot be written to when the PRCR.PRC1 is 0 differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIERn (n = 0 to 3), DPSIFRn (n = 0 to 3), DPSIEGRn (n = 0 to 2), and SYOCDCR

RA6T2:

[Registers]

- SBYCR, SNZCR, SNZEDCR0, SNZREQCR0, OPCCR, DPSBYCR, DPSWCR, DPSIERn (n = 0 to 2), DPSIFRn (n = 0 to 2), DPSIEGRn (n = 0 to 2), and SYOCDCR

4.1.3 Using UART of SCI0 in Snooze Mode

When using SCI0 in Snooze mode In the RA6T1 group products, the AGT1 underflow must be used for the interrupt request or snooze end request. When using UART in Snooze mode in the RA6T2 group products, ensure that the snooze request (RXD0 falling edge) does not conflict with the wakeup requests set by the WUPEN register. The conditions that must be satisfied for using SCI0 in Snooze mode differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- The clock source must be HOCO.
- MOCO, the main clock oscillator, and the PLL must be stopped before entering Software Standby mode.
- The RXD0 pin must be kept at the high level before entering Software Standby mode.
- A transition to Software Standby mode must not occur during an SCI communication.
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

RA6T2:

- The clock source must be HOCO.
- MOCO, PLL, PLL2, and main clock oscillator must be stopped before entering Software Standby mode.
- The RXD0 pin must be kept high before entering Software Standby mode.
- A transition to Software Standby mode must not occur during an SCI0 communication.
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

4.1.4 ELC Events in Snooze Mode

The ELC events available in Snooze mode differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC12n Window A/B compare match (ADC12n_WCMPM) (n = 0, 1)
- ADC12n Window A/B compare mismatch (ADC12n_WCMPUM) (n = 0, 1)
- Data operation circuit interrupt (DOC_DOPCI)

RA6T2:

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC Composite compare match 0 (ADC_CCMPM0)
- ADC Composite compare match 1 (ADC_CCMPM1)
- Data operation circuit interrupt (DOC_DOPCI)

4.1.5 Module-Stop Bit Write Timing

In the RA6T2 group products, it is possible to access the I/O register before the corresponding module-stop bit write completes. In this case, access to the I/O register may not proceed as intended. To avoid this issue, before accessing the I/O register, read back the module-stop bit that was written to confirm that the write is completed.

4.1.6 Cache Line Configuration Register

In the RA6T2 group products, writes to the Cache Line Configuration Register are allowed when the status is cache off (CACTL.ENS = 0 for S-cache, CACTL.ENC = 0 for C-cache).

4.1.7 Coherency

In the RA6T2 group products, the coherency between the cache and the internal SRAM must be guaranteed by software. When allocating shared memory between the CPU and a bus master such as DMAC in the cache support area, invalidate the cache data as necessary.

4.1.8 Security MPU

In the RA6T1 group products, the protected memory cannot be debugged if the security MPU is enabled. Disable the security MPU when debugging a secure program.

4.1.9 Access to the Registers during DMA Transfer

The registers that cannot be written to while the DMAC active state or DMA transfer enabled is set for the associated channel differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- DMSAR, DMDAR, DMCRA, DMCRB, DMTMD, DMINT, DMAMD, and DMOFR

RA6T2:

- DMSAR, DMDAR, DMCRA, DMCRB, DMTMD, DMINT, DMAMD, DMOFR, DMSBS, DMDBS, DMSRR, DMDRR, ICUSARC, and DMACSAR

4.1.10 When Resuming DMA Transfer

In the RA6T2 group products, a DMAC activation request might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMAC activation request is held in the DMAC. To prevent this, stop the DMAC activation requests by setting the DELSRn.DELS[8:0] bits in the ICU to 0.

When a DMAC activation request occurs after the last round of the DMA transfer is generated, clear the DMAC activation request with either of the following approaches.

- Clear the DMAC activation request with a DMA dummy transfer.
- Set the DMCNT.DTE bit to 0 and then set the ICU.DELSRn.IR flag to 0.

4.1.11 Interval of ELC Event Request

In the RA6T2 group products, if the clocks of Event Source and Event Destination are combined as shown in Table 57, the Event request may be lost if the interval between one Event request and the next is less than the following value (Event_Interval) for the same Event request signal.

However, this restriction does not apply if the Event Destination is GPT or ADC and uses a different ELSR register.

The event interval is expressed by the following formula:

Event_Interval [ns] = Period_of_Source_clock [ns] × 6 + Period_of_Destination_clock [ns] × 4

Table 57. Combination of Clocks with the Restricted Event Interval

Event Source	Source clock	Event Destination	Destination clock
Other than GPT	PCLKA or PCLKB	GPT	GPTCLK
		ADC	GPTCLK or PCLKC
GPT	PCLKD	ADC	GPTCLK or PCLKC
	GPTCLK	ADC	PCLKA or PCLKC
		DAC12	PCLKA
		I/O Port	PCLKB

4.1.12 Procedure for Specifying the Pin Functions

In the RA6T2 group products, when the security attribution of Pmn is set to 0, set the PWPRS register to write to the PmnPFS register.

4.1.13 Procedure for Using Port Group Input

To specify the rising, falling, or both edge detections for the port group input, set the PmnPFS.EOF/EOR bit in the RA6T1 group products, or set the EOFR[1:0] bits of the PmnPFS register in the RA6T2 group products.

4.1.14 Using Analog Functions

To use an analog function, specify the settings so that the pin acts as a general input port.

In the RA6T2 group products, the pin to which the PGA function (PGAINn, PGAVSSn (n = 0 to 3)) is assigned cannot be used as general ports when the PGA is set to pseudo-differential input mode.

When using the corresponding pin as general ports, set the corresponding PGA to single-ended input mode.

Then, set the corresponding pin to function as general ports.

4.1.15 Port mn Pin Function Select Register(PmnPFS) Setting

The notes on this register setting differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- In the Port mn Pin Function Select register (PmnPFS), the PSEL bits must be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, unexpected edges might be input for the input function or unexpected pulses might be output to the external pin for the output function.
- Only the allowed values (functions) should be specified in the PSEL bits of the PmnPFS register. If a value that is not allowed for the register is specified, the correct operation is not guaranteed.
- A single function should not be assigned to multiple pins by the PmnPFS register.
- PORT0 and PORT5 have analog functions such as the A/D converter and the D/A converter. When these pins are used as an analog function, to avoid loss of resolution, the PMR and PDR bits should be set to 0. After that, the ASEL bit should be set to 1.
- The initial value of the ASEL bit for P003 and P007 is 1. When these pins are not used as an analog function, to reduce the input leakage current, the ASEL bit should be set to 0. When using 64-pin product, clear the P007PFS.ASEL bit to 0.

RA6T2:

- In the Pmn Pin Function Select register (PmnPFS), the PSEL bits have to be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, the unexpected edges may be input at the input function or the unexpected pulses may be output to the external pin at the output function.
- Only the allowed values (functions) should be specified in the PSEL bits of the PmnPFS register. If a value which is not allowed for the register is specified, the correct operation is not guaranteed.
- The single function should not be assigned to the multiple pins by the PmnPFS register.
- The port 0 and ports A, B, C, and E have analog functions such as the A/D converter. When these pins are used as an analog function, in order to avoid the loss of resolution, the PMR bit should be set to 0 and PDR bit should be set to 0. After that, the ASEL bit should be set to 1.

4.1.16 Duplication of Requests to Stop Output for Port Output Enable for GPT

In the RA6T2 group products, while either the PIDF or IOCF flag in the POEGGn register is 1, cancellation of requests to stop by the detection signal set in the GTONCCRn register does not work. This is because the request to stop is still being output due to the value of the flag. That is, note that requests to stop output will not be canceled when a corresponding flag is set stop output in response to detection. Request signals to stop output in response to flag setting are obtained as the logical OR of the corresponding detection signals for stopping output.

4.1.17 Module-Stop Function Setting for GPT

In the RA6T2 group products, set the GTCLKCR register before releasing the module-stop state.

4.1.18 Priority Order of Each Event for GPT

(1) GTCR.CST bit

In the RA6T2 group products, if stop by the period count function conflicts with start by the CPU writing (GTCR register writing/GTSTR register writing), the period count function is finished with setting the GTST.PCF flag. The CST bit is not changed and the GTCNT continues to count.

(2) GTIOR.GTIOm registers

In the RA6T2 group products, when there is a conflict between buffer transfer operation and writing to the GTIOR.GTIOm register, writing to the GTIOR.GTIOm register has priority over buffer transfer operation.

When there is a conflict between updating the GTIOR.GTIOm register and reading by the CPU, pre-update data is read.

4.1.19 Interval of Interrupt Request for GPT

In the RA6T2 group products, when the core clock of GPT is GPTCLK, an interrupt may be lost if the interval between the same interrupt signal is shorter than the following value. However, this restriction does not apply to different interrupt signals.

Interrupt_Interval [ns] = Period_of_GPTCLK [ns] x 6 + Period_of_PCLKA [ns] x 4

Also, ADC can receive the A/D conversion start request from GPT without going through ELC by setting ADTRGGPTx register (x = 0 to 8).

When the clocks of GPT and ADC are combined as shown in Table 58, the A/D conversion start request may be lost if the interval between one A/D conversion start request and the next is less than the following value for the same A/D conversion start request. However, this restriction does not apply to different A/D conversion start requests.

Event_Interval [ns] = Period_of_GPT_core_clock [ns] x 6 + Period_of_ADC_core_clock [ns] x 4

Table 58. Combination of Clocks with the Restricted Event Interval

GPT core clock	ADC core clock
GPTCLK	PCLKA or PCLKC
PCLKD	PCLKC or GPTCLK

4.1.20 GTIOCnm Signal Input to PWM Delay Generation Circuit

In the RA6T2 group products, when controlling the delay of PWM waveform in PWM Delay Generation Circuit, the following limitations exist:

- In saw-wave mode, it is prohibited to change the GTIOCnm signal during the three clock cycles immediately before overflow or underflow.
- In saw-wave mode, it is prohibited to clear the GTCNT register by GTCSR during counting operation.
- In triangle-wave mode, it is prohibited to change the GTIOCnm signal during the three clock cycles immediately before trough.

If the above limitations are not followed, the edge of signal waveform output from PWM Delay Generation Circuit may disappear.

4.1.21 Register Write Interval for PWM Delay Generation Circuit

In the RA6T2 group products, when GPT core clock is GPTCLK, the written value may not be reflected if the interval between writing to the GTDLYRnA, GTDLYFnA, GTDLYRnB, or GTDLYFnA register is shorter than the following interval time. This restriction only applies to successive writes to the same register.

Write_Interval [ns] = Period_of_PCLKA [ns] x 6 + Period_of_GPTCLK [ns] x 4

4.1.22 Count Operation Start and Stop Control for AGT and AGTW

In the RA6T1 group products, clear the interrupt register before changing the TSTART bit from 0 to 1.

4.1.23 Output Pin Setting for AGT and AGTW

In the RA6T2 group products, when using the AGTWOn, AGTWIOn, AGTWOAn, or AGTWOBn pin as an output pin, set up the AGT and determine the initial output values. Then set the PmnPFS.PMR bit to 1.

When using the AGTWIOn pin as an input pin in pulse width measurement mode or pulse period measurement mode, set up the AGT and start the count operation. Then start to enter external events from the AGTWIOn pin. Invalidate the first measurement and validate the second and later completed measurements.

4.1.24 Reset of I/O Registers of the AGT and AGTW

In the RA6T1 group products, the I/O registers of the AGT and AGTW are not initialized by different types of resets. See below for details.

- RES pin reset: Not possible
- Power-on reset: Possible
- Voltage monitor 0 reset: Possible
- Independent watchdog timer reset: Not possible
- Watchdog timer reset: Not possible
- Voltage monitor 1 reset: Possible
- Voltage monitor 2 reset: Possible
- Software reset: Not possible
- SRAM parity error reset: Not possible
- Bus master MPU error reset: Not possible
- Bus slave MPU error reset: Not possible
- Stack pointer error reset: Not possible
- Deep Software Standby reset
  DEEPCUT[0] = 0: Not possible
- Deep Software Standby reset
  DEEPCUT[0] = 1: Possible

4.1.25 Selecting PCLKB, PCLKB/8, or PCLKB/2 as the Count Source of AGT or AGTW

In the RA6T1 group products, when a reset is generated, the operation of AGT cannot be guaranteed. Set the registers associated with AGT again.

4.1.26 Selecting AGTSCLK or AGTLCLK as the Count Source of AGT or AGTW

In the RA6T1 group products, the MSTPD2 bit in the MSTPCRD register must be set to 1 except when accessing the AGT1 registers. The MSTPD3 bit in the MSTPCRD register must be set to 1 except when accessing the AGT0 registers. When a reset occurs while MSTPD2 or MSTPD3 bit is 0, the operation of AGT1 or AGT0 cannot be guaranteed. Set the registers associated with AGT again.

4.1.27 ICU Event Link Setting Register n (IELSRn) Setting

Restrictions on setting of this register differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

Setting 47h to the ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1), or when enabling event link operation (ELSRm.ELS[8:0] = 47h).

RA6T2:

Setting 0x53 to ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x53).

Setting 0x52 to ICU Event Link Setting Register n (IELSRn.IELS[8:0]) is prohibited when enabling the IWDT reset assertion (OFS0.IWDTRSTIRQS = 0) or when enabling event link operation (ELSRn.ELS[8:0] = 0x52).

4.1.28 SCI Operation During Low Power Consumption State

The settings for using the power consumption reduction function differ between products of the RA6T1 and RA6T2 groups.

(1) Transmission

In the RA6T1 group products, stop the operation (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting the I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register. The TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected. The value is saved when FIFO is selected.

In the RA6T2 group products, do the following to confirm transmission end (CSR.TEND = 1):

- Set the output pin state after transmission operation is stopped by CCR1.SPB2DT, SPB2IO.
- Stop the transmission. (CCR0.TIE = 0, TE = 0, TEIE = 0).

To transmit data in the same transmission mode after cancellation of the low power consumption state, read SSR, SSR_FIFO, or SSR_SMCI in the RA6T1 group products, or read CSR in the RA6T2 group products.

(2) Reception

When using the address match function as a wakeup condition in the RA6T1 group products, set the CDR.CMPD and DCCR.DCME bits to 1 before enabling receive operations in the procedure for entering the low power mode. In the RA6T2 group products, set the compare data to CCR4.CMPD and set 1 to CCR0.DCME.

4.1.29 SCI Break Detection and Processing

In the RA6T1 group products with non-FIFO selected, a break can be detected by reading the RXDn pin value directly. In the RA6T2 group products, a break can be detected by reading the CSR.RXDMON bit value.

4.1.30 SCI Receive Error Flags and Transmit Operation in Clock synchronous and Simple SPI modes

In the RA6T1 group products, transmission cannot start when a receive error flag is set to 1, even if data is written to TDR or FTDRL. Therefore, be sure to set the receive error flags to 0 before starting transmission.

In the RA6T2 group products, transmission can start by writing transmit-data to TDR even if the receive error flag is set to 1. However, reception cannot be started.

4.1.31 Writing Data to TDR

(1) Non-FIFO selected

In the RA6T2 group products, data can be written to TDR anytime when CCR0.TE is 1. However, if new data is written to TDR when the transmit data is remaining in TDR, the previous data in TDR is lost because it has not been transferred to TSR yet. If you use DTC or DMAC, be sure to write the transmit data to TDR in the SCIn_TXI interrupt request handling routine.

(2) FIFO selected

In the RA6T2 group products, data can be written to transmit-FIFO(TDR) when CCR0.TE is 1. Check the number of writable data with the FTSR.T [5:0] bit.

4.1.32 Restrictions on SCI Clock Synchronous Transmission (Clock Synchronous Mode and Simple SPI Mode)

(1) Start of transmission

The wait time required from writing of the transmit data to TDR to the start of the external clock input differs between products of the RA6T1 and RA6T2 groups.

RA6T1:

1 PCLKA cycle + data output delay time for the slave (tDO) + setup time for the master (tSU), or longer

RA6T2:

Output AC spec of the MISO pin of this product and the input AC spec of the master reception + 1 PCLK cycle + synchronization delay, or longer

(2) Continuous transmission

In the RA6T1 group products, when updating TDR after bit [7] starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] (D7) to 4 PCLKA cycles or longer.

4.1.33 Restrictions on Using DMAC or DTC for SCI

(1) Non-FIFO selected

In the RA6T1 group products, data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when the transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not yet transferred to TSR. When using DMAC or DTC, be sure to write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

(2) FIFO selected

In the RA6T1 group products, it is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data using the FDR.T[4:0] bits.

4.1.34 External Clock Input for SCI in Clock Synchronous Mode and Simple SPI Mode

For the external clock SCKn input in clock synchronous mode and simple SPI mode in the RA6T1 group products, set 2 PCLKA cycles or more for the high-pulse period and low-pulse period, and 2 PCLKA cycles or more for the period.

4.1.35 Limitations on Simple SPI Mode for SCI

(1) Slave mode

The following wait times differ between products of the RA6T1 and RA6T2 groups.

The wait time required from writing of the transmit data to the TDR register to the start of the external clock input:

RA6T1:

1 PCLKA cycle + data output delay for the slave (tDO) + setup time for the master (tSU), or longer

RA6T2:

1 PCLK cycle + synchronization delay time + data output delay time (AC spec), or longer

The wait time required from the input of the low level on the SSn pin to the start of the external clock input

RA6T1:

At least 5 PCLKA cycles

RA6T2:

At least SSn input setup time (AC spec)

4.1.36 SCI Transmit Enable bit

In the RA6T2 group products, when the CCR0.TE bit is set to 0, the TXDn pin is placed in the high-impedance state in the initial register value. Prevent the TXDn line from entering the high-impedance state by using one of the following ways:

- Connect the pull-up resistance to the TXDn line.
- Before setting the CCR0.TE bit to 0, change the function of the pin to a general-purpose output port. After that, set the CCR0.TE bit to 1, and then change the function of the pin to TXDn.
- When the CCR0.TE bit is set to 0 in Asynchronous mode or Manchester mode, set CCR1 and the level determined for the TXDn pin.

The slave operation of the MISOn pin in Simple SPI mode is the same as for the above TXDn pin. Like the TXDn pin, prevent the MISOn pin from entering the high-impedance state by using the preceding step 1 or 2.

4.1.37 Register access when SCI operation clock is slower than bus clock

In the RA6T2 group products, if the operating clock (TCLK) is slower than the bus clock (PCLK), the time until this information is transmitted internally after writing to the CCR0.TE and CCR0.RE registers is slower than the bus access time. In particular, when trying to change the setting register after writing 0 and interrupting communication, do not change the setting register before the signal inside the IP is in the communication stopped state. To prevent this, after setting CCR0.TE and CCR0.RE to 0, check the CESR.TIST and CESR.RIST bits until they are 0 before setting the next register.

4.1.38 Interrupting SCI operation

In the RA6T2 group products, if 0 is written to CCR0.RE during data reception and the reception operation is interrupted, there is a possibility of an invalid state. In this case, do not use the received data (RDR register stored value) or the flag value of each status register. To interrupt the reception operation, stop the interrupt or event link reception side and then write 0 to the CCR0.RE bit.

4.1.39 SCI Common Control Register CCR3.BPEN Bit Setting

This register is only present in the RA6T2 group products. Set the BPEN bit only once when setting the CCR3 register in the SCI initialization flow. This bit cannot be changed after the initialization. To change this bit setting, start from the SCI initialization flow again.

4.1.40 Starting IIC Transfer

In the RA6T1 group products, if the IR flag associated with the IIC interrupt is 1 when the transfer is started (ICCR1.ICE bit = 1), follow the procedure in this section to clear the interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unexpected behavior of the IR flag.

To clear interrupts before starting transfer operation:

- Confirm that the ICCR1.ICE bit is 0.
- Set the relevant interrupt enable bits, such as ICIER.TIE, to 0.
- Read the relevant interrupt enable bits, such as ICIER.TIE, and confirm that the value is 0.
- Set the IR flag to 0.

4.1.41 Settings for the IIC Operating Clock

In the RA6T2 group products, the following relation is required between the frequencies of the bus clock (PCLKA) and transfer clock (IICCLK):

IICCLK/2 ≤ PCLKA ≤ IICCL

4.1.42 Settings for the CAN Operating Clock

In the RA6T1 group products, the following constraints must be satisfied.

When the CCLKS bit is 1: fPCLKB ≥ fCANMCLK

When the CCLKS bit is 0, the source of the peripheral module clock must be PLL.

4.1.43 Boundary Scan Function

In the RA6T1 group products, BSDL provides safe bits that must be configured according to the BSDL description. The pins that cannot be boundary-scanned differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- Power supply pins (VCC, VCL, VCL0, VSS, AVCC0, AVSS0)
- Analog reference pins (VREFH0, VREFL0, VREFH, VREFL)
- Clock pins (EXTAL, XTAL, XCIN, XCOUT)
- Reset pins (RES)
- Boundary-scan pins (TCK, TMS, TDI, TDO)

- RA6T2:
- Power supply pins (VCC, VCL, VSS, AVCC0, AVSS0)
- Analog reference pins (AVREFH0, AVREFL0)
- Clock pins (EXTAL, XTAL)
- Reset pins (RES)
- Boundary-scan pins (TCK, TMS, TDI, TDO)

4.1.44 Prohibition of changing the operation settings during A/D conversion operation

In the RA6T2 group products, the registers related to the operation setting of the A/D converter should be set while all A/D converters are stopped (ADSR.ADACTm = 0 and ADSR.CALACTm = 0 (m = 0, 1)). Changing (writing) of registers except for those listed below is prohibited during A/D conversion. If the operation setting is changed during A/D conversion, operation is not guaranteed.

[Registers that can be written while the A/D converter is operating]

- Status Clear Registers
  - Status clear registers related to A/D converter operation (ADERSCR, ADCALSCR, ADCALENDSCR, and ADSCANENDSCR)
  - A/D Conversion Overflow Status Clear Registers (ADOVFERSCR, ADOVFCHSCR0, and ADOVFEXSCR)
  - Limiter Clip Status Clear Registers (ADLIMGRSCR, ADLIMCHSCR0, and ADLIMEXSCR)
  - Compare Match Status Clear Registers (ADCMPTBSCR, ADCMPCHSCR0, and ADCMPEXSCR)
  - FIFO Error Status Clear register (ADFIFOERSCR)
- Software Trigger Registers (ADSYSTR, and ADSTRn (n = 0 to 8))
- A/D Converter Stop Register (ADSTOPR)
- A/D Converter Start Trigger Enable Register (ADTRGENR)*1

Writing during operation is only permitted for disabling the trigger input (ADTRGENR.STTRGENn = 0 (n = 0 to 8)) in order to stop the A/D conversion. To avoid unintended operation, do not change the trigger input to Enable (ADTRGENR.STTRGENn = 1) during operation.

4.1.45 Forced Stop of A/D Conversion Operation

The procedure for forced stop of A/D conversion operation differs between products of the RA6T1 and RA6T2 groups. For details, see Table 59 and Table 60.

Table 59. Procedure for Forced Stop of A/D Conversion Operation in the RA6T1 Group Products

No.	Procedure	Description
1	Disabling group A priority control	If the ADGSPCR.PGS bit is set to 1, set this bit to 0.
2	Disabling trigger input	In group scan mode, set the ADSTRGR register to 3F3Fh (set the TRSA[5:0] bit to 3Fh, and TRSB[5:0] bit to 3Fh) to disable the trigger input and set the ADCSR.GBADIE bit to 0 to prevent scan end interrupt. For any mode other than group scan mode, set the ADSTRGR.TRSA[5:0] bit to 3Fh to disable trigger inputs.
3	Disabling scan end events	If the scan end event is set at the ELC, set the ELSRn.ELS[8:0] bit to 000h.
4	Forcibly stopping the A/D converter	Set the ADCSR.ADST bit to 0 to perform software clear operation. Stop A/D conversion. A maximum of two ADCLK cycles are required.
5	End	Processing of forced stop is completed. A maximum of six ADCLK cycles are required to restart A/D conversion.

Table 60. Procedure for Forced Stop of A/D Conversion Operation in the RA6T2 Group Products

No.	Procedure	Description
1	Disabling trigger input	Disable the trigger input from the peripheral module. (Write ADTRGENR.STTRGENn = 0)
2	Waiting time	After setting the above Step 1, a wait time is required to safely stop the A/D converter. Proceed to the next processing after the specified waiting time has elapsed.
3	Checking the A/D converter status	Check if the A/D converter is operating after the waiting time of the above Step 2 has elapsed. If the A/D converter is running (ADSR.ADACTm = 1), proceed to Step 4. If the A/D converter is stopped (ADSR.ADACTm = 0), no further processing is required (proceed to Step 6).
4	Forcibly stopping the A/D converter	Forcibly stop the A/D converter by the ADSTOPR register. (Write ADSTOPR.ADSTOPm = 1)
5	Waiting for the A/D converter to stop	Wait until the A/D converter stops. (ADSR.ADACTm = 0)
6	End	Processing of forced stop is completed.

4.1.46 A/D Data Registers

The RA6T1 group products have the following constraints on reading registers.

The following registers must be read in halfword units:

- A/D Data Register
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register

If a register is read twice in byte units, that is, the upper byte and lower byte are read separately, the A/D-converted value initially read might not match with the A/D-converted value subsequently read. To prevent this, never read the data registers in byte units.

In the RA6T2 group products, when A/D conversion is performed multiple times on the same analog channel and you intend to keep the data for each A/D conversion for the same analog channel, perform one of the following methods:

- Read out data from registers at each scanning operation
  - At the end of scanning each scan group, read out the A/D conversion data of the analog channel that was subject to A/D conversion from ADDRn or ADEXDRm.
  - This method is effective if A/D conversion of the same analog channel is not performed more than once in the same scan group, and A/D conversion data can be read from the registers before the next scanning operation.
- Use FIFO function to hold data for each A/D conversion
  - By using FIFO, multiple A/D conversion data for the same analog channel can be kept.
  - Read out the A/D conversion data before FIFO overflow occurs.

4.1.47 Restrictions on Entering and Releasing the Low-Power States of ADC or ADC12

In the RA6T2 group products, when operating the A/D converter after the module-stop state or software standby mode is released, wait for the operation stabilization time specified in the Electrical Characteristics, execute Self-Calibration operation, and then start A/D conversion.

Also, when releasing the module-stop state again after entering into the module-stop state, make sure the shutdown time specified in the Electrical Characteristics has elapsed before releasing the module stop state.

Operations are not guaranteed if these restrictions are violated.

4.1.48 Using Analog Channels to which the PGA is Connected

The following notes apply to the RA6T1 group products.

When the PGA is used with pseudo-differential input enabled, a negative voltage can be input for AN000 to AN002 and PGAVSS000 for unit 0, and AN100 to AN102 and PGAVSS100 for unit 1 after setting the registers.

When the PGA is used with pseudo-differential input enabled, all PGA amplifiers in each unit must be set to pseudo differential input in the ADPGADCR0 register.

When the PGA is used with pseudo-differential input disabled, the associated PGAVSS pin must be connected to AVSS0. When the PGA is not used, the associated PGAVSS can be used as an input port or analog input.

When transitioning to the ADC module-stop state or Software Standby mode from the state of using PGA or sample-and-hold circuit, if the corresponding bit in ADPGACR or ADSHCR register of each ADC12 is set to 0 before transitioning, power consumption can be reduced.

The initial value of the ASEL bit of P003 and P007 is 1. When these pins are not used as an analog function, the ASEL bit should be set to 0 to reduce the input leakage current.

In the RA6T2 group products, the analog input pin, which is connected to PGA, is limited by the port function and the analog path depending on the PGA setting. The initial status of PGA setting after reset released depends on the setting on PGADEN[3:0] bits in Option Function Select Register 1 (OFS1, OFS1_SEC, OFS1_SEL).

4.1.49 ADC12 Operating Modes and Status Bits

In the RA6T1 group products, initialize or set again individually, if necessary, the voltage values in self-diagnosis, the determination of the first scan or second scan in double-trigger mode, and the status monitor bit in the compare function.

- Select the voltage values in self-diagnosis (ADCER.DIAGVAL[1:0]) after setting ADCER.DIAGLD to 1.
- Double trigger mode operates as the first scan after setting ADCSR.DBLE to 1 from 0.
- The status monitor bits (MONCMPA, MONCMPB, and MONCOMB) in the compare function are initialized after ADCMPCR.CMPAE and ADCMPCR.CMPBE are set to 0.
- The constant sampling function (ADSHMSR.SHMD = 1) is initialized after ADSHMSR.SHMD is set to 0. When the constant sampling function is used (setting ADSHMSR.SHMD = 1) again, wait 1 ADCLK cycle or more.

4.1.50 Port Settings when Using the ADC12 Input

When using the high-precision channels in the RA6T1 group products, do not use PORT 0 as a digital output port. Renesas also recommends not using the digital output that is also used as the A/D analog input, if normal precision channels are used. If the digital output that is also used as the A/D analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

4.1.51 Relationship between ADC12 Units 0 and 1 and the ACMPHS

In the RA6T1 group products, unit 0 and 1 cannot perform A/D conversion at the same time for the A/D conversion targets in Table 61.

Table 61. Mutually Exclusive A/D Conversion Targets

A/D conversion target	
Unit 0	**Unit 1**
Temperature sensor	
Internal reference voltage	
AN005/DA0	AN105/DA0
AN006/DA1	AN106/DA1

The A/D conversion targets in Table 62 should not be selected as ACMPHS input during A/D conversion, because these pins are multiplexed with the ADC12 and ACMPHS.

Table 62. ACMPHS Pins That Cannot Be Selected During A/D Conversion

A/D conversion target		
Unit 0	**Unit 1**	**ACMPHS**
AN000	—	ACMPHS0.IVCMP2
AN001	—	ACMPHS1.IVCMP2
AN002	—	ACMPHS2.IVCMP2
PGA P000 output	—	ACMPHS0.IVCMP3
PGA P001 output	—	ACMPHS1.IVCMP3
PGA P002 output	—	ACMPHS2.IVCMP3
AN005/DA0	—	ACMPHS0 to ACMPHS5.IVREF3
AN006/DA1	—	ACMPHS0 to ACMPHS5.IVCMP1
AN016	—	ACMPHS0 to ACMPHS5.IVREF0
AN017	—	ACMPHS0 to ACMPHS5.IVCMP0
Internal reference voltage	—	ACMPHS0 to ACMPHS5.IVREF2
—	AN100	ACMPHS3.IVCMP2
—	AN101	ACMPHS4.IVCMP2
—	AN102	ACMPHS5.IVCMP2
—	PGA P000 output	ACMPHS3.IVCMP3
—	PGA P001 output	ACMPHS4.IVCMP3
—	PGA P002 output	ACMPHS5.IVCMP3
—	AN105/DA0	ACMPHS3 to ACMPHS5.IVREF3
—	AN106/DA1	ACMPHS3 to ACMPHS5.IVCMP1
—	AN116	ACMPHS0 to ACMPHS5.IVREF1
—	Internal reference voltage	ACMPHS0 to ACMPHS5.IVREF2

4.1.52 ADC Synchronous Operation

In the RA6T2 group products, the Synchronous Operation function is enabled in the initial state after reset released. If Synchronous Operation function is not used, disable Synchronous Operation in the ADSYCR register.

4.1.53 Analog Channel shared among multiple A/D Converters

In the RA6T2 group products, to avoid degradation of the accuracy of the A/D conversion result, A/D conversion of the same analog channel (same analog signal source) from both ADC0 and ADC1 is prohibited, except for the self-diagnosis channel.

If this restriction is violated, the A/D conversion results are not guaranteed because the A/D conversion accuracy of the target analog channel may deteriorate significantly.

4.1.54 A/D Conversion Start Trigger

In the RA6T2 group products, A/D conversion start triggers for the same scan group are not accepted until scanning operation of the scan group is completed (in this case, A/D converter start triggers are ignored).

An A/D conversion trigger for the same scan group should be input after the scanning operation of its scan group is completed (ADSCANENDSR.SCENDFn = 1 (n = 0 to 8)) and after 6 PCLKA clock cycles or more have elapsed.

4.1.55 Restriction on Usage when Interference Reduction between D/A and A/D Conversion is Enabled

In the RA6T1 group products, when the DAADSCR.DAADST bit is 1, enabling interference prevention between D/A and A/D conversion, do not place the ADC12 in the module-stop state. Doing so can halt D/A conversion in addition to A/D conversion.

4.1.56 Initialization Procedure of the DAC Output to Internal Modules

In the RA6T2 group products, use the following initialization procedures for the DAC output to internal modules.

The example shows the case for channel 0.

- Set the DAASWCR.DAASW0 bit to 1.
- Set the DACR.DAE bit or the DACR.DAOE0 bit to 1.
- Write the value to be converted in the DADR0 register.

4.1.57 Constraints on TSN

In the RA6T1 group products, it is prohibited to use both channels of the ADC12 simultaneously for temperature sensor measurement.

4.1.58 Instruction Fetch from SRAM Area

In the RA6T1 group products, when using the SRAMHS to operate a program, initialize the SRAM area so that the CPU can correctly prefetch data. If the CPU prefetches data from an SRAM area that is not initialized, a parity error might occur. Initialize the additional 12-byte area from the end address of a program with a 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

4.1.59 Store Buffer of SRAM

In the RA6T1 group products, a store buffer is used for fast access between the SRAM and CPU. When a load instruction is executed from the same address after a store instruction to the SRAM, the load instruction might read data from the buffer instead of data from the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A).
- After writing to the SRAM (address = A), read data from an area other than SRAM (address = A), then read the SRAM (address = A).

4.1.60 Suspension During Programming/Erasure

In the RA6T2 group products, when processing of programming/erasure is stopped by issuing the P/E suspend command, the programming or erasure processing can be resumed by issuing the P/E resume command. If the flash sequencer enters the command-locked state for any reason and issues the forced stop command after the suspended processing is normally completed and the ERSSPD flag or PRGSPD flag is set to 1, the suspended processing cannot be resumed. In addition, the values in the area where the processing was suspended are not guaranteed. Erase that area.

4.1.61 Items Prohibited During Programming and Erasure, or Blank Checking

The items that are prohibited during programming and erasure differ between products of the RA6T1 and RA6T2 groups.

RA6T1:

- Permit the operating voltage from the power supply to go beyond the allowed range.
- Change the frequency of the peripheral clock.

RA6T2:

- Have the operating voltage from the power supply to go beyond the permitted range.
- Change the FWEPROR.FLWE[1:0] bits.
- Change the OPCCR.OPCM[2:0] bits.
- Change the SCKDIVCR.FCK[2:0] bits.
- Change the SCKSCR.CKSEL[2:0] bits.
- Transition to Software Standby mode or Deep Software Standby mode

4.1.62 Abnormal Termination of Programming and Erasure

In the RA6T1 group products, when programming or erasure ends abnormally because of the generation of a reset by the RES pin, the programming or erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming or erasure ends abnormally, the blank check function cannot determine whether the area was erased successfully. Erase the area again to ensure that the corresponding area is completely erased before use.

4.1.63 Programming/Erasure in Low-Speed Mode

In the RA6T2 group products, do not program or erase the flash memory when low-speed mode is selected with the operating power control register (OPCCR).

4.1.64 Emulator Connection

In the RA6T2 group products, Renesas provides an emulator which supports both debugging using SWD or JTAG communication and serial programming using SCI communication. This emulator makes it easy to switch between debugging and serial programming. Table 63 shows the pinout of 10 pin or 20 pin socket pinouts when using this emulator. The pinout of SWD and JTAG is Arm standard, and MD, TXD, RXD pins are added for the serial programming using SCI communication.

The serial programming interface must be used to program the TrustZone IDAU boundary register settings.

It is recommended to connect PA14/SWCLK/TCK and P201/MD pins using wired OR circuit on the board to use both debugging and serial programming.

Table 63. Pin Assign for Emulator

Pin No.	SWD	JTAG	Serial Programming using SCI
1	VCC	VCC	VCC
2	PA13/SWDIO	PA13/TMS	NC
4	PA14/SWCLK	PA14/TCK	P201/MD
	Wired OR with P201/MD	Wired OR with P201/MD	
6	PB03/SWO/TXD9	PB03/TDO/TXD9	PB03/TXD9
8	PA15/RXD9	PA15/TDI/RXD9	PA15/RXD9
9	GND detect	GND detect	GND detect
10	nRESET	nRESET	nRESET
12	PE02/TCLK	PE02/TCLK	NC
14	PE03/TDATA[0]	PE03/TDATA[0]	NC
16	PE04/TDATA[1]	PE04/TDATA[1]	NC
18	PE05/TDATA[2]	PE05/TDATA[2]	NC
20	PE06/TDATA[3]	PE06/TDATA[3]	NC
3, 5, 15, 17, 19	GND	GND	GND
7	NC	NC	NC
11, 13	NC	NC	NC

5. Overview of the Flexible Software Package

The Flexible Software Package (FSP) is an integrated software package having the following five features that provide high quality software for Renesas RA family MCUs. The FSP is equipped with Hardware-Abstraction Layer (HAL) drivers that achieve high performance and reduced footprint in memory. The FSP includes the various items of software shown in Figure 5.1.

The FSP is obtainable at the following URLs:

https://github.com/renesas/fsp/releases

https://www.renesas.com/fsp

- Quality:

FSP code quality is enforced by peer reviews, automated requirements-based testing, and automated static analysis.

- Ease of Use:

FSP provides uniform and intuitive APIs that are well documented. Each module is supported with detailed user documentation including example code.

- Scalability:

FSP modules can be used on any MCU in the RA family, provided the MCU has peripherals required by the module.

- Build Time Configurations:

FSP modules also have build-time configurations that can be used to optimize the size of the module for the feature set required by the application.

- e^2 studio IDE:

FSP provides a host of efficiency enhancing tools for developing projects targeting the Renesas RA series of MCU devices. The e2 studio IDE provides a familiar development cockpit from which the key steps of project creation, module selection and configuration, code development, code generation, and debugging are all managed.

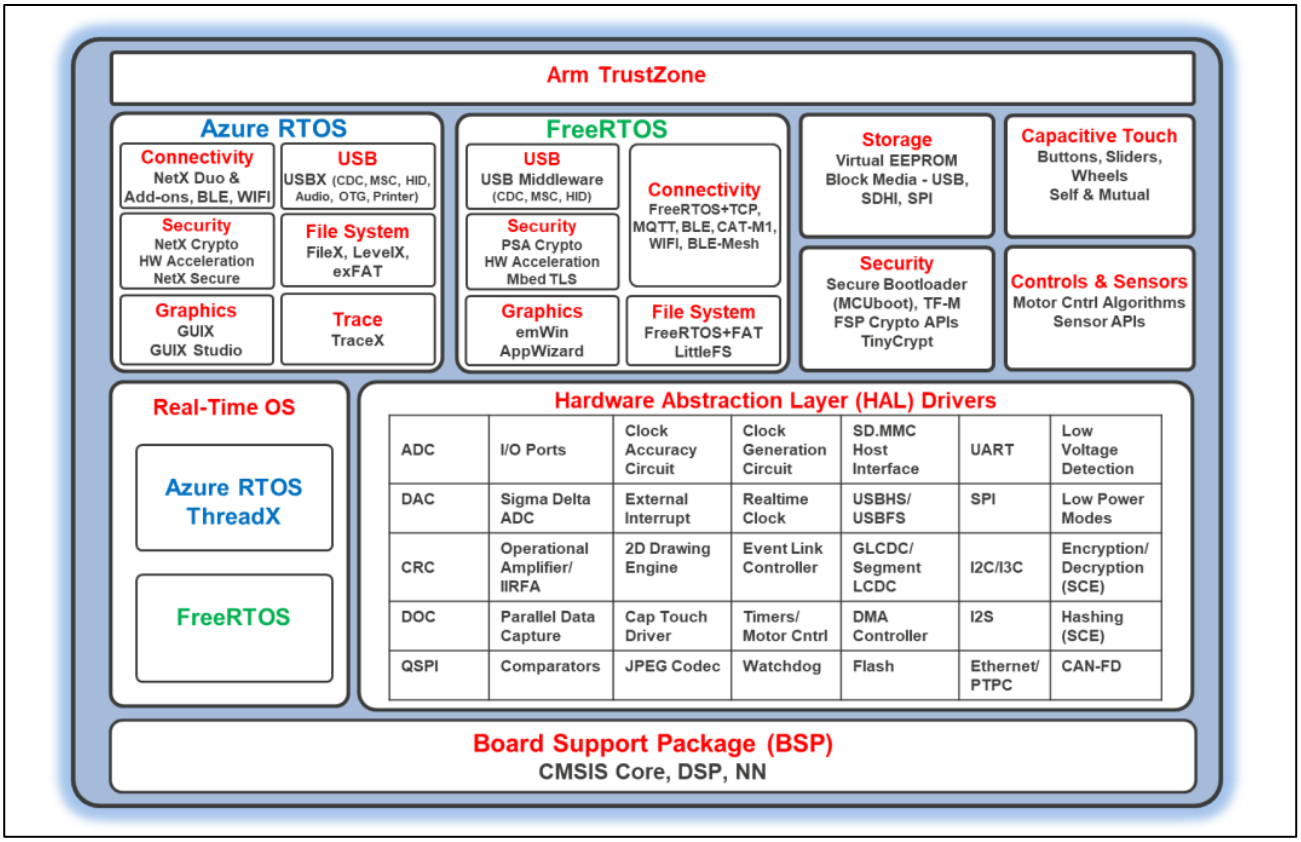


Figure 5. Flexible Software Package (FSP)

6. References

For the following documents, obtain the latest version or information from the Renesas Electronics Web site.

User's Manuals: Hardware

- RA6T1 Group User's Manual: Hardware Rev.1.10 (R01UH0897EU0110)
- RA6T2 Group User's Manual: Hardware Rev.1.20 (R01UH0951EJ0120)

Application Note:

Renesas RA Family Flash Memory Programming Rev.1.20 (R01AN5367EU120)

Technical Update/Technical News

(Please obtain the latest information from the Renesas Electronics website.)

Website and Support

Visit the following vanity URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information	www.renesas.com/ra
RA Product Support Forum	www.renesas.com/ra/forum
RA Flexible Software Package	www.renesas.com/FSP
Renesas Support	www.renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.28.22	—	First release document

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.