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M16C/64A Group, M16C/65 Group

Differences between M16C/64A and M16C/65

1. Abstract

This document describes differences between M16C/64A 100-pin version and M16C/65 100-pin version. Refer to each device's hardware manual for details.

2. Introduction

The explanation of this application note is applied to the following MCUs:

Applicable MCUs: M16C/64A 100-pin version, M16C/65 100-pin version

3. Differences

3.1 Differences in Functions

Table 3.1 lists Differences in Functions.

Table 3.1 Differences in Functions (1)

Item		M16C/64A	M16C/65
Minimum Instruction Execution Time		40 ns (f(BLCK) = 25 MHz, VCC1 = 2.7 to 5.5 V)	31.25 ns (f(BLCK) = 32 MHz, VCC1 = 2.7 to 5.5 V)
Clock Generator		Main clock, Sub clock, 125 kHz on-chip oscillator, PLL frequency synthesizer	Main clock, Sub clock, 125 kHz on-chip oscillator, PLL frequency synthesizer, 40 MHz on-chip oscillator
Power Consumption		TBD (25 MHz/VCC1 = VCC2 = 3 V) TBD (VCC1 = VCC2 = 3 V, stop mode)	TBD (32 MHz/VCC1 = VCC2 = 3 V) TBD (VCC1 = VCC2 = 3 V, stop mode)
External Bus	Bus wait	0 to 3 waits can be inserted	0 to 8 waits can be inserted
	Recovery cycle	No	0 to 3 cycles scan be inserted

Note:
1. Refer to the hardware manual for electrical characteristics and more details.

4. Detailed Comparison

4.1 Differences in Protections

Table 4.1 lists Differences in Registers Associated with Protect Functions.

Table 4.1 Differences in Registers Associated with Protect Functions

Symbol	Address		Bit	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
PRCR	000Ah	000Ah	0	Protect bit 0 Enable write to registers CM0, CM1, CM2, PLC0, and PCLKR	Protect bit 0 Enable write to registers CM0, CM1, CM2, PLC0, PCLKR, and FRA0

4.2 Difference in Clock Generators

Table 4.2 lists Differences in Clock Generators and Table 4.3 lists Difference in Registers Associated with Clock Generator.

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Table 4.2 Differences in Clock Generators

Item	M16C/64A	M16C/65
40 MHz on-chip oscillator	No	Yes

Table 4.3 Difference in Registers Associated with Clock Generator

Symbol	Address		Bit	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
FRA0	—	0022h	—	—	M16C/65 only

4.3 Difference in Buses

Table 4.4 lists Differences in Buses and Table 4.5 lists Difference in Registers Associated with Bus.

Table 4.4 Differences in Buses

Item	M16C/64A	M16C/65
External area wait	0 to 3 waits can be inserted by setting the CSiW bit in the CSR register and bits CSEi1W and CSEi0W in the CSE register (i = 0 to 3)	0 to 8 waits can be inserted by setting the CSiW bit in the CSR register, bits CSEi1W and CSEi0W in the CSE register, and bits EWCi1 to EWCi0 in the EWC register
Recovery cycle	No	0 to 3 cycles can be inserted by setting bits EWR1 to EWR0 in the EWR register

Table 4.5 Difference in Registers Associated with Bus

Symbol	Address		Bit	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
CSE	001Bh	001Bh	1 - 0	$\overline{CS0}$ wait expansion bit 11: Do not set	$\overline{CS0}$ wait expansion bit 11: Select wait states by bits EWC01 and EWC00 in the EWC register
			3 -2	$\overline{CS1}$ wait expansion bit 11: Do not set	$\overline{CS1}$ wait expansion bit 11: Select wait states by bits EWC11 and EWC10 in the EWC register
			5 - 4	$\overline{CS2}$ wait expansion bit 11: Do not set	$\overline{CS2}$ wait expansion bit 11: Select wait states by bits EWC21 and EWC20 in the EWC register
			7 - 6	$\overline{CS3}$ wait expansion bit 11: Do not set	$\overline{CS3}$ wait expansion bit 11: Select wait states by bits EWC31 and EWC30 in the EWC register
EWC	—	0011h	—	—	M16C/65 only
EWR	—	0009h	—	—	M16C/65 only

4.4 Differences in Timers

Table 4.6 lists Differences in Timers, and Table 4.7 lists Differences in Registers Associated with Timers.

Table 4.6 Differences in Timers

Item	M16C/64A	M16C/65
Count source	f1, f2, f8, f32, f64, fOCO-S, fC32	f1, f2, f8, f32, f64, fOCO-S, fOCO-F, fC32
Clock select prior to timer AB division	f1 only	Selectable from f1 and fOCO-F

Table 4.7 Differences in Registers Associated with Timers

Symbol	Address		Bits	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
TACS0 to TACS2	01D0h to 01D2h	01D0h to 01D2h	2 - 0	TAi count source select bit (i = 0, 2, 4) 100: Do not set	TAi count source select bit (i = 0, 2, 4) 100: fOCO-F
			6 - 4	TAj count source select bit (j = 1, 3) 100: Do not set	TAj count source select bit (j = 1, 3) 100: fOCO-F
TBCS0 TBCS1 TBCS2 TBCS3	01C8h 01C9h 01E8h 01E9h	01C8h 01C9h 01E8h 01E9h	2 - 0	TBi count source select bit (i =0, 2, 3, 5) 100: Do not set	TBi count source select bit (i = 0, 2, 3, 5) 100: fOCO-F
			6 - 4	TBj count source select bit (j = 1, 4) 100: Do not set	TBj count source select bit (j = 1, 4) 100: fOCO-F
TCKDIVC0	—	01CBh	—	—	M16C/65 only

4.5 Differences in Three-phase Motor Control Timer Functions

Table 4.8 lists Differences in Three-phase Motor Control Timer Functions.

Table 4.8 Differences in Three-phase Motor Control Timer Functions

Item	M16C/64A	M16C/65
Count source	f1, f2, f8, f32, f64, fOCO-S, fC32	f1, f2, f8, f32, f64, fOCO-S, fOCO-F, fC32

4.6 Differences in Serial Interfaces

Table 4.9 lists Differences in Serial Interfaces, and Table 4.10 lists Differences in Registers Associated with Serial Interface.

Table 4.9 Differences in Serial Interfaces

Item	M16C/64A	M16C/65
UART0 to UART2, UART5 to UART7 clock prior to division	f1 only	Selectable from f1 and fOCO-F
SI/O3, SI/O4 clock prior to division	f1 only	Selectable from f1 and fOCO-F

Table 4.10 Differences in Registers Associated with Serial Interface

Symbol	Address		Bit	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
S34C2	0278h	0278h	2	Reserved bit	SI/O3, SI/O4 before-division clock select bit 0: f1 1: fOCO-F
UCLKSEL0	—	0252h	—	—	M16C/65 only

4.7 Difference in A/D Converters

Table 4.11 lists Differences in A/D Converters and Table 4.12 lists Differences in Registers Associated with A/D Converter.

Table 4.11 Differences in A/D Converters

Item	M16C/64A	M16C/65
fAD	f1 only	Selectable from f1 and fOCO40M

Table 4.12 Differences in Registers Associated with A/D Converter

Symbol	Address		Bit	Differences	
	M16C/64A	M16C/65		M16C/64A	M16C/65
ADCON2	03D4h	03D4h	7	Reserved bit	fAD select bit 0: f1 1: fOCO40M

4.8 Differences in Flash Memories

Table 4.13 lists Differences in Software Commands.

Table 4.13 Differences in Software Commands

Software Command	MCU	First Bus Cycle		Second Bus Cycle	
		Address	Data	Address	Data
Read array	M16C/64A, M16C/65 (1)	X	XXFFh	—	—
	M16C/65 (2)	B0-7	XXFFh	B8	XXFFh
Read status register	M16C/64A, M16C/65 (1)	X	XX70h	X	SRD
	M16C/65 (2)	BA	XX70h	X	SRD
Clear status register	M16C/64A, M16C/65 (1)	X	XX50h	—	—
	M16C/65 (2)	B0-7	XX50h	B8	XX50h
Block erase	M16C/64A, M16C/65 (1)	X	XX20h	BA	XXD0h
	M16C/65 (2)	BA	XX20h	BA	XXD0h
Read lock bit status	M16C/64A, M16C/65 (1)	X	XX71h	BA	XXD0h
	M16C/65 (2)	BA	XX71h	BA	XXD0h
Block blank check	M16C/64A, M16C/65 (1)	X	XX25h	BA	XXD0h
	M16C/65 (2)	BA	XX25h	BA	XXD0h

Notes:
1. Program ROM 1 is 512 KB or less.
2. Program ROM 1 is more than 512 KB.

SRD: Data in the status register (D7 to D0)
BA: Highest-order block address (even address)
B0-7: Any even address in blocks 0 to 7, program ROM 2, or data flash
B8: Any even address in blocks after 8
X: Any even address in program ROM 1, program ROM 2, or data flash
XX: Eight high-order bits of command code (ignored)

5. Reference Documents

Hardware Manual
M16C/64A Group Hardware Manual
M16C/65 Group Hardware Manual
(The latest version of these documents can be downloaded from the Renesas Technology website.)

Technical News/Technical Update
(The latest version of these documents can be downloaded from the Renesas Technology website.)

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