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Renesas Electronics Corporation

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M16C/62P,M16C/64 Group

Differences between M16C/64 and M16C/62P

1. Abstract

This document is reference only and explains differences between M16C/64 group and M16C/62P group.

2. Introduction

The explanation of this issue is applied to the following condition

Applicable MCU - M16C/62P
- M16C/64

3. Points of the difference

3.1 Function Differences

Figure 3.1.1 shows Function Differences

Figure 3.1.1 Function Differences (Note:1)

Item	M16C/62P	M16C/64
Shortest Instruction Execution time	41.7ns(f (BCLK)=24MHz, VCC1=3.0V to 5.5V) 100ns(f (BCLK)=10MHz, VCC1=2.7V to 5.5V)	40ns(f (BCLK)=25MHz, VCC1=2.7V to 5.5V)
I/O Port	I/O:87 (Nch.O.D:2), Input port: 1	I/O:88 (Nch.O.D:3)
Disablement function of key input interruption, INT6 and INT7 in A/D converter operation mode	None	Have
NMI	Enable after reset is canceled.	Disable after reset is canceled. Selectable valid mode with PM24 bit.
CNVss	-	After reset is deserted, internal pull-up is valid maximum two cycles in 125kHz on-chip oscillator in single-chip mode.
CLKOUT	Retain status when entering stop mode.	Output “high” when entering stop mode
Port P8_2 to P8_4(INT0 to 2)	Common to peripheral function and port input.	Divide peripheral function and port input. (Same configuration as INT3 to 7)
Handling of unused pins	Vref pin: Connect the pin to Vss	Vref pin: Connect the pin to Vcc1

Item	M16C/62P	M16C/64
External Bus	-	Usable area has been changed due to placing SFR area (0D000h-0D7FFh) and program 2ROM area and enhanced Data Flash area.
DMAC	2ch (25 sources)	4ch(43 sources)
Low-Voltage Detection Circuit	Vdet3	Vdet0 (The name is changed)
	-	When using low-voltage detection circuit, be sure to set PM25 bit “1: clock supply enabled”. (PM25 bit: New additional bit.)
Cold Start-up/ Warm Start-up Flag	Vdet0: Unlinked	Vdet0: Linked
Frequency of the On-chip oscillator	About 1MHz	About 125kHz
CPU clock source after reset is canceled	Main Clock	125kHz On-chip Oscillator Clock
PLL	Multiplying factor : 2,4,6,8	Multiplying factor: 2,4,6,8 XIN: Through, 2 or 4 provides Before entering clock to PLL frequency synthesizer, be sure to divide clock form 2MHz to 5MHz.
	Multiplying factor modification; Only 1time after reset	Multiplying factor modification; Unlimited
SFR access wait (when CPU clock is over 16MHz)	2 wait	1wait
Protection	-	New protect bit 6 protects PRG2C register. Protect bit 3 protects VWOC register.

Item	M16C/62P	M16C/64
A/D Converter	Operation Frequency: 3.3V: f AD＝10MHz(±5LSB) 5.0V: f AD＝12MHz(±3LSB)	Operation Frequency: 3.0V: f AD＝10MH z (±3LSB) 3.3V: f AD＝16MHz (±3LSB) 5.0V: f AD＝25MHz(±3LSB)
	VrefCUT: Wait 1µS after connecting.	A/D Standby: Start in 1cycle after connecting.
	Selectable 10bit or 8bit conversion mode	Fixed 10bit conversion mode
	Selectable with/without sample and hold function	Fixed sample and hold function
	Available external Op-Amp connection mode	No external Op-Amp connection mode
	Can be used when operating with 2.0V≤Vref≤Vcc1	Be sure to use Vcc1, AVcc, Vref with same power supply
	ADST bit when using external trigger: After A/D conversion, ADST bit “1” is maintained.	ADST bit when using external trigger: After A/D conversion, ADST bit becomes “0”.
	The operation after writing “1” in ADST bit: ADST bit set to “1” shortly.	The operation after writing “1” in ADST bit: After the passage of dummy time period, ADST bit is set to “1”.
Timer A,B	Operation clocks: - From f1 to f32 in f1 clock - fc32	Operation clocks: -From f1 to f64 in f1 clock (One frequency circuit in timer A and B and Three-phase timer) - fc32 - On-Chip-Oscillator (125kHz)
	Fixed PWM output level	PWM output level can be inverted
	Select Up count or Down count: Selectable with TAjOUT pin (j=0 to 4)	Select Up count or Down count: Not selectable with TAjout pin (j=0 to 4)
	Timer Bi register in pulse measurement mode / Pulse period measurement mode: Disable to set the initial value (i=0 to 5)	Timer Bi register in pulse measurement mode / Pulse period measurement mode: Enable to set the initial value (i=0 to 5)
	Timer B over-flow flag: Disable to clear the flag while not counting.	Timer B overflow flag: Enable to clear the flag while not counting
	Timer A2 to A4 Tow-Phase Pulse Signal Processing Select bit in UP/Down flag register is write enable only.	Timer A2 to A4 Tow-Phase Pulse Signal Processing Select bit in UP/Down flag register is read and write enable.
Three-Phase Timer	Three-phase timer Output Cutoff: NMI pin	Three-phase timer Output Cutoff: SD pin

Item	M16C/62P	M16C/64
WDT	Common to start and refresh register	Reset register and Start register are divided. Optional function select address (OFS1) enables select and protect count source.
UART	UART3ch (UART 0 to 2)	UART6ch (UART 0 to 2,5 to 7)
	Operation Clock: From f1SIO to f32SIO in f1 clock	Operation Clock: From f1SIO to f32 SIO in f1 clock (Each URAT0 to 2,5 to 7 has one divider circuit)
SIO	Operation Clock: f1SIO, f2SIO, f8SIO, f32SIO	Operation Clock: f1SIO, f2SIO, f8SIO, f32SIO (One divider circuit belongs to SI/O3 and 4)
	SOUT Output: High impedance	SOUT Output: Selectable “High impedance” and “Last hold level” function.
Interrupt	32 vectors	64 vectors
	6 external interruption	8 external interruption (Add INT6,INT7)
	-	New interrupt source DMA2, DMA3, UART5, UART6, UART7, INT6, INT7

Item	M16C/62P	M16C/64
Flash ROM	Block:(256KB Version) - User Area: 4K+4K+8K+8K+8K+32K+64K+64K+64K - Boot ROM Area: 4K - Data Area: 4K	Block:(256KB Version) - Program 1 area: 64K+64K+64K+64K - Program 2 area: 16K - Data Flash: 4K+4K
	-	Flash distinction register (FIDR) is deleted
	-	User ROM area select bit (FMR05) is deleted
	-	New Data flash wait bit (FMR17) 1wait is required when connecting to data flash.
	Selectable protect option	Selectable protect option + WDT count source selection mode and count source protection mode
	-	Available Slow Read Mode
	-	Available Low-current Consumption mode
	-	Available User Boot Function
	-	Available Forced Erase Function
	-	Available Functions to prevent standard serial I/O mode
	Erase/Write time - For all area: 100 times - Block 1, Block A: 10,000 times - The other blocks: 1,000 times	Erase/Write time For all area :100 times
CPU Rewrite mode	Program command: 40h Unit: 1 word	Program command: 41h Unit: 2 word
	-	Setting procedure of EW0, EW1 mode has been changed.
	Available all unlock block erase command	No all unlock block erase command
Power Supply	Can be used when operating with VCC1≥VCC2≥2.7V	Be sure to use VCC1 and VCC2 with same current source. Note: Make sure to use Vref and AVCC with same current source, too.

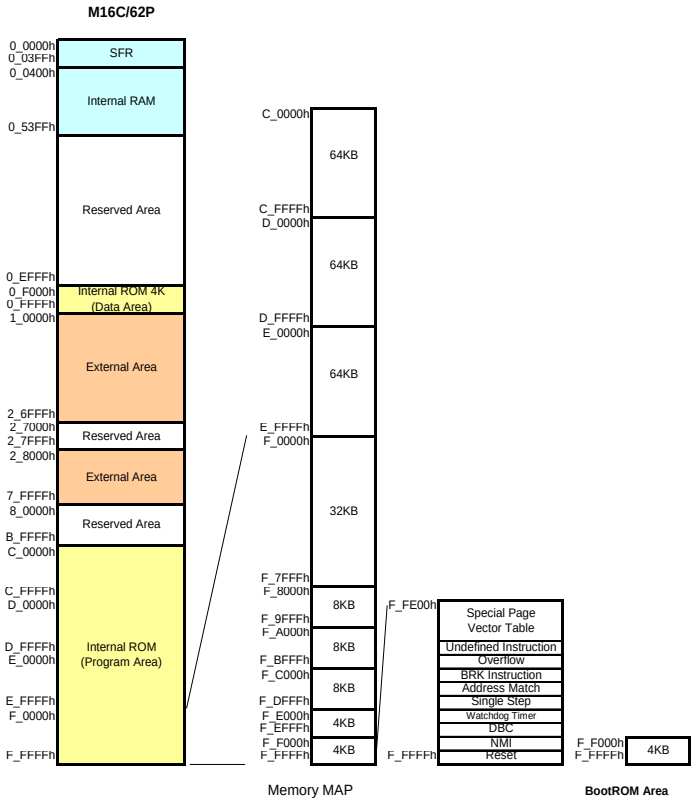
Item	M16C/62P	M16C/64
Consumption current	14mA (VCC1=5V, f(BCLK)=24MHz) 8mA (VCC1=3V, f(BCLK)=10MHz) 1.8µA (VCC1=3V,f(XCIN)=32kHz, Waite mode) 0.7µA (VCC1=3V, Stop mode)	20mA (VCC1=5V, f(BCLK)=25MHz) 5.7µA (VCC1=3V, f(XCIN)=32kHz, Waite mode) 3.0µA (VCC1=3V, Stop mode)
Parallel Writer	-	Adapter for M16C/64 is required

Note: Please refer to the hardware manual for more information of the details and the electrical characteristics.

3.2 Memory Map Comparison

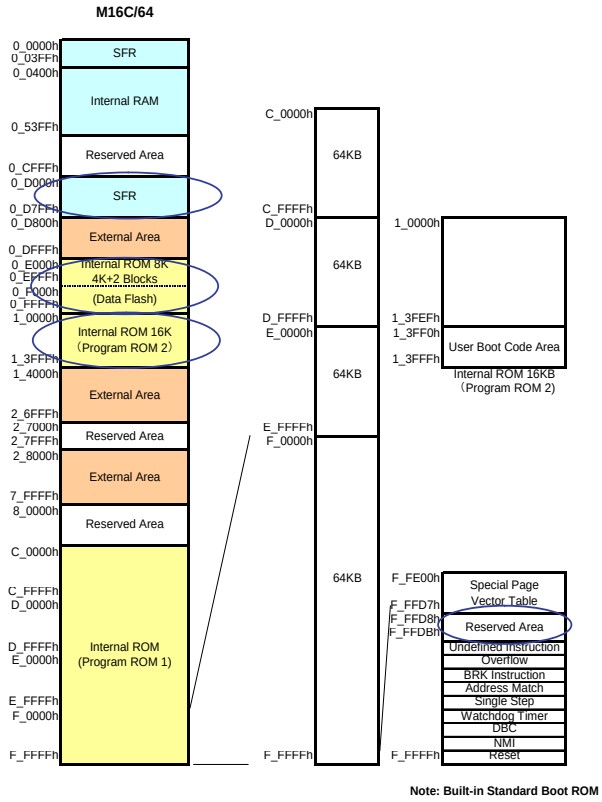
256K Version Memory Map

M16C/62P



M16C/64

Condition
In memory expansion mode
PM10 bit in PM1 register is "1"（Enable Data flash）
PM13 bit in PM1 regsiter is "1"（Enable all internal ROM, RAM)
PRG2C0 in PRG2C register is "0"（Enable Program ROM2）



Note: Built-in Standard Boot ROM

3.3 Variable Vector Table Comparison

Software Interrupt #	Vector Adodress (1) Address(L) to Address(H)	**M16C/62P** Interrupt Source	**M16C/64** Interrupt Source
0	+0 to +3(0000h to 0003h)	BRK Instruction	BRK Instruction
1	+4 to +7(0004h to 0007h)	(Reserved)	(Reserved)
2	+8 to +11(0008h to 000Bh)		INT7*
3	+12 to +15(000Ch to 000Fh)		INT6*
4	+16 to +19(0010h to 0013h)	INT3	INT3
5	+20 to +23(0014h to 0017h)	Timer B5	Timer B5
6	+24 to +27(0018h to 001Bh)	Timer B4, UART1 Bus Collision Detect	Timer B4, UART1 Bus Collision Detect
7	+28 to +31(001Ch to 001Fh)	Timer B3, UART0 Bus Collision Detect	Timer B3, UART0 Bus Collision Detect
8	+32 to +35(0020h to 0023h)	SI/O4,INT5	SI/O4,INT5
9	+36 to +39(0024h to 0027h)	SI/O3,INT4	SI/O3,INT4
10	+40 to +43(0028h to 002Bh)	UART2 Bus Collision Detect	UART2 Bus Collision Detect
11	+44 to +47(002Ch to 002Fh)	DMA0	DMA0
12	+48 to +51(0030h to 0033h)	DMA1	DMA1
13	+52 to +55(0034h to 0037h)	Key Input Interrupt	Key Input Interrupt
14	+56 to +59(0038h to 003Bh)	A/D	A/D
15	+60 to +63(003Ch to 003Fh)	UART2 Transmit,NACK2	UART2 Transmit,NACK2
16	+64 to +67(0040h to 0043h)	UART2 Receive,ACK2	UART2 Receive,ACK2
17	+68 to +71(0044h to 0047h)	UART0 Transmit,NACK0	UART0 Transmit,NACK0
18	+72 to +75(0048h to 004Bh)	UART0 Receive,ACK0	UART0 Receive,ACK0
19	+76 to +79(004Ch to 004Fh)	UART1Transmit,NACK1	UART1Transmit,NACK1
20	+80 to +83(0050h to 0053h)	UART1Receive,ACK1	UART1Receive,ACK1
21	+84 to +87(0054h to 0057h)	Timer A0	TimerA0
22	+88 to +91(0058h to 005Bh)	TimerA1	TimerA1
23	+92 to +95(005Ch to 005Fh)	TimerA2	TimerA2
24	+96 to +99(0060h to 0063h)	TimerA3	TimerA3
25	+100 to +103(0064h to 0067h)	TimerA4	TimerA4
26	+104 to +107(0068h to 006Bh)	TimerB0	TimerB0
27	+108 to +111(006Ch to 006Fh)	TimerB1	TimerB1
28	+112 to +115(0070h to 0073h)	TimerB2	TimerB2
29	+116 to +119(0074h to 0077h)	INT0	INT0
30	+120 to +123(0078h to 007Bh)	INT1	INT1
31	+124 to +127(007Ch to 007Fh)	INT2	INT2
32 to 40	+128 to +131(0080h to 0083h) to +160 to +163(00A0h to 00A3h)	(Reserved)	INT Instruction Interrupt*
41	+164 to +167(00A4h to 00A7h)		DMA2*
42	+168 to +171(00A8h to 00ABh)		DMA3*
43	+172 to +175(00ACh to 00AFh)		UART5 Bus Collision Detect*
44	+176 to +179(00B0h to 00B3h)		UART5 Transmit,NACK5*
45	+180 to +183(00B4h to 00B7h)		UART5 Receive,ACK5*
46	+184 to +187(00B8h to 00BBh)		UART6 Bus Collision Detect*
47	+188 to +191(00BCh to 00BFh)		UART6 Transmit,NACK6*
48	+192 to +195(00C0h to 00C3h)		UART6 Receive,ACK6*
49	+196 to +199(00C4h to 00C7h)		UART7 Bus Collision Detect*
50	+200 to +203(00C8h to 00CBh)		UART7 Transmit,NACK7*
51	+204 to +207(00CCh to 00CFh)		UART7 Receive,ACK7*
52	+208 to +211(00D0h to 00D3h)		(Reserved)
53	+212 to +215(00D4h to 00D7h)		(Reserved)
54	+216 to +219(00D8h to 00DBh)		(Reserved)
55	+220 to +223(00DCh to 00DFh)		(Reserved)
56	+224 to +227(00E0h to 00E3h)		(Reserved)
57	+228 to +231(00E4h to 00E7h)		(Reserved)
58	+232 to +235(00E8h to 00EBh)		(Reserved)
59	+236 to +239(00ECh to 00EFh)		(Reserved)
60	+240 to +243(00F0h to 00F3h)		(Reserved)
61	+244 to +247(00F4h to 00F7h)		(Reserved)
62	+248 to +251(00F8h to 00FBh)		(Reserved)
63	+252 to +255(00FCh to 00FFh)		(Reserved)

Note:*Changes

3.4 DMACRequest Factor Comparison

M16C/62P DMA Request Factor Select Register

DMA0

DSEL3～DSEL0	DMS=0(Basic Factor)	DMS=1(Extend Factor)
0000b	Falling edge of INT0 pin	—
0001b	Software Trigger	—
0010b	Timer A0	—
0011b	Timer A1	—
0100b	Timer A2	—
0101b	Timer A3	—
0110b	Timer A4	Both edge of INT0pin
0111b	Timer B0	Timer B3
1000b	Timer B1	Timer B4
1001b	Timer B2	Timer B5
1010b	UART0 Transmit	—
1011b	UART0 Receive	—
1100b	UART2 Transmit	—
1101b	UART2 Receive	—
1110b	A/D	—
1111b	UART1 Transmit	—

DMA1

DSEL3～DSEL0	DMS=0(Basic Factor)	DMS=1(Extend Factor)
0000b	Falling edge of INT1pin	—
0001b	Software Trigger	—
0010b	Timer A0	—
0011b	Timer A1	—
0100b	Timer A2	—
0101b	Timer A3	SI/O3
0110b	Timer A4	SI/O4
0111b	Timer B0	Both edge of INT1pin
1000b	Timer B1	—
1001b	Timer B2	—
1010b	UART0 Transmit	—
1011b	UART0 Receive/ACK0	—
1100b	UART2 Transmit	—
1101b	UART2 Receive/ACK2	—
1110b	A/D	—
1111b	UART1Receive/ ACK1	—

There is compatibility with existing factor of M16C/62P.

M16C/64 DMA Request Factor Select Register

DMA0

DSEL4～DSEL0	DMS=0(Basic Factor)	DMS=1(Extend Factor)
00000b	Falling edge of INT0pin	—
00001b	Software Trigger	—
00010b	TimerA0	—
00011b	TimerA1	—
00100b	TimerA2	—
00101b	TimerA3	—
00110b	TimerA4	Both edge of INT0pin
00111b	TimerB0	TimerB3
01000b	TimerB1	TimerB4
01001b	TimerB2	TimerB5
01010b	UART0 Transmit	—
01011b	UART0 Receive	—
01100b	UART2 Transmit	—
01101b	UART2 Receive	—
01110b	A/D	—
01111b	UART1 Transmit	—
10000b	UART1Receive	Falling edge of INT4pin
10001b	UART5 Transmit	Both edge of INT4pin
10010b	UART5 Receive	-
10011b	UART6 Transmit	-
10100b	UART6 Receive	-
10101b	UART7 Transmit	-
10110b	UART7 Receive	-
10111b	-	-
11XXXb	-	-

X : "0" or "1" - : indicate snosetting

DMA1

DSEL4～DSEL0	DMS=0(Basic Factor)	DMS=1(Extend Factor)
00000b	Falling edge of INT1pin	Reserved
00001b	Software Trigger	Reserved
00010b	TimerA0	Reserved
00011b	TimerA1	Reserved
00100b	TimerA2	Reserved
00101b	TimerA3	SI/O3
00110b	TimerA4	SI/O4
00111b	TimerB0	Both edge of INT1pin
01000b	TimerB1	Reserved
01001b	TimerB2	Reserved
01010b	UART0 Transmit	Reserved
01011b	UART0 Receive/ACK0	Reserved
01100b	UART2 Transmit	Reserved
01101b	UART2 Receive/ACK2	Reserved
01110b	A/D	Reserved
01111b	UART1Receive/ACK1	Reserved
10000b	UART1Transmit	Falling edge of INT5pin
10001b	UART5 Transmit	Both edge of INT5pin
10010b	UART5 Receive/ACK5	Reserved
10011b	UART6 Transmit	Reserved
10100b	UART6 Receive/ACK6	Reserved
10101b	UART7 Transmit	Reserved
10110b	UART7 Receive/ACK7	Reserved
10111b	Reserved	Reserved
11XXXb	—	—

X : "0" or "1" - : indicate snosetting

There is compatibility with existing factor of M16C/62P.

For the DMA Request Factor Select Register of M16C/64 DMA2, DMA3, refer to the Hardware Manual.

4. Reference Materials

Hard ware Manual

M16C/64 Group Hardware Manual
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Rev.	Date	Description	
		Page	Summary
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