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Renesas Electronics Corporation

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M16C/62P Group, R32C/111 Group

Differences between M16C/62P and R32C/111 (100 pin ver.)

1. Introduction

This document is a reference to confirm the functional changes from the M16C/62P (100-pin package version) to the R32C/111 (100-pin package version).
For the details of each function, refer to its respective hardware manual and/or software manual.

2. Applicable MCUs

This document is applicable to the following products:
M16C/62P, 100-pin package version and R32C/111, 100-pin package version

3. Overview of Comparison

3.1 Overview of Functions

Table 3.1 and Table 3.2 list the functions of each product.

Table 3.1 Comparison Chart: Overview of Functions (1/2)

Item	M16C/62P	R32C/111
Basic instructions	91	108 (including 14 deleted, 31 added, and 5 changed)
Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz / VCC1 = 3.0 to 5.5 V)	20 ns (f(CPU) = 50 MHz)
Multiplier	16-bit × 16-bit→32-bit	32-bit × 32-bit→64-bit
Multiply-accumulate unit	N/A (1)	32-bit × 32-bit + 64-bit→64-bit
FPU	N/A	Single precision (compliant with IEEE-754)
Barrel shifter	N/A	32 bits
Operating mode	Single-chip mode, memory expansion mode, microprocessor mode	Single-chip mode, memory expansion mode, microprocessor mode (optional (2))
Address space	1 Mbytes (expandable to 4 Mbytes by memory space expansion function)	4 Gbytes (available up to 64 Mbytes)
Voltage detector (optional (2))	Reset level detector, low voltage detector, coldstart/warmstart determination	Low voltage detector Low voltage detection interrupt
Clocks	• Main clock oscillation circuit: 0 to 16 MHz • PLL synthesizer: 10 to 24 MHz • On-chip oscillator: approx. 1 MHz • Frequency divide circuit: divide-by-i selectable (i = 1, 2, 4, 8, 10, and 16)	• Main clock oscillation circuit: 4 to 16 MHz • PLL synthesizer: 96 to 128 MHz • On-chip oscillator: approx. 125 kHz • Frequency divide circuit: divide-by-2 to divide-by-24 selectable
Interrupts	Interrupt vectors: 70	Interrupt vectors: 261
DMAC	• 2 channels • Request sources: 24	• 4 channels • Request sources: 51
DMAC II	N/A	Embedded
X/Y converter	N/A	Embedded
I/O ports	87 inputs/outputs, 1 input-only port	82 CMOS inputs/outputs, 2 input-only ports
Serial interface	• 3 channels (UART0 to UART2) -Synchronous serial interface -Asynchronous serial interface • 1 channel (UART2) -I2C bus, IEBus (3) mode • 2 channels (SI/O3, SI/O4) -Synchronous serial interface	• 9 channels (UART0 to UART8) -Synchronous serial interface -Asynchronous serial interface • 7 channels (UART0 to UART6) -I2C bus, special mode 2, IEBus (3) mode (optional (2))

Notes:
1. “Not applicable” and “not available” will hereinafter be referred to as “N/A” in tables.
2. Please contact a Renesas sales office to use the optional feature.
3. IEBus is a trademark of NEC Electronics Corporation.

Table 3.2 Comparison Chart: Overview of Functions (2/2)

Item	M16C/62P	R32C/111
Intelligent I/O	N/A	• Time measurement:16 bits × 16 • Waveform generation:16 bits × 19 • Serial interface: -Variable-length synchronous serial I/O mode -IEBus (1) mode (optional (2))
Flash memory	Erase and program power supply voltage: 3.3 ± 0.3 V, or 5.0 ± 0.5 V Erase and program endurance: 100 times (all areas) or 1,000 times (user ROM area except blocks A and 1) and 10,000 times (blocks A and 1)	Erase and program power supply voltage: Vcc1 = Vcc2 = 3.0 to 5.5 V Erase and program endurance: 1, 000 times (program area) and 10,000 times (data area) Forced erase function (optional (2)) Standard serial I/O mode disable function (optional (2))
Operating frequency/ Supply voltage	• 24 MHz / VCC1 = 3.0 to 5.5 V, VCC2 = 2.7 V to VCC1 • 10 MHz / VCC1= 2.7 to 5.5 V, VCC2 = 2.7 V to VCC1	50 MHz / VCC1 = 3.0 to 5.5 V, VCC2 = 3.0 V to VCC1
Current consumption	• 14 mA (VCC1 = VCC2 = 5.0 V, f(BCLK) = 24 MHz) • 8 mA (VCC1 = VCC2 = 3.0 V, f(BCLK) = 10 MHz) • 1.8 µA (VCC1 = VCC2 = 3.0 V, f(XCIN) = 32.768 kHz in wait mode) • 0.7 µA (VCC1 = VCC2 = 3.0 V in stop mode)	• 32 mA (VCC1 = VCC2 = 5.0 V, f(CPU) = 50 MHz) • 8 µA (VCC1 = VCC2 = 3.3 to 5.0 V, f(XCIN) = 32.768 kHz in wait mode) • 5 µA (VCC1 = VCC2 = 3.3 to 5.0 V, when all clocks and main regulator are stopped)

Notes:
1. IEBus is a trademark of NEC Electronics Corporation.
2. Please contact a Renesas sales office to use the optional feature.

3.2 Pin Characteristics

Table 3.3 to Table 3.5 list each pin characteristics and changes from the M16C/62P.

Table 3.3 Comparison Chart: Pin Characteristics (1/3)

M16C/62P	R32C/111	Changes
P9_4/TB4IN/DA1	P9_4/TB4IN/DA1/$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$	Added: $\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$
P9_2/TB2IN/SOUT3	VDC0	Added: VDC0 Deleted: P9_2/TB2IN/SOUT3
P9_1/TB1IN/SIN3	P9_1	Deleted:TB1IN/SIN3
P9_0/TB0IN/CLK3	VDC1	Added: VDC1 Deleted: P9_0/TB0IN/CLK3
BYTE	NSD	Added: NSD Deleted: BYTE
P8_4/$\overline{\text{INT2}}$/ZP	P8_4/$\overline{\text{INT2}}$	Deleted: ZP
P8_1/TA4IN/$\overline{\text{U}}$	P8_1/TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/IIO1_5/UD0B/UD1B	Added: $\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/IIO1_5/UD0B/UD1B
P8_0/TA4OUT/U	P8_0/TA4OUT/U/RXD5/SCL5/STXD5/UD0A/UD1A	Added: RXD5/SCL5/STXD5/UD0A/UD1A
P7_7/TA3IN	P7_7/TA3IN/CLK5/IIO1_4/UD0B/UD1B	Added: CLK5/IIO1_4/UD0B/UD1B
P7_6/TA3OUT	P7_6/TA3OUT/SRXD5/SDA5/TXD5/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/IIO1_3/UD0A/UD1A	Added: SRXD5/SDA5/TXD5/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/IIO1_3/UD0A/UD1A
P7_5/TA2IN/$\overline{\text{W}}$	P7_5/TA2IN/$\overline{\text{W}}$/RXD8/IIO1_2	Added: RXD8/IIO1_2
P7_4/TA2OUT/W	P7_4/TA2OUT/W/CLK8/IIO1_1	Added: CLK8/IIO1_1
P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8/IIO1_0	Added: $\overline{\text{SS2}}$/TXD8/IIO1_0
P7_1/TA0IN/TB5IN/RXD2/SCL2	P7_1/TA0IN/TB5IN/RXD2/SCL2/STXD2/IIO1_7/OUTC2_2/ISRXD2/IEIN	Added: STXD2/IIO1_7/OUTC2_2/ISRXD2/IEIN
P7_0/TA0OUT/TXD2/SDA2	P7_0/TA0OUT/TXD2/SDA2/SRXD2/IIO1_6/OUTC2_0/ISTXD2/IEOUT	Added: SRXD2/IIO1_6/OUTC2_0/ISTXD2/IEOUT
P6_7/TXD1/SDA1	P6_7/TXD1/SDA1/SRXD1	Added: SRXD1
P6_6/RXD1/SCL1	P6_6/RXD1/SCL1/STXD1	Added: STXD1
P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$/OUTC2_1/ISCLK2	Added: $\overline{\text{SS1}}$/OUTC2_1/ISCLK2 Deleted: $\overline{\text{CTS0}}$/CLKS1
P6_3/TXD0/SDA0	P6_3/TXD0/SDA0/SRXD0	Added: SRXD0
P6_2/RXD0/SCL0	P6_2/TB2IN/RXD0/SCL0/STXD0	Added: TB2IN/STXD0
P6_1/CLK0	P6_1/TB1IN/CLK0	Added: TB1IN
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/TB0IN/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$	Added: TB0IN/$\overline{\text{SS0}}$

Table 3.4 Comparison Chart: Pin Characteristics (2/3)

M16C/62P	R32C/111	Changes
P5_7/$\overline{RDY}$/CLKOUT	P5_7/$\overline{RDY}$/$\overline{CS3}$/$\overline{CTS7}$/$\overline{RTS7}$	Added: $\overline{CS3}$/$\overline{CTS7}$/$\overline{RTS7}$ Deleted: CLKOUT
P5_6/ALE	P5_6/ALE/$\overline{CS2}$/RXD7	Added: $\overline{CS2}$/RXD7
P5_5/$\overline{HOLD}$	P5_5/$\overline{HOLD}$/CLK7	Added:CLK7
P5_4/$\overline{HLDA}$	P5_4/$\overline{HLDA}$/$\overline{CS1}$/TXD7	Added: $\overline{CS1}$/TXD7
P5_3/BCLK	P5_3/CLKOUT/BCLK	Added: CLKOUT
P5_1/$\overline{WRH}$/$\overline{BHE}$ (1)	P5_1/$\overline{WR1}$/$\overline{BC1}$ (1)	
P5_0/$\overline{WRL}$/$\overline{WR}$ (2)	P5_0/$\overline{WR0}$/$\overline{WR}$ (2)	
P4_7/$\overline{CS3}$	P4_7/$\overline{CS0}$/A23/TXD6/SDA6/ SRXD6	Added: $\overline{CS0}$/A23/TXD6/SDA6/ SRXD6 Deleted: $\overline{CS3}$
P4_6/$\overline{CS2}$	P4_6/$\overline{CS1}$/A22/RXD6/SCL6/ STXD6	Added: $\overline{CS1}$/A22/RXD6/SCL6/ STXD6 Deleted: $\overline{CS2}$
P4_5/$\overline{CS1}$	P4_5/$\overline{CS2}$/A21/CLK6	Added: $\overline{CS2}$/A21/CLK6 Deleted: $\overline{CS1}$
P4_4/$\overline{CS0}$	P4_4/$\overline{CS3}$/A20/$\overline{CTS6}$/$\overline{RTS6}$/$\overline{SS6}$	Added: $\overline{CS3}$/A20/$\overline{CTS6}$/$\overline{RTS6}$/ $\overline{SS6}$ Deleted:$\overline{CS0}$
P4_3/A19	P4_3/A19/TXD3/SDA3/SRXD3/ OUTC2_0/ISTXD2/IEOUT	Added: TXD3/SDA3/SRXD3/ OUTC2_0/ISTXD2/IEOUT
P4_2/A18	P4_2/A18/RXD3/SCL3/STXD3/ ISRXD2/IEIN	Added: RXD3/SCL3/STXD3/ ISRXD2/IEIN
P4_1/A17	P4_1/A17/CLK3	Added: CLK3
P4_0/A16	P4_0/A16/$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$	Added: $\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$
P3_7/A15	P3_7/A15/ [A15/D15] /TA4IN/$\overline{U}$	Added: [A15/D15] /TA4IN/$\overline{U}$
P3_6/A14	P3_6/A14/ [A14/D14] /TA4OUT/U	Added: [A14/D14] /TA4OUT/U
P3_5/A13	P3_5/A13/ [A13/D13] /TA2IN/$\overline{W}$	Added: [A13/D13] /TA2IN/$\overline{W}$
P3_4/A12	P3_4/A12/ [A12/D12] /TA2OUT/W	Added: [A12/D12] /TA2OUT/W
P3_3/A11	P3_3/A11/ [A11/D11] /TA1IN/$\overline{V}$	Added: [A11/D11] /TA1IN/$\overline{V}$
P3_2/A10	P3_2/A10/ [A10/D10] /TA1OUT/V	Added: [A10/D10] /TA1OUT/V
P3_1/A9	P3_1/A9/ [A9/D9] /TA3OUT/UD0B/ UD1B	Added: [A9/D9] /TA3OUT/UD0B/ UD1B
P3_0/A8/ [A8/-] / [A8/D7]	P3_0/A8/ [A8/D8] /TA0OUT/UD0A/ UD1A	Added: [A8/D8] /TA0OUT/UD0A/ UD1A Deleted: [A8/-] / [A8/D7]

Notes:
1. $\overline{WRH}$ and $\overline{BHE}$ in the M16C/62P are respectively changed to $\overline{WR1}$ and $\overline{BC1}$ in the R32C/111.
2. $\overline{WRL}$ in the M16C/62P is changed to $\overline{WR0}$ in the R32C/111.

Table 3.5 Comparison Chart: Pin Characteristics (3/3)

M16C/62P	R32C/111	Changes
P2_7/A7/ [A7/D7] / [A7/D6] /AN2_7	P2_7/A7/ [A7/D7] /AN2_7	Deleted: [A7/D6]
P2_6/A6/ [A6/D6] / [A6/D5] /AN2_6	P2_6/A6/ [A6/D6] /AN2_6	Deleted: [A6/D5]
P2_5/A5/ [A5/D5] / [A5/D4]/AN2_5	P2_5/A5/ [A5/D5] /AN2_5	Deleted: [A5/D4]
P2_4/A4/ [A4/D4] / [A4/D3] /AN2_4	P2_4/A4/ [A4/D4] /AN2_4	Deleted: [A4/D3]
P2_3/A3/ [A3/D3] / [A3/D2] /AN2_3	P2_3/A3/ [A3/D3] /AN2_3	Deleted: [A3/D2]
P2_2/A2/ [A2/D2] / [A2/D1] /AN2_2	P2_2/A2/ [A2/D2] /AN2_2	Deleted: [A2/D1]
P2_1/A1/ [A1/D1] / [A1/D0] /AN2_1	P2_1/A1/ [A1/D1] /AN2_1	Deleted: [A1/D0]
P2_0/A0/ [A0/D0] / [A0/-] /AN2_0	P2_0/A / [A0/D0] /$\overline{BC0}$/ [$\overline{BC0}$/D0] / AN2_0	Added: $\overline{BC0}$/ [$\overline{BC0}$/D0] Deleted: [A0/-]
P1_7/D15/$\overline{INT5}$	P1_7/D15/$\overline{INT5}$/IIO0_7/IIO1_7	Added: IIO0_7/IIO1_7
P1_6/D14/$\overline{INT4}$	P1_6/D14/$\overline{INT4}$/IIO0_6/IIO1_6	Added: IIO0_6/IIO1_6
P1_5/D13/$\overline{INT3}$	P1_5/D13/$\overline{INT3}$/IIO0_5/IIO1_5	Added: IIO0_5/IIO1_5
P1_4/D12	P1_4/D12/IIO0_4/IIO1_4	Added: IIO0_4/IIO1_4
P1_3/D11	P1_3/D11/IIO0_3/IIO1_3	Added: IIO0_3/IIO1_3
P1_2/D10	P1_2/D10/IIO0_2/IIO1_2	Added: IIO0_2/IIO1_2
P1_1/D9	P1_1/D9/IIO0_1/IIO1_1	Added: IIO0_1/IIO1_1
P1_0/D8	P1_0/D8/IIO0_0/IIO1_0	Added: IIO0_0/IIO1_0
P9_7/$\overline{ADTRG}$/SIN4	P9_7/$\overline{ADTRG}$/RXD4/SCL4/STXD4	Added: RXD4/SCL4/STXD4 Deleted: SIN4
P9_6/ANEX1/SOUT4	P9_6/TXD4/SDA4/SRXD4/ANEX1	Added: TXD4/SDA4/SRXD4 Deleted: SOUT4

4. Detailed Comparison

4.1 CPU Function

Table 4.1 to Table 4.6 list the changes from the M16C/62P on instructions, bit length of internal registers, and flags.

Table 4.1 Chart: R32C/111 Instructions

Item	R32C/111
Added instructions	ADDF, ADSF, BITINDEX, BRK2, CLIP, CMPF, CNVIF, DIVF, DIV (1), DIVU (1), DIVX (1), EXITI, EXTZ, FREIT, INDEX Type, MAX, MIN, MUL (1), MULU (1), MULX, MULF, ROUND, SCCnd, SCMPU, SIN, SMOVU, SOUT, STOP, SUBF, SUNTIL, and SWHILE
Mnemonic changed instructions	EDIV (from DIV), EDIVU (from DIVU), EDIVX (from DIVX), EMUL (from MUL), and EMULU (from MULU)
Deleted instructions	ADJNZ, BAND, BNAND, BNOR, BNTST, BNXOR, BOR, BXOR, JMPS, JSRS, LDE, LDINTB, STE, and SBJNZ

Note:
1. These instructions are newly added with existing mnemonics. (Refer to Table 4.2).

Table 4.2 Comparison Chart: Mnemonic Changed Instructions and Their Bit Length (reference)

Mnemonic	M16C/62P	R32C/111
DIV, DIVU, DIVX	16 bit ÷ 8 bit = 8 bit (for byte) 32 bit ÷16 bit = 16 bit (for word)	8 bit ÷ 8 bit = 8 bit (for byte) 16 bit ÷16 bit = 16 bit (for word)
MUL, MULU	8 bit × 8 bit = 16 bit (for byte) 16 bit ×16 bit = 32 bit (for word)	8 bit × 8 bit = 8 bit (for byte) 16 bit ×16 bit = 16 bit (for word)

Table 4.3 Comparison Chart: Bit Processing Instructions (reference)

Mnemonic	M16C/62P	R32C/111
BSET	Two-byte basis operation BSET bit,R0 (bit = 0 to 15) Example: BSET bit,R0 (bit 0~15)	One-byte basis operation BSET bit,R0L (bit = 0 to 7) BSET bit,R0H (bit = 0 to 7) Example: BSET bit,R0L (bit 0~7) BSET bit,R0H (bit 0~7)

Table 4.4 Comparison Chart: Bit Length of Internal Registers

Internal Register	M16C/62P		R32C/111	
	Register	Bit length	Register	Bit length
Data registers (1)	R0, R1, R2, R3	16 bits Registers R0 and R1 can be respectively divided into upper and lower 8-bit registers	R0, R1, R2, R3	16 bits Registers R0, R1, R2, and R3 can be respectively divided into upper and lower 8-bit registers. Registers R2 and R0, R3 and R1 can be respectively merged into one 32-bit register
			R4, R5, R6, R7	16 bits Registers R7 and R5, R6 and R4 can be respectively merged into one 32-bit register
Address register (1)	A0, A1	16 bits	A0, A1, A2, A3	32 bits
Static base register	SB		SB (1)	
Frame base register (1)	FB		FB	
User stack pointer	USP		USP	
Interrupt stack pointer	ISP		ISP	
Interrupt table register	INTB	20 bits	INTB	32 bits
	INTBL	16 bits	N/A	N/A
	INTBH	4 bits	N/A	N/A
Program counter	PC	20 bits	PC	32 bits
Flag register	FLG	16 bits	FLG	32 bits
Fast interrupt registers	N/A	N/A	SVF	32 bits
	N/A	N/A	SVP	
	N/A	N/A	VCT	
DMAC-associated registers	N/A	N/A	DMD0, DMD1, DMD2, DMD3	32 bits
	N/A	N/A	DCT0, DCT1, DCT2, DCT3	24 bits
	N/A	N/A	DCR0, DCR1, DCR2, DCR3	
	N/A	N/A	DSA0, DSA1, DSA2, DSA3	32 bits
	N/A	N/A	DDA0, DDA1, DDA2, DDA3	
	N/A	N/A	DSR0, DSR1, DSR2, DSR3	
	N/A	N/A	DDR0, DDR1, DDR2, DDR3	

Note:
1. There are two banks of these registers.

Table 4.5 Comparison Chart: Register Bank

Internal Register		M16C/62P	R32C/111
Static base register	SB	Register bank 0	Register bank 0 Register bank 1

Table 4.6 Comparison Chart: Flag Registers

Item	M16C/62P		R32C/111	
	Flag	Bit position	Flag	Bit position
Floating-point underflow flag	N/A	N/A	FU	b8
Floating-point overflow flag	N/A	N/A	FO	b9
Fixed-point designation flag	N/A	N/A	DP	b16
Floating-point round mode	N/A	N/A	RND	b19 and b18

4.2 Resets

Hardware reset 1, low voltage detection (hardware reset 2), software reset, watchdog timer reset, and oscillation stop detection reset are implemented to reset the MCU. However, the low voltage detection and oscillation stop detection reset are available only in the M16C/62P.
Some SFRs remain uninitialized even after a reset operation.
Table 4.7 to Table 4.9 list the changes from the M16C/62P on reset operations.

Table 4.7 Comparison Chart: Non-reset Registers

Item	Register	State after reset	
		M16C/62P	R32C/111
Hardware reset 1	PUR1	Reset value depends on CNVSS pin setting: 00h when CNVSS pin is low, 02h when CNVSS pin is high	Initialized irrespective of CNVSS level
	WDC	WDC5 bit is not initialized	N/A
Brown-out detection (hardware reset 2) (available only in the M16C/62P)	PUR1	Reset value depends on CNVSS pin setting: 00h when CNVSS pin is low, 02h when CNVSS pin is high	N/A
	WDC	WDC5 bit is not initialized	N/A
Software reset	PM0	Bits PM01 and PM00 are not initialized	
	VCR1	Not initialized	N/A
	VCR2	Not initialized	N/A
	PUR1	Reset value depends on bits PM01 and PM00 setting: 00h when these bits are 00b, 02h when these bits are 01b, 02h when these bits are 10b	Initialized irrespective of bits PM01 and PM00 setting value
	WDC	WDC5 bit is not initialized	N/A
Watchdog timer reset	PM0	Bits PM01 and PM00 are not initialized	
	VCR1	Not initialized	N/A
	VCR2	Not initialized	N/A
	PUR1	Reset value depends on bits PM01 and PM00 setting: 00h when these bits are 00b, 02h when these bits are 01b, 02h when these bits are 10b	Initialized irrespective of bits PM01 and PM00 setting value
	WDC	WDC5 bit is not initialized	N/A
Oscillation stop detection reset (available only in the M16C/62P)	PM0	Bits PM01 and PM00 are not initialized	N/A
	CM2	Bits CM27, CM21, and CM20 are not initialized	N/A
	VCR1	Not initialized	N/A
	VCR2	Not initialized	N/A
	PUR1	Reset value depends on bits PM01 and PM00 setting: 00h when these bits are 00b, 02h when these bits are 01b, 02h when these bits are 10b	N/A
	WDC	WDC5 bit is not initialized	N/A

Table 4.8 Comparison Chart: Clock Source and Divide Ratio After a Reset

Item	M16C/62P	R32C/111
Clock source	Main clock	PLL self oscillation mode
CPU clock	Divide-by-8	Divide-by-12
Peripheral bus clock	Divide-by-8	Divide-by-12
Other clocks	N/A	• Base clock: divide-by-6 • CPU clock: base clock divide-by-2 • Peripheral bus clock: base clock divide-by-2

Table 4.9 Comparison Chart: Clock Source Before a Software Reset

Item	M16C/62P	R32C/111
Clock source	Main clock	PLL clock

4.3 Voltage Regulator

The internal voltage of the M16C/62P is generated by reducing the input voltage from the VCC1 pin with the voltage regulator(s). To stabilize the internal voltage, a decoupling capacitor should be connected between pins VDC1 and BDC0. The M16C/62P does not require any decoupling capacitor. Table 4.10 lists the change on the voltage regulator control register.

Table 4.10 Comparison Chart: Voltage Regulator Control Register

Symbol	Address		Bit	M16C/62P	R32C/111
	M16C/62P	R32C/111			
VRCR	N/A	40060h	-	N/A	Available only in the R32C/111

4.4 Low Voltage Detection

Table 4.11 lists the changes on SFRs associated with low voltage detection.

Table 4.11 Comparison Chart: Low Voltage Detection-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
VCR1	0019h	N/A	-	Available only in the M16C/62P	N/A
VCR2	001Ah	N/A	-	Available only in the M16C/62P	N/A
D4INT	001Fh	N/A	-	Available only in the M16C/62P	N/A
WDC	000Fh	4404Fh	5	Coldstart/warmstart determination flag	Reserved
LVDC	N/A	40062h	-	N/A	Available only in the R32C/111
DVCR	N/A	40064h	-	N/A	Available only in the R32C/111

4.5 Processor Modes

Table 4.12 lists the changes on SFRs associated with processor mode.

Table 4.12 Comparison Chart: Processor Mode-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
PM0	0004h	40044h	5, 4	Multiplexed bus space select bits	Reserved
			6	Port P4_0 to P4_3 function select bit	Reserved
PM1	0005h	N/A	-	Available only in the M16C/62P	N/A

4.6 Clocks

Table 4.13 to Table 4.17 respectively list the changes on clock characteristics, settings, and associated SFRs.

Table 4.13 Comparison Chart: Clock Characteristics (1/2)

Item	M16C/62P	R32C/111
CPU clock after reset	Main clock divided by 8	PLL frequency synthesizer (self-oscillation mode) divided by 12
Main clock division	Selectable from 1, 2, 4, 8, and 16	Selectable from 1, 2, 3, and 4
Base clock division	N/A	Selectable from 2, 3, 4, and 6
CPU clock division	N/A	Selectable from 1, 2, 3, and 4
Peripheral bus clock division	N/A	Selectable from 2, 3, and 4
PLL multiplexed ratio	Selectable from 2, 4, 6, and 8	Selectable from values specified in the hardware manual
Peripheral clocks	f1, f2, f8, f32, f1SIO, f2SIO, f8SIO, f32SIO, fAD, and fC32	f1, f8, f2n, f32, fAD, and fC32
Stop mode	Each has its own procedure to enter stop mode	
Transition from medium-speed mode (divided-by-8 mode) to stop mode or wait mode	Enabled	N/A
Transition from high-/medium-speed mode to stop mode or wait mode	Enabled	N/A
Transition from PLL mode (high/medium speed) to stop mode or wait mode	N/A	Disabled
Transition from PLL operating mode to stop mode or wait mode	Disabled	N/A
Transition from low-speed/low power dissipation mode (1) to stop mode or wait mode	Enabled	Enabled

Note:
1. “low-speed mode” and “low power dissipation mode” are used in M16C/62P. These words are respectively changed to “low speed mode” and “low power mode” in R32C/111.

Table 4.14 Comparison Chart: Clock Characteristics (2/2)

Item	M16C/62P	R32C/111
Transition from on-chip oscillator mode/on-chip oscillator low power dissipation mode to stop mode or wait mode	Enabled	N/A
Transition from PLL self-oscillation mode to stop mode or wait mode	N/A	Enabled: wait mode Disabled: stop mode
CPU clock when exiting from stop mode	Main clock divided by 8	Divide ratio of CPU clock when the STOP instruction is executed

Table 4.15 Comparison Chart: Clock-associated Settings

Item	M16C/62P	R32C/111
XIN-XOUT drive power	CM15 bit in the CM1 register	Bits CM15 and CM16 in the CM1 register
Main clock division	CM06 bit in the CM0 register and bits CM17 and CM16 in the CM1 register	Bits CCD0 and CCD1 in the CCR register
Base clock division	N/A	Bits BCD0 and BCD1 in the CCR register
Peripheral bus clock division	N/A	Bits PCD0 and PCD1 in the CCR register
PLL multiplexed ratio	Bits PLC2 to PLC00 in the PLC0 register	Setting value of registers PLC0 and PLC1 specified in the hardware manual

Table 4.16 Comparison Chart: Clock-associated Pin

Pin	M16C/62P	R32C/111
CLKOUT	P5_7	P5_3

Table 4.17 Comparison Chart: Clock-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
CCR	N/A	0004h	-	N/A	Available only in the R32C/111
PBC	N/A	001Fh-001Eh	-	N/A	Available only in the R32C/111
CM0	0006h	40046h	-	Address changed	
			6	Main clock division select bit 0	Watchdog timer function select bit
			7	System clock select bit	Reserved
CM1	0007h	40047h	-	Address changed	
			0	All clock stop control bit	PLL clock oscillator stop bit
			1	System clock select bit 1	Reserved
			5	XIN-XOUT drive capacity select bit	XIN-XOUT drive power select bits
			6	Main clock division select bit 1	
			7		Reserved
CM2	000Dh	4004Dh	-	Address changed	
			1	System clock select bit 2	Reserved
			7	Operation select bit (when an oscillation stop, re-oscillation is detected)	Reserved
PCLKR	025Eh	N/A	-	Available only in the M16C/62P	N/A
CM3	N/A	4005Ah	-	N/A	Available only in the R32C/111
TCSPR	N/A	035Fh	-	N/A	Available only in the R32C/111
PLC0	001Ch	40020h	-	Address changed	
			2 to 0	PLL multiplexing functor select bits (PLC02, PLC01, PLC00)	Main counter divide ratio setting bit (MCV2, MCV1, MCV0)
			3	N/A	Main counter divide ratio setting bit (MCV3)
			4	Reserved	Main counter divide ratio setting bit (MCV4)
			6, 5		Swallow counter divide ratio setting bit (SVC1, SVC0)
			7	Operation enable bit (PLC07)	Swallow counter divide ratio setting bit (SVC2)
PLC1	N/A	40021h	-	N/A	Available only in the R32C/111
PM2	001Eh	40053h	-	Address changed	
			0	Specifying wait when accessing SFR at PLL operation	Reserved
			2	WDT count source protect bit	N/A
			4	Reserved	NMI enable bit
			6	N/A	f2n clock source select bit
			7	N/A	Reserved
CPSRF	0381h	0341h	-	Address changed	
PM3	N/A	40048h	-	N/A	Available only in the R32C/111

4.7 Bus

Table 4.18 to Table 4.22 respectively list the changes on bus characteristics, settings, bus control pins, and associated SFRs.

Table 4.18 Comparison Chart: Bus Characteristics

Item	M16C/62P	R32C/111
Address space	1 Mbyte/4 Mbytes (refer to memory expansion function)	4 Gbytes (available up to 64 Mbytes)
Address bus width	12/16/20 bits	24 bits fixed
External space wait states	1 to 3 wait states based on BCLK cycle	1 to 28 wait states based on base clock cycle
Recovery cycle insert (Address hold time after read/write)	N/A	Available
SFR area wait states	1 or 2 wait states (when PLL is in operation)	No wait state, Settable by the CCR register (divide-by-1, 2, 3, or 4)

Table 4.19 Comparison Chart: Bus Settings

Item	M16C/62P	R32C/111
Address bus width	• PM06 bit in the PM0 register • PM11 bit in the PM1 register	N/A
Data bus width	• All external space bus width is set by the BYTE pin; H: 8 bits L: 16 bits	• Each external space bus width is set by the BW0 bit in registers EBC0 to EBC3; 0: 8 bits as width 1: 16 bits as width • Maximum width of each external space bus is set by the EXBW0 bit in the PBC register; 0: 8 bits as maximum width 1: 16 bits as maximum width • Bus width after a reset is set by the lower two bits of reset vector (applicable to external space CS0 only); 11b: 8 bits 10b: 16 bits
Chip select signals	CSi bit in the CSR register (i = 0 to 3)	Registers CSOP0 and CSOP1
SFR area bus timing	PM20 bit in the PM2 register	PBC register
External space bus timing	• CSiW bit in the CSR register (i = 0 to 3) • Bits CSEi0 and CSEi1 in the CSE register (i = 0 to 3)	EBCi register (i = 0 to 3)
BCLK output	PM07 bit in the PM0 register	• PM07 bit in the PM0 register • Bits CM00 and CM01 in the CM0 register

Table 4.20 Comparison Chart: Bus Control Pins (when 8-/16-bit width multiplexed bus format is selected and $\overline{RD}$, $\overline{WR0}$, and $\overline{WR1}$ outputs are selected)

Bus Control Signal	Output Pins	
	M16C/62P	R32C/111
$\overline{CS3}$	P4_7	P4_4 (A20) (1)
		P5_7 ($\overline{RDY}$) (1)
$\overline{CS2}$	P4_6	P4_5 (A21) (1)
		P5_6 (ALE) (1)
$\overline{CS1}$	P4_5	P4_6 (A22) (1)
		P5_4 ($\overline{HLDA}$) (1)
$\overline{CS0}$	P4_4	P4_7 (A23) (1)
$\overline{WRH}$/$\overline{WR1}$ (2)	P5_1	P5_1
$\overline{WRL}$/$\overline{WR0}$ (2)	P5_0	P5_0
A23	N/A	P4_7 ($\overline{CS0}$) (1)
A22	N/A	P4_6 ($\overline{CS1}$) (1)
A21	N/A	P4_5 ($\overline{CS2}$) (1)
A20	N/A	P4_4 ($\overline{CS3}$) (1)
A15	P3_7/A15	P3_7/A15/ [A15/D15]
A14	P3_6/A14	P3_6/A14/ [A14/D14]
A13	P3_5/A13	P3_5/A13/ [A13/D13]
A12	P3_4/A12	P3_4/A12/ [A12/D12]
A11	P3_3/A11	P3_3/A11/ [A11/D11]
A10	P3_2/A10	P3_2/A10/ [A10/D10]
A9	P3_1/A9	P3_1/A9/ [A9/D9]
A8	P3_0/A8/ [A8/D7]	P3_0A8/ [A8/D8]
[A7/D7] or [A7/D6]	P2_7/ [A7/D7] / [A7/D6]	P2_7/ [A7/D7] / [A7/D7]
[A6/D6] or [A6/D5]	P2_6/ [A6/D6] / [A6/D5]	P2_6/ [A6/D6] / [A6/D6]
[A5/D5] or [A5/D4]	P2_5/ [A5/D5] / [A5/D4]	P2_5/ [A5/D5] / [A5/D5]
[A4/D4] or [A4/D3]	P2_4/ [A4/D4] / [A4/D3]	P2_4/ [A4/D4] / [A4/D4]
[A3/D3] or [A3/D2]	P2_3/ [A3/D3] / [A3/D2]	P2_3/ [A3/D3] / [A3/D3]
[A2/D2] or [A2/D1]	P2_2/ [A2/D2] / [A2/D1]	P2_2/ [A2/D2] / [A2/D2]
[A1/D1] or [A1/D0]	P2_1/ [A1/D1] / [A1/D0]	P2_1/ [A1/D1] / [A1/D1]
[A0/D0] or A0	P2_0/ [A0/D0] / A0	P2_0/ [A0/D0] / [A0/D0]

Notes:
1. A control pin in parentheses above shares an output pin with a corresponding bus control pin. Either of them should be selected for using.
2. $\overline{WRH}$ and $\overline{WRL}$ in the M16C/62P are respectively changed to $\overline{WR1}$ and $\overline{WR0}$ in the R32C/111.

Table 4.21 Comparison Chart: Bus Control Pins (when 8-/16-bit width multiplexed bus format is selected and $\overline{RD}$, $\overline{WR}$, $\overline{BC0}$, and $\overline{BC1}$ outputs are selected)

Bus Control Signal	Output Pins	
	M16C/62P	R32C/111
$\overline{CS3}$	P4_7	P4_4 (A20) (1)
		P5_7 ($\overline{RDY}$) (1)
$\overline{CS2}$	P4_6	P4_5 (A21) (1)
		P5_6 (ALE) (1)
$\overline{CS1}$	P4_5	P4_6 (A22) (1)
		P5_4 ($\overline{HLDA}$) (1)
$\overline{CS0}$	P4_4	P4_7 (A23) (1)
$\overline{BHE}$/$\overline{BC1}$ (2)	P5_1	P5_1
A23	N/A	P4_7 ($\overline{CS0}$) (1)
A22	N/A	P4_6 ($\overline{CS1}$) (1)
A21	N/A	P4_5 ($\overline{CS2}$) (1)
A20	N/A	P4_4 ($\overline{CS3}$) (1)
A15	P3_7/A15	P3_7/A15/ [A15/D15]
A14	P3_6/A14	P3_6/A14/ [A14/D14]
A13	P3_5/A13	P3_5/A13/ [A13/D13]
A12	P3_4/A12	P3_4/A12/ [A12/D12]
A11	P3_3/A11	P3_3/A11/ [A11/D11]
A10	P3_2/A10	P3_2/A10/ [A10/D10]
A9	P3_1/A9	P3_1/A9/ [A9/D9]
A8 or [A8/D7]	P3_0A8/ [A8/D7]	P3_0A8/ [A8/D8]
[A7/D7] or [A7/D6]	P2_7/ [A7/D7] / [A7/D6]	P2_7/ [A7/D7] / [A7/D7]
[A6/D6] or [A6/D5]	P2_6/ [A6/D6] / [A6/D5]	P2_6/ [A6/D6] / [A6/D6]
[A5/D5] or [A5/D4]	P2_5/ [A5/D5] / [A5/D4]	P2_5/ [A5/D5] / [A5/D5]
[A4/D4] or [A4/D3]	P2_4/ [A4/D4] / [A4/D3]	P2_4/ [A4/D4] / [A4/D4]
[A3/D3] or [A3/D2]	P2_3/ [A3/D3] / [A3/D2]	P2_3/ [A3/D3] / [A3/D3]
[A2/D2] or [A2/D1]	P2_2/ [A2/D2] / [A2/D1]	P2_2/ [A2/D2] / [A2/D2]
[A1/D1] or [A1/D0]	P2_1/ [A1/D1] / [A1/D0]	P2_1/ [A1/D1] / [A1/D1]
[A0/D0] or A0	P2_0/ [A0/D0] / A0 (2)	P2_0/ [A0/D0] / [$\overline{BC0}$/D0] (2)

Notes:
1. A control pin in parentheses above shares an output pin with a corresponding bus control pin. Either of them should be selected for using.
2. $\overline{BHE}$ and A0 in the M16C/62P are respectively changed to $\overline{BC1}$ and $\overline{BC0}$ in the R32C/111.

Table 4.22 Comparison Chart: Bus-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
PM0	0004h	40044h	-	Address changed	
			5, 4	Multiplexed bus space select bits	Reserved
			6	Port P4_0 to P4_3 function select bit	Reserved
PM1	0005h	N/A	-	Available only in the M16C/62P	N/A
CSR	0008h	N/A	-	Available only in the M16C/62P	N/A
CSE	001Bh	N/A	-	Available only in the M16C/62P	N/A
DBR	000Bh	N/A	-	Available only in the M16C/62P	N/A
PBC	N/A	001Fh-001Eh	-	N/A	Available only in the R32C/111
CSOP0	N/A	40054h	-	N/A	Available only in the R32C/111
CSOP1	N/A	40055h	-	N/A	Available only in the R32C/111
CB01	N/A	001Ah	-	N/A	Available only in the R32C/111
CB12	N/A	0016h	-	N/A	Available only in the R32C/111
CB23	N/A	0012h	-	N/A	Available only in the R32C/111
EBC0	N/A	001Dh-001Ch	-	N/A	Available only in the R32C/111
EBC1	N/A	0019h-0018h	-	N/A	Available only in the R32C/111
EBC2	N/A	0015h-0014h	-	N/A	Available only in the R32C/111
EBC3	N/A	0011h-0010h	-	N/A	Available only in the R32C/111

4.8 Protection

Table 4.23 lists the changes on SFRs associated with the protection.

Table 4.23 Comparison Chart: Protection-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
PRCR	000Ah	4004Ah	-	Address changed	
			0	Protect bit 0: Write enable to registers CM0, CM1,CM2, PLC0, and PCLKR	Protect bit 0: Write enable to registers CM0, CM1, CM2, and PM3
			1	Protect bit 1: Write enable to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1	Protect bit 1: Write enable to registers PM0. PM2, INVC0, INVC1, IOBC, CSOP0, and CSOP1
			2	Protect bit 2: Write enable to registers PD9, S3C, and S4C	Protect bit 2: Write enable to registers PD9, P9_iS (i = 3 to 7), PLC0, and PLC1
			3	Protect bit 3: Write enable to registers VCR2 and D4INT	N/A
PRCR2	N/A	4405Fh	7	N/A	CM3 protect bit: Write enable to the CM3 register
PRCR3	N/A	4004Ch	1	N/A	Protect bit 31: Write enable to registers VRCR, LVDC, and DVCR
PRR	N/A	0007h	7 to 0	N/A	Write enable to registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0, EBC1, EBC2, EBC3, CB01, CB12, and CB23: AAh: write enabled other than AAh: write disabled

4.9 Interrupts

Table 4.24 to Table 4.26 respectively list the changes on interrupt and associated SFRs.
The relocatable vector tables and interrupt priority level select circuitry of each are different.

Table 4.24 Comparison Chart: Interrupts

Item	M16C/62P	R32C/111
Address match interrupt	Settable up to 4 addresses	N/A

Table 4.25 Comparison Chart: Interrupt-associated SFRs (1/2)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
TB0IC	005Ah	0094h	-	Address changed	
TB1IC	005Bh	0076h	-	Address changed	
TB2IC	005Ch	0096h	-	Address changed	
TB3IC	0047h	0078h	-	Address changed	
TB4IC	0046h	0098h	-	Address changed	
TB5IC	0045h	0061h	-	Address changed	
BCN0IC/ BCN3IC	N/A	0069h	-	N/A	Available only in the R32C/111
BCN1IC/ BCN4IC	N/A	0089h	-	N/A	Available only in the R32C/111
BCNIC (BCN2IC)	004Ah	0087h	-	Address changed The symbol changed from BCNIC to BCN2IC	
BCN5IC/ BCN6IC	N/A	0066h	-	N/A	Available only in the R32C/111
DM0IC	004Bh	0068h	-	Address changed	
DM1IC	004Ch	0088h	-	Address changed	
DM2IC	N/A	006Ah	-	N/A	Available only in the R32C/111
DM3IC	N/A	008Ah	-	N/A	Available only in the R32C/111
KUPIC	004Dh	008Bh	-	Address changed	
ADIC (AD0IC)	004Eh	006Bh	-	Address changed The symbol changed from ADIC to AD0IC	
S0TIC	0051h	0090h	-	Address changed	
S1TIC	0053h	0092h	-	Address changed	
S2TIC	004Fh	0081h	-	Address changed	
S3TIC	N/A	0083h	-	N/A	Available only in the R32C/111
S4TIC	N/A	0085h	-	N/A	Available only in the R32C/111
S5TIC	N/A	0062h	-	N/A	Available only in the R32C/111
S6TIC	N/A	0064h	-	N/A	Available only in the R32C/111
S7TIC	N/A	00DDh	-	N/A	Available only in the R32C/111
S8TIC	N/A	00DFh	-	N/A	Available only in the R32C/111
S0RIC	0052h	0072h	-	Address changed	
S1RIC	0054h	0074h	-	Address changed	
S2RIC	0050h	0063h	-	Address changed	
S3RIC	N/A	0065h	-	N/A	Available only in the R32C/111
S4RIC	N/A	0067h	-	N/A	Available only in the R32C/111
S5RIC	N/A	0082h	-	N/A	Available only in the R32C/111
S6RIC	N/A	0084h	-	N/A	Available only in the R32C/111
S7RIC	N/A	00FDh	-	N/A	Available only in the R32C/111
S8RIC	N/A	00FFh	-	N/A	Available only in the R32C/111
TA0IC	0055h	006Ch	-	Address changed	
TA1IC	0056h	008Ch	-	Address changed	

Table 4.26 Comparison Chart: Interrupt-associated SFRs (2/2)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
TA2IC	0057h	006Eh	-	Address changed	
TA3IC	0058h	006Eh	-	Address changed	
TA4IC	0059h	0070h	-	Address changed	
IIO0IC	N/A	006Dh	-	N/A	Available only in the R32C/111
IIO1IC	N/A	008Dh	-	N/A	Available only in the R32C/111
IIO2IC	N/A	006Fh	-	N/A	Available only in the R32C/111
IIO3IC	N/A	008Fh	-	N/A	Available only in the R32C/111
IIO4IC	N/A	0071h	-	N/A	Available only in the R32C/111
IIO5IC	N/A	0091h	-	N/A	Available only in the R32C/111
IIO6IC	N/A	0073h	-	N/A	Available only in the R32C/111
IIO7IC	N/A	0093h	-	N/A	Available only in the R32C/111
IIO8IC	N/A	0075h	-	N/A	Available only in the R32C/111
IIO9IC	N/A	0095h	-	N/A	Available only in the R32C/111
IIO10IC	N/A	0077h	-	N/A	Available only in the R32C/111
IIO11IC	N/A	0097h	-	N/A	Available only in the R32C/111
INT0IC	005Dh	009Eh	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
INT1IC	005Eh	007Eh	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
INT2IC	005Fh	009Ch	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
INT3IC	0044h	007Ch	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
INT4IC	0049h	009Ah	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
INT5IC	0048h	007Ah	-	Address changed	
			5	Reserved	Level/sense sensitive select bit
RIPL1	N/A	4407Fh	-	N/A	Available only in the R32C/111
RIPL2	N/A	4407Dh	-	N/A	Available only in the R32C/111
IFSR (IFSR0)	035Fh	4406Fh	-	Address changed The symbol changed from IFSR to IFSR0	
			6	Interrupt request factor select bit 0: SI/O3, 1: $\overline{\text{INT4}}$	UART0/UART3 interrupt source select bit
			7	Interrupt request factor select bit 0: SI/O4, 1: $\overline{\text{INT5}}$	UART1/UART4 interrupt source select bit
IFSR1	N/A	4406Dh	-	N/A	Available only in the R32C/111
IFSR2A	035Eh	N/A	-	Available only in the M16C/62P	N/A
RMAD0	0012h-0010h	N/A	-	Available only in the M16C/62P	N/A
RMAD1	0016h-0014h	N/A	-	Available only in the M16C/62P	N/A
RMAD2	01BAh-01B8h	N/A	-	Available only in the M16C/62P	N/A
RMAD3	01BEh-01BCh	N/A	-	Available only in the M16C/62P	N/A
AIER	0009h	N/A	-	Available only in the M16C/62P	N/A
AIER2	01BBh	N/A	-	Available only in the M16C/62P	N/A

4.10 Watchdog Timer

Table 4.27 and Table 4.28 respectively list the changes on watchdog timer and associated SFRs.

Table 4.27 Comparison Chart: Watchdog Timer

Item	M16C/62P	R32C/111
Clock source for watchdog timer	• CPU clock (PLL clock, main clock, on-chip oscillator clock) • Sub clock • On-chip oscillator clock	Peripheral bus clock (PLL clock, sub clock, or on-chip oscillator clock respectively divided by CCR register setting)
Watchdog timer prescaler divide ratio	Divide-by-2 (when sub clock is selected), -16, or -128	Divide-by-16, or -128
Count source protective mode	Enabled	N/A

Table 4.28 Comparison Chart: Watchdog Timer-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
CM0	0006h	40046h	-	Address changed	
			6	Main clock division select bit 0	Watchdog timer function select bit
			7	CPU clock select bit 0	Reserved
PM1	0005h	N/A	-	Available only in the M16C/62P	N/A
WDC	000Fh	4404Fh	-	Address changed	
			5	Coldstart/warmstart determination bit	Reserved
WDTS	000Eh	4404Eh	-	Address changed	

4.11 DMAC

The DMA controller is enhanced in the R32C/111. Table 4.29 to Table 4.31 respectively list the changes on DMAC characteristics, settings, and associated SFRs.

Table 4.29 Comparison Chart: DMAC

Item	M16C/62P	R32C/111
DMAC-associated registers	Allocated in SFRs	Allocated in CPU internal register and SFRs
Channels	2	4
Transfer memory space	From a given address in a 1-Mbyte space to a fixed address in the same space or from a fixed address in a 1-Mbyte space to a given address in the same space	From a given address in a 64-Mbyte space (00000000h to 01FFFFFFh and FE000000h to FFFFFFFFh) to another given address in the same space
Maximum transfer bytes	• 128 Kbytes (when a 16-bit data is transferred) • 64 Kbytes (when a 8-bit data is transferred)	• 64 Mbytes (when a 32-bit data is transferred) • 32 Mbytes (when a 16-bit data is transferred) • 16 Mbytes (when a 8-bit data is transferred)
Transfer unit	8 bits or 16 bits	8 bits, 16 bits, or 32 bits
Destination/source addresses	Fixed address: one specified address Forward address: address which is incremented by a transfer unit on each successive access. (Source address and destination address cannot be both fixed nor both icremented.)	Forward or fixed
Transfer cycles	Value set in the DMAi transfer counter (i = 0, 1) + 1	Value set in the DCTi register (i = 0 to 3)
DMA interrupt request generation timing	When the DMAi transfer counter underflows	When the DCTi register changes from 00000001h to 00000000h

Table 4.30 Comparison Chart: DMAC Settings

Item	M16C/62P	R32C/111
DMA request sources	Selected by bits DSEL3 to DSEL0 in the DMiSL register (i = 0, 1)	Selected by bits DSEL4 to DSEL0 in the DMiSL register (i = 0 to 3) or bits DSEL24 to DSEL20 in the DMiSL2 register
Transfer mode	DMiCON register (i = 0, 1)	DMDi register (i = 0 to 3)
Source address	SARi register (i = 0, 1)	DSAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DSRi register)
Destination address	DARi register (i = 0, 1)	DDAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DDRi register)
Transfer cycles	“Transfer cycles - 1” is set to the TCRi register (i = 0, 1)	Number of transfer cycles is set to the DCTi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DCRi register)

Table 4.31 Comparison Chart: DMAC-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
DM0SL	03B8h	44078h	-	Address changed	
			4	N/A	DMA request source select bit
			6	DMA request factor expansion select bit	N/A
			7	Software DMA request bit	N/A (1)
DM1SL	03BAh	44079h	-	Address changed	
			4	N/A	DMA request source select bit
			6	DMA request factor expansion select bit	N/A
			7	Software DMA request bit	N/A (2)
DM2SL	N/A	4407Ah	-	N/A	Available only in the R32C/111
DM3SL	N/A	4407Bh	-	N/A	Available only in the R32C/111
DM0SL2	N/A	44070h	-	N/A	Available only in the R32C/111
DM1SL2	N/A	44071h	-	N/A	Available only in the R32C/111
DM2SL2	N/A	44072h	-	N/A	Available only in the R32C/111
DM3SL2	N/A	44073h	-	N/A	Available only in the R32C/111
DM0CON	002Ch	N/A	-	Available only in the M16C/62P	N/A
DM1CON	003Ch	N/A	-	Available only in the M16C/62P	N/A
SAR0	0022h to 0020h	N/A	-	Available only in the M16C/62P	N/A
SAR1	0032h to 0030h	N/A	-	Available only in the M16C/62P	N/A
DAR0	0026h to 0024h	N/A	-	Available only in the M16C/62P	N/A
DAR1	0036h to 0034h	N/A	-	Available only in the M16C/62P	N/A
TCR0	0029h and 0028h	N/A	-	Available only in the M16C/62P	N/A
TCR1	0039h and 0038h	N/A	-	Available only in the M16C/62P	N/A
DMD0 to DMD3	N/A	CPU internal register (3)	-	N/A	Available only in the R32C/111
DCT0 to DCT3	N/A		-	N/A	Available only in the R32C/111
DCR0 to DCR3	N/A		-	N/A	Available only in the R32C/111
DSA0 to DSA3	N/A		-	N/A	Available only in the R32C/111
DSR0 to DSR3	N/A		-	N/A	Available only in the R32C/111
DDA0 to DDA3	N/A		-	N/A	Available only in the R32C/111
DDR0 to DDR3	N/A		-	N/A	Available only in the R32C/111

Notes:
1. Software DMA request bit is moved to bit 5 of the DM0SL2 register in the R32C/111.
2. Software DMA request bit is moved to bit 5 of the DM1SL2 register in the R32C/111.
3. The LDC instruction should be used to write to this register.

4.12 Timers

Table 4.32 and Table 4.33 respectively list the changes on timers and associated SFRs.

Table 4.32 Comparison Chart: Timers

Item	M16C/62P	R32C/111
Count sources	f1/f2, f8, f32, fC32	f1, f8, f2n, fC32
Pulse output function	MR0 bit in the TAiMR register (i = 0 to 4)	Function select register

Table 4.33 Comparison Chart: Timers-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
TA0 to TA4	0387h-0386h to 038Fh-038Eh	0347h-0346h to 034Fh-034Eh	-	Address changed	
TA0MR	0396h	0356h	-	Address changed	
			2	Pulse output function select bit	Reserved
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TA1MR	0397h	0357h	-	Address changed	
			2	Pulse output function select bit	Reserved
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TA2MR	0398h	0358h	-	Address changed	
			2	Pulse output function select bit	Reserved
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TA3MR	0399h	0359h	-	Address changed	
			2	Pulse output function select bit	Reserved
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TA4MR	039Ah	035Ah	-	Address changed	
			2	Pulse output function select bit	Reserved
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TABSR	0380h	0340h	-	Address changed	
UDF	0384h	0344h	-	Address changed	
ONSF	0382h	0342h	-	Address changed	
TRGSR	0383h	0343h	-	Address changed	
TCSPR	N/A	035Fh	-	N/A	Available only in the R32C/111
CPSRF	0381h	0341h	-	Address changed	
TB0 to TB2	0391h-0390h to 0395h-0394h	0351h-0350h to 0355h-0354h	-	Address changed	
TB3 to TB5	0351h-0350h to 0355h-0354h	0311h-0310h to 0315h-0314h	-	Address changed	
TB0MR	039Bh	035Bh	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TB1MR	039Ch	035Ch	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TB2MR	039Dh	035Dh	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TB3MR	035Bh	031Bh	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TB4MR	035Ch	031Ch	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TB5MR	035Dh	031Dh	-	Address changed	
			7, 6	Count source select bit (f1/f2, f32)	Count source select bit (f1, f2n)
TBSR	0340h	0300h	-	Address changed	

4.13 Three-phase Motor Control Timers

Table 4.34 and Table 4.35 respectively list the changes on three-phase motor control timers and associated SFR.

Table 4.34 Comparison Chart: Three-phase Motor Control Timers

Item	M16C/62P	R32C/111
Output function	N/A	Switchable pin combination: U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ of ports P7 and P8 or those of port P3
Count sources	f1/f2, f8, f32, fC32	f1, f8, f2n, fC32

Table 4.35 Comparison Chart: Three-phase Motor Control Timers-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
INVC0	0348h	0308h	-	Address changed	
INVC1	0349h	0309h	-	Address changed	
IOBC	N/A	40097h	-	N/A	Available only in the R32C/111
IDB0	034Ah	030Ah	-	Address changed	
IDB1	034Bh	030Bh	-	Address changed	
ICTB2	034Dh	030Dh	-	Address changed	
TB2SC	039Eh	035Eh	-	Address changed	
TA11	0343h-0342h	0303h-0302h	-	Address changed	
TA21	0345h-0344h	0305h-0304h	-	Address changed	
TA41	0347h-0346h	0307h-0306h	-	Address changed	
INVC1	034Ch	030Ch	-	Address changed	

4.14 Serial Interface

Table 4.36 to Table 4.41 respectively list the changes on serial interface, associated pins, and associated SFRs.

Table 4.36 Comparison Chart: Serial Interface

Item	M16C/62P	R32C/111
Synchronous/asynchronous serial interface	3 channels (UART0 to UART2)	9 channels (UART0 to UART8)
I^2C bus	3 channels (UART0 to UART2)	7 channels (UART0 to UART6)
Special mode 2	3 channels (UART0 to UART2)	7 channels (UART0 to UART6)
IEBus (1) mode	3 channels (UART0 to UART2)	7 channels (UART0 to UART6) (optional (2))
Special mode 4 (SIM mode)	1 channel (UART2)	N/A
Clock synchronous serial I/O	2 channels (SI/O3 and SI/O4)	N/A
Count sources	f1/f2, f8, f32	f1, f8, f2n
Transfer clock output from multiple pins	Selectable in UART1	N/A
Separate $\overline{CTS}/\overline{RTS}$ pin	Selectable in UART0	N/A
Output pin function	Available by setting UART-associated registers	Available by setting function select registers

Notes:
1. IEBus is a trademark of NEC Electronics Corporation.
2. Please contact a Renesas sales office to use the optional feature.

Table 4.37 Comparison Chart: Serial Interface-associated Pins (1/2)

Channel	Port	M16C/62P	R32C/111
UART0	P6_0	$\overline{CTS0}/\overline{RTS0}$	$\overline{CTS0}/\overline{RTS0}/\overline{SS0}$
	P6_1	CLK0	CLK0
	P6_2	RXD0/SCL0	RXD0/SCL0/STXD0
	P6_3	TXD0/SDA0	TXD0/SDA0/SRXD0
UART1	P6_4	$\overline{CTS1}/\overline{RTS1}/\overline{CT0}$/CLKS1	$\overline{CTS1}/\overline{RTS1}/\overline{SS1}$
	P6_5	CLK1	CLK1
	P6_6	RXD1/SCL1	RXD1/SCL1/STXD1
	P6_7	TXD1/SDA1	TXD1/SDA1/SRXD1
UART2	P7_0	TXD2/SDA2	TXD2/SDA2/SRXD2
	P7_1	RXD2/SCL2	RXD2/SCL2/STXD2
	P7_2	CLK2	CLK2
	P7_3	$\overline{CTS2}/\overline{RTS2}$	$\overline{CTS2}/\overline{RTS2}/\overline{SS2}$
SI/O3 / UART3	P9_0	CLK3	N/A
	P9_1	SIN3	N/A
	P9_2	SOUT3	N/A
	P4_0	N/A	$\overline{CTS3}/\overline{RTS3}/\overline{SS3}$
	P4_1	N/A	CLK3
	P4_2	N/A	RXD3/SCL3/STXD3
	P4_3	N/A	TXD3/SDA3/SRXD3

Table 4.38 Comparison Chart: Serial Interface-associated Pins (2/2)

Channel	Port	M16C/62P	R32C/111
SI/O4 / UART4	P9_4	N/A	$\overline{\text{CTS4}}$/$\overline{\text{RTS4}}$/$\overline{\text{SS4}}$
	P9_5	CLK4	CLK4
	P9_6	SOUT4	TXD4/SDA4/SRXD4
	P9_7	SIN4	RXD4/SCL4/STXD4
UART5	P7_6	N/A	TXD5/SDA5/SRXD5
	P7_7	N/A	CLK5
	P8_0	N/A	RXD5/SCL5/STXD5
	P8_1	N/A	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$
UART6	P4_4	N/A	$\overline{\text{CTS6}}$/$\overline{\text{RTS6}}$/$\overline{\text{SS6}}$
	P4_5	N/A	CLK6
	P4_6	N/A	RXD6/SCL6/STXD6
	P4_7	N/A	TXD6/SDA6/SRXD6
UART7	P5_4	N/A	TXD7
	P5_5	N/A	CLK7
	P5_6	N/A	RXD7
	P5_7	N/A	$\overline{\text{CTS7}}$/$\overline{\text{RTS7}}$
UART8	P7_3	N/A	TXD8
	P7_4	N/A	CLK8
	P7_5	N/A	RXD8
	P7_6	N/A	$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$

Table 4.39 Comparison Chart: Serial Interface-associated SFRs (1/3)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
U0MR	03A0h	0368h	-	Address changed	
U1MR	03A8h	02E8h	-	Address changed	
U2MR	0378h	0338h	-	Address changed	
U3MR	N/A	0328h	-	Address changed	
U4MR	N/A	02F8h	-	Address changed	
U5MR	N/A	1C8h	-	Address changed	
U6MR	N/A	1D8h	-	N/A	Available only in the R32C/111
U7MR	N/A	1E0h	-	N/A	Available only in the R32C/111
U8MR	N/A	1E8h	-	N/A	Available only in the R32C/111
U0C0	03A4h	036Ch	-	Address changed	
			2	$\overline{CRS}$/$\overline{RTS}$ function select bit	Reserved
U1C0	03ACh	02ECh	-	Address changed	
			2	$\overline{CRS}$/$\overline{RTS}$ function select bit	Reserved
U2C0	037Ch	033Ch	-	Address changed	
			2	$\overline{CRS}$/$\overline{RTS}$ function select bit	Reserved
U3C0	N/A	032Ch	-	N/A	Available only in the R32C/111
U4C0	N/A	02FCh	-	N/A	Available only in the R32C/111
U5C0	N/A	01CCh	-	N/A	Available only in the R32C/111
U6C0	N/A	01DCh	-	N/A	Available only in the R32C/111
U7C0	N/A	01E4h	-	N/A	Available only in the R32C/111
U8C0	N/A	01ECh	-	N/A	Available only in the R32C/111
U0C1	03A5h	036Dh	-	Address changed	
			4	N/A	UART0 transmit interrupt source select bit
			5	N/A	UART0 continuous receive mode enable bit
			7	Error signal output enable bit	Reserved
U1C1	03ADh	02EDh	-	Address changed	
			4	N/A	UART1 transmit interrupt source select bit
			5	N/A	UART1 continuous receive mode enable bit
			7	Error signal output enable bit	Reserved
U2C1	037Dh	033Dh	-	Address changed	
			7	Error signal output enable bit	Reserved
U3C1	N/A	032Dh	-	N/A	Available only in the R32C/111
U4C1	N/A	02FDh	-	N/A	Available only in the R32C/111
U5C1	N/A	01CDh	-	N/A	Available only in the R32C/111
U6C1	N/A	01DDh	-	N/A	Available only in the R32C/111
U7C1	N/A	01E5h	-	N/A	Available only in the R32C/111
U8C1	N/A	01EDh	-	N/A	Available only in the R32C/111
UCON	03B0h	N/A	-	Available only in the M16C/62P	N/A
U78CON	N/A	01F0h	-	N/A	Available only in the R32C/111
U0SMR	036Fh	0367h	-	Address changed	
			4	LSYN bit (1)	Reserved
U1SMR	0373h	02E7h	-	Address changed	
			4	LSYN bit (1)	Reserved
U2SMR	0377h	0337h	-	Address changed	
			4	LSYN bit (1)	Reserved

Note:
1. This bit functions as LSTN bit for the following products: M3062LFGFP and M3062LFGPFP. For other products, this bit is reserved.

Table 4.40 Comparison Chart: Serial Interface-associated SFRs (2/3)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
U3SMR	N/A	0327h	-	N/A	Available only in the R32C/111
U4SMR	N/A	02F7h	-	N/A	Available only in the R32C/111
U5SMR	N/A	01C7h	-	N/A	Available only in the R32C/111
U6SMR	N/A	01D7h	-	N/A	Available only in the R32C/111
U0SMR2	036Eh	0366h	-	Address changed	
U1SMR2	0372h	02E6h	-	Address changed	
U2SMR2	0376h	0336h	-	Address changed	
U3SMR2	N/A	0326h	-	N/A	Available only in the R32C/111
U4SMR2	N/A	02F6h	-	N/A	Available only in the R32C/111
U5SMR2	N/A	01C6h	-	N/A	Available only in the R32C/111
U6SMR2	N/A	01D6h	-	N/A	Available only in the R32C/111
U0SMR3	036Dh	0365h	-	Address changed	
			0	N/A	$\overline{SS}$ pin function enable bit
			2	N/A	Serial input pin set bit
			4	N/A	Mode error flag
U1SMR3	036Dh	0365h	-	Address changed	
			0	N/A	$\overline{SS}$ pin function enable bit
			2	N/A	Serial input pin set bit
			4	N/A	Mode error flag
U2SMR3	036Dh	0365h	-	Address changed	
			0	N/A	$\overline{SS}$ pin function enable bit
			2	N/A	Serial input pin set bit
			4	N/A	Mode error flag
U3SMR3	N/A	0325h	-	N/A	Available only in the R32C/111
U4SMR3	N/A	02F5h	-	N/A	Available only in the R32C/111
U5SMR3	N/A	01C5h	-	N/A	Available only in the R32C/111
U6SMR3	N/A	01D5h	-	N/A	Available only in the R32C/111
U0SMR4	036Ch	0364h	-	Address changed	
U1SMR4	0370h	02E4h	-	Address changed	
U2SMR4	0374h	0334h	-	Address changed	
U3SMR4	N/A	0324h	-	N/A	Available only in the R32C/111
U4SMR4	N/A	02F4h	-	N/A	Available only in the R32C/111
U5SMR4	N/A	01C4h	-	N/A	Available only in the R32C/111
U6SMR4	N/A	01D4h	-	N/A	Available only in the R32C/111
U0BRG	03A1h	0369h	-	Address changed	
U1BRG	03A9h	02E9h	-	Address changed	
U2BRG	0379h	0339h	-	Address changed	
U3BRG	N/A	0329h	-	N/A	Available only in the R32C/111
U4BRG	N/A	02F9h	-	N/A	Available only in the R32C/111
U5BRG	N/A	01C9h	-	N/A	Available only in the R32C/111
U6BRG	N/A	01D9h	-	N/A	Available only in the R32C/111
U7BRG	N/A	01E1h	-	N/A	Available only in the R32C/111
U8BRG	N/A	01E9h	-	N/A	Available only in the R32C/111
U0TB	03A3h-03A2h	036Bh-036Ah	-	Address changed	
U1TB	03ABh-03AAh	02EBh-02EAh	-	Address changed	
U2TB	037Bh-037Ah	033Bh-033Ah	-	Address changed	
U3TB	N/A	032Bh-032Ah	-	N/A	Available only in the R32C/111
U4TB	N/A	02FBh-02FAh	-	N/A	Available only in the R32C/111
U5TB	N/A	01CBh-01CAh	-	N/A	Available only in the R32C/111

Table 4.41 Comparison Chart: Serial Interface-associated SFRs (3/3)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
U6TB	N/A	01DBh-01DAh	-	N/A	Available only in the R32C/111
U7TB	N/A	01E3h-01E2h	-	N/A	Available only in the R32C/111
U8TB	N/A	01EBh-01EAh	-	N/A	Available only in the R32C/111
U0RB	03A7h-03A6h	036Fh-036Eh	-	Address changed	
U1RB	03AFh-03AEh	02EFh-02EEh	-	Address changed	
U2RB	037Fh-037Eh	033Fh-033Eh	-	Address changed	
U3RB	N/A	032Fh-032Eh	-	N/A	Available only in the R32C/111
U4RB	N/A	02FFh-02FEh	-	N/A	Available only in the R32C/111
U5RB	N/A	01CFh-01CEh	-	N/A	Available only in the R32C/111
U6RB	N/A	01DFh-01DEh	-	N/A	Available only in the R32C/111
U7RB	N/A	01E7h-01E6h	-	N/A	Available only in the R32C/111
U8RB	N/A	01EFh-01EEh	-	N/A	Available only in the R32C/111
IFSR (IFSR0)	035Fh	4406Fh	-	Address changed The symbol changed from IFSR to IFSR0	
			6	Interrupt request factor select bit 0: SI/O3, 1: $\overline{\text{INT4}}$	UART0/UART3 interrupt source select bit
			7	Interrupt request factor select bit 0: SI/O4, 1: $\overline{\text{INT5}}$	UART1/UART4 interrupt source select bit
IFSR2A	035Eh	N/A	-	Available only in the M16C/62P	N/A
IFSR1	N/A	4406Dh	-	N/A	Available only in the R32C/111
S3C	0362h	N/A	-	Available only in the M16C/62P	N/A
S4C	0366h	N/A	-	Available only in the M16C/62P	N/A
S3BRG	0363h	N/A	-	Available only in the M16C/62P	N/A
S4BRG	0367h	N/A	-	Available only in the M16C/62P	N/A
S3TRR	0360h	N/A	-	Available only in the M16C/62P	N/A
S4TRR	0364h	N/A	-	Available only in the M16C/62P	N/A

4.15 A/D Converter

Table 4.42 and Table 4.43 respectively list the changes on DMAC characteristics and associated SFRs.

Table 4.42 Comparison Chart: A/D Converter

Item	M16C/62P	R32C/111
Operation clock, ϕAD	fAD, fAD/2, fAD/3, fAD/4, fAD/6, or fAD/12	fAD, fAD/2, fAD/3, fAD/4, fAD/6, or fAD/8
Notes on operation clock	The ϕAD frequency should be 12 MHz or below. When VCC1 is under 4.0 V, divide fAD so that the ϕAD frequency becomes 10 MHz or below	The ϕAD frequency should be as follows: When VCC1 = 5 V; 16 MHz or below When VCC1 = 3.3 V; 10 MHz or below
Operating modes	5 modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweet mode 0 • Repeat sweep mode 1	7 modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweet mode 0 • Repeat sweep mode 1 • Multi-port single sweep mode • Multi-port repeat sweep mode 0
A/D conversion start conditions	• Software trigger • External trigger (Retrigger is enabled)	• Software trigger • External trigger (Retrigger is enabled) • Hardware trigger (Retrigger is enabled)

Table 4.43 Comparison Chart: A/D converter associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
ADCON0 (AD0CON0)	03D6h	0396h	-	Address changed The symbol changed from ADCON0 to AD0CON0	
ADCON1 (AD0CON1)	03D7h	0397h	-	Address changed The symbol changed from ADCON1 to AD0CON1	
ADCON2 (AD0CON2)	03D4h	0394h	-	Address changed The symbol changed from ADCON2 to AD0CON2	
			4	Frequency select bit 2	N/A (1)
ADCON3	NA	0395h	-	NA	Available only in the R32C/111
ADCON4	NA	0392h	-	NA	Available only in the R32C/111
AD0 (AD00)	03C1h-03C0h	0381h-0380h	-	Address changed The symbol changed from AD0 to AD00	
AD1 (AD01)	03C3h-03C2h	0383h-0382h	-	Address changed The symbol changed from AD1 to AD01	
AD2 (AD02)	03C5h-03C4h	0385h-0384h	-	Address changed The symbol changed from AD2 to AD02	
AD3 (AD03)	03C7h-03C6h	0387h-0386h	-	Address changed The symbol changed from AD3 to AD03	
AD4 (AD04)	03C9h-03C8h	0389h-0388h	-	Address changed The symbol changed from AD4 to AD04	
AD5 (AD05)	03CBh-03CAh	038Bh-038Ah	-	Address changed The symbol changed from AD5 to AD05	
AD6 (AD06)	03CDh-03CCh	038Dh-038Ch	-	Address changed The symbol changed from AD6 to AD06	
AD7 (AD07)	03CFh-03CEh	038Fh-038Eh	-	Address changed The symbol changed from AD7 to AD07	

Note:
1. Frequency select bit 2 is moved to bit 2 of the AD0CON3 register in the R32C/111.

4.16 D/A Converter

Table 4.44 lists the change on SFRs associated with the D/A converter.

Table 4.44 Comparison Chart: D/A Converter-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
DACON1	03DCh	039Ch	-	Address changed	
DA0	03D8h	0398h	-	Address changed	
DA1	03DAh	039Ah	-	Address changed	

4.17 CRC Calculator

Table 4.45 lists the change on SFRs associated with the CRC calculator.

Table 4.45 Comparison Chart: D/A Converter-associated SFRs

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
CRCD	03BDh-03BCh	037Dh-037Ch	-	Address changed	
CRCIN	03BEh	037Eh	-	Address changed	

4.18 Ports

4.18.1 Port Pi Registers and Port Pi Direction Registers

Table 4.46 to Table 4.48 respectively list the changes on port Pi-associated registers (i = 0 to 10).

Table 4.46 Comparison Chart: Port Pi registers (i = 0 to 10)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
P0	03E0h	03C0h	-	Address changed	
P1	03E1h	03C1h	-	Address changed	
P2	03E4h	03C4h	-	Address changed	
P3	03E5h	03C5h	-	Address changed	
P4	03E8h	03C8h	-	Address changed	
P5	03E9h	03C9h	-	Address changed	
P6	03ECh	03CCh	-	Address changed	
P7	03EDh	03CDh	-	Address changed	
P8	03F0h	03D0h	-	Address changed	
P9	03F1h	03D1h	0	P9_0	Reserved
			1	P9_1	P9_1 (input only port)
			2	P9_2	Reserved
P10	03F4h	03D4h	-	Address changed	

Table 4.47 Comparison Chart: Port Pi Direction Registers (i = 0 to 10)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
PD0	03E2h	03C2h	-	Address changed	
PD1	03E3h	03C3h	-	Address changed	
PD2	03E6h	03C6h	-	Address changed	
PD3	03E7h	03C7h	-	Address changed	
PD4	03EAh	03CAh	-	Address changed	
PD5	03EBh	03CBh	-	Address changed	
PD6	03EEh	03CEh	-	Address changed	
PD7	03EFh	03CFh	-	Address changed	
PD8	03F2h	03D2h	-	Address changed	
PD9	03F3h	03D3h	0	PD9_2	Reserved
			1	PD9_1	Reserved
			2	PD9_0	Reserved
PD10	03F6h	03D6h	-	Address changed	

Table 4.48 Comparison Chart: Port Pi Pull-up Control Registers (i = 0 to 10)

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
PUR0	03FCh	03F0h	-	Address changed	
PUR1	03FDh	03F1h	-	Address changed	
			4	P6_0 to P6_3 pull-up control bit	Reserved
			5	P6_4 to P6_7 pull-up control bit	Reserved
			6	P7_2 to P7_3 pull-up control bit	Reserved
			7	P7_4 to P7_7 pull-up control bit	Reserved
PUR2	03DAh	03F2h	-	Address changed	
			0	P8_0 to P8_3 pull-up control bit	P6_0 to P6_3 pull-up control bit
			1	P8_4 to P8_7 pull-up control bit	P6_4 to P6_7 pull-up control bit
			2	P9_0 to P9_3 pull-up control bit	P7_2 to P7_3 pull-up control bit
			3	P9_4 to P9_7 pull-up control bit	P7_4 to P7_7 pull-up control bit
			4	P10_0 to P10_3 pull-up control bit	P8_0 to P8_3 pull-up control bit
			5	P10_4 to P10_7 pull-up control bit	P8_4 to P8_7 pull-up control bit
			6	NA	P9_1 and P9_3 pull-up control bit
			7	NA	P9_4 to P9_7 pull-up control bit
PUR3	N/A	03F3h	-	NA	Available only in the R32C/111

4.18.2 Port I/O Function Selection

In the R32C/111, an output function of either the programmable I/O port or a peripheral function is selected by the port Pi_j function select registers (i = 0 to 10, j = 0 to 7). As for the input function, if a peripheral function input is assigned to multiple pins, an input pin to be connected is selected by the input function select register. Refer to the hardware manual for details.

4.19 Flash Memory

4.19.1 Flash Memory

Table 4.49 to Table 4.51 respectively list the changes on flash memory, software commands, and associated registers.

Table 4.49 Comparison Chart: Flash Memory

Item	M16C/62P	R32C/111
Unit to be programmed	2 bytes	8 bytes
Erase and program endurance	100 times (all areas) or 1,000 times (user ROM area except blocks A and 1) and 10,000 times (blocks A and 1)	1, 000 times (program area) and 10,000 times (data area)
Software commands	8	9

Table 4.50 Comparison Chart: Software Commands

Item	M16C/62P				R32C/111			
	First command		Second command		First command		Second command	
	Address	Data	Address	Data	Address	Data	Address	Data
Read array mode shift	x	xxFFh	N/A	N/A	FFFFF800h	00FFh	N/A	N/A
Read status register mode shift (1)	x	xx70h	N/A	N/A	FFFFF800h	0070h	N/A	N/A
Clear status register	x	xx50h	N/A	N/A	FFFFF800h	0050h	N/A	N/A
Program (2, 3)	WA	xx40h	WA	WD	FFFFF800h	0043h	WA	WD
Erase all unlocked block	x	xxA7h	x	xxD0h	N/A	N/A	N/A	N/A
Block erase	x	xx20h	BA	xxD0h	FFFFF800h	0020h	BA	00D0h
Lock bit program	BA	xx77h	BA	xxD0h	FFFFF800h	0077h	BA	00D0h
Read lock bit status	x	xx71h	BA	xxD0h	FFFFF800h	0071h	BA	00D0h
Read lock bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0071h	N/A	N/A
Protect bit program	N/A	N/A	N/A	N/A	FFFFF800h	0067h	PBA	00D0h
Read protect bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0061h	N/A	N/A

WA: Even address to be written
WD: 16-bit write data
BA: Even address in specified block
PBA: Address of the protect bit
x: Any even address in the user ROM area
xx: Upper byte of command code (ignored)
N/A: Not applicable

Notes:
1. This command cannot be executed in EW1 mode.
2. In the M16C/62P, a set of command consists of two words from the first command to the second. The program is performed in 16-bit (1-word) unit.
3. In the R32C/111, a set of command consists of five words from the first command to the fifth. The program is performed in 64-bit (4-word) unit. The higher 29 bits of the address WA should be fixed and the lower three bits of respective command from the second to fifth should be set to 000b, 010b, 100b, and 110b for the addresses 0h, 2h, 4h, and 6h, or 8h, Ah, Ch, and Eh.
4. This command should be executed in RAM.

Table 4.51 Comparison Chart: Flash Memory-associated SFRs

Symbol	Address		Bits	Differences	
	M16C/62P	R32C/111		M16C/62P	R32C/111
FIDR	01B4h	N/A	-	Available only in the M16C/62P	N/A
FMR0	0057h	40000h	7 to 0	Register configuration is completely different	
FMR1	0055h	40009h	7 to 0	Register configuration is completely different	
FMCR	N/A	0006h	-	N/A	Available only in the R32C/111
FEBC0	N/A	001Dh-001Ch	-	N/A	Available only in the R32C/111
FEBC3	N/A	0011Dh-0010Ch	-	N/A	Available only in the R32C/111
FPR0	N/A	40008h	-	N/A	Available only in the R32C/111
FMSR0	N/A	40001h	-	N/A	Available only in the R32C/111
FBPM0	N/A	4000Ah	-	N/A	Available only in the R32C/111
FBPM0	N/A	4000Bh	-	N/A	Available only in the R32C/111

4.19.2 Flash Memory Block Configuration

The R32C/111 has the different block configuration of flash memory from that of the M16C/62P. Refer to the yellow blocks in Figure 4.1 below.

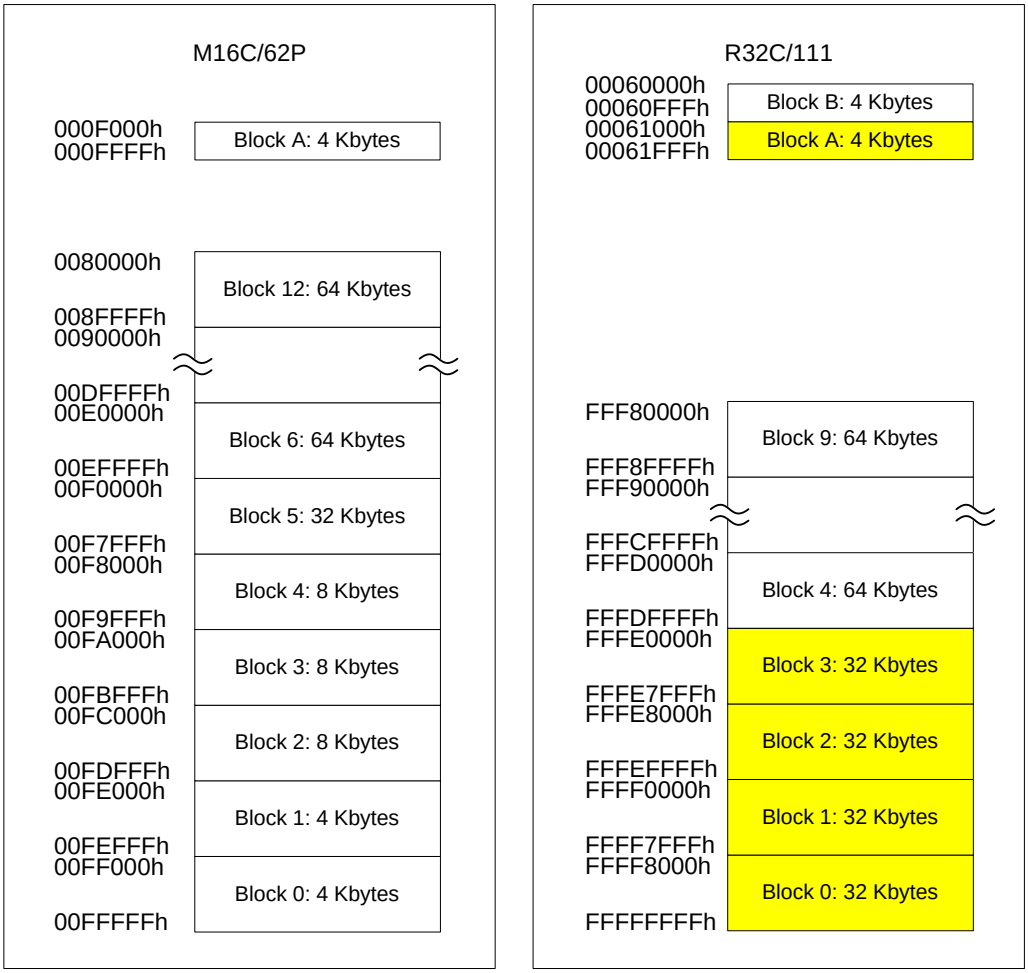

Figure 4.1 Comparison Diagram: Flash Memory Block Configuration

4.19.3 ID Code Protection

Figure 4.2 shows the stored ID code location of respective product.

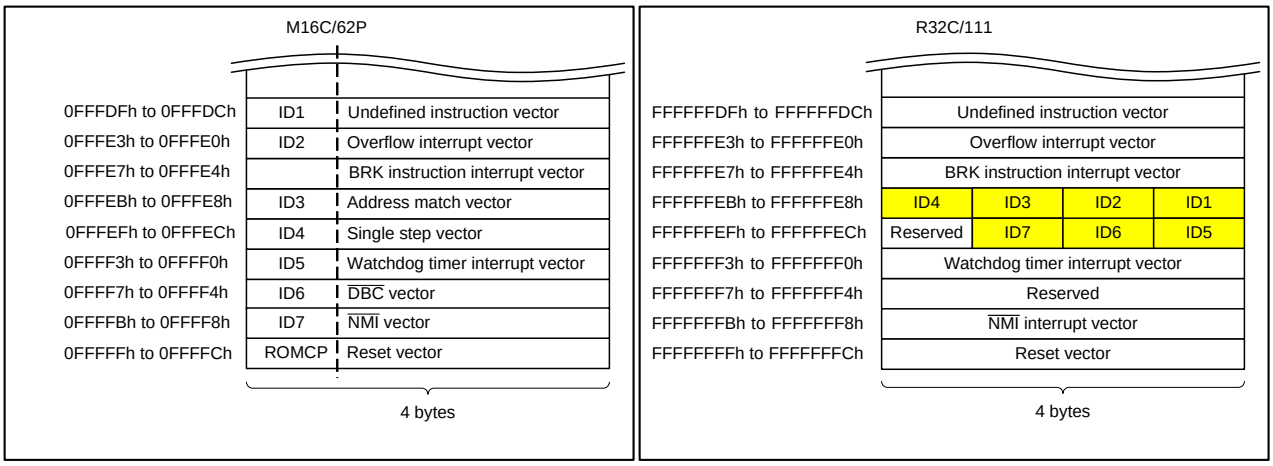

Figure 4.2 Comparison Diagram: Addresses for ID Code Stored

4.19.4 ROM Code Protection

Table 4.52 lists the change on ROM code protection-associated register.

Table 4.52 Comparison Chart: ROM Code Protection

Symbol	Address		Bits	M16C/62P	R32C/111
	M16C/62P	R32C/111			
ROMCP	FFFFFh	N/A	7, 6	Available only in the M16C/62P	N/A

In the R32C/111, each block has two protect bits. Table 4.53 lists the addresses of the protect bits. If any of these protect bits is set to 0 (protected), all areas are protected.
To set the protect bit to 0, execute the protect bit program command. To set the protect bit to 1, erase all the block(s) to which the protect bit was set to 0 (protected). Refer to the hardware manual.

Table 4.53 R32C/111 Protect Bit Addresses

Block	Protect bit 0	Protect bit 1
Block B	00060100h	00060300h
Block A	00061100h	00061300h
Block 9	FFF80100h	FFF80300h
Block 8	FFF90100h	FFF90300h
Block 7	FFFA0100h	FFFA0300h
Block 6	FFFB0100h	FFFB0300h
Block 5	FFFC0100h	FFFC0300h
Block 4	FFFD0100h	FFFD0300h
Block 3	FFFE0100h	FFFE0300h
Block 2	FFFE8100h	FFFE8300h
Block 1	FFFF0100h	FFFF0300h
Block 0	FFFF8100h	FFFF8300h

4.20 Added Peripheral Functions

The following functions are newly added to the R32C/111:

- Fast interrupt
- DMAC II
- X/Y conversion
- Intelligent I/O

4.21 Differences in Development Tools

Table 4.54 lists the differences in development tools.

Table 4.54 Comparison Chart: Development Tools

Tools	For M16C/62P	For R32C/111
C compiler (including simulator debugger)	M3T-NC30WA	C compiler package for R32C Series (R0C56400XSW01R)
Real-time OS	M3T-MR30/4	M3T-MR100/4
Emulator debugger	PC7501	E30A (R0E00030AKCT100)
Emulation probe	M3062PT2-EPB	N/A
Compact emulator	M3062PT3-CPE	N/A
Renesas Stater Kits	R0K33062PS001BE	R0K564112S000BE

5. List of References

- Hardware Manuals
  - M16C/62P Group Hardware Manual (Rev.2.41) issued on Jan.10, 2006.
  - R32C/111 Group Hardware Manual, (Rev.1.10) issued on Oct.21, 2008.

- Technical News/Technical Update

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REVISION HISTORY — Differences between M16C/62P and R32C/111 (100 pin ver.)

Rev.	Date	Description	
		Page	Summary
0.01	Aug 29, 2008	—	Initial release
1.01	Feb. 03, 2010	—	Information is updated to reflect the R32C/111 Hardware Manual Rev.1.10.

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