M16C/29 Group, R32C/111 Group

Differences between M16C/29 and R32C/111 (64-pin Packages)

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1. Introduction

This is a reference document to show the functional changes between the M16C/29 and R32C/111 64-pin packages. For details on functions, refer to the user's manual for each group.

2. Applicable MCUs

This document is applicable to the following products:
M16C/29 and R32C/111 64-pin packages

3. Overview of Comparison

3.1 Overview of Functions

Table 3.1 and Table 3.2 list the functions of each product.

Table 3.1 Comparison of Functions (1/2)

Item	M16C/29	R32C/111
Basic instructions	91	108
Minimum instruction execution time	50 ns (f(BCLK) = 20 MHz)	20 ns (f(CPU) = 50 MHz)
Multiplier	16-bit × 16-bit → 32-bit	32-bit × 32-bit → 64-bit
Multiply-accumulate unit	16-bit × 16-bit + 32-bit → 32-bit	32-bit × 32-bit + 64-bit → 64-bit
FPU	N/A	Single precision (IEEE-754 compliant)
Barrel shifter	N/A	32 bits
Address space	1 Mbyte	4 Gbytes (of which 64 MBytes are usable)
Low voltage detector	Available	Available (optional (1))
Clocks	• Main clock oscillation circuit: 0 to 20 MHz • Sub clock oscillation circuit: 32.768 kHz (Typ), 50 kHz (MAX) • PLL synthesizer: 10 to 20 MHz • On-chip oscillator: 1 MHz (Typ), 2 MHz (Typ), 16 MHz (Typ) • Frequency divide circuit: divided-by-i selectable (i = 1, 2, 4, 8, 16)	• Main clock oscillation circuit: 4 to 16 MHz • Sub clock oscillation circuit: 32.768 kHz (Typ), 62.5 kHz (MAX) • PLL synthesizer: 96 to 128 MHz • On-chip oscillator: 125 kHz (Typ) • Frequency divide circuit: divided-by-2 to divided-by-24 selectable
Interrupts	Interrupt vectors: 72	Interrupt vectors: 261
DMAC	• 2 channels • Request sources: 31	• 4 channels • Request sources: 45
DMAC II	N/A	Available
I/O ports	• Input-only port: N/A • CMOS I/O ports: 55 • N-channel open drain port: N/A • A pull-up resistor is selectable for every 4 input ports	• Input-only port: 1 • CMOS I/O ports: 49 • N-channel open drain ports: 2 • A pull-up resistor is selectable for every 4 input ports
Timers	Timer B: 16-bit timer × 3	Timer B: 16-bit timer × 6 (2)
Serial interface	Asynchronous/synchronous serial interface × 3 channels • Special mode 1, I^2C-bus (UART2) • Special mode 2, (UART2) • Special mode 3, IEBus mode (UART2) • Special mode 4, SIM mode (UART2) Synchronous serial interface × 1 channel	Asynchronous/synchronous serial interface × 6 channels • I^2C-bus (UART0 to UART3, UART5) • Special mode 2 (UART0 to UART3, UART5) • IEBus (optional (1)) (UART0 to UART3, UART5)

Notes:
1. Please contact a Renesas Electronics sales office to use the optional feature.
2. Timer B4 can only be used in timer mode.

Table 3.2 Comparison of Functions (2/2)

Item	M16C/29	R32C/111
A/D Converter	10-bit resolution × 16 channels Operating modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweep mode 0 • Repeat sweep mode 1 • Simultaneous sample sweep mode • Delayed trigger mode 0 • Delayed trigger mode 1	10-bit resolution × 20 channels Operating modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweep mode 0 • Repeat sweep mode 1 • Multi-port single sweep mode • Multi-port repeat sweep mode 0
D/A Converter	N/A	Available
CRC Calculator	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable CRC Snoop	1 polynomial (CRC-CCITT)
X-Y conversion circuit	N/A	Available
Intelligent I/O	• Time measurement: 16 bits × 8 • Waveform generation: 16 bits × 8 • Serial interface: N/A - Two-phase pulse signal processing mode (Group 1)	• Time measurement: 16 bits × 16 • Waveform generation: 16 bits × 19 • Serial interface: - Variable-length synchronous serial I/O - IEBus (optional (1)) - Two-phase pulse signal processing (Group 0 and Group 1)
Multi-master I^2C-bus Interface	1 channel	N/A
CAN	CAN Specification 2.0B × 1 channel	N/A
Flash memory	Erase and program voltage: 2.7 to 5.5 V Erase and program endurance: 1,000 times (program area) and 10,000 times (data area)	Programming and erasure supply voltage: VCC1 = 3.0 to 5.5 V Ease and program endurance: 1,000 times (program area) and 10,000 times (data area) Forcible erase function Standard serial I/O mode disable function
Operating frequency/ Supply voltage	• 20 MHz/VCC = 3.0 to 5.5 V • 10 MHz/VCC = 2.7 to 5.5 V	50 MHz/VCC1 = 3.0 to 5.5 V
Current consumption	• 18 mA (VCC = 5.0 V, f(BCLK) = 20 MHz) 3.0 µA (VCC = 5.0 V, f(XCIN) = 32 kHz in wait mode) • 0.8 µA (VCC = 5.0 V in stop mode)	• 35 mA (VCC1 = 5.0 V, f(CPU) = 50 MHz) • 8 µA (VCC1 = 3.3 to 5.0 V, f(XCIN) = 32.768 kHz in wait mode) • 5 µA (VCC1 = 3.3 to 5.0 V when all clocks and main regulator are stopped)

Note:
1. Please contact a Renesas Electronics sales office to use the optional feature.

3.2 Pin Characteristics

Table 3.3 and Table 3.4 list the characteristics and changes from the M16C/29.

Table 3.3 Comparison of Pin Characteristics (1/2)

M16C/29	R32C/111	Changes
P9_1/TB1IN/AN3_1	VDC1	Deleted: P9_1/TB1IN/AN3_1 Added: VDC1
P9_0/TB0IN/CLKOUT/AN3_0	NSD	Deleted: P9_0/TB0IN/CLKOUT/AN3_0 Added: NSD
P8_5/$\overline{\text{NMI}}$/SD	P8_5/$\overline{\text{NMI}}$	Deleted: SD
P8_4/$\overline{\text{INT2}}$/ZP	P8_4/$\overline{\text{INT2}}$	Deleted: ZP
P8_1/TA4IN/$\overline{\text{U}}$	P8_1/TA4IN/$\overline{\text{U}}$/$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/IIO1_5/UD0B/UD1B	Added: $\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$/IIO1_5/UD0B/UD1B
P8_0/TA4OUT/U	P8_0/TA4OUT/U/RXD5/SCL5/STXD5/UD0A/UD1A	Added: RXD5/SCL5/STXD5/UD0A/UD1A
P7_7/TA3IN	P7_7/TA3IN/CLK5/IIO1_4/UD0B/UD1B	Added: CLK5/IIO1_4/UD0B/UD1B
P7_6/TA3OUT	P7_6/TA3OUT/TXD5/SDA5/SRXD5/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/IIO1_3/UD0A/UD1A	Added: TXD5/SDA5/SRXD5/$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$/IIO1_3/UD0A/UD1A
P7_5/TA2IN/$\overline{\text{W}}$	P7_5/TA2IN/$\overline{\text{W}}$/RXD8/IIO1_2	Added: RXD8/IIO1_2
P7_4/TA2OUT/W	P7_4/TA2OUT/W/CLK8/IIO1_1	Added: CLK8/IIO1_1
P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1	P7_3/TA1IN/$\overline{\text{V}}$/$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$/TXD8/IIO1_0	Deleted: TXD1 Added: $\overline{\text{SS2}}$/TXD8/IIO1_0
P7_2/TA1OUT/V/CLK2/RXD1	P7_2/TA1OUT/V/CLK2	Deleted: RXD1
P7_1/TA0IN/RXD2/SCL2/CLK1	P7_1/TA0IN/RXD2/SCL2/TB5IN/STXD2/IIO1_7/OUTC2_2/ISRXD2/IEIN	Deleted: CLK1 Added: TB5IN/STXD2/IIO1_7/OUTC2_2/ISRXD2/IEIN
P7_0/TA0OUT/TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P7_0/TA0OUT/TXD2/SDA2/SRXD2/IIO1_6/OUTC2_0/ISTXD2/IEOUT	Deleted: $\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1 Added: SRXD2/IIO1_6/OUTC2_0/ISTXD2/IEOUT
P6_7/TXD1	P6_7/TXD1/SDA1/SRXD1	Added: SDA1/SRXD1
P6_6/RXD1	P6_6/RXD1/SCL1/STXD1	Added: SCL1/STXD1
P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{CTS0}}$/CLKS1	P6_4/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$/OUTC2_1/ISCLK2	Deleted: $\overline{\text{CTS0}}$/CLKS1 Added: $\overline{\text{SS1}}$/OUTC2_1/ISCLK2
P6_3/TXD0	P6_3/TXD0/SDA0/SRXD0	Added: SDA0/SRXD0
P6_2/RXD0	P6_2/RXD0/TB2IN/SCL0/STXD0	Added: TB2IN/SCL0/STXD0
P6_1/CLK0	P6_1/CLK0/TB1IN	Added: TB1IN
P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	P6_0/$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/TB0IN/$\overline{\text{SS0}}$	Added: TB0IN/$\overline{\text{SS0}}$

Table 3.4 Comparison of Pin Characteristics (2/2)

M16C/29	R32C/111	Changes
P3_3	P3_3/TA1IN/$\overline{V}$/$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$	Added: TA1IN/$\overline{V}$/$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$
P3_2/SOUT3	P3_2/TA1OUT/V/TXD3/SDA3/SRXD3	Deleted: SOUT3 Added: TA1OUT/V/TXD3/SDA3/SRXD3
P3_1/SIN3	P3_1/TA3OUT/RXD3/SCL3/STXD3/UD0B/UD1B	Deleted: SIN3 Added: TA3OUT/RXD3/SCL3/STXD3/UD0B/UD1B
P3_0/CLK3	P3_0/CLK3/TA0OUT/UD0A/UD1A	Added: TA0OUT/UD0A/UD1A
P2_7/OUTC1_7/INPC1_7 (1)	P2_7/IIO0_7/AN2_7 (1)	Deleted: OUTC1_7/INPC1_7 Added: IIO0_7/AN2_7
P2_6/OUTC1_6/INPC1_6 (1)	P2_6/IIO0_6/AN2_6 (1)	Deleted: OUTC1_6/INPC1_6 Added: IIO0_6/AN2_6
P2_5/OUTC1_5/INPC1_5 (1)	P2_5/IIO0_5/AN2_5 (1)	Deleted: OUTC1_5/INPC1_5 Added: IIO0_5/AN2_5
P2_4/OUTC1_4/INPC1_4 (1)	P2_4/IIO0_4/AN2_4 (1)	Deleted: OUTC1_4/INPC1_4 Added: IIO0_4/AN2_4
P2_3/OUTC1_3/INPC1_3 (1)	P2_3/IIO0_3/AN2_3 (1)	Deleted: OUTC1_3/INPC1_3 Added: IIO0_3/AN2_3
P2_2/OUTC1_2/INPC1_2 (1)	P2_2/IIO0_2/AN2_2 (1)	Deleted: OUTC1_2/INPC1_2 Added: IIO0_2/AN2_2
P2_1/OUTC1_1/INPC1_1/SCLMM (1)	P2_1/IIO0_1/AN2_1 (1)	Deleted: OUTC1_1/INPC1_1/SCLMM Added: IIO0_1/AN2_1
P2_0/OUTC1_0/INPC1_0/SDAMM (1)	P2_0/IIO0_0/AN2_0 (1)	Deleted: OUTC1_0/INPC1_0/SDAMM Added: IIO0_0/AN2_0
P1_7/$\overline{INT5}$/INPC1_7/IDU	P1_7/$\overline{INT5}$/IIO0_7/IIO1_7	Deleted: INPC1_7/IDU Added: IIO0_7/IIO1_7
P1_6/$\overline{INT4}$/IDW	P1_6/$\overline{INT4}$/IIO0_6/IIO1_6	Deleted: IDW Added: IIO0_6/IIO1_6
P1_5/$\overline{INT3}$/$\overline{ADTRG}$/IDV	P1_5/$\overline{INT3}$/$\overline{ADTRG}$/IIO0_5/IIO1_5	Deleted: IDV Added: IIO0_5/IIO1_5
P9_3/CTX/AN2_4	P9_3/TB3IN/DA0	Deleted: CTX/AN2_4 Added: TB3IN/DA0
P9_2/CRX/AN3_2/TB2IN	VDC0	Deleted: P9_2/CRX/AN3_2/TB2IN Added: VDC0

Note:
1. OUTC1_i and INPC1_i in the M16C/29 are merged into IIO0_i in the R32C/111 (i = 1 to 7).

4. Detailed Comparison

4.1 CPU Functions

Table 4.1 to Table 4.4 list the changes from the R32C/111 on instructions, bit length of internal registers, and flags.

Table 4.1 Instructions Changed in R32C/111

Item	R32C/111
Added instructions	ADDF, ADSF, BITINDEX, BRK2, CLIP, CMPF, CNVIF, DIVF, DIV (1), DIVU (1), DIVX (1), EXITI, EXTZ, FREIT, INDEX Type, MAX, MIN, MUL (1), MULU (1), MULF, MULX, ROUND, SCCnd, SCMPU, SIN, SMOVU, SOUT, STOP, SUBF, SUNTIL, SWHILE
Mnemonic changed instructions	EDIV (from DIV), EDIVU (from DIVU), EDIVX (from DIVX), EMUL (from MUL), and EMULU (from MULU)
Deleted instructions	ADJNZ, BAND, BNAND, BNOR, BNTST, BNXOR, BOR, BXOR, JMPS, JSRS, LDE, LDINTB, STE, and SBJNZ

Note:
1. These instructions are newly added with existing mnemonics (refer to Table 4.2).

Table 4.2 Comparison of Mnemonic Changed Instructions and Their Bit Lengths (Reference)

Mnemonic	M16C/29	R32C/111
DIV, DIVU, DIVX	16 bits ÷ 8 bits = 8 bits (for byte) 32 bits ÷ 16 bits = 16 bits (for word)	8 bits ÷ 8 bits = 8 bits (for byte) 16 bits ÷ 16 bits = 16 bits (for word)
MUL, MULU	8 bits × 8 bits = 16 bits (for byte) 16 bits ×16 bits = 32 bits (for word)	8 bits × 8 bits = 8 bits (for byte) 16 bits × 16 bits = 16 bits (for word)
Bit operation	Bit operation of the register can be set from bits 0 to 15. Example: BSET bit, R0 (bit 0 to15)	Bit operation of the register can be set from bits 0 to 7. Examples: BSET bit, R0L (bits from 0 to 7) BSET bit, R0H (bits from 0 to 7)

Table 4.3 Comparison of Bit Length of Internal Registers

Internal Register	M16C/29		R32C/111	
	Register	Bit length	Register	Bit length
Flag register	FLG	16 bits	FLG	32 bits
Data registers (1)	R0, R1, R2, R3	16 bits Registers R0 and R1 can be divided into upper and lower 8-bit registers, respectively. Registers R2 and R0, and R3 and R1 can be merged into one 32-bit register.	R0, R1, R2, R3	16 bits Registers R0, R1, R2, and R3 can be divided into upper and lower 8-bit registers, respectively. Registers R2 and R0, and R3 and R1 can be merged into one 32-bit register.
			R4, R5, R6, R7	16 bits Registers R7 and R5, and R6 and R4 can be merged into one 32-bit register.
Address registers (1)	A0, A1	16 bits	A0, A1, A2, A3	32 bits
Static base register	SB		SB	32 bits (1)
Frame base register (1)	FB		FB	32 bits
User stack pointer	USP		USP	
Interrupt stack pointer	ISP		ISP	
Program counter	PC	19 bits	PC	
Interrupt vector table base register	INTB		INTB	
Fast interrupt-associated registers (there is no fast interrupt function in M16C/29)	N/A	N/A	SVF	
			SVP	
			VCT	
DMAC-associated registers (in M16C/29, DMAC-associated registers are allocated to the SFR areas)			DMD0, DMD1, DMD2, DMD3	
			DCT0, DCT1, DCT2, DCT3	24 bits
			DCR0, DCR1, DCR2, DCR3	
			DSA0, DSA1, DSA2, DSA3	32 bits
			DDA0, DDA1, DDA2, DDA3	
			DSR0, DSR1, DSR2, DSR3	
			DDR0, DDR1, DDR2, DDR3	

Note:
1. There are two banks of these registers.

Table 4.4 Comparison of Flag Registers

Item	M16C/29		R32C/111	
	Flag	Bit position	Flag	Bit position
Floating-point underflow flag	N/A	N/A	FU	b8
Floating-point overflow flag	N/A	N/A	FO	b9
Fixed-point designation flag	N/A	N/A	DP	b16
Floating-point round mode	N/A	N/A	RND	b19 and b18

4.2 Resets

Hardware reset 1, low voltage detection (hardware reset 2) (only in M16C/29), software reset, and watchdog timer reset are used to reset the MCU. However, the oscillation stop detection reset is available only in M16C/29.

Some SFRs remain uninitialized even after a reset operation.

Table 4.5 to Table 4.7 list the changes from the M16C/29 on reset operations.

Table 4.5 Comparison of Non-reset Registers

Item	Register	State After Reset	
		M16C/29	R32C/111
Software reset	PM0	N/A	Not initialized
	VCR1 and VCR2	Not initialized	N/A
Watchdog timer reset	PM0	N/A	Not initialized
	VCR1 and VCR2	Not initialized	N/A
Oscillation stop detection reset	CM2	Bits CM27, CM21, and CM20 are not initialized	N/A
	VCR1 and VCR2	Not initialized	N/A

Table 4.6 Comparison of Clock Sources and Division Ratios After a Reset

Item	M16C/29	R32C/111
Clock source	On-chip oscillator clock f2(ROC)	PLL self oscillation mode
Base clock	N/A	Divided-by-6
CPU clock	Divided-by-16	Divided-by-12
Peripheral bus clock	Divided-by-16	Divided-by-12

Table 4.7 Comparison of Clock Sources Before a Software Reset

Item	M16C/29	R32C/111
Clock source	No restrictions	PLL clock

4.3 Voltage Regulator

The supply voltage for internal logic in R32C/111 is generated by reducing the input voltage from the VCC1 pin with the voltage regulators. To stabilize the internal voltage, connect a decoupling capacitor between pins VDC1 and VDC0. M16C/29 does not require a decoupling capacitor. Table 4.8 lists the change in the voltage regulator control register.

Table 4.8 Comparison of Voltage Regulator Control Register

Symbol	Address		Bit	M16C/29	R32C/111
	M16C/29	R32C/111			
VRCR	-	40060h	-	-	Available only in the R32C/111

4.4 Low Voltage Detection

Table 4.9 lists the changes in SFRs associated with low voltage detection.

Table 4.9 Comparison of Low Voltage Detection-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
VCR1	0019h	-	-	Available only in the M16C/29	-
VCR2	001Ah	-	-	Available only in the M16C/29	-
D4INT	001Fh	-	-	Available only in the M16C/29	-
LVDC	-	40062h	-	-	Available only in the R32C/111
DVCR	-	40064h	-	-	Available only in the R32C/111

4.5 Processor Modes

Table 4.10 lists the changes in SFRs associated with processor modes.

Table 4.10 Comparison of Processor Mode-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
PM0	0004h	40044h	-	Address changed	
			1, 0	Reserved bit	Processor Mode Bit (1)
			2	Reserved bit	R/W Mode Select Bit (1)
			7	Reserved bit	BCLK Output Function Select Bit (1)
PM1	0005h	-	-	Available only in the M16C/29	-

Note:
1. The R32C/111 64-pin package is available only in single-chip mode. Do not change the setting.

4.6 Clocks

Table 4.11 to Table 4.13 list the changes in clock characteristics, settings, and associated SFRs, respectively.

Table 4.11 Comparison of Clock Characteristics

Item	M16C/29	R32C/111
CPU clock after reset	On-chip oscillator clock f2(ROC) divided-by-16	PLL frequency synthesizer (self-oscillation mode) divided-by-12
XIN-XOUT drive power	Switchable (2 ways)	Switchable (3 ways)
Main clock division	Selectable from no division, divided-by-2, -4, -8, or -16	Selectable from no division, divided-by-2, -3, or -4
Base clock division	N/A	Selectable from divided-by-2, -3, -4, or -6
CPU clock division	N/A	Selectable from no division, divided-by-2, -3, or -4
Peripheral bus clock division	N/A	Selectable from divided-by-2, -3, or -4
PLL multiplication rate	Selectable from multiply-by-2 or -4	Selectable from values specified in the user's manual
Peripheral function clock	f1, f2, f8, f32, fAD, f1SIO, f2SIO, f8SIO, f32SIO, and fC32	f1, f8, f2n, f32, fAD, and fC32
Stop mode	Each group has its own procedure to enter stop mode	
Transition from high speed mode to stop mode	Enabled	N/A
Transition from PLL self-oscillation mode to wait mode	N/A	Enabled
Exit from wait mode by serial interface interrupt	Enabled in every UART channel	Enabled in all UART channels except UART8
CPU clock when exiting stop mode	The CPU clock to be used is determined by the CPU clock that was being used when the MCU entered stop mode: Sub clock: sub clock Main clock: main clock divided-by-8 On-chip oscillator clock: on-chip oscillator clock divided-by-8	Division ratio of the CPU clock when the STOP instruction is executed

Table 4.12 Comparison of Clock-associated Settings

Item	M16C/29	R32C/111
XIN-XOUT drive power	CM15 bit in the CM1 register	Bits CM16 and CM15 in the CM1 register
Main clock division	CM07 bit in the CM0 register and bits CM17 and CM16 in the CM1 register	Bits CCD1 and CCD0 in the CCR register
Base clock division	N/A	Bits BCD1 and BCD0 in the CCR register
Peripheral bus clock division	N/A	Bits PCD1 and PCD0 in the CCR register
PLL multiplication rate	Bits PLC02 to PLC00 in the PLC0 register	Setting value of registers PLC1 and PLC0 specified in the user's manual

Table 4.13 Comparison of Clock-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
CCR	-	0004h	-	-	Available only in the R32C/111
PBC	-	001Fh to 001Eh	-	-	Available only in the R32C/111
CM0	0006h	40046h	-	Address changed	
			6	Main clock division select bit 0	Watchdog Timer Function Select Bit
			7	System clock select bit	Reserved
CM1	0007h	40047h	-	Address changed	
			0	All clock stop control bit	PLL Clock Oscillator Stop Bit
			1	System clock select bit 1	Reserved
			5	XIN-XOUT drive capacity select bit	XIN-XOUT Drive Power Select Bit
			6	Main clock division select bit 1	
			7		Reserved
CM2	000Ch	4004Dh	-	Address changed	
			0	Oscillation stop, re-oscillation detection bit	Oscillator Stop Detection Enable Bit
			1	System clock select bit 2	Reserved
			2	Oscillation stop, re-oscillation detection flag	Oscillation Stop Detection Flag
			3	XIN monitor flag	Main Clock Monitor Flag
			7	Operation select bit (when an oscillation stop, re-oscillation is detected)	Reserved
PLC0	001Ch	40020h	-	Address changed	
			2 to 0	PLL multiplying factor select bit (PLC02 to PLC00)	Main Counter Divide Ratio Setting Bit (MCV4 to MCV0)
			4, 3	Reserved	
			6, 5	Reserved	Swallow Counter Divide Ratio Setting Bit (SVC2 to SVC0)
			7	Operation enable bit (PLC07)	
PLC1	-	40021h	-	-	Available only in the R32C/111
PM2	001Eh	40053h	-	Address changed	
			0	Specifying wait when accessing SFR	Reserved
			2	WDT count source protective bit	Reserved
			4	P8_5/$\overline{\text{NMI}}$ configuration bit	Reserved
			6	Reserved	f2n Clock Source Select Bit
ROCR	025Ch	-	-	Available only in the M16C/29	-
PCLKR	025Eh	-	-	Available only in the M16C/29	-
CCLKR	025Fh	-	-	Available only in the M16C/29	-
CM3	-	4005Ah	-	-	Available only in the R32C/111
PM3	-	40048h	-	-	Available only in the R32C/111
CPSRF	-	0341h	-	-	Available only in the R32C/111
TCSPR	-	035Fh	-	-	Available only in the R32C/111

4.7 Protection

Table 4.14 lists the changes in SFRs associated with the protection.

Table 4.14 Comparison of Protection-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
PRCR	000Ah	4004Ah	-	Address changed	
			0	Protect bit 0 Write enable to registers CM0, CM1, CM2, ROCR, PLC0, PCLKR, and CCLKR	Protect Bit 0: Write enable to registers CM0, CM1, CM2, and PM3
			1	Protect bit 1 Write enable to registers PM0, PM1, PM2, TB2SC, INVC0, and INVC1	Protect Bit 1 Write enable to registers PM0, PM2, CSOP0, CSOP1, INVC0, INVC1, and IOBC
			2	Protect bit 2 Write enable to registers PD9, PACR, S4C, and NDDR	Protect Bit 2 Write enable to registers PD9, P9_iS (i = 3 to 7), PLC0, and PLC1
			3	Protect bit 3: Write enable to registers VCR2 and D4INT	-
PRCR2	-	4405Fh	7	-	CM3 Protect Bit: Write enable to the CM3 register
PRCR3	-	4004Ch	1	-	Protect Bit 31: Write enable to registers VRCR, LVDC, and DVCR
PRR	-	0007h	7 to 0	-	Write enable to registers CCR, FMCR, PBC, FEBC0, FEBC3, EBC0, EBC1, EBC2, EBC3, CB01, CB12, and CB23: AAh: write enabled other than AAh: write disabled

4.8 Interrupts

Table 4.15 to Table 4.18 list the changes in interrupts and associated SFRs.
The relocatable vector tables and interrupt priority level select circuitry are different.

Table 4.15 Comparison of Interrupts

Item	M16C/29	R32C/111
Address match interrupt	Settable up to 2 addresses	N/A

Table 4.16 Comparison of Interrupt-associated SFRs (1/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
TB5IC	-	0061h	-	-	Available only in the R32C/111
S5TIC	-	0062h	-	-	Available only in the R32C/111
S2RIC	0050h	0063h	-	Address changed	
S3RIC	-	0065h	-	-	Available only in the R32C/111
BCN5IC/ BCN6IC	-	0066h	-	-	Available only in the R32C/111
DM0IC	004Bh	0068h	-	Address changed	
BCN0IC/ BCN3IC	-	0069h	-	-	Available only in the R32C/111
DM2IC	-	006Ah	-	-	Available only in the R32C/111
AD0IC	-	006Bh	-	-	Available only in the R32C/111
TA0IC	0055h	006Ch		Address changed	
IIO0IC	-	006Dh	-		Available only in the R32C/111
TA2IC	0057h	006Eh		Address changed	
IIO2IC	-	006Fh	-	-	Available only in the R32C/111
TA4IC	0059h	0070h	-	Address changed	
IIO4IC	-	0071h	-	-	Available only in the R32C/111
S0RIC	0052h	0072h	-	Address changed	
IIO6IC	-	0073h	-	-	Available only in the R32C/111
S1RIC	0054h	0074h	-	Address changed	
IIO8IC	-	0075h	-	-	Available only in the R32C/111
TB1IC	005Bh	0076h	-	Address changed	
IIO10IC	-	0077h	-	-	Available only in the R32C/111
TB3IC	-	0078h	-	-	Available only in the R32C/111
INT5IC	-	007Ah	-	-	Available only in the R32C/111
INT3IC	0044h	007Ch	-	Address changed	
			5	Reserved	Level/Edge Sensitive Select Bit
INT1IC	005Eh	007Eh	-	Address changed	
			5	Reserved	Level/Edge Sensitive Select Bit
S2TIC	004Fh	0081h	-	Address changed	
S5RIC	-	0082h	-	-	Available only in the R32C/111
S3TIC	-	0083h	-	-	Available only in the R32C/111
BCN2IC	-	0087h	-	-	Available only in the R32C/111

Table 4.17 Comparison of Interrupt-associated SFRs (2/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
DM1IC	004Ch	0088h	-	Address changed	
BCN1IC/ BCN4IC	-	0089h	-	-	Available only in the R32C/111
DM3IC	-	008Ah	-	-	Available only in the R32C/111
KUPIC	004Eh	008Bh	-	Address changed	
TA1IC	0056h	008Ch	-	Address changed	
IIO1IC	-	008Dh	-	-	Available only in the R32C/111
TA3IC	0058h	008Eh	-	Address changed	
IIO3IC	-	008Fh	-	-	Available only in the R32C/111
S0TIC	0051h	0090h	-	Address changed	
IIO5IC	-	0091h	-	-	Available only in the R32C/111
S1TIC	0053h	0092h	-	Address changed	
IIO7IC	-	0093h	-	-	Available only in the R32C/111
TB0IC	005Ah	0094h	-	Address changed	
IIO9IC	-	0095h	-	-	Available only in the R32C/111
TB2IC	005Ch	0096h	-	Address changed	
IIO11IC	-	0097h	-	-	Available only in the R32C/111
TB4IC	-	0098h	-	-	Available only in the R32C/111
INT4IC	-	009Ah	-	-	Available only in the R32C/111
INT2IC	005Fh	009Ch	-	Address changed	
			5	Reserved	Level/Edge Sensitive Select Bit
INT0IC	005Dh	009Eh	-	Address changed	
			5	Reserved	Level/Edge Sensitive Select Bit
IIO0IR	-	00A0h	-	-	Available only in the R32C/111
IIO1IR	-	00A1h	-	-	Available only in the R32C/111
IIO2IR	-	00A2h	-	-	Available only in the R32C/111
IIO3IR	-	00A3h	-	-	Available only in the R32C/111
IIO4IR	-	00A4h	-	-	Available only in the R32C/111
IIO5IR	-	00A5h	-	-	Available only in the R32C/111
IIO6IR	-	00A6h	-	-	Available only in the R32C/111
IIO7IR	-	00A7h	-	-	Available only in the R32C/111
IIO8IR	-	00A8h	-	-	Available only in the R32C/111
IIO9IR	-	00A9h	-	-	Available only in the R32C/111
IIO10IR	-	00AAh	-	-	Available only in the R32C/111
IIO11IR	-	00ABh	-	-	Available only in the R32C/111
IIO0IE	-	00B0h	-	-	Available only in the R32C/111
IIO1IE	-	00B1h	-	-	Available only in the R32C/111
IIO2IE	-	00B2h	-	-	Available only in the R32C/111
IIO3IE	-	00B3h	-	-	Available only in the R32C/111

Table 4.18 Comparison of Interrupt-associated SFRs (3/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
IIO4IE	-	00B4h	-	-	Available only in the R32C/111
IIO5IE	-	00B5h	-	-	Available only in the R32C/111
IIO6IE	-	00B6h	-	-	Available only in the R32C/111
IIO7IE	-	00B7h	-	-	Available only in the R32C/111
IIO8IE	-	00B8h	-	-	Available only in the R32C/111
IIO9IE	-	00B9h	-	-	Available only in the R32C/111
IIO10IE	-	00BAh	-	-	Available only in the R32C/111
IIO11IE	-	00BBh	-	-	Available only in the R32C/111
S8TIC	-	00DFh	-	-	Available only in the R32C/111
S8RIC	-	00FFh	-	-	Available only in the R32C/111
RIPL2	-	4407Dh	-	-	Available only in the R32C/111
RIPL1	-	4407Fh	-	-	Available only in the R32C/111
IFSR1	-	4406Dh	-	-	Available only in the R32C/111
IFSR0	-	4406Fh	-	-	Available only in the R32C/111
AIER	0009h	-	-	Available only in the M16C/29	-
RMAD0	0012h to 0010h	-	-	Available only in the M16C/29	-
RMAD1	0016h to 0014h	-	-	Available only in the M16C/29	-
D4INT	001Fh	-	-	Available only in the M16C/29	-
C01WKIC	0041h	-	-	Available only in the M16C/29	-
C0RECIC	0042h	-	-	Available only in the M16C/29	-
C0TRMIC	0043h	-	-	Available only in the M16C/29	-
ICOC0IC	0045h	-	-	Available only in the M16C/29	-
ICOC1IC/ IICIC	0046h	-	-	Available only in the M16C/29	-
BTIC/ SCLDAIC	0047h	-	-	Available only in the M16C/29	-
S4IC/ INT5IC	0048h	-	-	Available only in the M16C/29	-
S3IC/ INT4IC	0049h	-	-	Available only in the M16C/29	-
BCNIC	004Ah	-	-	Available only in the M16C/29	-
C01ERRIC	004Dh	-	-	Available only in the M16C/29	-
ADIC	004Eh	-	-	Available only in the M16C/29	-
ICTB2	034Dh	-	-	Available only in the M16C/29	-
IFSR2A	035Eh	-	-	Available only in the M16C/29	-
IFSR	035Fh	-	-	Available only in the M16C/29	-
C0ICR	0217h to 0216h	-	-	Available only in the M16C/29	-

4.9 Watchdog Timer

Table 4.19 and Table 4.20 list the changes in watchdog timer and associated SFRs.

Table 4.19 Comparison of Watchdog Timer

Item	M16C/29	R32C/111
Clock source for watchdog timer	• CPU clock divided by the values in bits CM06, CM17, and CM16 (PLL clock, main clock, on-chip oscillator clock) • Sub clock • On-chip oscillator clock	• Peripheral bus clock (PLL clock, sub clock, on-chip oscillator clock, or main clock divided by the values in the CCR register
Watchdog timer prescaler division ratio	Divided-by-2 (when sub clock is selected), -16, or -128	Divided-by-16 or -128
Count source protect mode	Available	N/A
Watchdog timer reset function	Depends on the PM12 bit setting	Depends on the CM06 bit setting

Table 4.20 Comparison of Watchdog Timer-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
CM0	0006h	40046h	-	Address changed	
			6	Main clock division select bit 0	Watchdog timer function select bit
			7	CPU clock select bit 0	Reserved
PM1	0005h	-	-	Available only in the M16C/29	-
WDC	000Fh	4404Fh	-	Address changed	
WDTS	000Eh	4404Eh	-	Address changed	

4.10 DMAC

Table 4.21 to Table 4.24 list the changes in DMAC characteristics, settings, and associated SFRs, respectively.

Table 4.21 Comparison of DMAC

Item	M16C/29	R32C/111
Number of channels	2	4
Transfer memory space	• From any address in a 1-Mbyte space to a fixed address • From a fixed address to any address in a 1-Mbyte space • From a fixed address to a fixed address	From a given address in a 64-Mbyte space (00000000h to 01FFFFFFh and FE000000h to FFFFFFFFh) to another given address in the same space
Maximum transfer bytes	128 Kbytes (when 16-bit data is transferred) 64 Kbytes (when 8-bit data is transferred)	64 Mbytes (when 32-bit data is transferred) 32 Mbytes (when 16-bit data is transferred) 16 Mbytes (when 8-bit data is transferred)
Transfer unit	8 bits or 16 bits	8 bits, 16 bits, or 32 bits
Destination address	Fixed address: one specified address Forward address: address which is incremented by a transfer unit on each successive access. (The source address and destination address cannot both be icremented.)	Incrementing address or non Incrementing address
Number of transfers	Value set to the DMAi transfer counter + 1 (i = 0, 1)	Value set to the DCTj register (j = 0 to 3)
DMA interrupt request generation timing	When the DMAi transfer counter underflows	When the DCTj register changes from 00000001h to 00000000h

Table 4.22 Comparison of DMAC Settings

Item	M16C/29	R32C/111
DMA request sources	Selected by setting bits DSEL3 to DSEL0 in the DMiSL register (i = 0, 1)	Selected by setting bits DSEL4 to DSEL0 in the DMiSL register or bits DSEL24 to DSEL20 in the DMiSL2 register (i = 0 to 3)
Source address	Registers SAR0 and SAR1	DSAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DSRi register)
Destination address		DDAi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DDRi register)
Transfer cycles	Transfer cycles - 1 is set to the TCRi register (i = 0, 1)	Number of transfer cycles is set to the DCTi register (i = 0 to 3) (reloaded value in repeat transfer mode is set to the DCRi register)

Table 4.23 Comparison of DMAC-associated SFRs (1/2)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
DM0SL	03B8h	44078h	-	Address changed	
			4	-	DMA request source select bit
			5	-	Software DMA request bit
			6	DMA request cause expansion select bit	-
			7	Software DMA request bit	-
DM1SL	03BAh	44079h	-	Address changed	
			4	-	DMA request source select bit
			5	-	Software DMA request bit
			6	DMA request cause expansion select bit	-
			7	Software DMA request bit	-
DM2SL	-	4407Ah	-	-	Available only in the R32C/111
DM3SL	-	4407Bh	-	-	Available only in the R32C/111
DM0SL2	-	44070h	-	-	Available only in the R32C/111
DM1SL2	-	44071h	-	-	Available only in the R32C/111
DM2SL2	-	44072h	-	-	Available only in the R32C/111
DM3SL2	-	44073h	-	-	Available only in the R32C/111
DMD0 to DMD3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DCT0 to DCT3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DCR0 to DCR3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DSA0 to DSA3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DSR0 to DSR3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DDA0 to DDA3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DDR0 to DDR3	-	CPU internal register (1)	-	-	Available only in the R32C/111
DM0CON	002Ch	-	-	Available only in the M16C/29	-
DM1CON	003Ch	-	-	Available only in the M16C/29	-

Note:
1. Use the LDC instruction to write to this register.

Table 4.24 Comparison of DMAC-associated SFRs (2/2)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
SAR0	0022h to 0020h	-	-	Available only in the M16C/29	-
SAR1	0032h to 0030h	-		Available only in the M16C/29	-
DAR0	0026h to 0024h	-		Available only in the M16C/29	-
DAR1	0036h to 0034h	-		Available only in the M16C/29	-
TCR0	0029h to 0028h	-		Available only in the M16C/29	-
TCR1	0039h to 0038h	-		Available only in the M16C/29	-

4.11 Timers

Table 4.25 and Table 4.27 list the changes in timers and associated SFRs.

Table 4.25 Comparison of Timers

Item	M16C/29	R32C/111
Timer B	16 bit timer × 3	16 bit timer × 6 (1)
Count sources	f1 or f2 f8 f32 fC32	f1 f8 f2n fC32
Timer B modes	• Timer mode • Event counter mode • Pulse period and pulse width measurement mode • A/D trigger mode	• Timer mode • Event counter mode • Pulse Period/Pulse-width Measure Mode

Note:
1. Timer B4 is usable only in timer mode.

Table 4.26 Comparison of Timer-associated SFRs (1/2)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
TBSR	-	0300h	-	-	Available only in the R32C/111
TB3	-	0311h to 0310h	-	-	Available only in the R32C/111
TB4	-	0313h to 0312h	-	-	Available only in the R32C/111
TB5	-	0315h to 0314h	-	-	Available only in the R32C/111
TB3MR	-	031Bh	-	-	Available only in the R32C/111
TB4MR	-	031Ch	-	-	Available only in the R32C/111
TB5MR	-	031Dh	-	-	Available only in the R32C/111
TABSR	0380h	0340h	-	Address changed	
CPSRF	0381h	0341h	-	Address changed	
ONSF	0382h	0342h	-	Address changed	
TRGR	0383h	0343h	-	Address changed	
UDF	0384h	0344h	-	Address changed	
TA0	0387h to 0386h	0347h to 0346h	-	Address changed	
TA1	0389h to 0388h	0349h to 0348h	-	Address changed	
TA2	038Bh to 038Ah	034Bh to 034Ah	-	Address changed	
TA3	038Dh to 038Ch	034Dh to 034Ch	-	Address changed	
TA4	038Fh to 038Eh	034Fh to 034Eh	-	Address changed	
TB0	0391h to 0390h	0351h to 0350h	-	Address changed	
TB1	0393h to 0392h	0353h to 0352h	-	Address changed	
TB2	0395h to 0394h	0355h to 0354h	-	Address changed	
TA0MR	0396h	0356h	-	Address changed	
			2	Pulse output function select bit	Reserved (1)
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TA1MR	0397h	0357h	-	Address changed	
			2	Pulse output function select bit	Reserved (1)
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		

Table 4.27 Comparison of Timer-associated SFRs (2/2)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
TA2MR	0398h	0358h	-	Address changed	
			2	Pulse output function select bit	Reserved (1)
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TA3MR	0399h	0359h	-	Address changed	
			2	Pulse output function select bit	Reserved (1)
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TA4MR	039Ah	035Ah	-	Address changed	
			2	Pulse output function select bit	Reserved (1)
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TB0MR	039Bh	035Bh	-	Address changed	
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TB1MR	039Ch	035Ch	-	Address changed	
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TB2MR	039Dh	035Dh	-	Address changed	
			6	Count source select bit (f1 or f2, or f32)	Count source select bit (f1 or f2n)
			7		
TCSPR	-	035Fh	-	-	Available only in the R32C/111

Note:
1. When using pulse output, select the TAiOUT output function with the port function select register (i = 0 to 4).

4.12 Three-phase Motor Control Timers

Table 4.28 and Table 4.29 list the changes in three-phase motor control timers and associated SFRs.

Table 4.28 Comparison of Three-phase Motor Control

Item	M16C/29	R32C/111
Forced cutoff input	Input “L“ to the $\overline{SD}$ pin	Input “L“ to the $\overline{NMI}$ pin
Switchable output function	N/A	Switchable pins: pins V and $\overline{V}$ of port P7, or pins V and V# port P3
Carrier wave cycle	Count source: f1, f2, f8, f32, or fC32	Count source: f1, f8, f2n, or fC32
Three-phase PWM output width		
Dead time	Count source: f1, f2, f1 divided-by-2, or f2 divided-by-2	Count source: f1 or f1 divided-by-2

Table 4.29 Comparison of Three-phase Motor Control

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
TA11	0343h to 0342h	0303h to 0302h	-	Address changed	
TA21	0345h to 0344h	0305h to 0304h	-	Address changed	
TA41	0347h to 0346h	0307h to 0306h	-	Address changed	
INVC0	0348h	0308h	-	Address changed	
			0	Effective interrupt output polarity select bit	ICTB2 Count Condition Select Bit
			1	Effective interrupt output specification bit	
			4	Positive and negative phases concurrent output disable bit	Simultaneous Conduction Prevention Bit
			5	Positive and negative phases concurrent output detect flag	Simultaneous Conduction Detection Flag
INVC1	0349h	0309h	-	Address changed	
IDB0	034Ah	030Ah	-	Address changed	
IDB1	034Bh	030Bh	-	Address changed	
DTT	034Ch	030Ch	-	Address changed	
ICTB2	034Dh	030Dh	-	Address changed	
TB2SC	039Eh	035Eh	-	Address changed	
			1	Three-phase output port SD control bit 1	-
			2	Timer B0 operation mode select bit	-
			3	Timer B1 operation mode select bit	-
			4	Trigger select bit	-
IOBC	-	40097h	-	-	Available only in the R32C/111
PDRF	034Fh	-	-	Available only in the M16C/29	-
PFCR	0358h	-	-	Available only in the M16C/29 (1)	-
TPRC	025Ah	-	-	Available only in the M16C/29	-

Note:
1. When using the three-phase PWM output or port output switch function, select the three-phase PWM output function with the port function control register.

4.13 Serial Interface

Table 4.30 to Table 4.34 list the changes in serial interface, associated pins, and associated SFRs.

Table 4.30 Comparison of Serial Interface

Item	M16C/29	R32C/111
Synchronous/asynchronous serial interface	3 channels (UART0 to UART2)	6 channels (UART0 to UART3, UART5, UART8)
Special mode 1 (I^2C-bus mode)	1 channel (UART2)	5 channels (UART0 to UART3, UART5)
Special mode 2	1 channel (UART2)	5 channels (UART0 to UART3, UART5)
Special mode 3 (Bus collision detection, IEBus mode)	1 channel (UART2)	5 channels (UART0 to UART3, UART5) (Optional (1))(2)
Special mode 4 (SIM mode)	1 channel (UART2)	N/A
Synchronous serial interface	1 channel (SIO3)	N/A

Notes:
1. Please contact a Renesas Electronics sales office to use the optional feature.
2. In R32C/111, special mode 4 is bus collision detection and IEBus mode.

Table 4.31 Comparison of Serial Interface-associated Pins

Channel	Pin	M16C/29	R32C/111
UART0	P6_0	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$	$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$/$\overline{\text{SS0}}$
	P6_1	CLK0	CLK0
	P6_2	RXD0	RXD0/SCL0/STXD0
	P6_3	TXD0	TXD0/SDA0/SRXD0
	P6_4	CTS0	-
UART1	P6_4	$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/CLKS1	$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/$\overline{\text{SS1}}$
	P6_5	CLK1	CLK1
	P6_6	RXD1	RXD1/SCL1/STXD1
	P6_7	TXD1	TXD1/SDA1/SRXD1
	P7_0	$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$/CLKS1	-
	P7_1	CLK1	-
	P7_2	RXD1	-
	P7_3	TXD1	-
UART2	P7_0	TXD2/SDA2	TXD2/SDA2/SRXD2
	P7_1	RXD2/SCL2	RXD2/SCL2/STXD2
	P7_2	CLK2	CLK2
	P7_3	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$	$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/$\overline{\text{SS2}}$
SIO3/UART3	P3_0	CLK3	CLK3
	P3_1	SIN3	RXD3/SCL3/STXD3
	P3_2	SOUT3	TXD3/SDA3/SRXD3
	P3_3	-	$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$/$\overline{\text{SS3}}$
UART5	P7_6	-	TXD5/SDA5/SRXD5
	P7_7	-	CLK5
	P8_0	-	RXD5/SCL5/STXD5
	P8_1	-	$\overline{\text{CTS5}}$/$\overline{\text{RTS5}}$/$\overline{\text{SS5}}$
UART8	P7_3	-	TXD8
	P7_4	-	CLK8
	P7_5	-	RXD8
	P7_6	-	$\overline{\text{CTS8}}$/$\overline{\text{RTS8}}$

Table 4.32 Comparison of Serial Interface-associated SFRs (1/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
U0MR	03A0h	0368h	-	Address changed	
			7	Reserved	TXD, RXD Input/Output Polarity Switch Bit
U1MR	03A8h	02E8h	-	Address changed	
			7	Reserved	TXD, RXD Input/Output Polarity Switch Bit
U2MR	0378h	0338h	-	Address changed	
U3MR	-	0328h	-	-	Available only in the R32C/111
U5MR	-	01C8h	-	-	Available only in the R32C/111
U8MR	-	01E8h	-	-	Available only in the R32C/111
U0C0	03A4h	036Ch	-	Address changed	
			2	$\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit	Reserved
U1C0	03ACh	02ECh	-	Address changed	
			2	$\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit	Reserved
U2C0	037Ch	033Ch	-	Address changed	
			2	$\overline{\text{CTS}}/\overline{\text{RTS}}$ function select bit	Reserved
U3C0	-	032Ch	-	-	Available only in the R32C/111
U5C0	-	01CCh	-	-	Available only in the R32C/111
U8C0	-	01ECh	-	-	Available only in the R32C/111
U0C1	03A5h	036Dh	-	Address changed	
			4	-	UART0 Transmit Interrupt Source Select Bit
			5	-	UART0 Continuous Receive Mode Enable Bit
			6	-	Logical Inversion Select Bit
U1C1	03ADh	02EDh	-	Address changed	
			4	-	UART1 Transmit Interrupt Source Select Bit
			5	-	UART1 Continuous Receive Mode Enable Bit
			6	-	Logical Inversion Select Bit
U2C1	037Dh	033Dh	-	Address changed	
			7	Error signal output enable bit	Reserved
U3C1	-	032Dh	-	-	Available only in the R32C/111
U5C1	-	01CDh	-	-	Available only in the R32C/111
U8C1	-	01EDh	-	-	Available only in the R32C/111
UCON	03B0h	-	-	Available only in the M16C/29	-
U78CON	-	01F0h	-	-	Available only in the R32C/111

Table 4.33 Comparison of Serial Interface-associated SFRs (2/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
U0SMR	-	0367h	-	-	Available only in the R32C/111
U1SMR	-	02E7h	-	-	Available only in the R32C/111
U2SMR	0377h	0337h	-	Address changed	
U3SMR	-	0327h	-	-	Available only in the R32C/111
U5SMR	-	01C7h	-	-	Available only in the R32C/111
U0SMR2	-	0366h	-	-	Available only in the R32C/111
U1SMR2	-	02E6h	-	-	Available only in the R32C/111
U2SMR2	0376h	0336h	-	Address changed	
U3SMR2	-	0326h	-	-	Available only in the R32C/111
U5SMR2	-	01C6h	-	-	Available only in the R32C/111
U0SMR3	-	0365h	-	-	Available only in the R32C/111
U1SMR3	-	02E5h	-	-	Available only in the R32C/111
U2SMR3	0375h	0335h	-	Address changed	
			0	-	$\overline{SS}$ pin function enable bit
			2	-	Clock-phase Set Bit
			4	-	Serial input pin set bit
U3SMR3	-	0325h	-	-	Available only in the R32C/111
U5SMR3	-	01C5h	-	-	Available only in the R32C/111
U0SMR4	-	0364h	-	-	Available only in the R32C/111
U1SMR4	-	02E4h	-	-	Available only in the R32C/111
U2SMR4	0374h	0334h	-	Address changed	
U3SMR4	-	0324h	-	-	Available only in the R32C/111
U5SMR4	-	01C4h	-	-	Available only in the R32C/111
U0TB	03A3h to 03A2h	036Bh to 036Ah	-	Address changed	
U1TB	03ABh to 03AAh	02EBh to 02EAh	-	Address changed	
U2TB	037Bh to 037Ah	033Bh to 033Ah	-	Address changed	
U3TB	-	032Bh to 032Ah	-	-	Available only in the R32C/111
U5TB	-	01CBh to 01CAh	-	-	Available only in the R32C/111
U8TB	-	01EBh to 01EAhh	-	-	Available only in the R32C/111

Table 4.34 Comparison of Serial Interface-associated SFRs (3/3)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
U0RB	03A7h to 03A6h	036Fh to 036Eh	-	Address changed	
U1RB	03AFh to 03AEh	02EFh to 02EEh	-	Address changed	
U2RB	037Fh to 037Eh	033Fh to 033Eh	-	Address changed	
U3RB	-	032Fh to 032Eh	-	-	Available only in the R32C/111
U5RB	-	01CFh to 01CEh	-	-	Available only in the R32C/111
U8RB	-	01EFh to 01EEh	-	-	Available only in the R32C/111
U0BRG	03A1h	0369h	-	Address changed	
U1BRG	03A9h	02E9h	-	Address changed	
U2BRG	0379h	0339h	-	Address changed	
U3BRG	-	0329h	-	-	Available only in the R32C/111
U5BRG	-	01C9h	-	-	Available only in the R32C/111
U8BRG	-	01E9h	-	-	Available only in the R32C/111
IFSR0	-	4406Fh	-	-	Available only in the R32C/111
IFSR1	-	4406Dh	-	-	Available only in the R32C/111
S3BRG	0363h	-	-	Available only in the M16C/29	-
PACR	025Dh	-	-	Available only in the M16C/29	-
S3C	0362h	-	-	Available only in the M16C/29	-
S3TRR	0360h	-	-	Available only in the M16C/29	-

4.14 A/D Converter

Table 4.35 to Table 4.37 list the changes in A/D converter, associated pins, and associated SFRs.

Table 4.35 Comparison of A/D Converters

Item	M16C/29	R32C/111
Operating modes	8 modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweep mode 0 • Repeat sweep mode 1 • Simultaneous sample sweep mode • Delayed trigger mode 0 • Delayed trigger mode 1	7 modes: • One-shot mode • Repeat mode • Single sweep mode • Repeat sweep mode 0 • Repeat sweep mode 1 • Multi-port single sweep mode • Multi-port repeat sweep mode 0
Analog input pins	16 pins AN0 to AN7, AN0_0 to AN0_3, AN2_4, AN3_0 to AN3_2	20 pins AN0 to AN7, AN0_0 to AN0_3, AN2_0 to AN2_7

Table 4.36 Comparison of A/D Converter-associated Pins

Channel	Pin	M16C/29	R32C/111
AN2_0	44	-	P2_0
AN2_1	43	-	P2_1
AN2_2	42	-	P2_2
AN2_3	41	-	P2_3
AN2_4	40	P9_3	P2_4
AN2_5	39	-	P2_5
AN2_6	38	-	P2_6
AN2_7	37	-	P2_7
AN3_0	2	P9_0	-
AN3_1	1	P9_1	-
AN3_2	64	P9_2	-

Table 4.37 Comparison of A/D Converter-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
ADCON0 (AD0CON0)	03D6h	0396h	-	The symbol changed from ADCON0 to AD0CON0	
ADCON1 (AD0CON1)	03D7h	0397h	-	The symbol changed from ADCON1 to AD0CON1	
ADCON2 (AD0CON2)	03D4h	0394h	-	The symbol changed from ADCON2 to AD0CON2	
			4	Frequency select bit 2	-
			5	Trigger Select Bit 1	External Trigger Request Source Select Bit
AD0CON3	-	0395h	-	-	Available only in the R32C/111
AD0CON4	-	0392h	-	-	Available only in the R32C/111
AD0 (AD00)	03C1h to 03C0h	0381h to 0380h	-	Address changed The symbol changed from AD0 to AD00	
AD1 (AD01)	03C3h to 03C2h	0383h to 0382h	-	Address changed The symbol changed from AD1 to AD01	
AD2 (AD02)	03C5h to 03C4h	0385h to 0384h	-	Address changed The symbol changed from AD2 to AD02	
AD3 (AD03)	03C7h to 03C6h	0387h to 0386h	-	Address changed The symbol changed from AD3 to AD03	
AD4 (AD04)	03C9h to 03C8h	0389h to 0388h	-	Address changed The symbol changed from AD4 to AD04	
AD5 (AD05)	03CBh to 03CAh	038Bh to 038Ah	-	Address changed The symbol changed from AD5 to AD05	
AD6 (AD06)	03CDh to 03CCh	038Dh to 038Ch	-	Address changed The symbol changed from AD6 to AD06	
AD7 (AD07)	03CFh to 03CEh	038Fh to 038Eh	-	Address changed The symbol changed from AD7 to AD07	
ADTRGCON	03D2h	-	-	Available only in the M16C/29	-
ADSTA0	03D3h	-	-	Available only in the M16C/29	-
TB2SC	039Eh	-	-	Available only in the M16C/29	-

4.15 CRC Calculation Circuit

Table 4.38 and Table 4.39 list the changes in CRC calculation circuit and associated SFRs.

Table 4.38 Comparison of CRC Calculation Circuits

Item	M16C/29	R32C/111
A generator polynomial	CRC-CCITT($X^{16}+X^{12}+X^5+1$) CRC-16($X^{16}+X^{15}+X^2+1$)	CRC-CCITT($X^{16}+X^{12}+X^5+1$)
MSB/LSB selectable	Available	N/A
CRC Snoop	Available	N/A

Table 4.39 Comparison of CRC Calculation Circuit-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
CRCD	03BDh to 03BCh	037Dh to 037Ch	-	Address changed	
CRCIN	03BEh	037Eh	-	Address changed	
CRCMR	03B6h	-	-	Available only in the M16C/29	-
CRCSAR	03B5h to 03B4h	-	-	Available only in the M16C/29	-

4.16 Intelligent I/O

In M16C/29, intelligent I/O is referred to as timer S.

Table 4.40 and Table 4.44 list the changes in the configuration of intelligent I/O and associated SFRs.

Table 4.40 Comparison of Intelligent I/O

Item	M16C/29	R32C/111
Base timer	• Group 0: No timers • Group 1: One timer (two-phase pulse processing provided) Includes a base timer reset register • Group 2: No timers	• Group 0: One timer (two-phase pulse processing provided) • Group 1: One timer (two-phase pulse processing provided) • Group 2: One timer (two-phase pulse processing not provided)
Time measurement	• Group 0: No channels • Group 1: 16 bits × 8 channels Includes a digital debounce filter on channel 7 • Group 2: No channels	• Group 0: 16 bits × 8 channels • Group 1: 16 bits × 8 channels • Group 2: No channels
Waveform generation	• Group 0: No channels • Group 1: 16 bits × 8 channels • Group 2: No channels	• Group 0: 16 bits × 8 channels • Group 1: 16 bits × 8 channels • Group 2: 16 bits × 3 channels
Serial interface	• Group 0: No channels • Group 1: No channels • Group 2: No channels	• Group 0: No channels • Group 1: No channels • Group 2: One channel Variable-length synchronous serial I/O mode, IEBus mode (optional (1))

Note:

1. Please contact a Renesas Electronics sales office to use the optional feature.

Table 4.41 Comparison of Intelligent I/O-associated SFRs (1/4)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
G0BT	-	01A1h to 01A0h	-	-	Available only in the R32C/111
G0BCR0	-	01A2h	-	-	Available only in the R32C/111
G0BCR1	-	01A3h	-	-	Available only in the R32C/111
G0TMCR0	-	0198h	-	-	Available only in the R32C/111
G0TMCR1	-	0199h	-	-	Available only in the R32C/111
G0TMCR2	-	019Ah	-	-	Available only in the R32C/111
G0TMCR3	-	019Bh	-	-	Available only in the R32C/111
G0TMCR4	-	019Ch	-	-	Available only in the R32C/111
G0TMCR5	-	019Dh	-	-	Available only in the R32C/111
G0TMCR6	-	019Eh	-	-	Available only in the R32C/111
G0TMCR7	-	019Fh	-	-	Available only in the R32C/111
G0POCR0	-	0190h	-	-	Available only in the R32C/111
G0POCR1	-	0191h	-	-	Available only in the R32C/111
G0POCR2	-	0192h	-	-	Available only in the R32C/111
G0POCR3	-	0193h	-	-	Available only in the R32C/111
G0POCR4	-	0194h	-	-	Available only in the R32C/111
G0POCR5	-	0195h	-	-	Available only in the R32C/111
G0POCR6	-	0196h	-	-	Available only in the R32C/111
G0POCR7	-	0197h	-	-	Available only in the R32C/111
G0TM0/ G0PO0	-	0181h to 0180h	-	-	Available only in the R32C/111
G0TM1/ G0PO1	-	0183h to 0182h	-	-	Available only in the R32C/111
G0TM2/ G0PO2	-	0185h to 0184h	-	-	Available only in the R32C/111
G0TM3/ G0PO3	-	0187h to 0186h	-	-	Available only in the R32C/111
G0TM4/ G0PO4	-	0189h to 0188h	-	-	Available only in the R32C/111
G0TM5/ G0PO5	-	018Bh to 018Ah	-	-	Available only in the R32C/111
G0TM6/ G0PO6	-	018Dh to 018Ch	-	-	Available only in the R32C/111
G0TM7/ G0PO7	-	018Fh to 018Eh	-	-	Available only in the R32C/111
G0TPR6	-	01A4h	-	-	Available only in the R32C/111
G0TPR7	-	01A5h	-	-	Available only in the R32C/111
G0FE	-	01A6h	-	-	Available only in the R32C/111
G0FS	-	01A7h	-	-	Available only in the R32C/111

Table 4.42 Comparison of Intelligent I/O-associated SFRs (2/4)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
G1BT	0321h to 0320h	0121h to 0120h	-	Address changed	
G1BCR0	0322h	0122h	-	Address changed	
			2	Base timer reset cause select bit 4	Count Source Divide Ratio Select Bit (DIV4 to DIV0)
			3	Reserved	
			4	Reserved	
			5	Reserved	
			6	Channel 7 input select bit	
G1BCR1	0323h	0123h	-	Address changed	
			0	Reserved	Base timer reset cause select bit 0
G1TMCR0	0318h	0118h	-	Address changed	
G1TMCR1	0319h	0119h	-	Address changed	
G1TMCR2	031Ah	011Ah	-	Address changed	
G1TMCR3	031Bh	011Bh	-	Address changed	
G1TMCR4	031Ch	011Ch	-	Address changed	
G1TMCR5	031Dh	011Dh	-	Address changed	
G1TMCR6	031Eh	011Eh	-	Address changed	
G1TMCR7	031Fh	011Fh	-	Address changed	
G1POCR0	0310h	0110h	-	Address changed	
			2	-	Operating Mode Select Bit
			6	-	Base Timer Reset Enable Bit
G1POCR1	0311h	0111h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR2	0312h	0112h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR3	0313h	0113h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR4	0314h	0114h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR5	0315h	0115h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR6	0316h	0116h	-	Address changed	
			2	-	Operating Mode Select Bit
G1POCR7	0317h	0117h	-	Address changed	
			2	-	Operating Mode Select Bit

Table 4.43 Comparison of Intelligent I/O-associated SFRs (3/4)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
G1TM0/ G1PO0	0301h to 0300h	0101h to 0100h	-	Address changed	
G1TM1/ G1PO1	0303h to 0302h	0103h to 0102h	-	Address changed	
G1TM2/ G1PO2	0305h to 0304h	0105h to 0104h	-	Address changed	
G1TM3/ G1PO3	0307h to 0306h	0107h to 0106h	-	Address changed	
G1TM4/ G1PO4	0309h to 0308h	0109h to 0108h	-	Address changed	
G1TM5/ G1PO5	030Bh to 030Ah	010Bh to 010Ah	-	Address changed	
G1TM6/ G1PO6	030Dh to 030Ch	010Dh to 010Ch	-	Address changed	
G1TM7/ G1PO7	030Fh to 030Eh	010Fh to 010Eh	-	Address changed	
G1TRP6	0324h	0124h	-	Address changed	
G1TRP7	0325h	0125h	-	Address changed	
G1FE	0326h	0126h	-	Address changed	
G1FS	0327h	0127h	-	Address changed	
G1DV	032Ah	-	-	Available only in the M16C/29	-
G1BTRR	0329h to 0328h	-	-	Available only in the M16C/29	-
G1IR	0330h	-	-	Available only in the M16C/29	-
G1IE0	0331h	-	-	Available only in the M16C/29	-
G1IE1	0332h	-	-	Available only in the M16C/29	-
P17DDR	033Fh	-	-	Available only in the M16C/29	-
G2BT	-	0161h to 0160h	-	-	Available only in the R32C/111
G2BCR0	-	0162h	-	-	Available only in the R32C/111
G2BCR1	-	0163h	-	-	Available only in the R32C/111
G2POCR0	-	0150h	-	-	Available only in the R32C/111
G2POCR1	-	0151h	-	-	Available only in the R32C/111
G2POCR2	-	0152h	-	-	Available only in the R32C/111
G2POCR3	-	0153h	-	-	Available only in the R32C/111
G2POCR4	-	0154h	-	-	Available only in the R32C/111
G2POCR5	-	0155h	-	-	Available only in the R32C/111
G2POCR6	-	0156h	-	-	Available only in the R32C/111
G2POCR7	-	0157h	-	-	Available only in the R32C/111

Table 4.44 Comparison of Intelligent I/O-associated SFRs (4/4)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
G2PO0	-	0141h to 0140h	-	-	Available only in the R32C/111
G2PO1	-	0143h to 0142h	-	-	Available only in the R32C/111
G2PO2	-	0145h to 0144h	-	-	Available only in the R32C/111
G2PO3	-	0147h to 0146h	-	-	Available only in the R32C/111
G2PO4	-	0149h to 0148h	-	-	Available only in the R32C/111
G2PO5	-	014Bh to 014Ah	-	-	Available only in the R32C/111
G2PO6	-	014Dh to 014Ch	-	-	Available only in the R32C/111
G2PO7	-	014Fh to 014Eh	-	-	Available only in the R32C/111
G2FE	-	0166h	-	-	Available only in the R32C/111
G2RTP	-	0167h	-	-	Available only in the R32C/111
BTSR	-	0164h	-	-	Available only in the R32C/111
G2TB	-	016Dh to 016Ch	-	-	Available only in the R32C/111
G2RB	-	016Fh to 016Eh	-	-	Available only in the R32C/111
G2MR	-	016Ah	-	-	Available only in the R32C/111
G2CR	-	016Bh	-	-	Available only in the R32C/111
IECR	-	0172h	-	-	Available only in the R32C/111
IEAR	-	0171h to 0170h	-	-	Available only in the R32C/111
IETIF	-	0173h	-	-	Available only in the R32C/111
IERIF	-	0174h	-	-	Available only in the R32C/111

4.17 Ports

4.17.1 Port Pi Registers and Port Pi Direction Registers

Table 4.45 to Table 4.48 list the changes in the port Pi register and port Pi direction register (i = 0 to 3, 6 to 10).

Table 4.47 lists the changes in port Pi pull-up control register.

Table 4.45 Comparison of Port Pi Registers (i = 0 to 3, 6 to 10)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
P0	03E0h	03C0h	-	Address changed	
P1	03E1h	03C1h	-	Address changed	
P2	03E4h	03C4h	-	Address changed	
P3	03E5h	03C5h	-	Address changed	
P6	03ECh	03CCh	-	Address changed	
P7	03EDh	03CDh	-	Address changed	
P8	03F0h	03D0h	-	Address changed	
P9	03F1h	03D1h	-	Address changed	
			0	Port P90 bit	-
			1	Port P91 bit	-
			2	Port P92 bit	-
P10	03F4h	03D4h	-	Address changed	

Table 4.46 Comparison of Port Pi Direction Registers (i = 0 to 3, 6 to 10)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
PD0	03E2h	03C2h	-	Address changed	
PD1	03E3h	03C3h	-	Address changed	
PD2	03E6h	03C6h	-	Address changed	
PD3	03E7h	03C7h	-	Address changed	
PD6	03EEh	03CEh	-	Address changed	
PD7	03EFh	03CFh	-	Address changed	
PD8	03F2h	03D2h	-	Address changed	
PD9	03F3h	03D3h	-	Address changed	
			0	Port P90 direction bit	-
			1	Port P91 direction bit	-
			2	Port P92 direction bit	-
PD10	03F6h	03D6h	-	Address changed	

Table 4.47 Comparison of Port Pi Pull-up Control Registers (i = 0 to 3, 6 to 10)

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
PUR0	03FCh	03F0h	-	Address changed	
PUR1	03FDh	03F1h	0	-	P4_0 to P4_3 pull-up control bit
			1	-	P4_4 to P4_7 pull-up control bit
			2	-	P5_0 to P5_3 pull-up control bit
			3	-	P5_4 to P5_7 pull-up control bit
			4	P6_0 to P6_3 pull-up control bit	-
			5	P6_4 to P6_7 pull-up control bit	-
			6	P7_0 to P7_3 pull-up control bit	-
			7	P7_4 to P7_7 pull-up control bit	-
PUR2	03FEh	03F2h	-	Address changed	
			0	P8_0 to P8_3 pull-up control bit	P6_0 to P6_3 pull-up control bit
			1	P8_4 to P8_7 pull-up control bit	P6_4 to P6_7 pull-up control bit
			2	P9_0 to P9_3 pull-up control bit	P7_0 to P7_3 pull-up control bit
			3	P9_4 to P9_7 pull-up control bit	P7_4 to P7_7 pull-up control bit
			4	P10_0 to P10_3 pull-up control bit	P8_0 to P8_3 pull-up control bit
			5	P10_4 to P10_7 pull-up control bit	P8_4 to P8_7 pull-up control bit
			6	-	P9_3 pull-up control bit
PUR3	-	03F3h	-	-	Available only in the R32C/111

Table 4.48 Comparison of Port-associated SFRs

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
PACR	025Dh	-	-	Available only in the M16C/29	-
NDDR	033Eh	-	-	Available only in the M16C/29	-

4.17.2 Port I/O Function Selection

In the R32C/111 Group, when a programmable I/O port and output signals from a peripheral function share a pin, the output function of the corresponding pin is selected by setting the port Pi_j function select register. When input signals from a peripheral function are allotted to multiple pins, set the input function select register to decide which pin input should be connected to the peripheral functions.

Table 4.49 lists the Port I/O Function Select Registers (i = 0 to 3, 6 to 10; j = 0 to 7).

Table 4.49 Comparison of Port I/O Function Select Registers

Item	M16C/29	R32C/111
Output function	-	Port Pi_j function select registers (Pi_jS (i = 0 to 3, 6 to 10; j = 0 to 7)
Input function	-	Input function select registers (IFS0, IFS2, IFS3, and IFS7)

4.18 Flash Memory

4.18.1 Flash Memory

Table 4.50 to Table 4.52 list the changes in flash memory, software commands, and associated registers.

Table 4.50 Comparison of Flash Memory

Item	M16C/29	R32C/111
Rewrite modes	Four modes: CPU rewrite mode, standard serial I/O mode, parallel I/O mode, CAN I/O (1)	Three modes: CPU rewrite mode, standard serial I/O mode, parallel I/O mode)
Program operation	2-byte units	8-byte units
Lock bit protection type	Blocks 0 to 5 are write protected by setting the FMR16 bit. In addition, block 0 and block 1 are write protected by setting the FMR02 bit.	Protect is enabled in block units by setting a lock bit.
Commands	5	9
Others		Forcible erase function Standard serial I/O mode disable function

Note:
1. These modes only apply to the Normal-version.

Table 4.51 Comparison of Software Commands

Command	M16C/29				R32C/111			
	First command		Second command		First command		Second command	
	Address	Data	Address	Data	Address	Data	Address	Data
Read array mode shift	x	xxFFh	N/A	N/A	FFFFF800h	00FFh	N/A	N/A
Read status register mode shift (1)	x	xx70h	N/A	SRD	FFFFF800h	0070h	N/A	N/A
Clear status register	x	xx50h	N/A	N/A	FFFFF800h	0050h	N/A	N/A
Program (2, 3)	WA	xx40h	WA	WD	FFFFF800h	0043h	WA	WD
Block erase	x	xx20h	BA	xxD0h	FFFFF800h	0020h	BA	00D0h
Lock bit program	N/A	N/A	N/A	N/A	FFFFF800h	0077h	BA	00D0h
Read lock bit status	N/A	N/A	N/A	N/A	FFFFF800h	0071h	BA	00D0h
Read lock bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0071h	N/A	N/A
Protect bit program	N/A	N/A	N/A	N/A	FFFFF800h	0067h	PBA	00D0h
Read protect bit status mode shift (4)	N/A	N/A	N/A	N/A	FFFFF800h	0061h	N/A	N/A

SRD: Status register data (D7 to D0)
WA: Even address to be written
WD: 16-bit write data
BA: Even address in specified block
PBA: Address of the protect bit
x: Any even address in the user ROM area
xx: Upper byte of command code (ignored)
N/A: Not applicable

Notes:
1. This command cannot be executed in EW1 mode.
2. In M16C/29, a set of command consists of 2 words from the first command to the second. The program is performed in 16-bit (1-word) units.
3. In R32C/111, a set of command consists of 5 words from the first command to the fifth. The program is performed in 64-bit (4-word) units. The higher 29 bits of the address WA should be fixed and the 3 lower bits of respective command from the second to fifth should be set to 000b, 010b, 100b, and 110b for the addresses 0h, 2h, 4h, and 6h, or 8h, Ah, Ch, and Eh.
4. This command should be executed in RAM.

Table 4.52 Comparison of Flash Memory-associated SFRs

Symbol	Address		Bits	Differences	
	M16C/29	R32C/111		M16C/29	R32C/111
FMR0	01B7h	40000h	7 to 0	Register configuration is completely different	
FMR1	01B5h	40009h	7 to 0	Register configuration is completely different	
FMR4	01B3h	-	-	Available only in the M16C/29	-
FMCR	-	0006h	-	-	Available only in the R32C/111
FEBC0	-	001Dh to 001Ch	-	-	Available only in the R32C/111
FEBC3	-	0011h to 0010h	-	-	Available only in the R32C/111
FPR0	-	40008h	-	-	Available only in the R32C/111
FMSR0	-	40001h	-	-	Available only in the R32C/111
FBPM0	-	4000Ah	-	-	Available only in the R32C/111
FBPM1	-	4000Bh	-	-	Available only in the R32C/111

4.18.2 Flash Memory Block Configuration

The R32C/111 has a different flash memory block configuration from that of M16C/29.
Figure 4.1 shows a diagram of the Flash Memory Block Configuration.

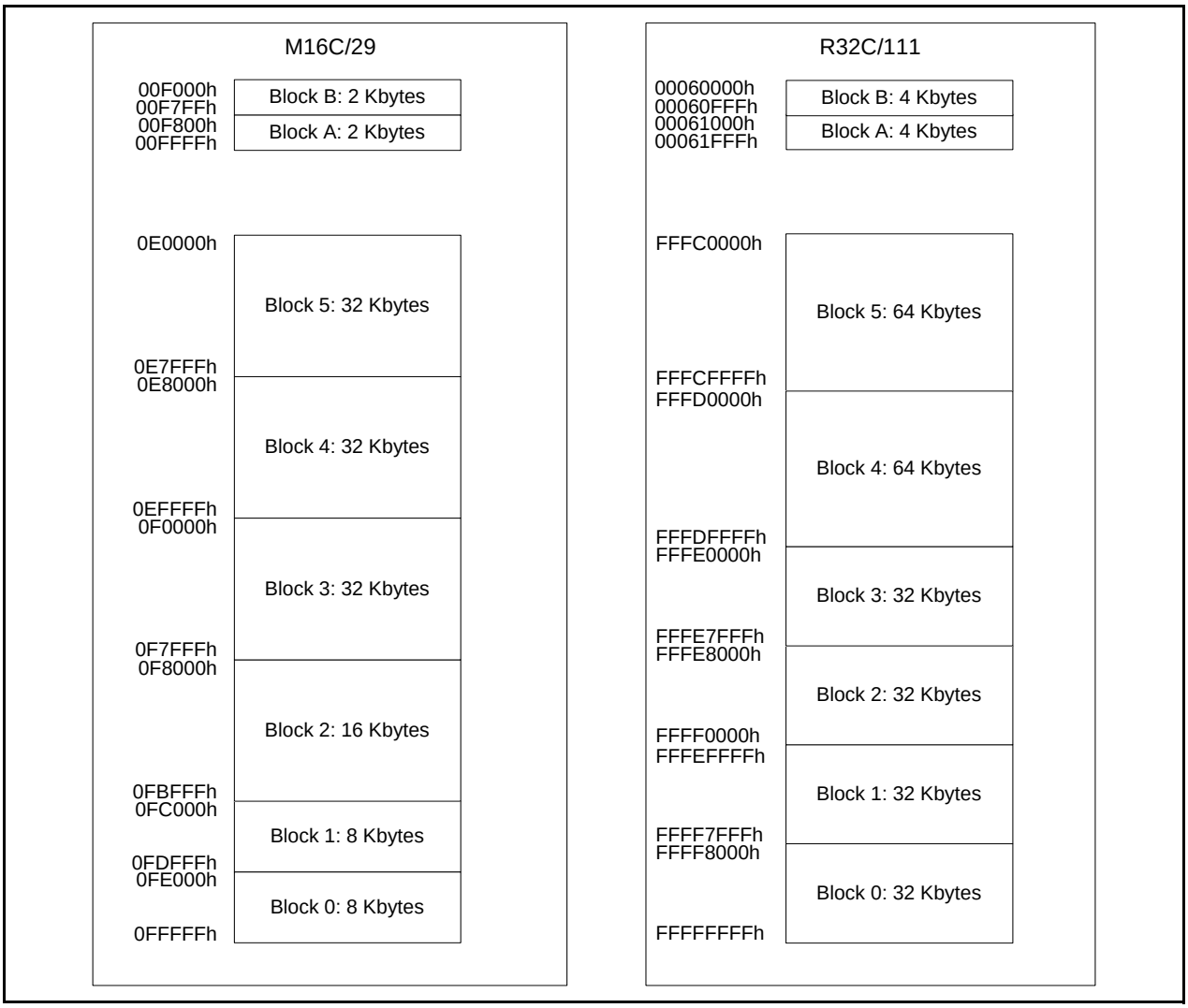

Figure 4.1 Flash Memory Block Configurations

4.18.3 ID Code Protection

The R32C/111 has a different ID code store address block configuration from that of M16C/29. Figure 4.2 shows the stored ID code addresses of both groups.

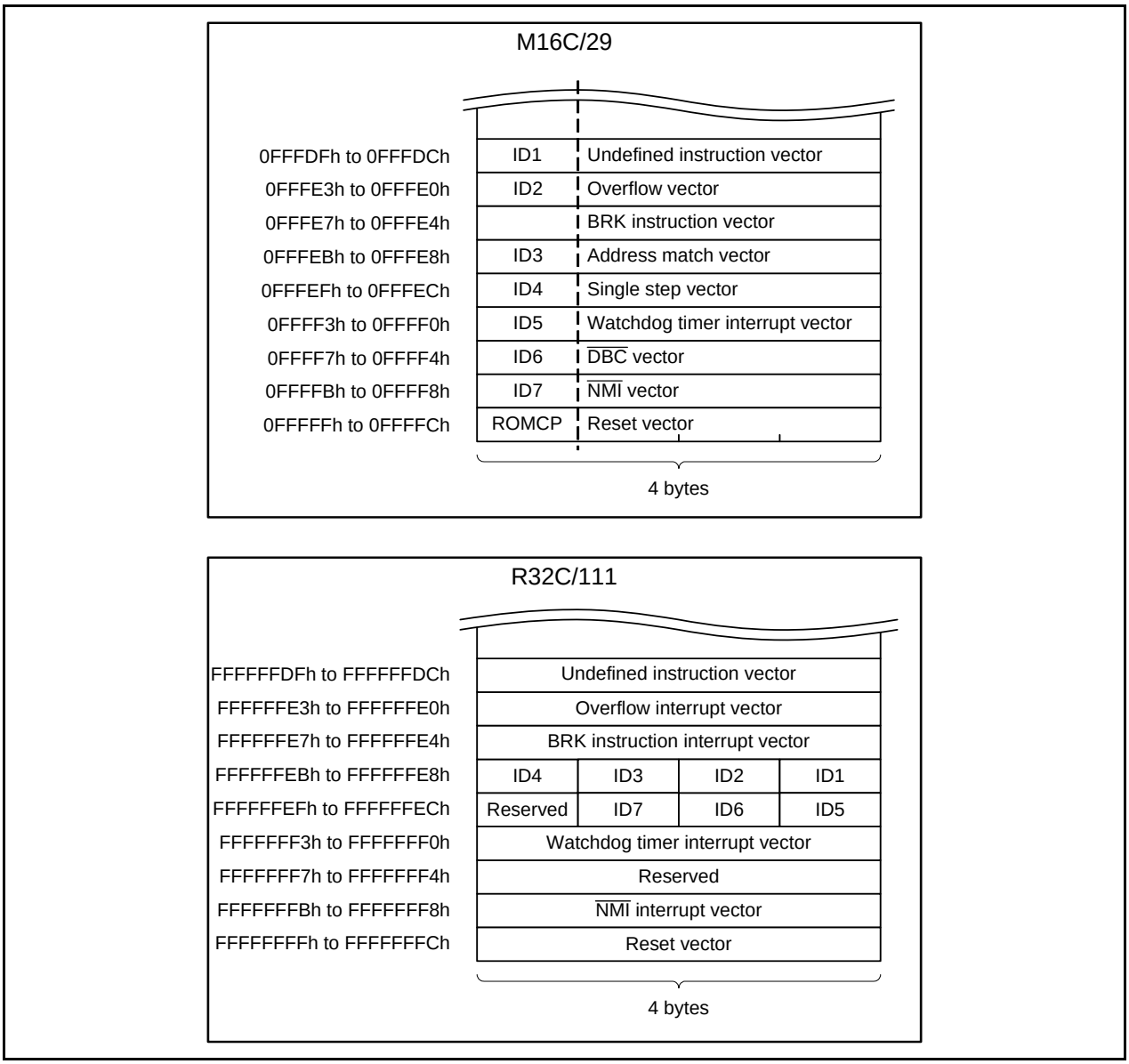

Figure 4.2 Comparison Diagram: Addresses for Storing ID Codes

4.18.4 ROM Code Protection

Table 4.53 lists the change in ROM code protection-associated register.

Table 4.53 Comparison of ROM Code Protection

Symbol	Address		Bits	M16C/29	R32C/111
	M16C/29	R32C/111			
ROMCP	0FFFFFh	-	7, 6	Available only in the M16C/29	-

In R32C/111, each block has two protect bits. Table 4.54 lists the addresses of the protect bits. If any of these protect bits is set to 0 (protected), all areas are protected. Refer to the user's manual for details.

Table 4.54 R32C/111 Protect Bit Addresses

Block	Protect Bit 0	Protect Bit 1
Block B	00060100h	00060300h
Block A	00061100h	00061300h
Block 5	FFFC0100h	FFFC0300h
Block 4	FFFD0100h	FFFD0300h
Block 3	FFFE0100h	FFFE0300h
Block 2	FFFE8100h	FFFE8300h
Block 1	FFFF0100h	FFFF0300h
Block 0	FFFF8100h	FFFF8300h

4.19 Development Tools

Table 4.55 lists the differences in the development tools.

Table 4.55 Comparison of Development Tools

Tools	For M16C/29	For R32C/111
C compiler (including simulator debugger)	C Compiler for M16C Series and R8C Family (M3T-NC30WA)	C compiler package for R32C Series
Real-time OS	M3T-MR30/4	M3T-MR100/4
Emulator debugger	PC7501	E30A (R0E00030AKCT100)
Emulation probe	M3028BT-EPB-3	-
Compact emulator	M3028BT2-CPE-3	-
Renesas Starter Kit	R0K330290S001BE	R0K564112S000BE

5. Reference Documents

M16C/29 Group User's Manual: Hardware Rev.1.12
R32C/111 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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Revision History	M16C/29 Group, R32C/111 Group Differences between M16C/29 and R32C/111 (64-pin Packages)

Rev.	Date	Description	
		Page	Summary
1.00	July 15, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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