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7548/49 Group, 7544 Group (QzROM)

Differences between 7548/49 Group and 7544 Group (QzROM)

1. Differences between 7548/49 Group and 7544 Group (QzROM)

	7544 Group (QzROM)	7548/49 Group	
		7548	7549
Applicable Product	M37544G2A-XXXSP/GP M37544G2ASP/GP	M37548G3-XXXFP M37548G3FP M37548G2-XXXFP M37548G2FP M37548G1-XXXFP M37548G1FP	M37549G3-XXXFP M37549G3FP M37549G2-XXXFP M37549G2FP M37549G1-XXXFP M37549G1FP
Package	PRDP0032BA-A (32P4B): 32-pin SDIP PLQP0032GB-A (32P6U-A): 32-pin LQFP	PLSP0020JB-A (20P2F-A): 20-pin SSOP	PRSP0024GA-A (24P2Q-A): 24-pin SSOP
ROM Type: ROM/RAM Size (Bytes)	QzROM: 8K/256	QzROM: 2K/192 (for G1) QzROM: 4K/256 (for G2) QzROM: 6K/256 (for G3)	
Programmable I/O	25	15	19
LED Ports	14 (Total electrical current: 60 mA)	8	
Interrupts	12 sources, 12 vectors	12 sources, 12 vectors	
	(five external sources)	(four external sources)	
Timer	8-bit x 2 (Timer 1, X)	8-bit x 2 (Timer 1, 2)	
	16-bit x 1 (Timer A)	16-bit x 1 (Timer A)	
Output Compare	Not available	3-channels	
Input Capture	Not available	1-channel	
A/D Converter	8-bit x 6-channels	10-bit x 6-channels	10-bit x 8-channels
On-Chip Oscillator	2MHz(Typ.)	High-speed: 4MHz(Typ.)	
		Low-speed: 250kHz(Typ.)	
Power-On Reset	Not available	Built-in type	
Low Voltage Detection Circuit	Not available	Built-in type	
Power Source Voltage (ceramic oscillation)	2.2 to 5.5 V	1.8 to 5.5 V	
Power Source Voltage (on-chip oscillator)	1.8 to 5.5V @2MHz	4.0 to 5.5V @4MHz 1.8 to 5.5V @250kHz	
Function Set ROM Area	Address $FFD4_{16}$	Addresses $FFD4_{16}$ to $FFDB_{16}$	

(cont.)

Function Set ROM Data	Not available	Built-in type
Oscillation Method Selection	Not available	Available
Low-speed On-chip Oscillator Control	Not available	Available
STP Instruction Function Selection	Not available	Available
WDT H Count Source Selection	Not available	Available
WDT Source Clock Selection	Not available	Available
WDT Disable Bit	Not available	Available
LVD Circuit Valid Bit	Not available	Available
LVD Valid Bit in STP Mode	Not available	Available

2. Pin Configuration of 7548/49 Group and 7544 Group (QzROM)

The 7548/49 Group and 7544 Group (QzROM) are NOT pin compatible. The differences of the pin configuration and package type are indicated below.

7544 Group (QzROM) Pin Configuration & Package Type

Left side (pins 1–16):
- 1 — P1$_2$/S$_{CLK}$
- 2 — P1$_3$/$\overline{S_{RDY}}$
- 3 — P1$_4$/CNTR$_0$
- 4 — P2$_0$/AN$_0$
- 5 — P2$_1$/AN$_1$
- 6 — P2$_2$/AN$_2$
- 7 — P2$_3$/AN$_3$
- 8 — P2$_4$/AN$_4$
- 9 — P2$_5$/AN$_5$
- 10 — V$_{REF}$
- 11 — $\overline{RESET}$
- 12 — CNV$_{SS}$
- 13 — V$_{CC}$
- 14 — X$_{IN}$
- 15 — X$_{OUT}$
- 16 — V$_{SS}$

Right side (pins 32–17):
- 32 — P1$_1$/TxD
- 31 — P1$_0$/RxD
- 30 — P0$_7$(LED$_7$)
- 29 — P0$_6$(LED$_6$)
- 28 — P0$_5$(LED$_5$)
- 27 — P0$_4$(LED$_4$)
- 26 — P0$_3$(LED$_3$)/TX$_{OUT}$
- 25 — P0$_2$(LED$_2$)
- 24 — P0$_1$(LED$_1$)
- 23 — P0$_0$(LED$_0$)/CNTR$_1$
- 22 — P3$_7$(LED$_{13}$)/INT$_0$
- 21 — P3$_4$(LED$_{12}$)/INT$_1$
- 20 — P3$_3$(LED$_{11}$)
- 19 — P3$_2$(LED$_{10}$)
- 18 — P3$_1$(LED$_9$)
- 17 — P3$_0$(LED$_8$)

Device marking: M37544G2A-XXXSP / M37544G2ASP

Package type: PRDP0032BA-A (32P4B)
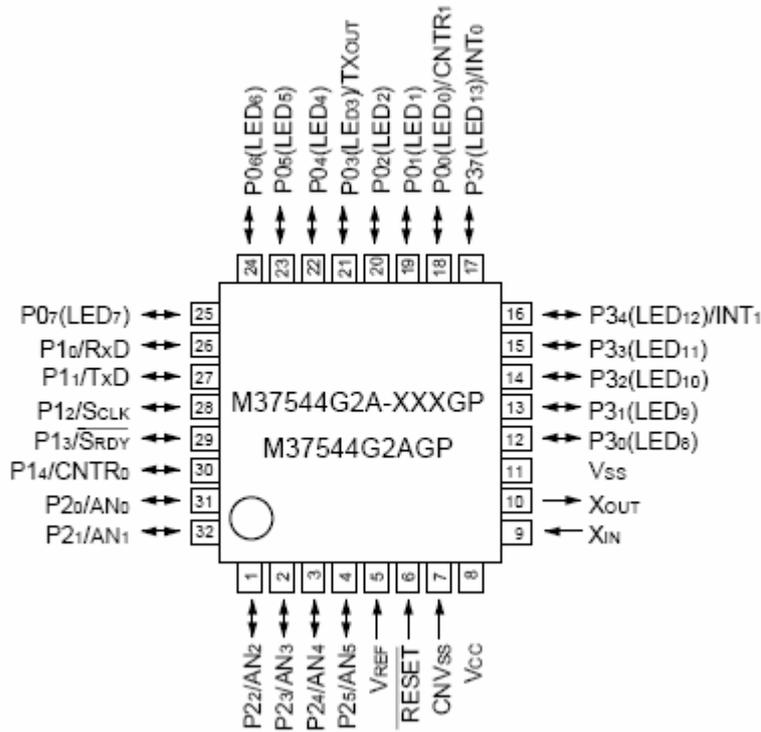
Package type: PLQP0032GB-A (32P6U-A)

7548/49 Group Pin Configuration & Package Type
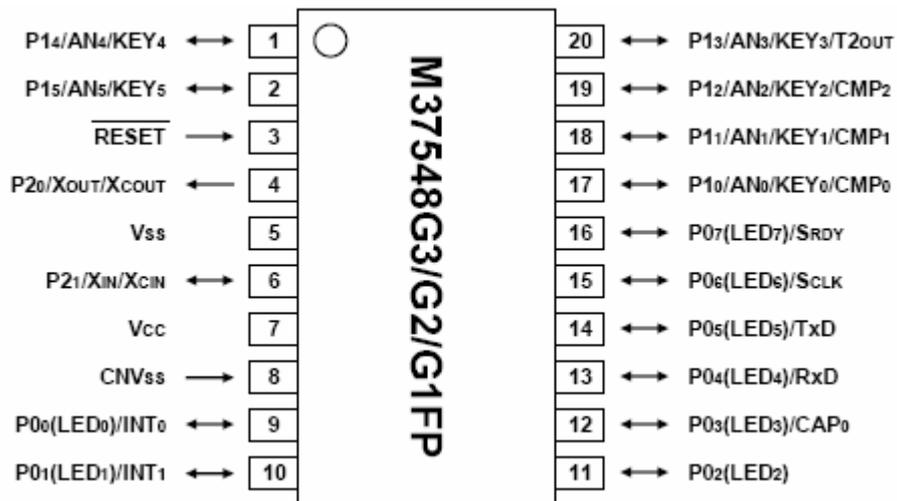
Package type: PLSP0020JB-A (20P2F-A)
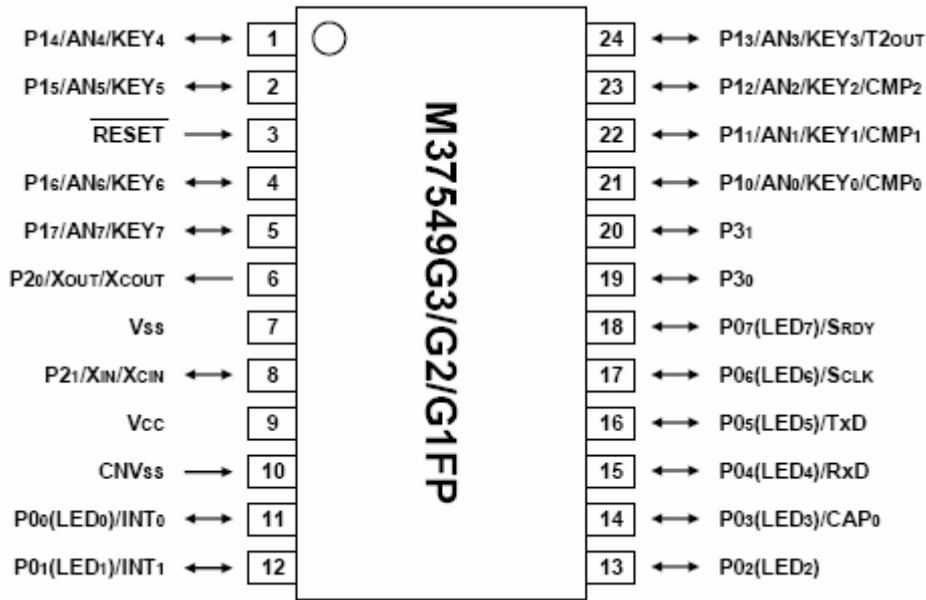
Package type: PRSP0024GA-A (24P2Q-A)

3. SFR of 7548/49 Group and 7544 Group (QzROM)

The differences of the SFRs between the 7548/49 Group and 7544 Group (QzROM) are indicated below.

	7544 Group (QzROM)	7548/49 Group
0000_{16}	Port P0 (P0)	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)	Port P3 (P3) *only 7549
0007_{16}	Port P3 direction register (P3D)	Port P3 direction register (P3D)*only 7549
0008_{16}	Reserved	Reserved
0009_{16}	Reserved	Reserved
$000A_{16}$	Reserved	Reserved
$000B_{16}$	Reserved	Reserved
$000C_{16}$	Reserved	Port P0 drive capacity control register (DCCR)
$000D_{16}$	Reserved	Port P0 Pull-up control register (PULL0)
$000E_{16}$	Reserved	Port P1 Pull-up control register (PULL1)
$000F_{16}$	Reserved	Key-on wake-up input select register(KEYS)
0010_{16}	Reserved	Capture/compare register (low-order) (CRAL)
0011_{16}	Reserved	Capture/compare register (high-order) (CRAH)
0012_{16}	Reserved	Capture/compare register R/W pointer (CCRP)
0013_{16}	Reserved	Compare output mode register (CMOM)
0014_{16}	Reserved	Timer A (low-order) (TAL)
0015_{16}	Reserved	Timer A (high-order) (TAH)

	7544 Group (QzROM)	7548/49 Group
0016_{16}	Pull-up control register (PULL)	Reserved
0017_{16}	Port P1P3 control register (P1P3C)	Reserved
0018_{16}	Transmit/Receive buffer register (TB/RB)	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)	Baud rate generator (BRG)
$001D_{16}$	Timer A mode register (TAM)	Reserved
$001E_{16}$	Timer A (low-order) (TAL)	Reserved
$001F_{16}$	Timer A (high-order) (TAH)	Reserved
0020_{16}	Reserved	Reserved
0021_{16}	Reserved	Reserved
0022_{16}	Reserved	Reserved
0023_{16}	Reserved	Reserved
0024_{16}	Reserved	Reserved
0025_{16}	Reserved	Reserved
0026_{16}	Reserved	Reserved
0027_{16}	Reserved	Reserved
0028_{16}	Prescaler 1 (PRE1)	Prescaler 12 (PRE12)
0029_{16}	Timer 1 (T1)	Timer 1 (T1)
$002A_{16}$	Reserved	Timer 2 (T2)
$002B_{16}$	Timer X mode register (TXM)	Timer mode register (TM)
$002C_{16}$	Prescaler X (PREX)	Timer count source set register (TCSS)
$002D_{16}$	Timer X (TX)	Compare register re-load register (CMPR)
$002E_{16}$	Timer count source set register1 (TCSS1)	Capture/compare port register (CCPR)
$002F_{16}$	Timer count source set register2 (TCSS2)	Capture/compare status register (CCSR)
0030_{16}	Reserved	Compare interrupt source set register (CISR)
0031_{16}	Reserved	Capture software trigger register (CSTR)
0032_{16}	Reserved	Capture mode register (CAPM)
0033_{16}	Reserved	Reserved
0034_{16}	A/D control register (ADCON)	A/D control register (ADCON)
0035_{16}	A/D register (AD)	A/D conversion register (low-order) (ADL)
0036_{16}	Reserved	A/D conversion register (high-order) (ADH)
0037_{16}	Reserved	Clock mode register (CLKM)
0038_{16}	MISRG	Oscillation stop detection register (CLKSTP)
0039_{16}	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)
$003A_{16}$	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)

Note: Do not access to the SFR reserved area.

      : New SFR in 7548/49

      : Changed in 7548/49

4. Function Set ROM Area of 7548/49 Group and 7544 Group (QzROM)

Function set ROM data and addresses are changed to the 7548/49 Group with additional new ROM data as indicated below.

	7544 Group (QzROM)	**7548/49 Group**
FFD4$_{16}$	ROM code protect	Renesas shipment test area
FFD5$_{16}$	——	Renesas shipment test area
FFD6$_{16}$	——	Renesas shipment test area
FFD7$_{16}$	——	Renesas shipment test area
FFD8$_{16}$	——	Function set ROM data 0
FFD9$_{16}$	——	Function set ROM data 1
FFDA$_{16}$	——	Function set ROM data 2
FFDB$_{16}$	——	ROM code protect

☐ : Difference
☐ : New Function set ROM

5. Interrupt Vector of 7548/49 Group and 7544 Group (QzROM)

Interrupt sources and interrupt vector addresses are changed to the 7548/49 Group with additional registers as indicated below. The bits in interrupt request registers and interrupt control registers are also changed.
(Please refer to their datasheet for the detail information)

7544 Group (QzROM) and 7548/49 Group Differences = ☐

Vector address		Priority	7544 Group (QzROM) Interrupt Source	7548/49 Group Interrupt Source
High-order	**Low-order**			
FFFD$_{16}$	FFFC$_{16}$	1	Reset	Reset
FFFB$_{16}$	FFFA$_{16}$	2	Serial I/O receive	Serial I/O receive
FFF9$_{16}$	FFF8$_{16}$	3	Serial I/O transmit	Serial I/O transmit
FFF7$_{16}$	FFF6$_{16}$	4	INT$_0$	INT$_0$
FFF5$_{16}$	FFF4$_{16}$	5	INT$_1$	INT$_1$
FFF3$_{16}$	FFF2$_{16}$	6	Key-on wake-up	Key-on wake-up
FFF1$_{16}$	FFF0$_{16}$	7	CNTR$_0$	Capture
FFEF$_{16}$	FFEE$_{16}$	8	CNTR$_1$	Compare
FFED$_{16}$	FFEC$_{16}$	9	Timer X	Timer A
FFEB$_{16}$	FFEA$_{16}$	10	Reserved area	Timer 2
FFE9$_{16}$	FFE8$_{16}$	11	Reserved area	A/D conversion
FFE7$_{16}$	FFE6$_{16}$	12	Timer A	Timer 1
FFE5$_{16}$	FFE4$_{16}$	13	Reserved area	Reserved area
FFE3$_{16}$	FFE2$_{16}$	14	A/D conversion	Reserved area
FFE1$_{16}$	FFE0$_{16}$	15	Timer 1	Reserved area
FFDF$_{16}$	FFDE$_{16}$	16	Reserved area	Reserved area
FFDD$_{16}$	FFDC$_{16}$	17	BRK instruction	BRK instruction

6. Clock Generating Circuit of 7548/49 Group and 7544 Group (QzROM)

The differences of clock generating circuit between the 7548/49 Group and 7544 Group (QzROM) are indicated below.
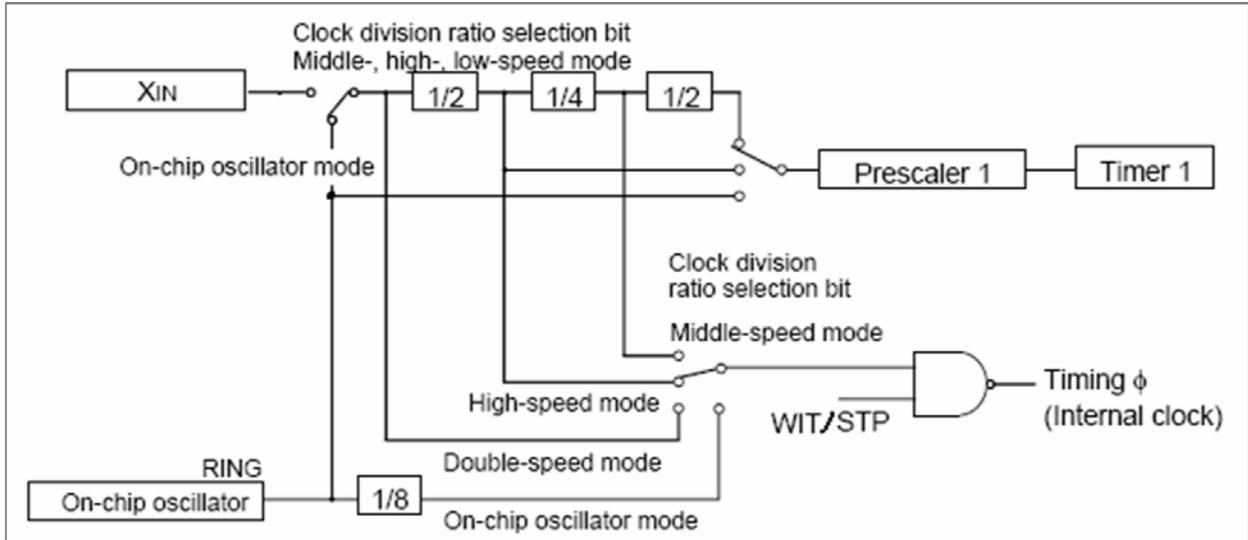

**Figure 1 7544 Group (QzROM) Clock Generating Circuit Block Diagram**
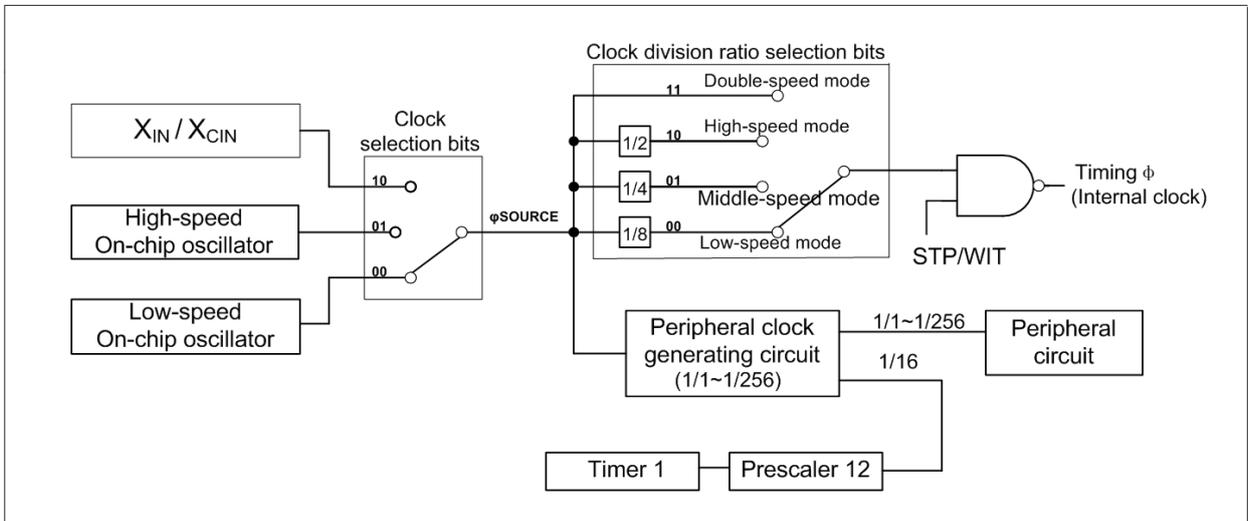
Figure 2 7548/49 Group Clock Generating Circuit Block Diagram

7. Timer of 7548/49 Group and 7544 Group (QzROM)

The differences of timers between the 7548/49 Group and 7544 Group (QzROM) are indicated below. Compared with the 7544 Group (QzROM), some functions of the timer 2 and timer A are reduced in the 7548/49 Group. However, the output compare and input capture functions are added for some special application.

7544 Group (QzROM) Timer		**7548/49 Group Timer**	
Timer 1 (Prescaler 1)	Count source: f(XIN)/16, f(XIN)/2, or on-chip oscillator output selectable (set using the TCSS2 register)	Timer 1 (Prescaler 12)	Count source: f(φSOURCE)/16, or f(X_{CIN}):32kHz quartz crystal oscillation (set using the CLKM and TCSS register)
Timer X (Prescaler X)	Count source: f(XIN)/16, f(XIN)/2, or on-chip oscillator output selectable (set using the TCSS1 register)	Timer 2 (Prescaler 12)	Count source: f(φSOURCE)/16, f(φSOURCE)/256, Prescaler 12 output, Timer A underflow (set using the CLKM and TCSS register)
	Timer X has four operating modes: (set using the TXM register) (1) Timer mode (2) Pulse output mode (3) Event counter mode (4) Pulse width measurement mode		Timer 2 has two operating modes: (set using the TM register) (1) Timer mode (2) Pulse output mode
Timer A (16-bit)	Count source: f(XIN)/16, f(XIN)/2, or on-chip oscillator output selectable (set using the TCSS2 register)	Timer A (16-bit)	Count source: f(φSOURCE)/16, f(φSOURCE)/2, f(φSOURCE)/32, f(φSOURCE)/64, f(φSOURCE)/128, f(φSOURCE)/256, f(LSOCO), f(X_{CIN}) (set using the CLKM and TCSS register)
	Timer A has four operating modes: (set using the TAM register) (1) Timer mode (2) Period measurement mode (3) Event counter mode (4) Pulse width HL continuously measurement mode		Timer A has three operating modes: (1) Timer mode (2) Output compare mode (3) Input capture mode

8. Reference Document

Datasheets
7544 Group Datasheet (QzROM version)
7548 Group Datasheet
7549 Group Datasheet
(Use the latest version of the document on the Renesas Technology Web site.)

Technical Update/Technical News
(Use the latest version of the document on the Renesas Technology Web site.)

7548/49 Group, 7544 Group (QzROM)
Differences between 7548/49 Group and 7544 Group (QzROM)

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Revision Record

Rev.	Date	Description	
		Page	**Summary**
1.00	Oct.07.06	-	First edition issued
1.01	Mar.05.08	All	7544 Group → 7544 Group (QzROM)
		1	Modified the applicable product name and ROM type of 7544 Group (QzROM)
		7	Figure 2 updated (Added "X$_{CIN}$"; sysclk → Φ source; Deleted "System" and "CPU")
		8	The table content of 7548/49 Group updated

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