

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 7544 Group, 7540 Group

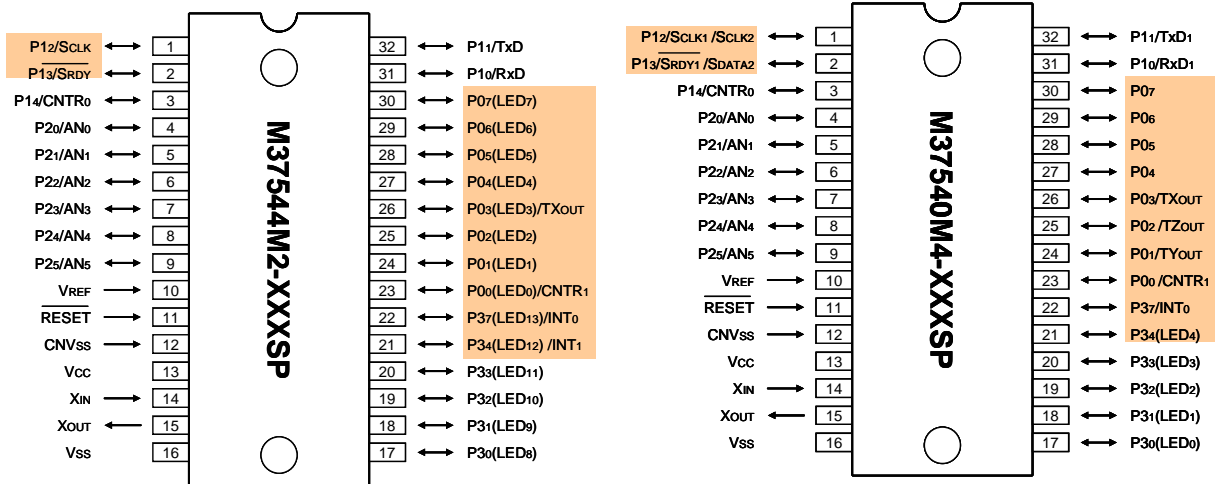
### Differences between 7544 Group and 7540 Group

#### 1. Differences between 7544 Group / 7540 Group

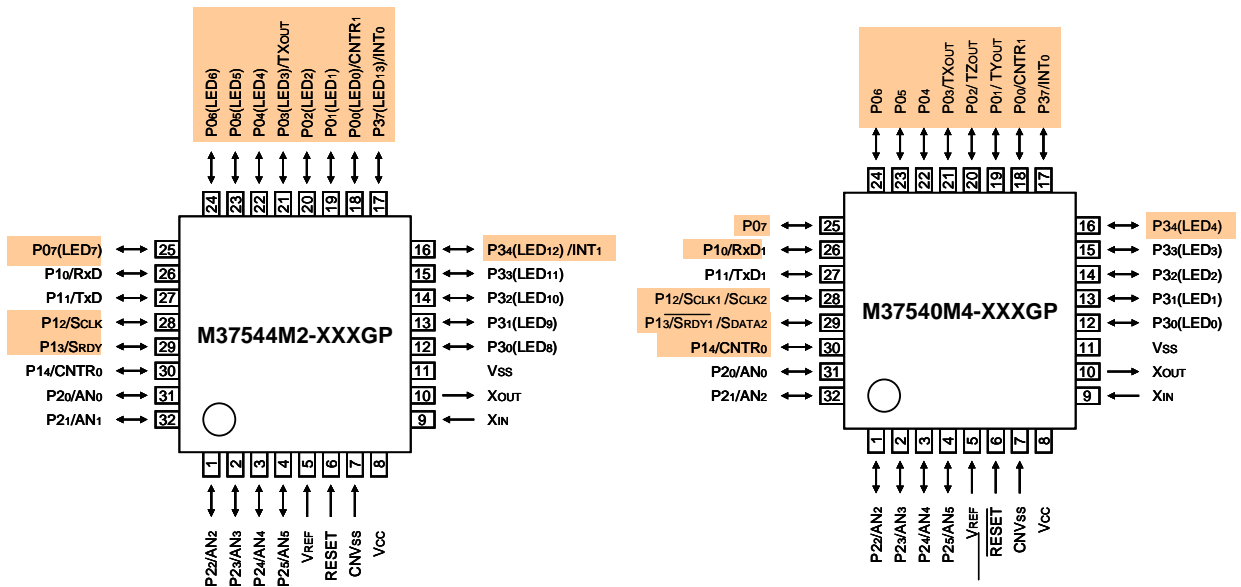
	7544 Group	7540 Group
Applicable Product	M37544M2-XXXSP/FP/GP/HP M37544G2SP/GP/HP (HP for ES only) M37544G2A-XXXSP/GP M37544G2ASP/GP	M37540M2-XXXSP/FP/GP M37540M4-XXXSP/FP/GP M37540E8SP/FP/GP
Package	32-pin LQFP, 32-pin SDIP, 36-pin WQFN	32-pin SSOP, 36-pin LQFP, 32-pin SDIP
ROM Type: ROM/RAM Size	MASK: 8K/256 One-Time PROM: 8K/256 QzROM: 8K/256	MASK: 8K/384, 16K/512 One-Time PROM: 32K/768
Instruction Execution Time (Shortest Instruction )	0.25 $\mu$ s (8 MHz double-speed mode)	0.34 $\mu$ s (6 MHz double-speed mode)
Programmable I/O Port	25	29 (36-pin version) 25 (32-pin version)
Interrupts	12 sources, 12 vectors	15 sources, 15 vectors (36-pin version) 14 sources, 14 vectors (32-pin version)
Timer	8-bit x 2, 16-bit x 1	8-bit x 4, 16-bit x 1
Serial Interface	8-bit x 1: Serial I/O (UART or clock synchronous type)	8-bit x 2: Serial I/O1 (UART or clock synchronous type) Serial I/O2 (Clock synchronous type)
A/D Converter	8-bit x 6 channels	10-bit x 8 channels (36-pin version) 10-bit x 6 channels (32-pin version)
LED Port	14 (Total electrical current: 80 mA)	7 (36-pin version) 5 (32-pin version)
Power Source Voltage	MASK, One-Time PROM: 4.0 to 5.5 V QzROM: 1.8 to 5.5 V	2.2 to 5.5 V
ROM Code Protect	Available only in QzROM version	Not available
ID Code Check Function	Available only in One-Time PROM version	Not available

2. Pin Configuration 7544 Group/7540 Group

7544 Group/7540 Group Difference =



Package Type: PRDP0032BA-A (32P4B)



Package Type: PLQP0032GB-A (32P6U-A)

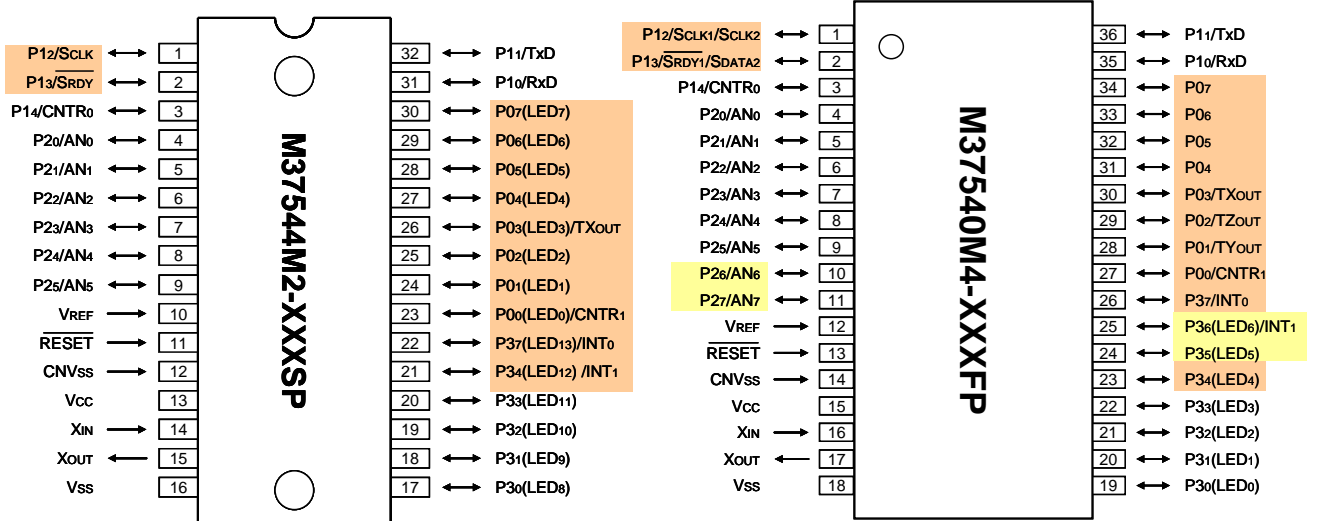
36-pin SSOP package is not available in the 7544 Group.

32-pin SDIP is compared for reference only.

The pin numbers do not match.

7544 Group/7540Group Difference =

Reduced ports in the 7544 Group =



Package Type: PRDP0032BA-A (32P4B)

Package Type: PRSP0036GA-A (36P2R-A)

### 3. Interrupt Vector, ROM Code Protect Address, ID Code Storage Address

#### 7544 Group/7540 Group

<Interrupt Vector>                      7544 Group/7540 Group Difference =  

Vector address		Priority	7544 Group Interrupt Source	7540 Group Interrupt Source
High-order	Low-order			
FFFD <sub>16</sub>	FFFC <sub>16</sub>	1	Reset	Reset
FFFB <sub>16</sub>	FFFA <sub>16</sub>	2	Serial I/O receive	Serial I/O1 receive
FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	3	Serial I/O transmit	Serial I/O1 transmit
FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	4	INT <sub>0</sub>	INT <sub>0</sub>
FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	5	INT <sub>1</sub>	INT <sub>1</sub>
FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	6	Key-on wake-up	Key-on wake-up
FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	7	CNTR <sub>0</sub>	CNTR <sub>0</sub>
FFEF <sub>16</sub>	FFEE <sub>16</sub>	8	CNTR <sub>1</sub>	CNTR <sub>1</sub>
FFED <sub>16</sub>	FFEC <sub>16</sub>	9	Timer X	Timer X
FFEB <sub>16</sub>	FFEA <sub>16</sub>	10	Reserved area	Timer Y
FFE9 <sub>16</sub>	FFE8 <sub>16</sub>	11	Reserved area	Timer Z
FFE7 <sub>16</sub>	FFE6 <sub>16</sub>	12	Timer A	Timer A
FFE5 <sub>16</sub>	FFE4 <sub>16</sub>	13	Reserved area	Serial I/O2 Interrupt
FFE3 <sub>16</sub>	FFE2 <sub>16</sub>	14	A/D conversion	A/D conversion
FFE1 <sub>16</sub>	FFE0 <sub>16</sub>	15	Timer 1	Timer 1
FFDF <sub>16</sub>	FFDE <sub>16</sub>	16	Reserved area	Reserved area
FFDD <sub>16</sub>	FFDC <sub>16</sub>	17	BRK Instruction	BRK Instruction

#### <ROM Code Protect Address>

7544 Group

7540 Group

FFD4 <sub>16</sub>	<b>ROM code protect address (QzROM)</b> User ROM area (MASK) ID code storage address (One-Time PROM) (See below)	User ROM area
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ROM code protect is assigned to address FFD4<sub>16</sub> in **the QzROM version of the 7544 Group**. If you select write to protect bit with a serial programmer, or select programming by Renesas Technology before shipment to enable protect, 00<sub>16</sub> is set to this address. Otherwise, FF<sub>16</sub> is set. The address cannot be used by user programs.

#### <ID Code Storage Address>

7544 Group

7540 Group

FFD4 <sub>16</sub> to FFDA <sub>16</sub>	<b>ID code storage address (One-Time PROM)</b> ROM code protect address / User ROM area (QzROM) (See above) User ROM area (MASK)	User ROM area
------------------------------------------------	----------------------------------------------------------------------------------------------------------------------------------------	---------------

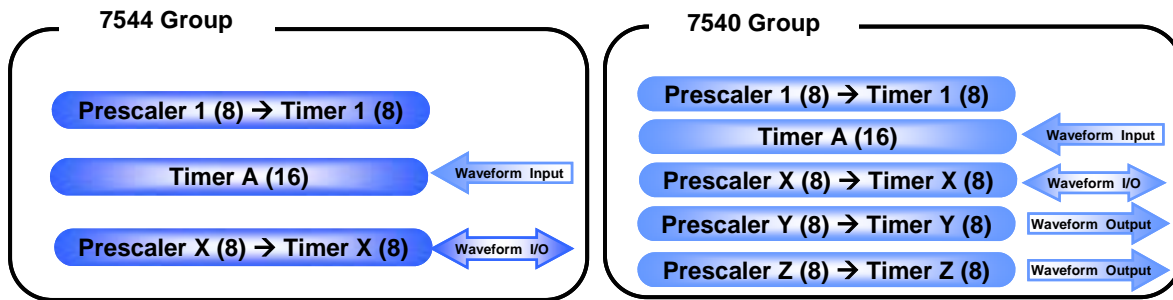
ID codes are assigned to addresses FFD4<sub>16</sub> to FFDA<sub>16</sub> in **the One-Time PROM version of the 7544 Group**. These are used for the ID code check function in serial write mode. If the ID code storage addresses are not blank, the ID codes sent from the serial programmer and the ID codes written to the ROM are checked to see if they match. If the codes do not match, commands sent from the programmer are not acknowledged. These addresses cannot be used by user programs.

#### 4. SFR 7544 Group/7540 Group

	7544 Group	7540 Group	
0000 <sub>16</sub>	Port P0 (P0)	Port P0 (P0)	
0001 <sub>16</sub>	Port P0 direction register (P0D)	Port P0 direction register (P0D)	
0002 <sub>16</sub>	Port P1 (P1)	Port P1 (P1)	
0003 <sub>16</sub>	Port P1 direction register (P1D)	Port P1 direction register (P1D)	
0004 <sub>16</sub>	Port P2 (P2)	Port P2 (P2)	
0005 <sub>16</sub>	Port P2 direction register (P2D)	Port P2 direction register (P2D)	
0006 <sub>16</sub>	Port P3 (P3)	Port P3 (P3)	
0007 <sub>16</sub>	Port P3 direction register (P3D)	Port P3 direction register (P3D)	
0008 <sub>16</sub>	Reserved	Reserved	
0009 <sub>16</sub>	Reserved	Reserved	
000A <sub>16</sub>	Reserved	Reserved	
000B <sub>16</sub>	Reserved	Reserved	
000C <sub>16</sub>	Reserved	Reserved	
000D <sub>16</sub>	Reserved	Reserved	
000E <sub>16</sub>	Reserved	Reserved	
000F <sub>16</sub>	Reserved	Reserved	
0010 <sub>16</sub>	Reserved	Reserved	
0011 <sub>16</sub>	Reserved	Reserved	
0012 <sub>16</sub>	Reserved	Reserved	
0013 <sub>16</sub>	Reserved	Reserved	
0014 <sub>16</sub>	Reserved	Reserved	
0015 <sub>16</sub>	Reserved	Reserved	
0016 <sub>16</sub>	Pull-up control register (PULL)	Pull-up control register (PULL)	Changed function with same name
0017 <sub>16</sub>	Port P1P3 control register (P1P3C)	Port P1P3 control register (P1P3C)	Changed function with same name
0018 <sub>16</sub>	Transmit/Receive buffer register (TB/RB)	Transmit/Receive buffer register (TB/RB)	Same function with different name
0019 <sub>16</sub>	Serial I/O status register (SIOSTS)	Serial I/O1 status register (SIO1STS)	Changed function with same name
001A <sub>16</sub>	Serial I/O control register (SIOCON)	Serial I/O1 control register (SIO1CON)	Changed function with same name
001B <sub>16</sub>	UART control register (UARTCON)	UART control register (UARTCON)	Same function with different name
001C <sub>16</sub>	Baud rate generator (BRG)	Baud rate generator (BRG)	Same function with different name
001D <sub>16</sub>	Timer A mode register (TAM)	Timer A mode register (TAM)	Same function with different name
001E <sub>16</sub>	Timer A register (low-order) (TAL)	Timer A register (low-order) (TAL)	Same function with different name
001F <sub>16</sub>	Timer A register (high-order) (TAH)	Timer A register (high-order) (TAH)	Same function with different name
0020 <sub>16</sub>	Reserved	Timer Y, Z mode register (TYZM)	Unavailable SFR
0021 <sub>16</sub>	Reserved	Prescaler Y (PREY)	Unavailable SFR
0022 <sub>16</sub>	Reserved	Timer Y secondary (TYS)	Unavailable SFR
0023 <sub>16</sub>	Reserved	Timer Y primary (TYP)	Unavailable SFR
0024 <sub>16</sub>	Reserved	Timer Y, Z waveform output register (PUM)	Unavailable SFR
0025 <sub>16</sub>	Reserved	Prescaler Z (PREZ)	Unavailable SFR
0026 <sub>16</sub>	Reserved	Timer Z secondary (TZS)	Unavailable SFR
0027 <sub>16</sub>	Reserved	Timer Z primary (TZP)	Unavailable SFR
0028 <sub>16</sub>	Prescaler 1 (PRE1)	Prescaler 1 (PRE1)	Same function with different bit name
0029 <sub>16</sub>	Timer 1 (T1)	Timer 1 (T1)	Same function with different bit name
002A <sub>16</sub>	Reserved	One-shot start register (ONS)	Unavailable SFR
002B <sub>16</sub>	Timer X mode register (TXM)	Timer X mode register (TXM)	Same function with different bit name
002C <sub>16</sub>	Prescaler X (PREX)	Prescaler X(PREX)	Same function with different bit name
002D <sub>16</sub>	Timer X (TX)	Timer X (TX)	Same function with different bit name
002E <sub>16</sub>	Timer count source set register 1 (TCSS1)	Timer count source set register (TCSS)	Same function with different bit name
002F <sub>16</sub>	Timer count source set register 2 (TCSS2)	Reserved	New SFR
0030 <sub>16</sub>	Reserved	Serial I/O2 control register (SIO2CON)	Unavailable SFR
0031 <sub>16</sub>	Reserved	Serial I/O2 register (SIO2)	Unavailable SFR
0032 <sub>16</sub>	Reserved	Reserved	New SFR
0033 <sub>16</sub>	Reserved	Reserved	New SFR
0034 <sub>16</sub>	A/D control register (ADCON)	A/D control register (ADCON)	Same function with different bit name
0035 <sub>16</sub>	A/D register (AD)	A/D conversion register (low-order) (ADL)	Same function with different bit name
0036 <sub>16</sub>	Reserved	A/D conversion register (high-order) (ADH)	Unavailable SFR
0037 <sub>16</sub>	Reserved	Reserved	New SFR
0038 <sub>16</sub>	MISRG	MISRG	Same function with different bit name
0039 <sub>16</sub>	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)	Same function with different bit name
003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)	Same function with different bit name
003B <sub>16</sub>	CPU mode register (CPUM)	CPU mode register (CPUM)	Same function with different bit name
003C <sub>16</sub>	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)	Same function with different bit name
003D <sub>16</sub>	Interrupt request register 2 (IREQ2)	Interrupt request register 2 (IREQ2)	Same function with different bit name
003E <sub>16</sub>	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)	Same function with different bit name
003F <sub>16</sub>	Interrupt control register 2 (ICON2)	Interrupt control register 2 (ICON2)	Same function with different bit name

Note: Do not access to the SFR reserved areas.

### 5. Timer Composition 7544 Group/7540 Group



#### Added Functions to the timers of the 7544 Group

Compared with the 7540 Group, the number of the timer is reduced in the 7544 Group. However, the following functions are added to three timers to enhance usability.

Timer	7544 Group	7540 Group
Timer 1 (Prescaler 1)	Count source $f(XIN)/16$ , $f(XIN)/2$ , or on-chip oscillator output selectable	Count source $f(XIN)/16$ fixed
Timer A	Count source $f(XIN)/16$ , $f(XIN)/2$ , or on-chip oscillator output selectable	Count source $f(XIN)/16$ fixed
Timer X	Write to latch and timer simultaneously or write to latch only selectable	Write to latch and timer simultaneously only



## 6. Notes on Replacement

1. The A/D converter of the 7544 Group has an 8-bit resolution. The characteristics of the A/D converter vary between the 7544 Group and 7540 Group. Careful evaluation with ES samples or CS samples is recommended before mass-production.

2. To add timer functions are in the 7544 Group, a register is added as indicated below. When additional functions are not used, handle the register as follows.

- (1) Do not write to the added register. (Keep the initial value after a reset)
- (2) Write the initial value after a reset to the added register.

Address	7544 Group	7540 Group
2F <sub>16</sub>	Timer count source set register 2 (Initial value: 00 <sub>16</sub> )	(Reserved)

3. The bits in the following registers of the 7544 Group are functionally changed for expanded or reduced functions.

Address (Register Name)	Bit	7544 Group	7540 Group
16 <sub>16</sub> (Pull-up control register)	Bit 6	Disable	P35, P36 pull-up control bit
17 <sub>16</sub> (Port P1P3 control register)	Bit 2	P10, P12 input level selection bit	P10, P12, P13 input level selection bit
2B <sub>16</sub> (Timer X mode register)	Bit 5	Timer X write control bit	Disable (returns 0 when read)
3D <sub>16</sub> (Interrupt request register 2)	Bit 0	Disable (returns 0 when read)	Timer Y interrupt request bit
	Bit 1	Disable (returns 0 when read)	Timer Z interrupt request bit
	Bit 3	Disable (returns 0 when read)	Serial I/O2 interrupt request bit
3F <sub>16</sub> (Interrupt control register 2)	Bit 0	Disable (returns 0 when read)	Timer Y interrupt enable bit
	Bit 1	Disable (returns 0 when read)	Timer Z interrupt enable bit
	Bit 3	Disable (returns 0 when read)	Serial I/O2 interrupt enable bit

4. The names and functions of the following registers of the 7544 Group are changed for reduced functions.

Address	Bit	7544 Group (Timer count source set register 1)	7540 Group (Timer count source set register)
2E <sub>16</sub>	Bit 0	Timer X count source selection bit (no function change)	Timer X count source selection bit
	Bit 1		
	Bit 2	Disable (returns 0 when read)	Timer X count source selection bit
	Bit 3	Disable (returns 0 when read)	
	Bit 4	Disable (returns 0 when read)	
	Bit 5	Disable (returns 0 when read)	Always set 0
	Bit 6	Disable (returns 0 when read)	
	Bit 7	Disable (returns 0 when read)	Disable (returns 0 when read)

5. The following registers are reduced in the 7544 Group for reduced functions.  
Do not access to the addresses indicated below.

Address	7544 Group	7540 Group
20 <sub>16</sub>	Reserved	Timer Y, Z mode register
21 <sub>16</sub>	Reserved	Prescaler Y
22 <sub>16</sub>	Reserved	Timer Y secondary
23 <sub>16</sub>	Reserved	Timer Y primary
24 <sub>16</sub>	Reserved	Timer Y, Z waveform output control register
25 <sub>16</sub>	Reserved	Prescaler Z
26 <sub>16</sub>	Reserved	Timer Z secondary
27 <sub>16</sub>	Reserved	Timer Z primary
2A <sub>16</sub>	Reserved	One-shot start register
30 <sub>16</sub>	Reserved	Serial I/O2 control register
31 <sub>16</sub>	Reserved	Serial I/O2 register
36 <sub>16</sub>	Reserved	A/D conversion register (high-order)

6. ROM code protect is assigned to address FFD4<sub>16</sub> in the QzROM version of the 7544 Group. If you select write to protect bit with a serial programmer, or select programming by Renesas Technology before shipment to enable protect, 00<sub>16</sub> is set to this address. Otherwise, FF<sub>16</sub> is set. The address cannot be used by user programs.
7. ID codes are stored at addresses FFD4<sub>16</sub> to FFDA<sub>16</sub> in the One-Time PROM version of the 7544 Group. These are used for the ID code check function in serial write mode. If the ID code storage addresses are not blank, the ID codes sent from the serial programmer and the ID codes written to the ROM are checked to see if they match. If the codes do not match, commands sent from the programmer are not acknowledged. These addresses cannot be used by user programs.
8. The power source voltage of the 7544 Group is 4.0 to 5.5 V for the MASK version and the One-Time PROM version, and 1.8 to 5.5 V for the QzROM version. This differs from the power source voltage of the 7540 Group (2.2 to 5.5 V).
9. Applicable programmers differ among the One-Time PROM of the 7540 Group, the One-Time PROM of the 7544 Group, and the QzROM of the 7544 Group. Check the Development Environment Guide on the 7544 Group page of the Renesas Technology website for information on suitable programmers for the 7544 Group.  
On-board programming is also available in the QzROM version of the 7544 Group.  
Check the programmer manual for information on how to set pins for on-board programming.  
Instructions on setting the pins of the Renesas FDT + E8 + IC socket board for on-board programming are contained in "**On-Board Programming for QzROM/FLASH with E8**". To locate this document by searching by keyword on the Renesas Technology website, enter the document number "rej99b1146" in the search box.
10. Although the 7544 Group has been designed with full consideration given to compatibility of characteristics, operation margins, noise immunity, noise radiation, etc., may vary. Careful evaluation with ES or CS samples is recommended before mass-production using the 7544 Group.
11. For details of absolute maximum ratings, electrical characteristics, and operating conditions, refer to the datasheet of the product in question. The XIN-XOUT oscillation circuit constants may vary depending on the product. Contact the oscillator manufacturer to select an appropriate oscillator and oscillation circuit constants so that the product used for mass production will obtain a stable operating clock with your systems and conditions. Additional care is required when the voltage range or temperature range is wide. Also, we recommend considering the wiring patterns of the feedback resistors, the damping resistors, and the load capacity beforehand when designing circuits.

7. Reference Document

Data Sheet

7544 Group Data sheet

7540 Group Data sheet

User's Manual

7540 Group User's Manual

(Use the most recent version of the document on the Renesas Technology website)

Technical News/Technical Update

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<b>REVISION HISTORY</b>	<b>Differences between 7544 Group and 7540 Group</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Jun.13.06	—	First edition issued

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