To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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7544 Group, 7531 Group

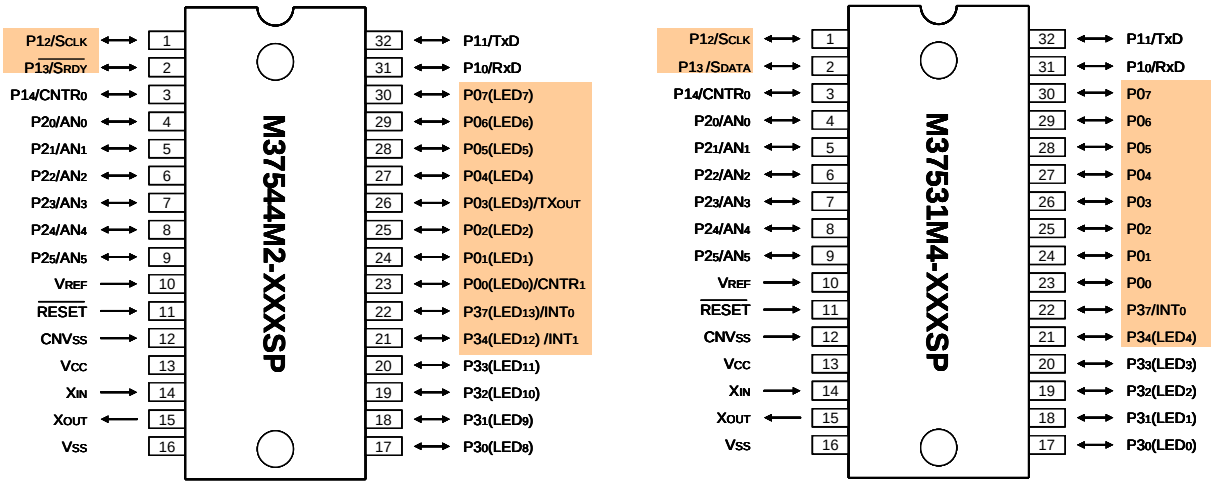
Differences between 7544 Group and 7531 Group

1. Differences between 7544 Group / 7531 Group

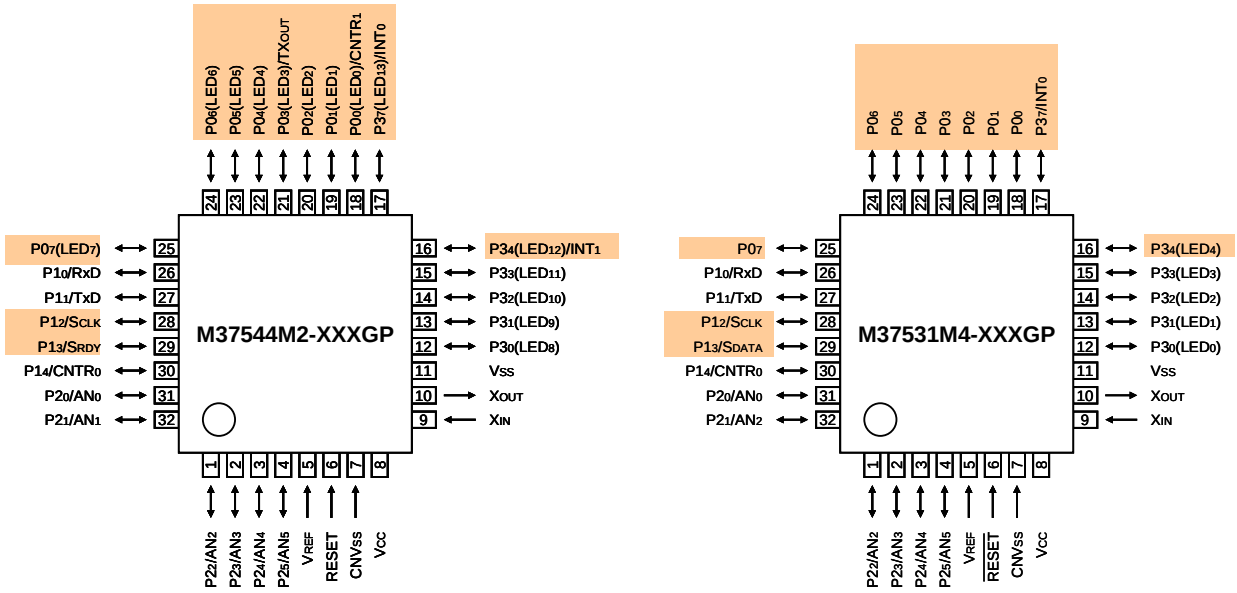
	7544 Group	7531 Group
Applicable Product	M37544M2-XXXSP/FP/GP/HP M37544G2SP/GP/HP (HP for ES only) M37544G2A-XXXSP/GP M37544G2ASP/GP	M37531M4/M4T-XXXSP/FP/GP M37531E4SP/FP/GP M37531M4V/E4T/E4V-XXXGP M37531M8-XXXSP/FP/GP M37531E8SP/FP
ROM Type: ROM/RAM Size	MASK: 8K/256 One-Time PROM: 8K/256 QzROM: 8K/256	MASK: 8K/256, 16K/384 One-Time PROM: 8K/256, 16K/384
Basic Machine-Language Instruction	71 (including DIV and MUL instructions)	69
Instruction Execution Time (Shortest Instruction)	0.25 μs (8 MHz double-speed mode)	0.5 μs (8 MHz high-speed mode)
Programmable I/O Port	25	29 (36-pin version) 25 (32-pin version)
I/O Port Pull-up Control Register	Initial value: 00_{16} (Port P0, P3: Pull-up off)	Initial value: FF_{16} (Port P0, P3: pull-up on)
LED Port	14 (Total electrical current: 80 mA)	7 (36-pin version) 5 (32-pin version)
Interrupt Source	12 sources, 12 vectors (external 5 sources)	32-pin version: 11 sources, 8 vectors (external 3 sources) 36-pin version: 12 sources, 8 vectors (external 4 sources)
Timer	8-bit x 2, 16-bit x 1	8-bit x 3
Serial Interface	8-bit x 1: Serial I/O (UART or clock synchronous type)	8-bit x 2: Serial I/O1 (For UART only) Serial I/O2 (Clock synchronous type)
A/D Converter	8-bit x 6 channels	10-bit x 8 channels (36-pin version) 10-bit x 6 channels (32-pin version)
Clock Generating Circuit	Ceramic resonator/Quartz-crystal oscillator/ External RC oscillation/On-chip oscillator oscillation	Ceramic resonator/Quartz-crystal oscillator/ External RC oscillation/ (On-chip oscillator only for power-on)
Oscillation Stop Detection Function	Available	Not available
Power Source Voltage	MASK, One-Time PROM: 4.0 to 5.5 V QzROM: 1.8 to 5.5 V	2.2 to 5.5 V
ROM Code Protect	Available only in QzROM version	Not available
ID Code Check Function	Available only in One-Time PROM version	Not available

2. Pin Configuration 7544 Group/7531 Group

7544 Group/7531 Group Difference =

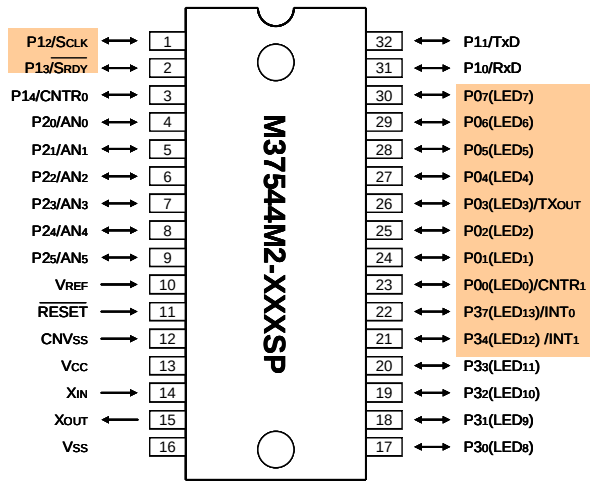


Package Type: PRDP0032BA-A (32P4B)

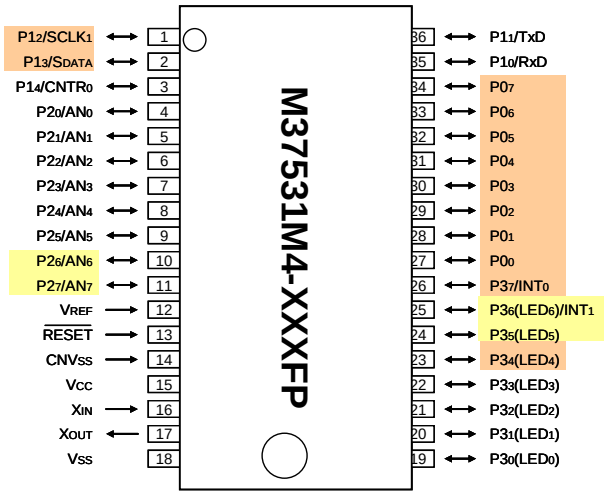


Package Type: PLQP0032GB-A (32P6U-A)

36-pin SSOP package is not available in the 7544 Group.
32-pin SDIP is compared for reference only.
The pin numbers do not match.
7544 Group/7531 Group Difference =
Reduced ports in the 7544 Group =



Package Type: PRDP0032BA-A (32P4B)



Package Type: PRSP0036GA-A (36P2R-A)

3. Interrupt Vector, ROM Code Protect Address, ID Code Storage Address

7544 Group/7531 Group

<Interrupt Vector> 7544 Group/7531 Group Difference =

Vector address		Priority	7544 Group Interrupt Source	7531 Group Interrupt Source
High-order	Low-order			
FFFD16	FFFC16	1	Reset	Reset
FFFB16	FFFA16	2	Serial I/O receive	Serial I/O1 receive
FFF916	FFF816	3	Serial I/O transmit	Serial I/O1 transmit/INT1
FFF716	FFF616	4	INT0	INT0
FFF516	FFF416	5	INT1	Timer X/Key-on wake-up
FFF316	FFF216	6	Key-on wake-up	Timer 1
FFF116	FFF016	7	CNTR0	Timer 2/Serial I/O2
FFEF16	FFEE16	8	CNTR1	CNTR0/ A/D Conversion
FFED16	FFEC16	9	Timer X	BRK Instruction
FFEB16	FFEA16	10	Reserved area	
FFE916	FFE816	11	Reserved area	
FFE716	FFE616	12	Timer A	
FFE516	FFE416	13	Reserved area	
FFE316	FFE216	14	A/D conversion	
FFE116	FFE016	15	Timer 1	
FFDF16	FFDE16	16	Reserved area	
FFDD16	FFDC16	17	BRK Instruction	

<ROM Code Protect Address>

	7544 Group	7531 Group
FFD416	**ROM code protect address (QzROM)** User ROM area (MASK) ID code storage address (One-Time PROM) (See below)	User ROM area

ROM code protect is assigned to address FFD416 in **the QzROM version of the7544 Group**. If you select write to protect bit with a serial programmer, or select programming by Renesas Technology before shipment to enable protect, 0016 is set to this address. Otherwise, FF16 is set. The address cannot be used by user programs.

<ID Code Storage Address>

	7544 Group	7531 Group
FFD416 to FFDA16	**ID code storage address (One-Time PROM)** ROM code protect address / User ROM area (QzROM) (See above) User ROM area (MASK)	User ROM area

ID codes are assigned to addresses FFD416 to FFDA16 in **the One-Time PROM version of the 7544 Group**. These are used for the ID code check function in serial write mode. If the ID code storage addresses are not blank, the ID codes sent from the serial programmer and the ID codes written to the ROM are checked to see if they match. If the codes do not match, commands sent from the programmer are not acknowledged. These addresses cannot be used by user programs.

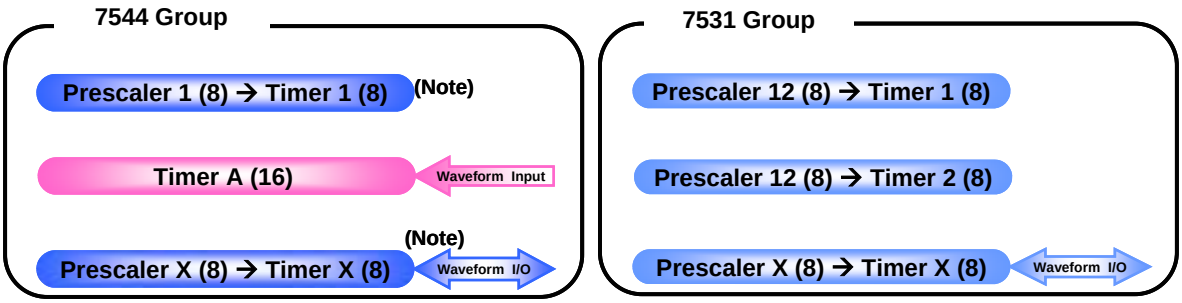
4. SFR 7544 Group/7531 Group

	7544 Group	**7531** Group
0000₁₆	Port P0 (P0)	Port P0 (P0)
0001₁₆	Port P0 direction register (P0D)	Port P0 direction register (P0D)
0002₁₆	Port P1 (P1)	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)	Port P2 (P2)
0005₁₆	Port P2 direction register (P2D)	Port P2 direction register (P2D)
0006₁₆	Port P3 (P3)	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)	Port P3 direction register (P3D)
0008₁₆	Reserved	Reserved
0009₁₆	Reserved	Reserved
000A₁₆	Reserved	Reserved
000B₁₆	Reserved	Reserved
000C₁₆	Reserved	Reserved
000D₁₆	Reserved	Reserved
000E₁₆	Reserved	Reserved
000F₁₆	Reserved	Reserved
0010₁₆	Reserved	Reserved
0011₁₆	Reserved	Reserved
0012₁₆	Reserved	Reserved
0013₁₆	Reserved	Reserved
0014₁₆	Reserved	Reserved
0015₁₆	Reserved	Reserved
0016₁₆	Pull-up control register (PULL)	Pull-up control register (PULL)
0017₁₆	Port P1P3 control register (P1P3C)	Port P1P3 control register (P1P3C)
0018₁₆	Transmit /Receive buffer register (TB/RB)	Transmit/Receive buffer register (TB/RB)
0019₁₆	Serial I/O status register (SIOSTS)	Serial I/O1 status register (SIO1STS)
001A₁₆	Serial I/O control register (SIOCON)	Serial I/O1 control register (SIO1CON)
001B₁₆	UART control register (UARTCON)	UART control register (UARTCON)
001C₁₆	Baud rate generator (BRG)	Baud rate generator (BRG)
001D₁₆	Timer A mode register (TAM)	Reserved
001E₁₆	Timer A register (low-order) (TAL)	Reserved
001F₁₆	Timer A register (high-order) (TAH)	Reserved
0020₁₆	Reserved	Reserved
0021₁₆	Reserved	Reserved
0022₁₆	Reserved	Reserved
0023₁₆	Reserved	Reserved
0024₁₆	Reserved	Reserved
0025₁₆	Reserved	Reserved
0026₁₆	Reserved	Reserved
0027₁₆	Reserved	Reserved
0028₁₆	Prescaler 1 (PRE1)	Prescaler 12 (PRE12)
0029₁₆	Timer 1 (T1)	Timer 1 (T1)
002A₁₆	Reserved	Timer 2 (T2)
002B₁₆	Timer X mode register (TXM)	Timer X mode register (TXM)
002C₁₆	Prescaler X (PREX)	Prescaler X (PREX)
002D₁₆	Timer X (TX)	Timer X (TX)
002E₁₆	Timer count source set register 1 (TCSS1)	Timer count source set register (TCSS)
002F₁₆	Timer count source set register 2 (TCSS2)	Reserved
0030₁₆	Reserved	Serial I/O2 control register (SIO2CON)
0031₁₆	Reserved	Serial I/O2 register (SIO2)
0032₁₆	Reserved	Reserved
0033₁₆	Reserved	Reserved
0034₁₆	A/D control register (ADCON)	A/D control register (ADCON)
0035₁₆	A/D register (AD)	A/D conversion register (low-order) (ADL)
0036₁₆	Reserved	A/D conversion register (high-order) (ADH)
0037₁₆	Reserved	Reserved
0038₁₆	MISRG	MISRG
0039₁₆	Watchdog timer control register (WDTCON)	Watchdog timer control register (WDTCON)
003A₁₆	Interrupt edge selection register (INTEDGE)	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1 (IREQ1)	Interrupt request register 1 (IREQ1)
003D₁₆	Interrupt request register 2 (IREQ2)	Reserved
003E₁₆	Interrupt control register 1 (ICON1)	Interrupt control register 1 (ICON1)
003F₁₆	Interrupt control register 2 (ICON2)	Reserved

: Changed function
: New SFR
: Reduced in 7544 Group

Note: Do not access to the SFR reserved areas.

5. Timer Composition 7544 Group/7531 Group



8-bit timer 1 and timer X are common to both of the Groups. (Note)

The 7544 Group has 16-bit timer A, but no 8-bit timer 2.

Note: Added Functions to timer 1 and timer X of the 7544 Group

The following functions are added to timer 1 and timer X of the 7544 Group to enhance usability.

Timer	7544 Group	7531 Group
Timer 1 (Prescaler 1)	Count source f(XIN)/16, f(XIN)/2, or on-chip oscillator output selectable	Count source f(XIN)/16 fixed
Timer X	-Write to latch and timer simultaneously or write to latch only selectable - Timer output (TXOUT: CNTR0 inverted output) - f(XIN) is added for count source	Write to latch and timer simultaneously only

6. Notes on Replacement

1. The A/D converter of the 7544 Group has an 8-bit resolution. The characteristics of the A/D converter vary between the 7544 Group and 7531 Group. Careful evaluation with ES samples or CS samples is recommended before mass-production.

2. To add timer A and count source select functions in the 7544 Group, registers are added as indicated below. When additional functions are not used, handle the registers as follows.

(1) When timer A is not used

Set the timer A count stop bit (bit 7) in the timer A mode register to 1 to stop timer A.

By stopping timer A, power consumption can be reduced.

(2) Setting the same count source for timer 1 as the 7531 Group

Keep the initial value for timer 1 count source selection bits (bits 0 and 1), or set them to the same value of 00 (f(XIN)/16 select)

Address	7544 Group	7531 Group
$1D_{16}$	Timer A mode register (TAM)	(Blank)
$1E_{16}$	Timer A register (low-order) (TAL)	(Blank)
$1F_{16}$	Timer A register (high-order) (TAH)	(Blank)
$2F_{16}$	Timer count source set register (TCSS2)	(Blank)

3. Interrupt sources and interrupt vector addresses are added to the 7544 Group with additional registers as indicated below. The bits in interrupt request register 1 and interrupt control register 1 are also changed. (Refer to 4. on the following page.)
The interrupt request bits, interrupt control bits, and vector addresses are changed even though the functions are the same as those of with the 7531 Group.

Address	7544 Group	7531 Group
$3D_{16}$	Interrupt request register 2 (IREQ2)	(Blank)
$3F_{16}$	Interrupt request register 2 (IREQ2)	(Blank)

4. The bits in the following registers of the 7544 Group are functionally changed for expanded or reduced functions.

Address (Register Name)	Bit	7544 Group	7531 Group
16_{16} (Pull-up control register)	Bit 6	Disable	$P3_5$, $P3_6$ pull-up control bit
17_{16} (Port P1P3 control register)	Bit 1	$P3_4$/INT_1 input level selection bit	$P3_6$/INT_1 input level selection bit
	Bit 2	$P1_0$, $P1_2$ input level selection bit	$P1_0$, $P1_2$, $P1_3$ input level selection bit
$1A_{16}$ (Serial I/O control register)	Bit 1	Serial I/O synchronous clock selection bit	Disable (returns 1 when read)
	Bit 2	S_{RDY} output enable bit	Continuous transmit enable bit
	Bit 6	Serial I/O mode selection bit	Serial I/O1 enable bit (low-order)
	Bit 7	Serial I/O enable bit	Serial I/O1 enable bit (high-order)
$2B_{16}$ (Timer X mode register)	Bit 4	$P0_3$/TX_{OUT} output enable bit	Disable (returns 0 when read)
	Bit 5	Timer X write control bit	Disable (returns 0 when read)
$2E_{16}$ (Timer count source set register)	Bit 0	Timer X count source selection bit	Timer X count source selection bit
	Bit 1	Timer X count source selection bit	Disable (returns 0 when read)
38_{16} (MISRG)	Bit 1	Ceramic/crystal or RC oscillation stop detection enable bit	Reserved bit 0
	Bit 7	Oscillation stop detection status bit	Disable (returns 0 when read)
$3A_{16}$ (Interrupt edge selection register)	Bit 4	Disable (returns 0 when read)	Serial I/O1 or INT1 interrupt selection bit
	Bit 5	Disable (returns 0 when read)	Timer X or key-on wakeup interrupt selection bit
	Bit 6	Disable (returns 0 when read)	Timer 2 or serial I/O2 interrupt selection bit
	Bit 7	P00 key-on wakeup selection bit	CNTR0 or A/D conversion interrupt selection bit
$3B_{16}$ (CPU mode register)	Bit 3	On-chip oscillator control bit	Disable (returns 0 when read)
	Bit 4	XIN oscillation control bit	Disable (returns 0 when read)
$3C_{16}$ (Interrupt request register 1)	Bit 1	Serial I/O transmit interrupt request bit	Serial I/O1 transmit or INT1 interrupt request bit
	Bit 3	INT1 interrupt request bit	Timer X or key-on wakeup interrupt request bit
	Bit 4	Key-on wakeup interrupt request bit	Timer 1 interrupt request bit
	Bit 5	CNTR0 interrupt request bit	Timer 2 or serial I/O2 interrupt request bit
	Bit 6	CNTR1 interrupt request bit	CNTR0 or A/D conversion interrupt request bit
	Bit7	Timer X interrupt request bit	Disable (returns 0 when read)
$3E_{16}$ (Interrupt control register 1)	Bit 1	Serial I/O transmit interrupt enable bit	Serial I/O1 transmit or INT1 interrupt enable bit
	Bit 3	INT1 interrupt enable bit	Timer X or key-on wakeup enable bit
	Bit 4	Key-on wakeup interrupt enable bit	Timer 1 interrupt enable bit
	Bit 5	CNTR0 interrupt enable bit	Timer 2 or serial I/O2 interrupt enable bit
	Bit 6	CNTR1 interrupt enable bit	CNTR0 or A/D conversion interrupt enable bit
	Bit 7	Timer X interrupt enable Bit	Disable (returns 0 when read)

5. The following registers are reduced in the 7544 Group for reduced functions.
Do not access to the addresses indicated below.

Address	7544 Group	7531 Group
$2A_{16}$	Reserved	Timer 2
30_{16}	Reserved	Serial I/O2 control register
31_{16}	Reserved	Serial I/O2 register
36_{16}	Reserved	A/D conversion high-order register

6. ROM code protect is assigned to address FFD4$_{16}$ in the QzROM version of the7544 Group. If you select write to protect bit with a serial programmer, or select programming by Renesas Technology before shipment to enable protect, 00$_{16}$ is set to this address. Otherwise, FF$_{16}$ is set. The address cannot be used by user programs.

7. ID codes are stored at addresses FFD4$_{16}$ to FFDA$_{16}$ in the One-Time PROM version of the 7544 Group. These are used for the ID code check function in serial write mode. If the ID code storage addresses are not blank, the ID codes sent from the serial programmer and the ID codes written to the ROM are checked to see if they match. If the codes do not match, commands sent from the programmer are not acknowledged. These addresses cannot be used by user programs.

8. The power source voltage of the 7544 Group is 4.0 to 5.5 V for the MASK version and the One-Time PROM version, and 1.8 to 5.5 V for the QzROM version. This differs from the power source voltage of the 7531 Group (2.2 to 5.5 V).

9. Applicable programmers differ among the One-Time PROM of the 7531 Group, the One-Time PROM of the 7544 Group, and the QzROM of the 7544 Group. Check the Development Environment Guide on the 7544 Group page of the Renesas Technology website for information on suitable programmers for the 7544 Group.
   On-board programming is also available in the QzROM version of the 7544 Group.
   Check the programmer manual for information on how to set pins for on-board programming.
   Instructions on setting the pins of the Renesas FDT + E8 + IC socket board for on-board programming are contained in "***On- Board Programming for QzROM/FLASH with E8***". To locate this document by searching by keyword on the Renesas Technology website, enter the document number "rej99b1146" in the search box.

10. Although the 7544 Group has been designed with full consideration given to compatibility of characteristics, operation margins, noise immunity, noise radiation, etc., may vary. Careful evaluation with ES or CS samples is recommended before mass-production using the 7544 Group.

11. For details of absolute maximum ratings, electrical characteristics, and operating conditions, refer to the datasheet of the product in question. The XIN-XOUT oscillation circuit constants may vary depending on the product. Contact the oscillator manufacturer to select an appropriate oscillator and oscillation circuit constants so that the product used for mass production will obtain a stable operating clock with your systems and conditions. Additional care is required when the voltage range or temperature range is wide. Also, we recommend considering the wiring patterns of the feedback resistors, the damping resistors, and the load capacity beforehand when designing circuits.

7. Reference Document

Data Sheet
7544 Group Data sheet
7531 Group Data sheet

User's Manual
7531 Group User's Manual
(Use the most recent version of the document on the Renesas Technology website)

Technical News/Technical Update
(Use the most recent version of the document on the Renesas Technology website)

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REVISION HISTORY	Differences between 7544 Group and 7531 Group

Rev.	Date	Description	
		Page	Summary
1.00	Jun.13.06	—	First edition issued

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