To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

H8/300L

Detailed Usage of ADC (ADC)

Introduction

Digital systems are increasingly used in almost all applications (domestic appliances, measurement and control). The variables measured (temperature, pressure and light intensity) by the sensors are analog (continuous value). Analog-to-digital converters (ADC) are used to convert these measured signals into digital representation so that they can be processed by microprocessors/microcontrollers.

This document focuses on the built-in ADC of the SLP MCU. Generally, the usage of ADC is based on these four factors:

- Number of channels
- Resolution
- Conversion time
- Error rate

The following topics are covered in this application note:

- General ADC configuration and characteristics
- Characteristics of SLP ADC module
- Design guidelines for ADC interfacing
- Application of ADC
- A step-by-step guide of designing a signal conditioning circuit to the ADC

Target Device

SLP Series 38024

Contents

1. ADC Overview

Figure 1 shows the block diagram of an ADC.

- An appropriate sensor/transducer is required to convert the physical parameter (e.g. temperature, pressure, flow-rate, etc) into an electrical voltage or current.
- If the output of the sensor/transducer is in the milli-volt range, amplification is required to condition it to a usable range.
- The active filter will remove undesired signals.
- The sample-and-hold block samples the analog input voltage and then holds this voltage at its output for conversion by the ADC.
- The ADC block operates on the sampled signal and converts it to a N-bit digital code. A reference range is divided into 2^N different levels. The N-bit output code corresponds to the reference level closest to the sampled signal.

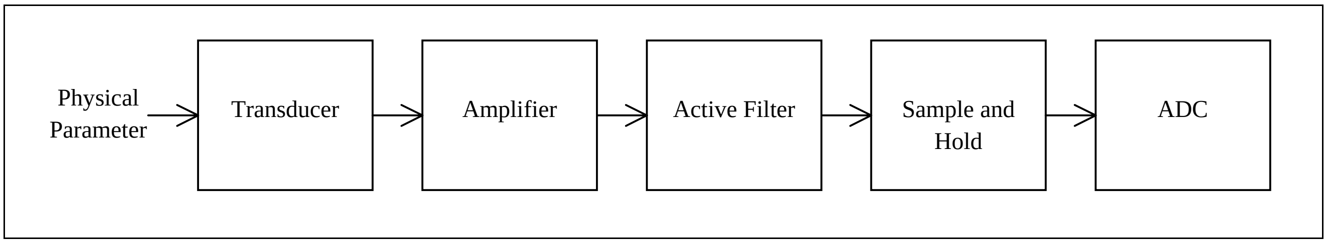


Figure 1 ADC Block Diagram

Figure 2 shows the practical ideal transfer function of a 3-bit ADC, where the analog input within a certain range is represented by a limited number of digital output codes. The resolution of an ADC is expressed as the number of bits of its output code. For example, an ADC with an N-bit resolution has 2^N possible digital codes. The full-scale range is divided into 2^N – 1 step widths (first and last steps are only ½ step width) where each step width is defined as follows:

$$1 \text{ step width} = 1 \text{ LSB} = \frac{FSR}{2^n - 1}$$

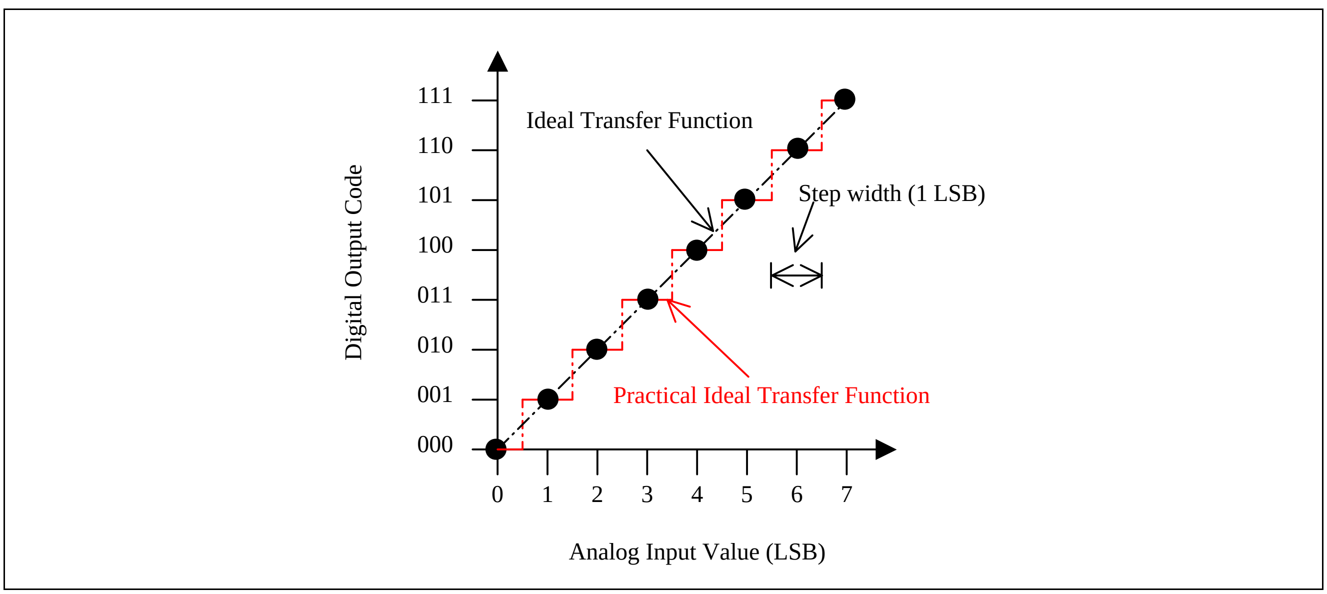


Figure 2 ADC Transfer Function

2. Sampling Theorem

The continuous analog data must be sampled at discrete intervals (t_s), which must be carefully selected to ensure an accurate representation of the original signal. If more samples (higher sampling rates) are taken, the digital representation will be more accurate. If fewer samples are taken, a critical point is reached where the signal information is lost.

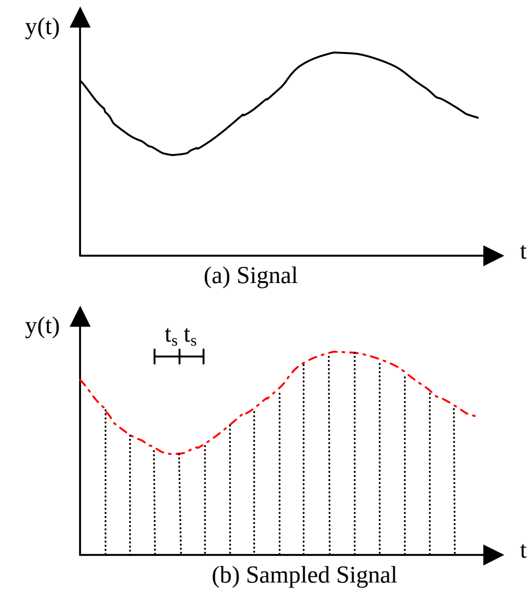


Figure 3 Sampling

The Shannon Sampling Theorem states that the original signal may be recovered without distortion if the input spectrum does not contain frequency components higher than $f_s/2$ (Nyquist frequency). Note that sampling the analog signal f_a at a sampling rate f_s produces alias frequency components $n(f_s - f_a)$ and $n(f_s + f_a)$ where n = 1, 2, 3, …. Referring to Figure 4, problems occur when the input signal exceeds the Nyquist bandwidth ($f_s/2$). An anti-aliasing filter has to be inserted to prevent unwanted in-band aliasing.

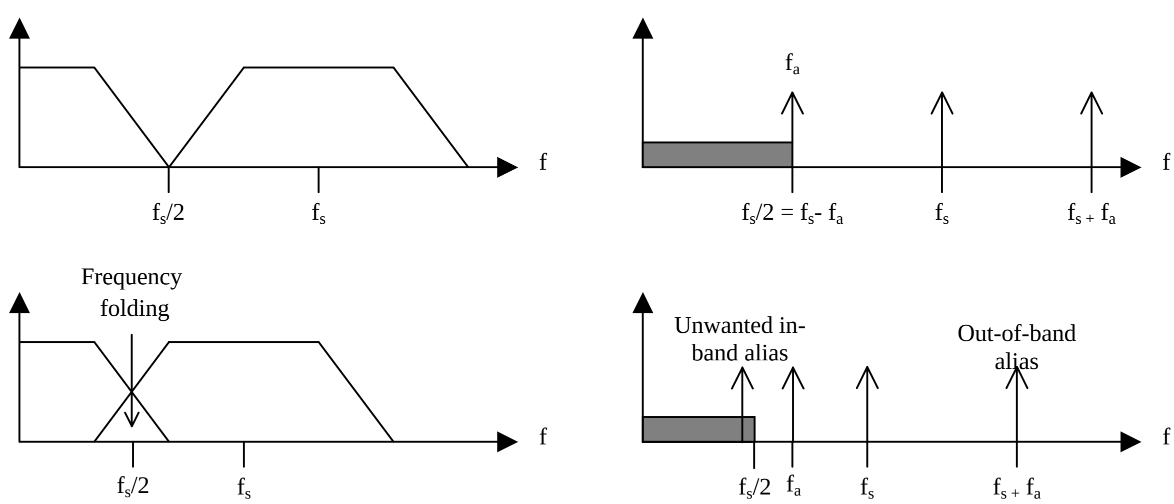


Figure 4 Aliasing Effects in Frequency Domain

For example, the reasons for setting the sampling frequency of audio CDs at 44.1kHz are as follows:

- The frequency range for sound is from 20Hz to 20kHz.
- Maximum input frequency, f_a = 20kHz.
- Minimum sampling frequency, $f_s \geq 2f_a$ = 40kHz
- The sampling frequency is set at $1.1f_s$ (44kHz) to compensate for the roll-off from pass-band to stop-band (Figure 5).
- Around 1982, only VCRs are capable of storing such high rates. The relevant television standards are:
    - NTSC: 490 lines/frame, 3 samples/line, 30 frames/s → 44100 samples/s
    - PAL: 588 lines/frame, 3 samples/line, 25 frames/s → 44100 samples/s

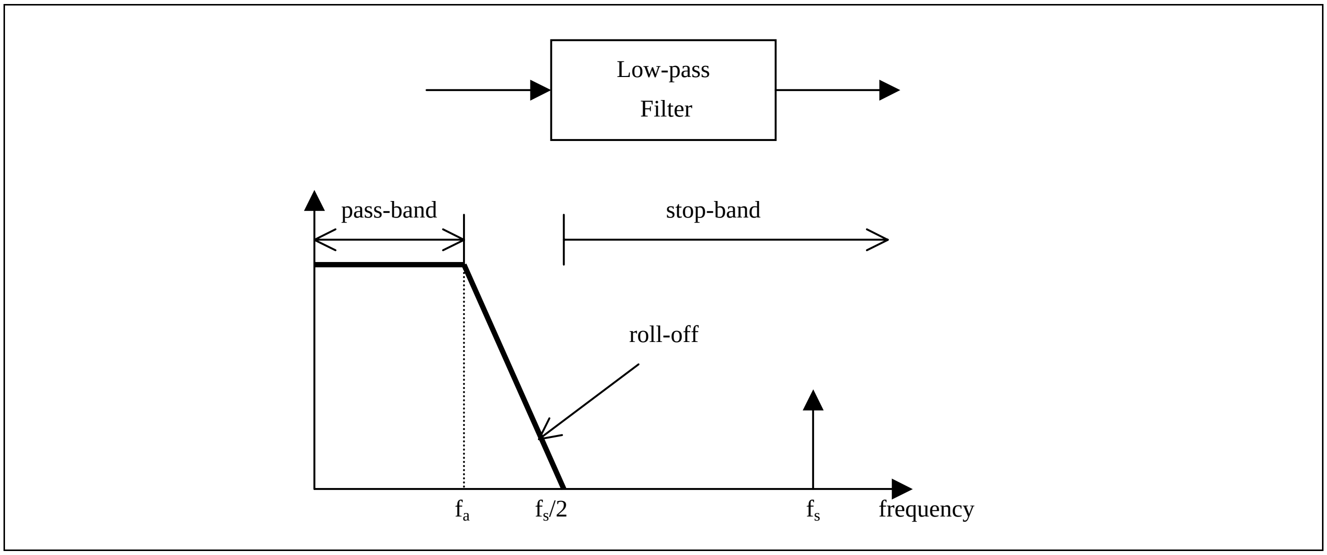


Figure 5 Low-pass Filter

3. ADC Errors

The errors affecting the ADC accuracy are as follows:

- Quantization Error
- Differential Nonlinearity (DNL) Error
- Integral Nonlinearity (INL) Error

The absolute error is defined as the maximum deviation from an actual transition versus an ideal transition for any code and it includes the sum of all error contributions listed above.

3.1 Quantization Error

The analog input to an ADC is a continuous signal with an infinite number of possible states, whereas its output is a finite number of discrete digital levels. During the conversion from analog to digital format, certain parts of the analog signal with different input levels are represented by the same digital output code. Quantization error refers to the difference between the actual analog value and the digital representation of that value. It is ±½LSb and is inherent in the ADC process. Refer to Figure 6.

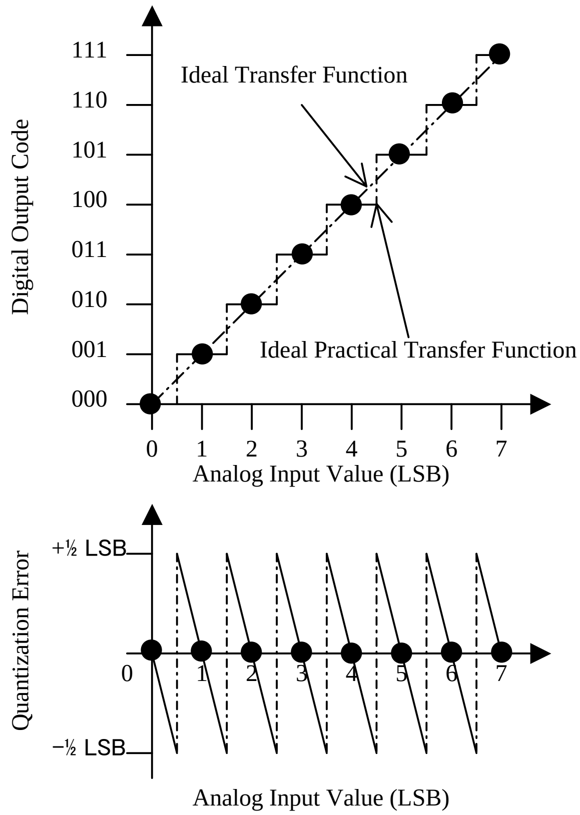


Figure 6 Quantization Error

The only way to reduce quantization error is to use a higher-resolution ADC. For example,

- Full-scale range of the converter is 5V and the resolution is 10 bits.
  1 LSB = $5V/2^{10}$ = 4.883mV
  Quantization error = ±0.5 × 4.883mV = ±2.442mV

- Full-scale range of the converter is 5V and the resolution is 12 bits.
  1 LSB = $5V/2^{12}$ = 1.221mV
  Quantization error = ±0.5 × 1.221mV = ±0.611mV

3.2 Differential Nonlinearity Error

In Figure 7, the DNL error is the difference between an actual step width and the ideal value of 1 LSB. If the step width is exactly 1 LSB, then the DNL error is 0. If the DNL exceeds 1 LSB, the magnitude of the output gets smaller for an increase in the input magnitude. It is also possible to have missing codes i.e., one or more of the possible 2^n binary codes are never output.

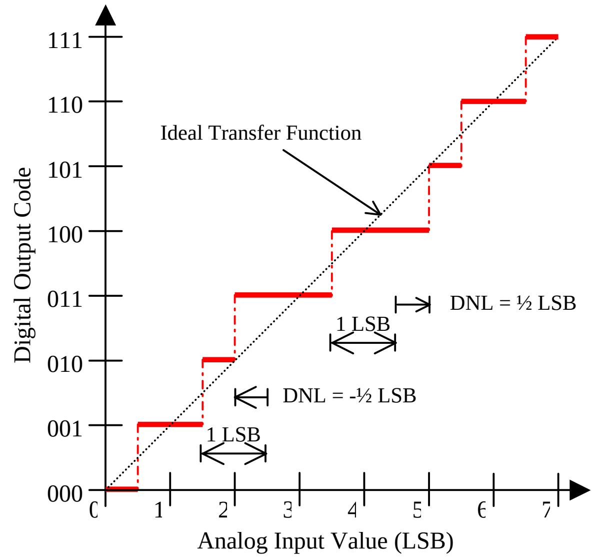


Figure 7 DNL Error

3.3 Integral Nonlinearity Error

The deviation of the values on the actual transfer function from the ideal straight line is known as the INL error as shown in Figure 8. The deviations are measured at the transitions from one step to the next.

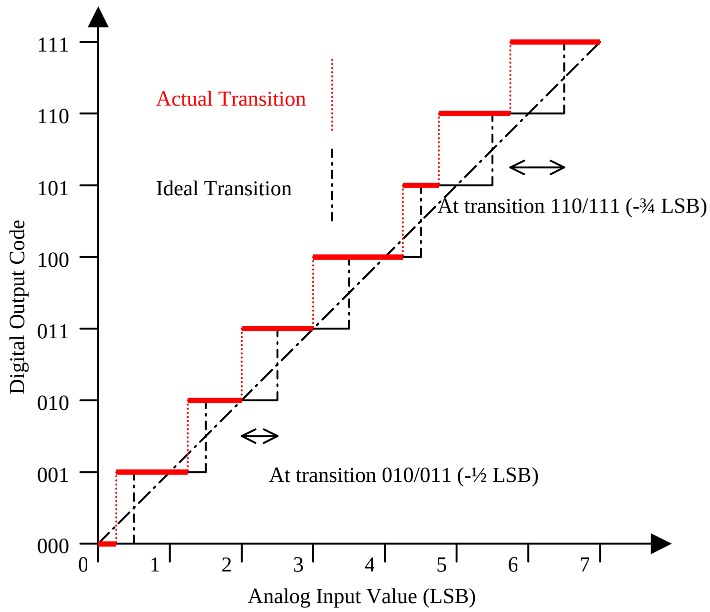


Figure 8 INL Error

4. Features of SLP ADC

The H8/38024 SLP series includes an on-chip resistance-ladder-based successive-approximation ADC. Figure 9 shows the block diagram of the ADC for the SLP MCU. The ADC features are as follows:

- Eight input channels of 10-bit resolution each
- Conversion time: 12.4µs (min) at 5MHz operation, 124µs (max)
- Built-in sample-and-hold function
- Interrupt requested on completion of ADC
- ADC can be started by external trigger input
- Use of module standby mode enables this module to be placed in standby mode independently when not used

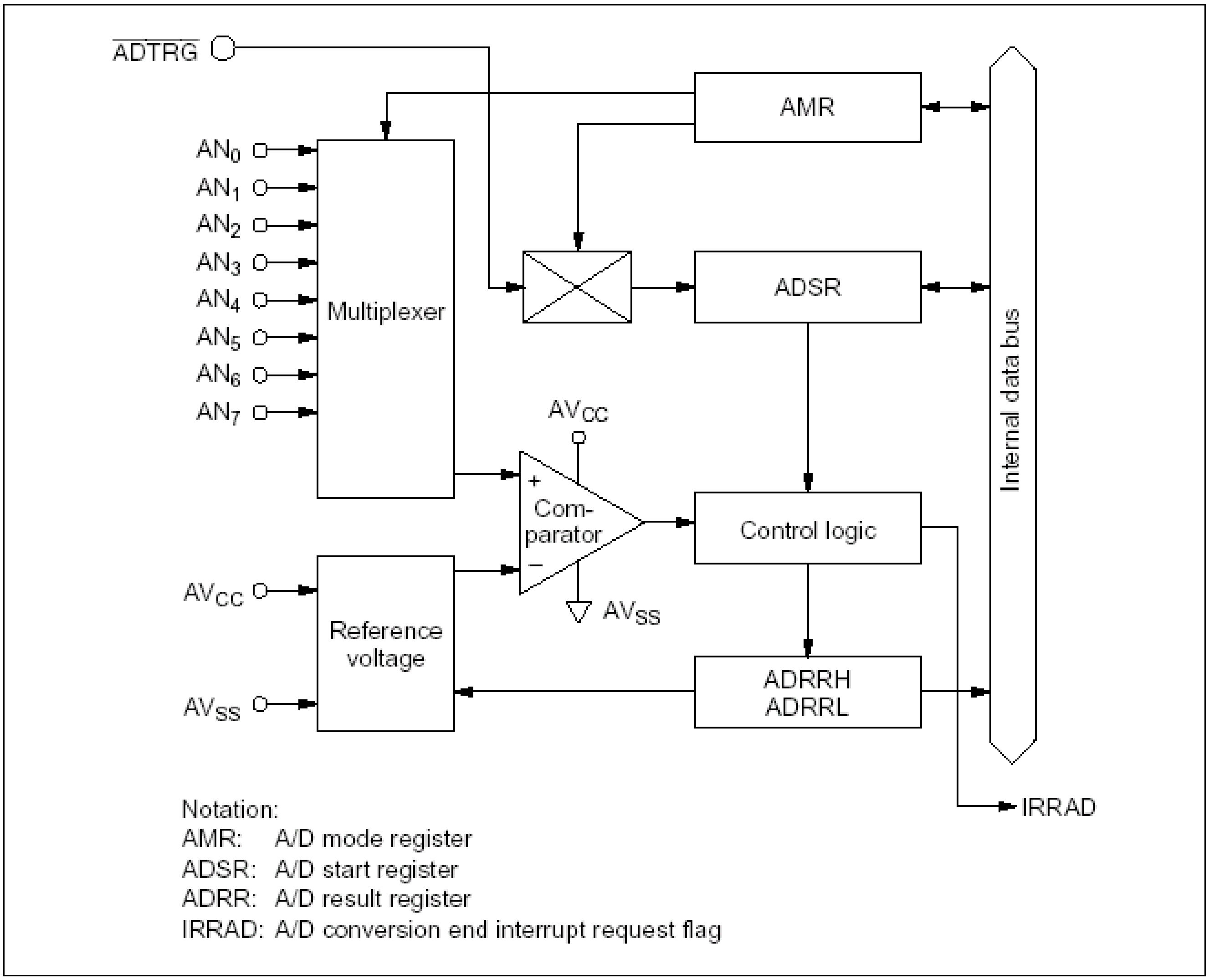


Figure 9 Block Diagram of ADC

The characteristics of the ADC are summarized in Table 1.

Table 1 SLP ADC Characteristics

Item	Values		Unit	Test Conditions
	Min	Max		
Resolution	—	10	Bit	—
Quantization Error	—	±0.5	LSB	—
Nonlinearity Error	—	±2.5	LSB	AV_{cc} = 2.7V to 5.5V V_{cc} = 2.7V to 5.5V
	—	±5.5		AV_{cc} = 2.0V to 5.5V V_{cc} = 2.0V to 5.5V
	—	±7.5		Other than the above at 62µs conversion time
Absolute Accuracy	—	±3.0	LSB	AV_{cc} = 2.7V to 5.5V V_{cc} = 2.7V to 5.5V
	—	±6.0		AV_{cc} = 2.0V to 5.5V V_{cc} = 2.0V to 5.5V
	—	±8.0		Other than the above at 62µs conversion time
Conversion Time	12.4	124	µs	AV_{cc} = 2.7V to 5.5V V_{cc} = 2.7V to 5.5V
	62	124		Except the above
Analog input capacitance (C_{AIN})	—	15.0	pF	—
Allowable signal source impedance (R_{AIN})	—	10.0	kΩ	—

4.1 Design Guidelines

The following guidelines should be followed in mixed-signal designs:

- Keep all Power and Ground traces short and wide to limit resistance and inductance.

- A simple method for controlling noise is to have separate supplies for the (i) slower low-current analog functions and (ii) faster medium-power digital functions as shown in Figure 10.
  - The ferrite beads together with the bypass capacitors form a low-pass filter network, reducing the high-frequency noise. It resists varying current and also provides a low-impedance AC short to ground on either side.
  - Select a ferrite bead designed for the noise frequency range.
  - For broadband high-frequency noise, two or more capacitors in parallel are often required to filter out all the high frequency noise components. The bypass capacitors also provide an immediate local supply of energy for transient power supply demands.

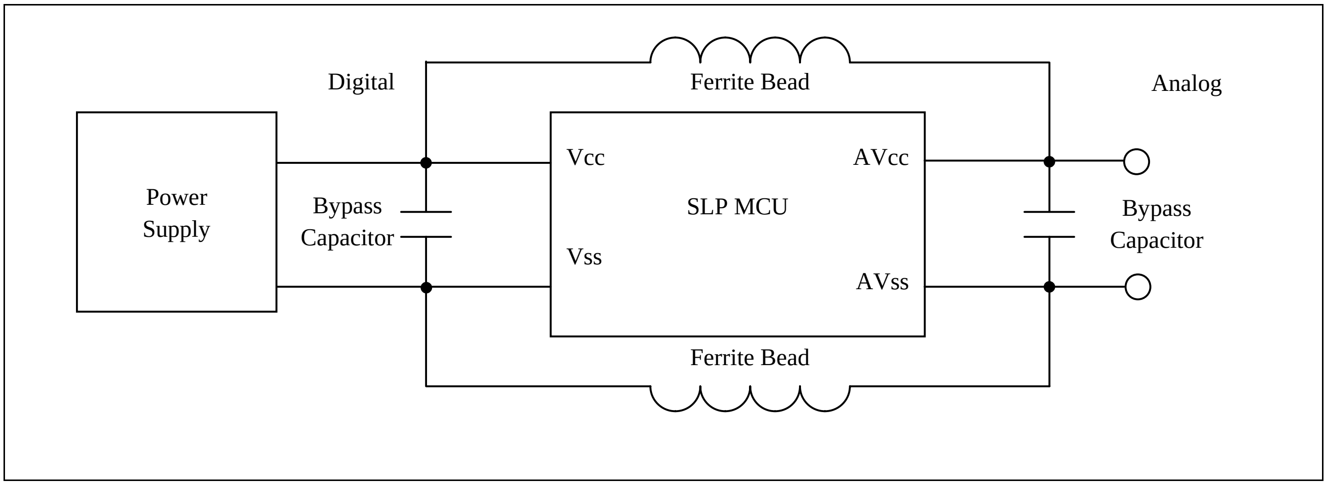
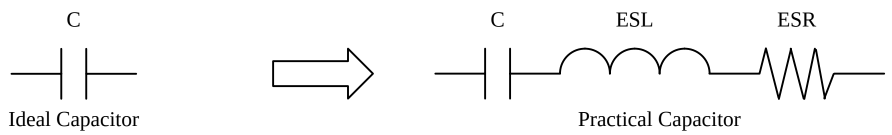


Figure 10 Split Supplies

- Figure 11 shows the equivalent circuit of a capacitor. The frequency response of the practical capacitor is as follows:
  - At low frequency, the impedance is capacitive.
  - At self-resonant frequency (SRF), the capacitive and inductive reactances cancel each other, leaving only a resistive component. It is the upper frequency limit of the capacitor and is defined as

$$f_o = \frac{1}{2\Pi\sqrt{ESL \bullet C}}$$

  - Beyond the SRF, the inductive reactance takes over.



1. Equivalent Series Resistance (ESR)
2. Equivalent Series Inductance (ESL)

Figure 11 Equivalent Circuit of a Capacitor

Table 2 Impedance of Capacitor

Frequency	Low	SRF	High
Impedance	Capacitive	Resistive	Inductive

The addition of resistive/inductive component between the capacitor and device increases the parasitic inductance and resistance, thereby reducing the effectiveness of the capacitor. Therefore, all bypass capacitors must be mounted as close as possible to their devices. The traces connecting the capacitor to the device must be kept short and wide to minimize any stray impedance that may interfere with the energy transfer between the capacitor and device. Table 3 lists a comparison of commonly used capacitors [5].

Table 3 Comparison of Capacitors

Type	Advantages	Disadvantages
Chip multi-layer ceramic (NPO)	Wide range of values Low inductance Small case size Good stability Inexpensive	Limited to small values
Aluminum Electrolytic	Large values High currents High voltages Small size	High leakage Usually polarized Poor stability Poor accuracy Inductive
Tantalum Electrolytic	Large values Small size Medium inductance	Moderate leakage Usually polarized Poor stability Poor accuracy Expensive

- Sensor signals are especially susceptible to ground noises due to their low level outputs and high output impedance (little power). Since sensors usually do not possess drive capability to overpower even the lowest levels of introduced noise, it is always better to prevent the introduction of noise:
  - — Use a short/wide common ground between the sensor and receiver (ADC or amplifier).
  - — Limit the ground connection to the sensor at the receiver only as shown in Figure 12.
  - — Isolate the sensor, connections, input filter and receiver from high-power and fast rise-time circuits.
  - — Introduce a low-pass filter on all analog sensor inputs to the ADC.

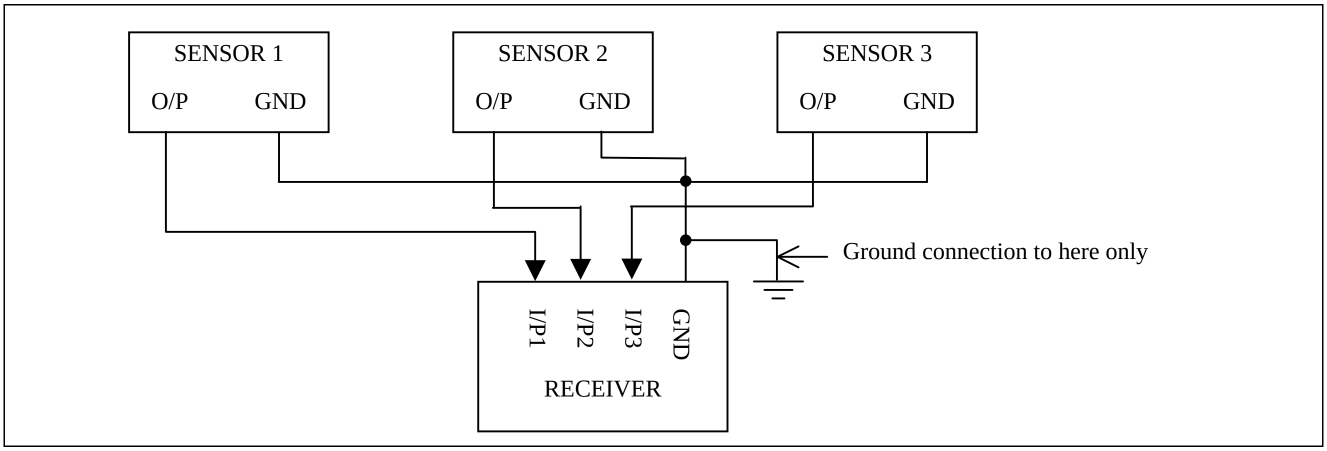


Figure 12 Sensor Ground Connections

- The maximum allowable signal impedance is 10kΩ. If the output impedance of the sensor exceeds 10kΩ, the input capacitance of the ADC sample-and-hold circuitry will not be charged sufficiently to ensure ADC precision. Figure 13 shows the equivalent ADC circuitry for the SLP MCU. If the external capacitance is large, the input load is effectively the internal 10kΩ input impedance. As a result of this low-pass filter effect, high-speed analog signals may not be reproduced correctly.

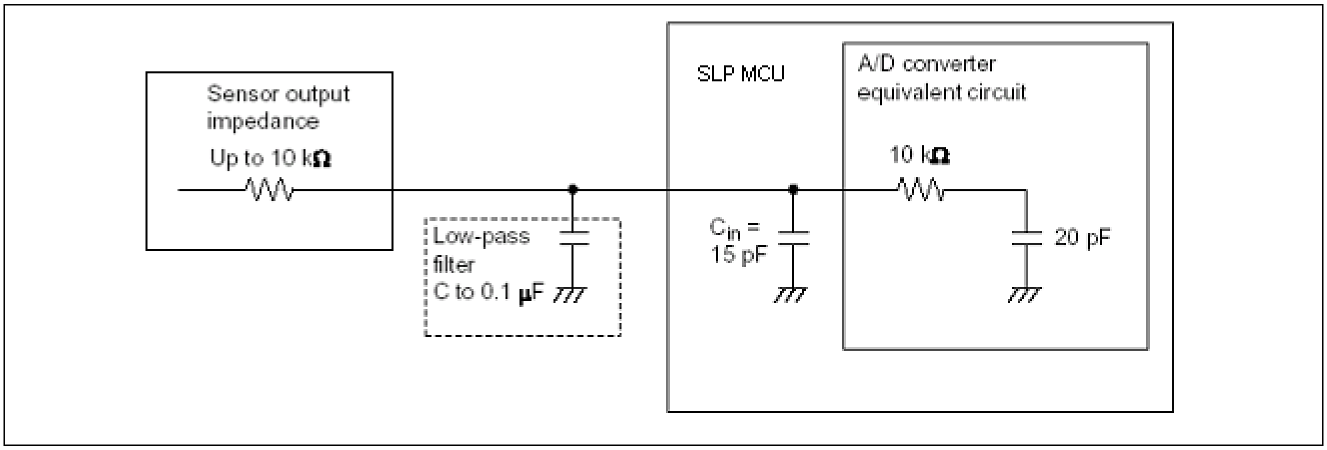


Figure 13 ADC Equivalent Circuit

- A low-impedance buffer should be inserted when converting a high-speed analog signal as shown in Figure 14. The buffer provides a high-impedance for the sensor and a low-impedance drive for the ADC.

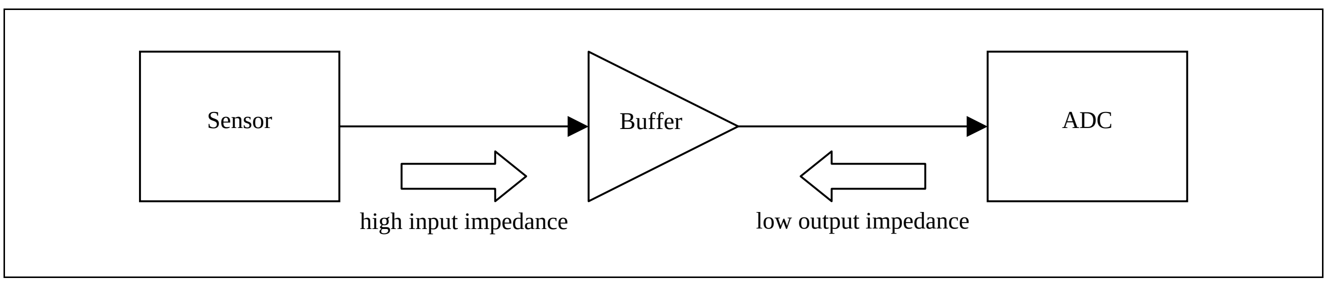
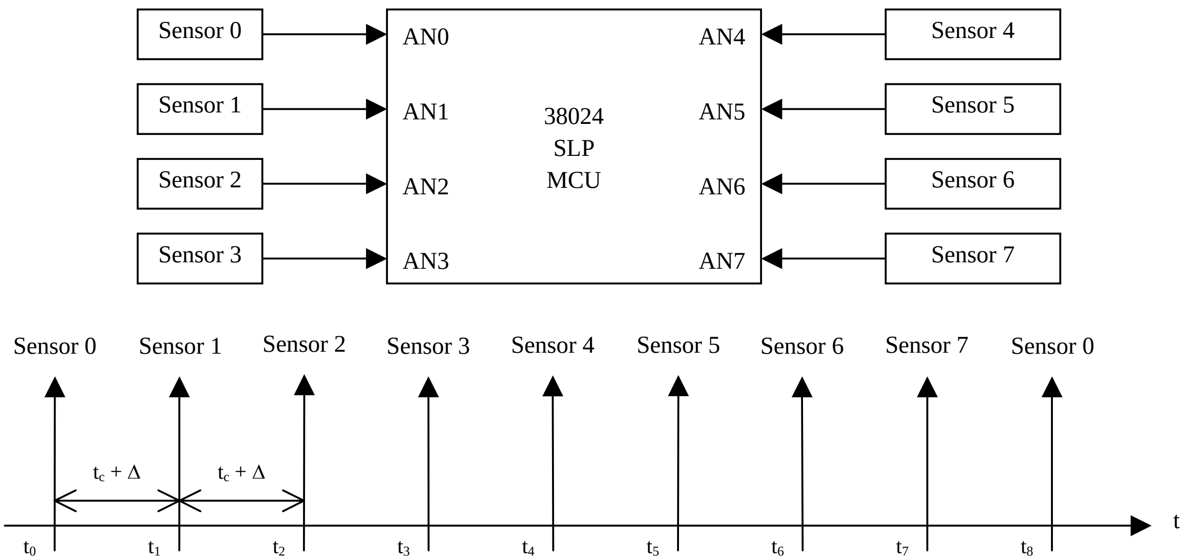


Figure 14 Signal Isolation

4.2 Application Example

In this example, eight different sensors are connected to the eight analog inputs (AN0 to AN7) of the 38024 SLP MCU as shown in Figure 15. The oscillator frequency is 10MHz and conversion time is set at 12.4µs. Due to the internal ADC structure, only one channel can be converted at a time.



1. t_c = conversion time = 12.4µs
2. Δ = processing time

Figure 15 Application Example

Table 4 shows an assembly language program segment for the conversion of AN0.

Table 4 Assembly Language Listing

Address (hexadecimal)	Assembler	Comments	Number of States
400	BSET #4, @H'FFFA	Clear ADC module standby mode	8
404	MOV.B #H'34, R0L	Set ADC speed to 62/Φ and select AN0	2
406	MOV.B R0L, @H'FFC6		4
408	BCLR #6, @FFF4	Disable ADC end interrupt	8
40C	BCLR #7, @FFC7	Start ADC	8
410	BTST #7, @H'FFC7	Read ADSR	6
414	BNE @H'410	Check for ADSF = 0	4
416	MOV.B @H'FFC4, R1H	Read ADRRH	4
418	MOV.B @H'FFC5 R1L	Read ADRRL	4

The flowchart of the above program segment is shown in Figure 16. Software polling is used to convert the sensor input at ANO. The codes described only involve the reading of the ADC result. As such, it applies to the capturing of analog input data and excludes further processing.

Time taken for ADC conversion and processing time is

$$t_c + \Delta = 12.4\mu s + \frac{(8+2+4+8+8+6+4+4+4)}{5MHz} = 22\mu s$$

The sampling frequency (f_s) is

$$f_s = \frac{1}{8 \times 22\mu s} = 5.682kHz$$

Applying Shannon's Sampling Theorem, the maximum signal frequency (f_a) that can be measured is

$$f_s \geq 2f_a$$

$$f_a \leq \frac{5.682kHz}{2} = 2.841kHz$$

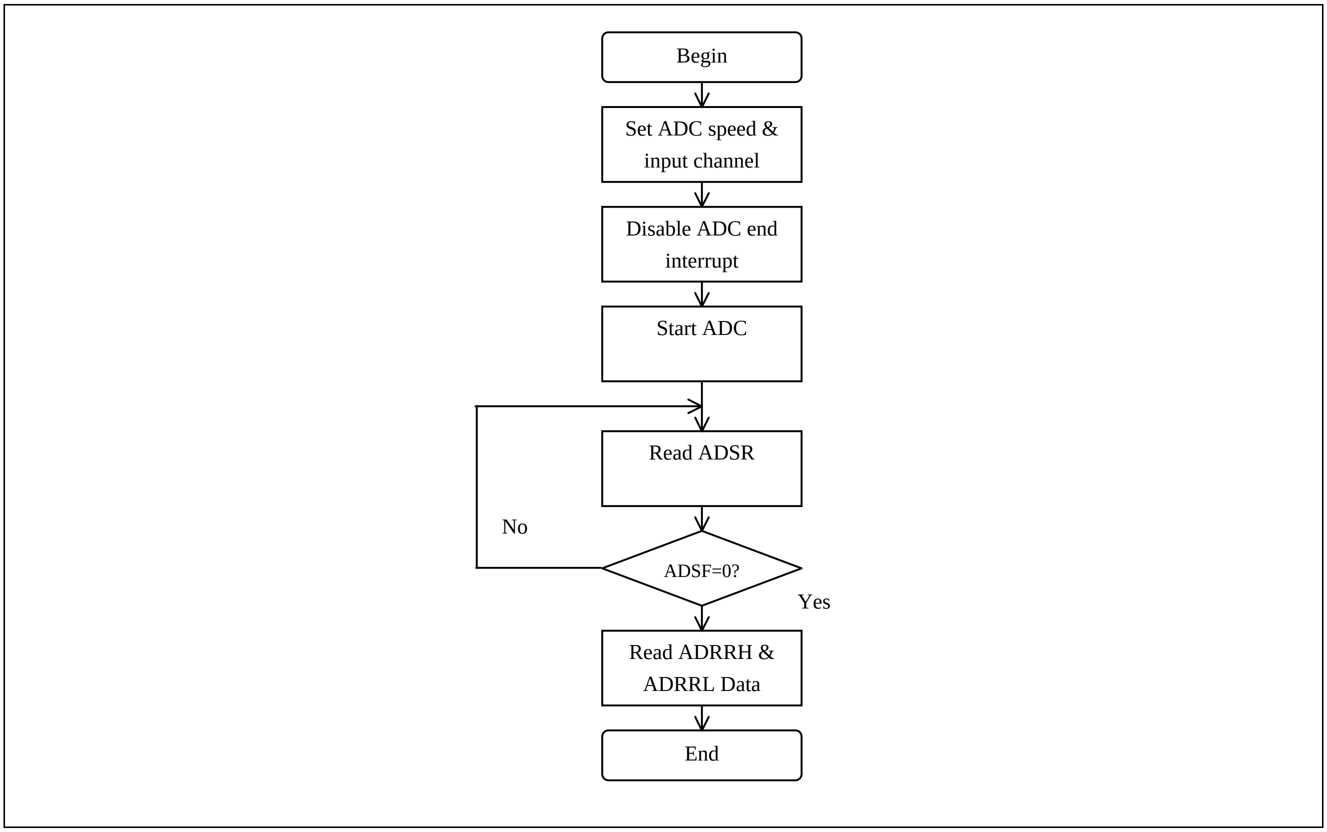


Figure 16 Flowchart

If only one sensor is used, the sampling frequency (f_s) is

$$f_s = \frac{1}{22\mu s} = 45.455kHz$$

Applying Shannon's Sampling Theorem, the maximum signal frequency (f_a) that can be measured is

$$f_a \leq \frac{45.455kHz}{2} = 22.728kHz$$

In this case, the MCU will be able to track an analog signal with rate of change greater than 22µs.

5. Signal Conditioning

In this section, the amplifier described in [2] is referred. Since the outputs of many sensors are in the milli-volt range, amplification is required to condition the output voltage to a usable range before they are fed into the input of an ADC. Refer to Figure 17. This 3-stage amplifier can be used on low-level differential-output sensors. The functions of the potentiometers in this circuit are:

- RG adjusts the gain either to calibrate or to quickly change the span for an application. Span refers to the difference between the output of the sensor at full-scale and zero.
- RU positions the positive offset at the desired level. For example, if the offset after the application of a desired amount of gain is 0.25V and the desired offset is 0.5V, then VU of 0.25V is necessary. VU only provides a positive offset shift. Adjusting RU sets VU to the desired level.
- RD positions the negative offset at the desired level. For example, if the offset after the application of a desired amount of gain is 1.0V and the desired offset is 0.5V, then VD of 0.5V is necessary. VD only provides a positive offset shift. Adjusting RD sets VD to the desired level.

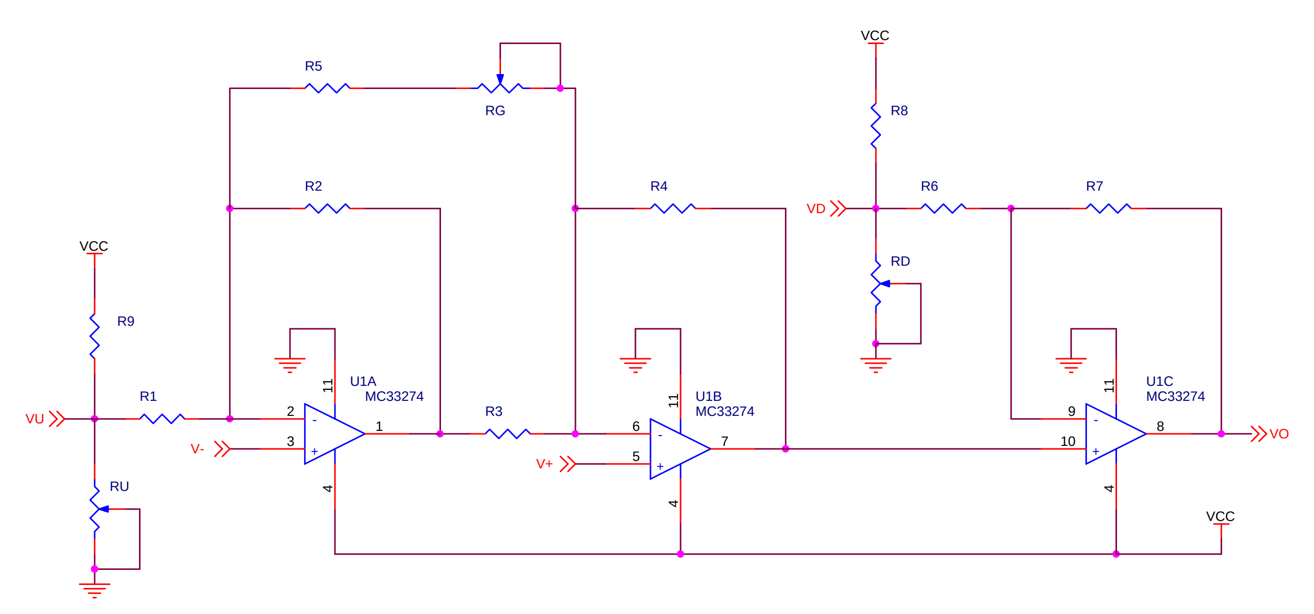


Figure 17 Amplifier

By setting R4 = R1, and R2 = R3, the output of the amplifier (pin 8 of U1C) shown in Figure 17 is:

$$VO = \left(1+\frac{R7}{R6}\right)\bullet\left\{\left(1+\frac{R4}{R3}+\frac{2\bullet R4}{R5+RG}\right)\bullet[(V+)-(V-)]+VU\right\}-\frac{R7}{R6}\bullet VD$$

The output at the second stage (pin 7 of U1B) is

$$VO = \left\{\left(1+\frac{R4}{R3}+\frac{2\bullet R4}{R5+RG}\right)\bullet[(V+)-(V-)]+VU\right\}$$

In general, the ratio of R4 to R3 should equal the ratio of R1 to R2. For simplification, Set R4 = R1 and R3 = R2. R3 and R2 should be in the order of tens to hundreds of ohms. The effective parallel resistance of the voltage dividers for VU and VD should be at least an order of magnitude smaller than R1 and R2, and the sum of R6 and R7 respectively. Using high feedback resistors greater than 10kΩ for U1B and U1C maximizes the dynamic range of the amplifier by allowing the outputs to saturate closer to the supply rails.

The procedures to design the 3-stage sensor amplifier are as follows:

- **Step 1**. **Obtain the maximum and minimum offset values and spans from the sensor's data specifications**. In this example, the sensor used is the Motorola MPX10 10kPa Uncompensated Silicon Pressure Sensor. Based on an excitation voltage of 3V, the specifications are as follows:

Table 5 Sensor Specifications

Parameter	Minimum (mV)	Maximum (mV)
Span	20	50
Offset	0	35

- **Step 2**. **Consider ratio-metric outputs**. The data specifications indicate the minimum and maximum span and offset for an excitation voltage of 3V. The output of many sensors is ratio-metric to the supply excitation voltage i.e., the following formula can be applied to scale the output for the actual supply voltage:

$$V_A^{'} = V_A \times \frac{V_S^{'}}{V_S}$$

where $V_A^{'}$ and V_A refer to the output at the actual ($V_S^{'}$) and data sheet (V_S) supply voltages respectively. Based on the actual supply voltage of 3.3V, the scaled span and offset are listed in Table 6.

Table 6 Scaled Sensor Specifications

Parameter	Minimum (mV)	Maximum (mV)
Scaled Span	22	55
Scaled Offset	0	38.5

- **Step 3**. **Determine desired amplified span and offset**. In this example, the output of the amplifier is fed into the A/D input of the 38024 SLP MCU with reference voltages of 0V and 3.3V i.e., AV_{SS} = 0V and AV_{CC} = 3.3V. Select the amplified span = 2.7V with an offset voltage of 0.3V. These values are chosen to achieve a margin of 0.3V at either end.

Table 7 Amplified Output

Pressure	Amplified Output (V)
Zero	0.3
Full-scale	3.0

- **Step 4**. **Calculate the gain range**. Calculate the minimum and maximum gains required to achieve a 2.5V span.

$$\text{Maximum Gain} = \frac{\text{Desired Span}}{\text{Minimum Span}} = \frac{2.7\text{V}}{22\text{mV}} = 123$$

$$\text{Minimum Gain} = \frac{\text{Desired Span}}{\text{Maximum Span}} = \frac{2.7\text{V}}{55\text{mV}} = 49$$

- **Step 5**. **Implement level shift**. Depending on the range of the amplified offset voltage, a positive, negative or both types of level shift may be required to achieve the desired offset voltage level.

$$\text{OFFSET}_1 = \text{Maximum Gain} \times \text{Maximum Offset} = 123 \times 38.5\text{mV} = 4.736\text{V}$$

$$\text{OFFSET}_2 = \text{Minimum Gain} \times \text{Minimum Offset} = 49 \times 0\text{mV} = 0\text{V}$$

- **Step 6**. **Determine amount of level shift**. The range of the required level shift is calculated as follows:

$$V_{SHIFT1} = \text{Desired Offset} - OFFSET_1 = (0.3 - 4.736)V = -4.436V = VD$$

$$V_{SHIFT2} = \text{Desired Offset} - OFFSET_2 = (0.3 - 0)V = 0.3V = VU$$

If either V_{SHIFT1} or V_{SHIFT2} is positive, then a positive level shift is necessary. If either V_{SHIFT1} or V_{SHIFT2} is negative, then a negative level shift is necessary. Therefore, to calibrate any randomly selected MPX10 sensor to have a 0.3V offset, a negative level as high as 4.436V and a positive level shift as high as 0.3V are required.

- **Step7**. **Calculate gain-setting resistor values**. When selecting resistors, ±0.1% tolerance resistors with low temperature-coefficient are recommended and the value closest to the calculated value should be used. Select potentiometers with more turns (how many turns going from zero to full-scale resistance) to achieve finer gain and offset calibration adjustments.

— Set R7 to 10kΩ.

— Calculate the following ratios.

$$RATIO_{-SHIFT} = \frac{V_{CC}}{V_D} = \frac{3.3}{4.436} = 0.744$$

$$RATIO_{+SHIFT} = \frac{V_{CC}}{V_U} = \frac{3.3}{0.3} = 11$$

— If $RATIO_{+SHIFT} > RATIO_{-SHIFT}$ and $RATIO_{-SHIFT} > 1$, then R6 = R7. Else,

$$\frac{V_{CC}}{V_D} > 1 \Rightarrow R6 \leq R7 \bullet \frac{V_{CC}}{V_D}$$

— If $RATIO_{+SHIFT} < RATIO_{-SHIFT}$ and $RATIO_{+SHIFT} > 1$, then R6 = R7. Else,

$$R6 \leq R7 \bullet \frac{V_{CC}}{V_U}$$

— In this example, $RATIO_{+SHIFT} > RATIO_{-SHIFT}$ and $RATIO_{-SHIFT} < 1$,

$$R6 \leq R7 \bullet \frac{V_{CC}}{V_D} = 10k\Omega \bullet \frac{3.3V}{4.436V} = 7.439k\Omega$$

— To simplify the calculations, set the ratio of R7 to R6 to an integer while satisfying the above requirement. Set the ratio at 2 with R6 = 5kΩ. R2 and R3 are typically between 100Ω and 2kΩ. R1 and R4 should be at least 10kΩ. Select R2 = R3 =1kΩ and calculate

$$R1 = R4 = \left(0.80 \bullet \frac{\text{MINIMUM GAIN}}{1+\frac{R7}{R6}} - 1 \right) \bullet R2 = \left(0.80 \bullet \frac{49}{1+\frac{10}{5}} - 1 \right) \bullet 1k\Omega = 12.067k\Omega$$

Nearest value is 12.1kΩ.

— When selecting the value for R5, make sure its value is equal to or less than the calculated value.

$$R5 = \frac{2 \bullet R4}{\frac{\text{MAXIMUM GAIN}}{1+\frac{R7}{R6}} - \frac{R4}{R2} - 1} = \frac{2 \bullet 12.1k\Omega}{\frac{123}{1+\frac{10}{5}} - \frac{12.1}{1} - 1} = 867\Omega$$

Nearest value is 866Ω.

— The maximum required value for the potentiometer is

$$R5 = \frac{2 \bullet R4}{\frac{\text{MINIMUM GAIN}}{1+\frac{R7}{R6}} - \frac{R4}{R2} - 1} - R5 = \frac{2 \bullet 12.1k\Omega}{\frac{49}{1+\frac{10}{5}} - \frac{12.1}{1} - 1} - 866\Omega = 6.619k\Omega$$

- **Step 8. Calculate offset-adjust resistor values**.

— For positive level shift, set R9 = 0.1•R1 = 0.1•12.1kΩ=1.21kΩ

$$RU = \frac{\left[\frac{VU}{\left(1+\frac{R7}{R6}\right) \bullet V_{CC}} \right] \bullet R9}{1 - \frac{VU}{\left(1+\frac{R7}{R6}\right) \bullet V_{CC}}} = \frac{\left[\frac{0.3}{\left(1+\frac{10}{5}\right) \bullet 3.3} \right] \bullet 1.21k\Omega}{1 - \frac{0.3}{\left(1+\frac{10}{5}\right) \bullet 3.3}} = 37.8\Omega$$

— For negative level shift, set R8 = 0.1•(R6 + R7) = 0.1•(10+5)kΩ=1.5kΩ

$$RU = \frac{\left[\frac{VD}{\frac{R7}{R6} \bullet V_{CC}} \right] \bullet R8}{1 - \frac{VD}{\frac{R7}{R6} \bullet V_{CC}}} = \frac{\left[\frac{4.436}{\frac{10}{5} \bullet 3.3} \right] \bullet 1.5k\Omega}{1 - \frac{4.436}{\frac{10}{5} \bullet 3.3}} = 3.075k\Omega$$

- **Step 9. Calibration**
  1. Set all the potentiometers to zero.
  2. Apply zero pressure to the sensor. Adjust either RU or RD (but never both) to achieve the desired offset of 0.3V.
  3. Apply full-scale pressure to the sensor. Adjust RG to attain the full-scale output of 3.0V.
  4. The offset will be affected by the gain adjustment. Repeat steps 1 to 3 until the desired offset and span are achieved.

6. References

1. Paul Horowitz and Winfield Hill, *The Art of Electronics*, 2nd Edition, 1989, Cambridge University Press.
2. Eric Jacobsen, *Designing Amplifiers for Sensor Applications: A Cookbook Approach*, pg 119-128, January 1996, EDN.
3. Donald Christiansen, *Electronics Engineers' Handbook*, Fourth Edition, 1997, McGraw-Hill.
4. *H8/38024, H8/38024S, H8/38024F-ZTAT Group Hardware Manual*, Revision 4, 26 May 2003, Renesas Technology Corporation.
5. *Capacitor Comparison Chart*, http://www.analog.com/library/analogDialogue/archives/30-2/chart.html.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.20.03	—	First edition issued