

Designing Hard-switched Bridges with GaN

1. Diode-free bridges.

GaN power HEMTs are nearly ideal switches for many applications. A particular advantage in bridge circuits is that they can carry the freewheeling current without the need of an additional anti-parallel diode. Figure 1 compares a traditional high-voltage half bridge to a half bridge made with GaN devices. In the traditional half bridge each switch (shown here as an IGBT) is paired with a freewheeling diode. Because the HEMT channel exists in pure, undoped GaN, there is no parasitic p-n junction to provide an unwanted current path, and bidirectional flow of majority carriers can be realized in the channel.

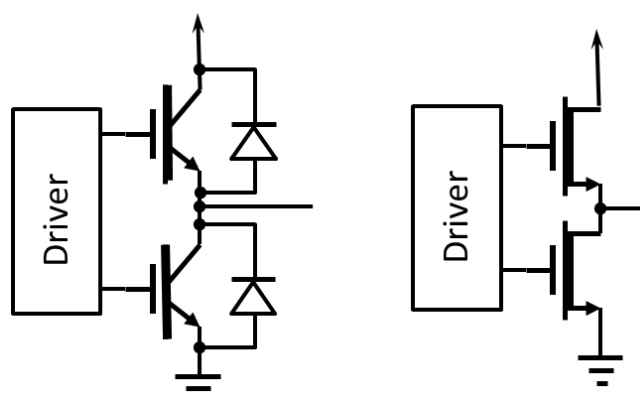


Figure 1: Comparison of a traditional high-voltage half bridge to a GaN half bridge.

In Renesas's cascode hybrid transistors the freewheeling current does indeed flow in the body diode of a silicon FET, but because it is a low voltage part, the injected charge is very small. Figure 2 indicates the current path for three modes of operation. In the reverse conducting mode the conduction loss may be reduced by enhancing the silicon FET (driving $V_{gs} > V_{th}$). As indicated in the figure, the voltage drop from source to drain decreases by about

0.8V with a 5A reverse current when the gate is enhanced.

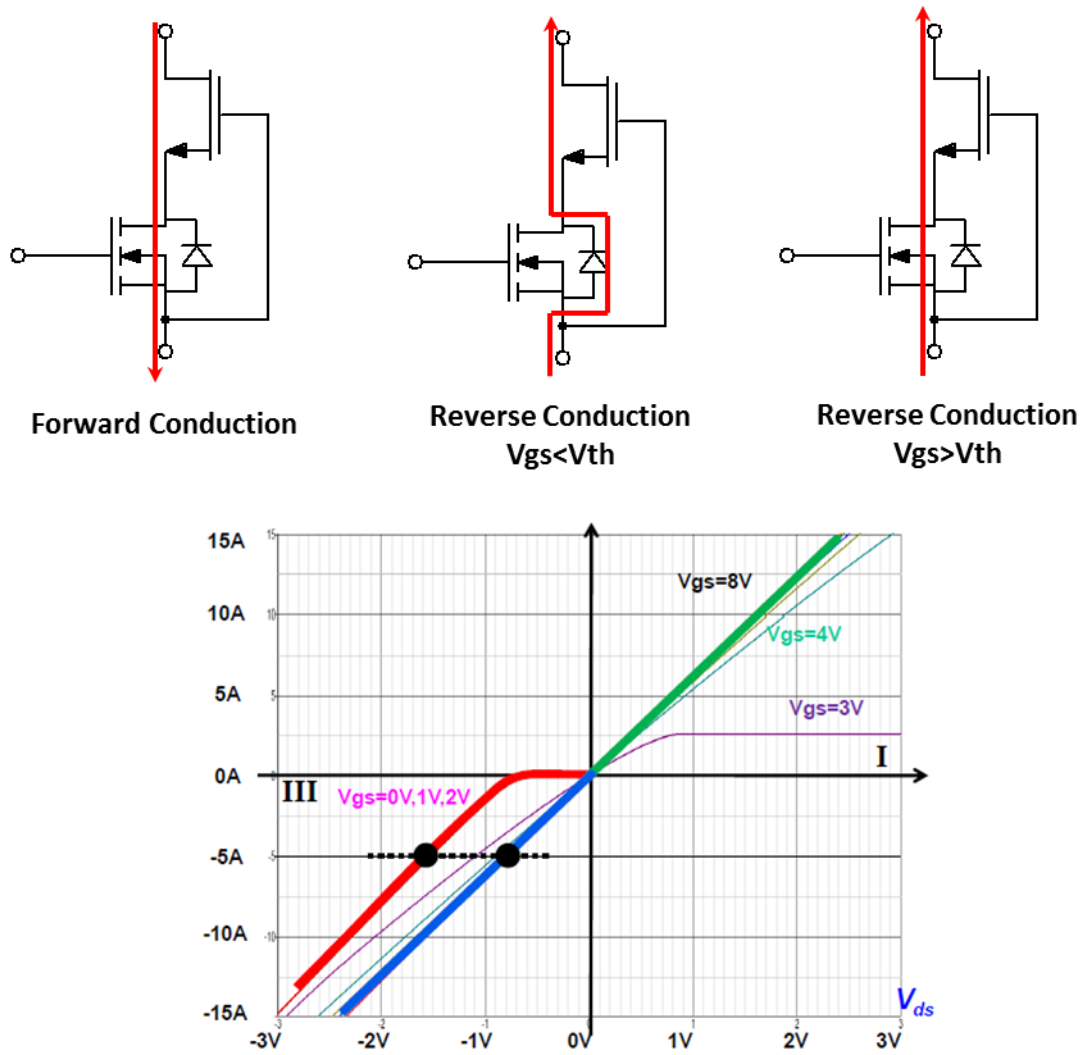


Figure 2: Current paths in the cascode GaN switch for three operating modes, and the corresponding IV characteristic.

Some transistor technologies include junctions which could, if permitted, serve the function of the freewheeling diode, the body diode of a MOSFET being one example. The reverse recovery charge for these devices will be much larger than for a GaN transistor with similar ratings. Figure 3 compares the total reverse-recovery charge for a Renesas HEMT to a low-Qrr superjunction silicon MOSFET. The Qrr ratio, Si/GaN, varies with exact part numbers, but is typically 20 or greater.

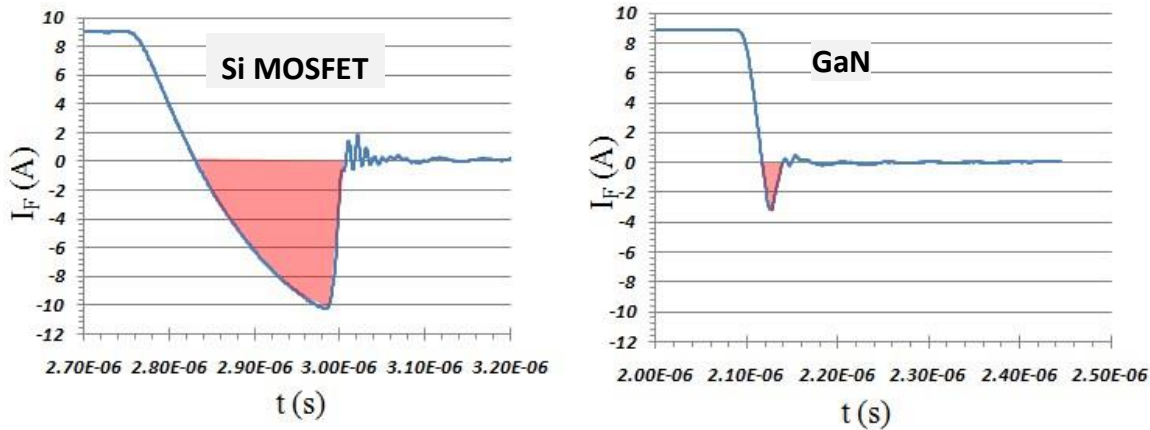


Figure 3: Reverse recovery charge test result for a Si MOSFET and a GaN HEMT with similar on resistance, showing a 20x reduction in Q_{rr} .

2. PCB layout. The parasitic inductances of the input (gate) and output (drain) loops contribute significantly to overshoot, ringing, and stability in general.

Output Loop: Although the various charges are low with GaN switches, they are not zero, and there will be a very fast transient current during switching as these charges are redistributed. This current will flow from the positive supply node, through both transistors to the negative supply node. To minimize ringing due to this transient, inductances in this path should be minimized. Referring to Figure 4, these inductances are indicated as $LS1$, $LD1$, $LS2$, and $LD2$. To minimize these, low impedance power and ground traces, or planes, should be used and bypass capacitance should be placed as close as possible to the transistors. It is not critical to minimize inductance L_{out} since it is in series with the load inductance, and to a first approximation simply adds to it. The connection between the high-side (Q1) source pin and the low-side (Q2) drain pin should also be very short. Placing the two transistors back-to-back on a common heat sink helps accomplish this. Figure 5 shows a portion of the layout of a Renesas half-bridge evaluation board, indicating the placement of the power transistors.

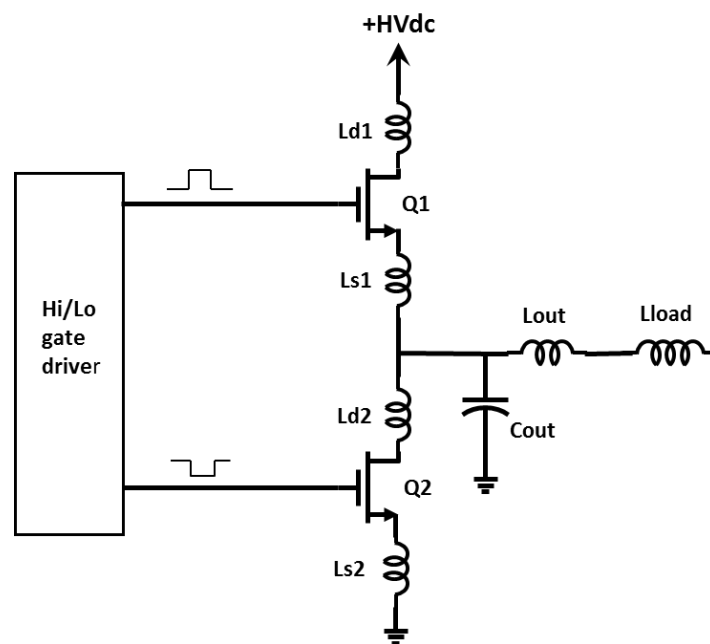
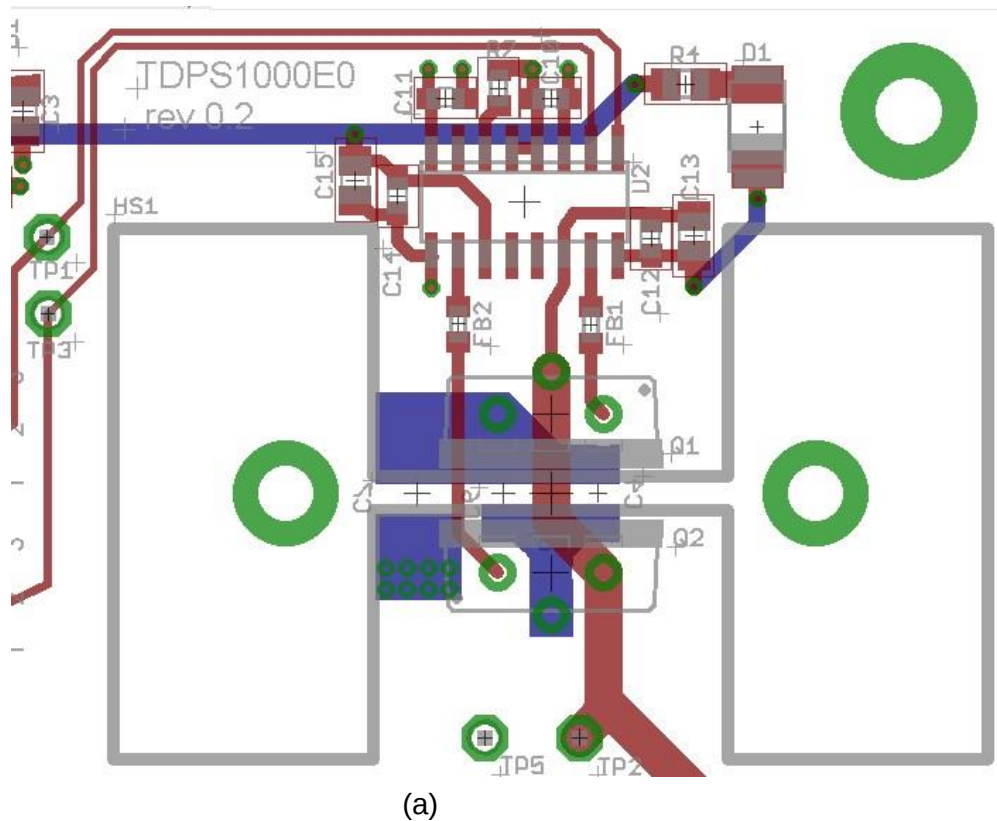


Figure 4: Parasitic elements in the output loop

Figure 5 (c) highlights details of the output loop layout. To minimize inductance, the drain of Q1 is connected directly to the power plane; the source of Q2 is connected directly to the ground plane. The power and ground planes are on internal layers of the PCB, not visible in the figure. The switching node is formed by the wide trace connecting the source of Q1 to the drain of Q2. Note that Renesas GaN HEMTs in TO220 packages have a pin configuration of G-S-D, as opposed to the traditional MOSFET configuration of G-D-S. Placement of the source pin in the center reduces coupling between the input and output loops. Figure 5 (d) shows the placement of high-voltage SMD bypass capacitors on the backside of the PCB for minimum series inductance.



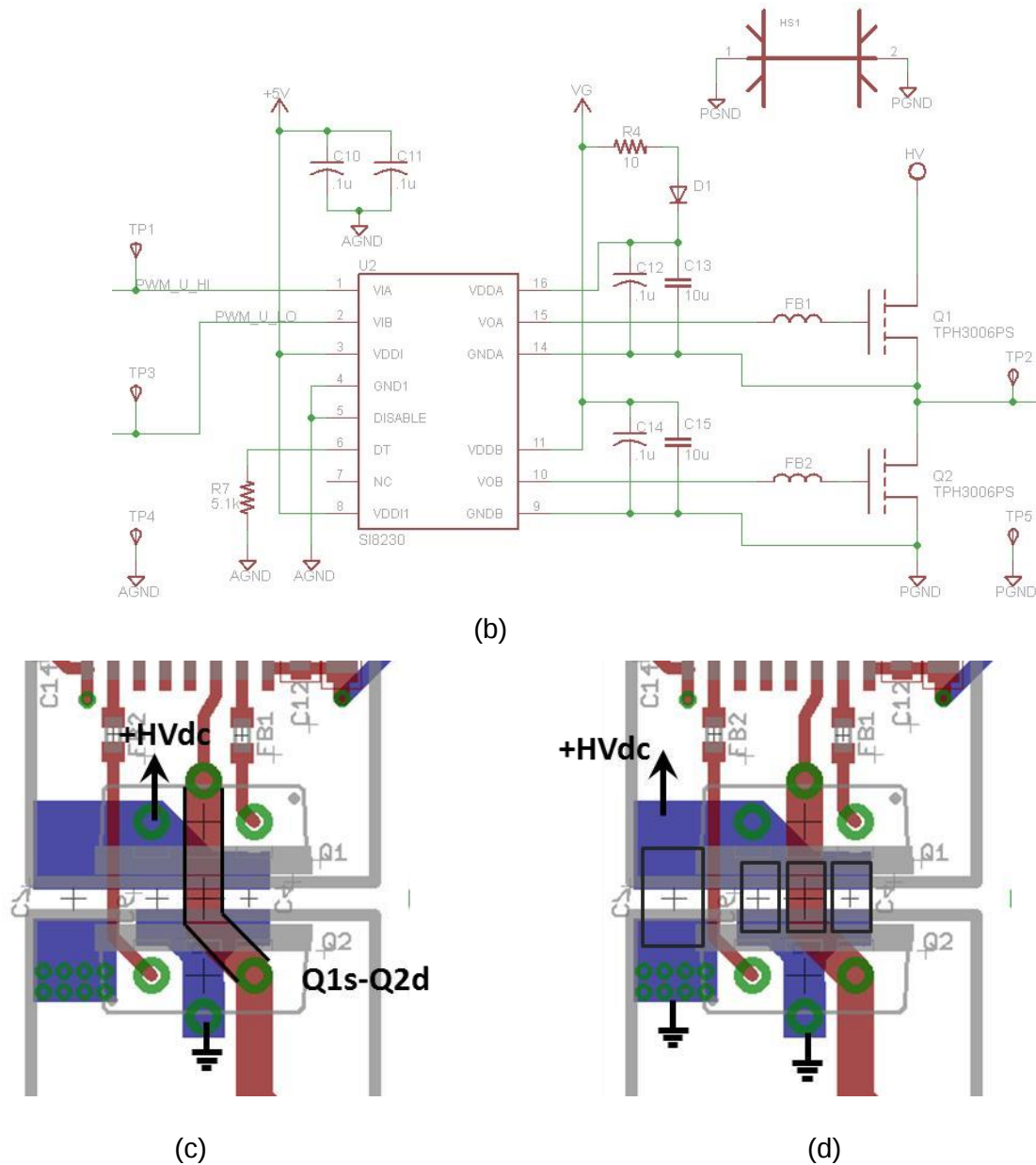


Figure 5: PCB layout. (a) Power-stage (b) corresponding schematic section
(c) detail of power connections (d) detail of bypassing: SMD capacitors on PCB backside.

Capacitance on the switching node, indicated as C_{out} in Figure 4, adds directly to switching loss, and so the total area of copper which forms the switching node should be kept low, but not so low that inductance becomes significant. A typical 4-layer board with 12 mils (0.3 mm) between outer trace and internal ground plane adds about 15pF/cm². At 100kHz switching, each 1cm² would add $P=1/2 CV^2f_s = 120\text{mW}$ switching loss, for example.

Gate-drive loop. As with the output loop, minimizing inductance in the input, or gate-drive loop is critical. Particularly important is the source inductance (LS2 in Figure 4, for example), which is common to both loops. Any voltage developed across this inductance due to a change in the output current, dI_D/dt , will appear in the input loop. A low impedance layout will minimize this inductance, as previously discussed. However, the TO220 package unavoidably adds inductance in the source lead,

as shown in Figure 6. This inductance cannot be further reduced, and so its impact must be recognized and mitigated.*

*Many advanced leadless packages are indeed available, or proposed, with lower parasitic inductance to fully realize the advantages of GaN devices. However, leaded packages are still dominant in industrial applications because of their simplicity for PCB assembly and capability for a wide variety of heatsinking techniques. For that reason this analysis focuses on the TO220 package.

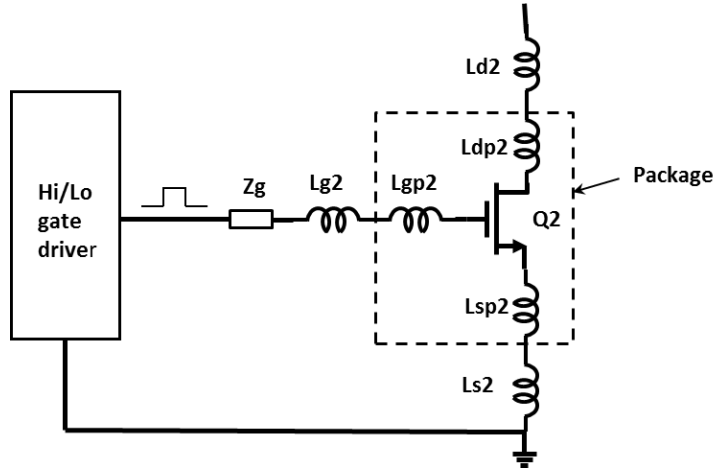


Figure 6: input loop showing parasitic inductances internal and external to the transistor package

During the initial phase of the turn-on transient, as the drain current rises from zero up to the value of the load current ($0 < I_D < I_{LOAD}$), the rate of change, dI_D/dt , is determined by the gate current. There is no significant change in V_{ds} , and therefore no displacement current included in I_D . A voltage $V=LdI/dt$ develops across the source inductance which will subtract from the gatedrive voltage. Slowing the dI/dt transition by reducing I_g will reduce the corresponding voltage on the source inductance and also reduce excitation of any related parasitic resonance. Using a gate resistor in the place of Z_g in Figure 6 would effectively decrease I_g . A gate resistor will not, however, provide the additional function of limiting slew rate at the switching node: $d(V_{ds})/dt$. This is because the feedback capacitance, C_{rss} , of the cascode combination is low. The common method of limiting C_{rss} discharge with a gate resistor will not be effective since the dominant output capacitance (C_{ds}) is not discharged through the gate resistor. Simply choosing a gate driver with a lower output current is a better way to limit I_g and dI/dt .

Once the drain current has risen to the level of the load current during turn-on of the GaN cascode switch ($I_D > I_{LOAD}$), a very fast dV/dt transition occurs. Values in the range of 100V/ns are common. A transient displacement current through C_{oss} due to $d(V_{ds})/dt$ will flow in the parasitic source inductance, causing ringing. This ringing voltage couples to the input circuit through C_{iss} of the transistor, and will tend to generate transient currents there. It is found that using a small SMD ferrite bead for Z_g effectively opposes such transient currents and inhibits coupling of the signal, although the voltage waveform on the gate pin is not obviously damped. The following combination of oscilloscope images and simulation results illustrates the behavior.

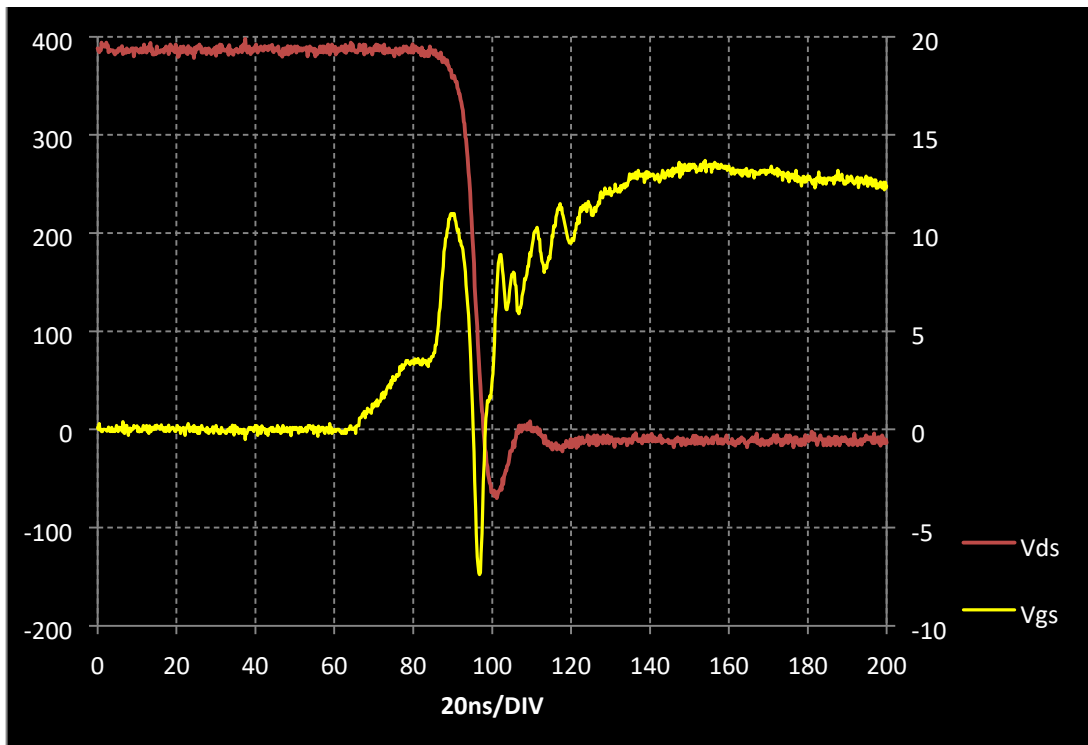
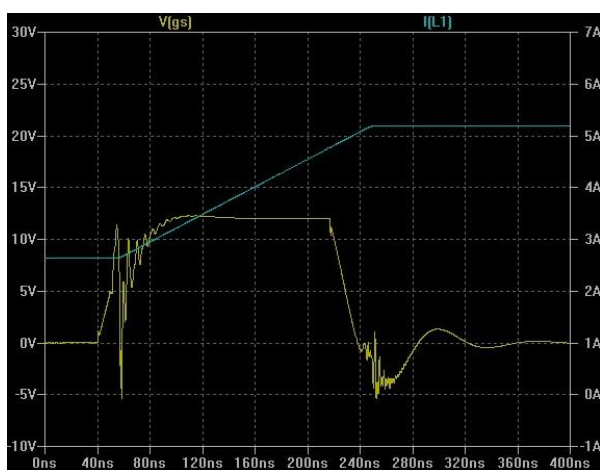
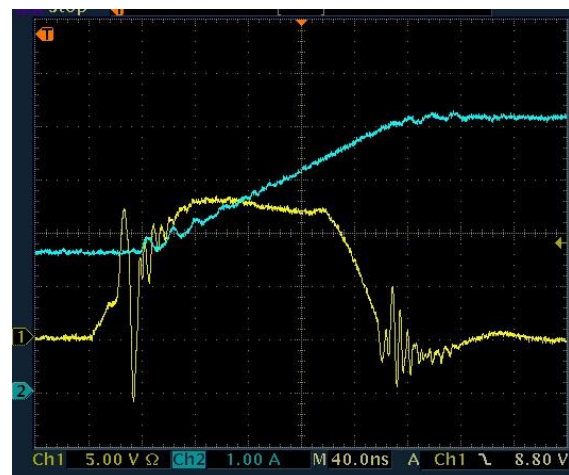


Figure 7: Vds and Vgs oscilloscope capture. 200:400V boost converter

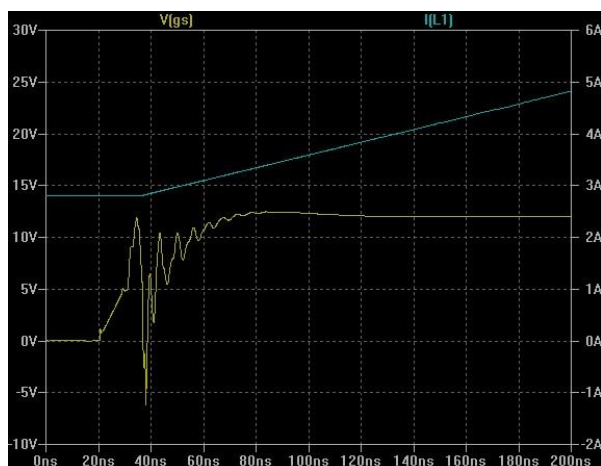
Figure 7 is an oscilloscope capture of the turn-on transient in a boost converter, showing the Vds and Vgs waveforms for the low-side transistor (Q2). In this and the following, except as noted, a ferrite bead with 120 ohms impedance at 100MHz was used in series with each gate. Boostmode is used for this study for ease of measuring Vgs. Because measurement of signals internal to the package is impractical, simulation is used to study the internal signals. Comparison of the actual and simulated external signals confirms validity of the model. Figure 8, for example, compares the actual and simulated external gate voltage and drain current during a multi-pulse test in boost mode.



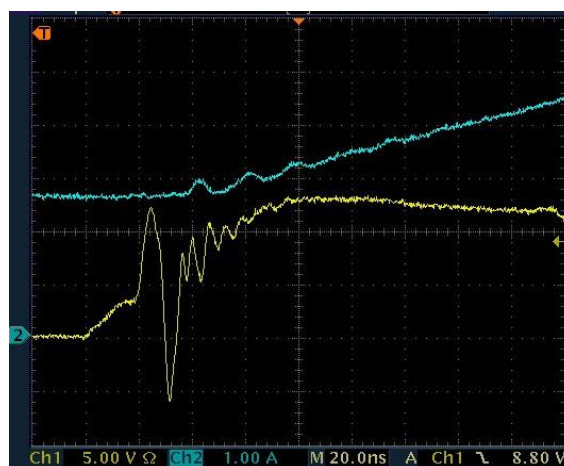
(a) simulated Vgs (on package pins)



(b) actual Vgs (on package pins)



(c) simulated Vgs (zoomed)



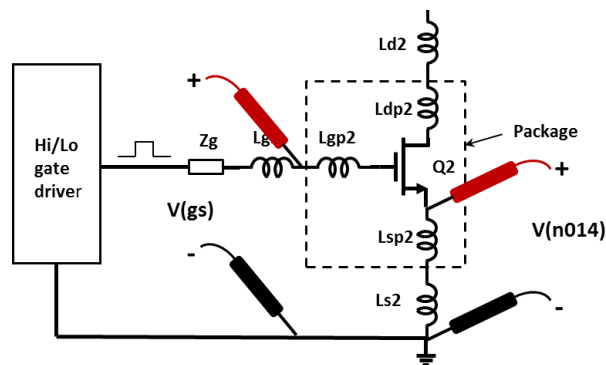
(d) actual Vgs (zoomed)

Figure 8: comparison of simulated and measured Vgs waveforms (yellow) and drain current (blue)

Figure 9 shows simulated voltages on the internal source node and external gate pin, with respect to circuit ground. It is seen that high-frequency ringing on the gate pin is identical to the ringing voltage on the source inductance. The input capacitance, C_{iss} , is sufficiently large that the actual gate-to-source voltage on the FET die is relatively unchanged by this signal. Figure 10 compares the external Vgs waveform to this actual internal gate-to-source voltage.



Figure 9: simulation showing voltage on the internal source node.



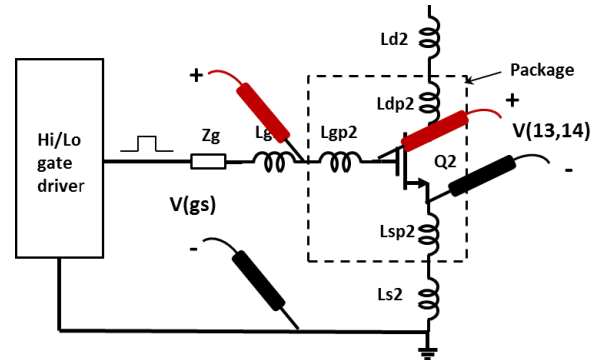
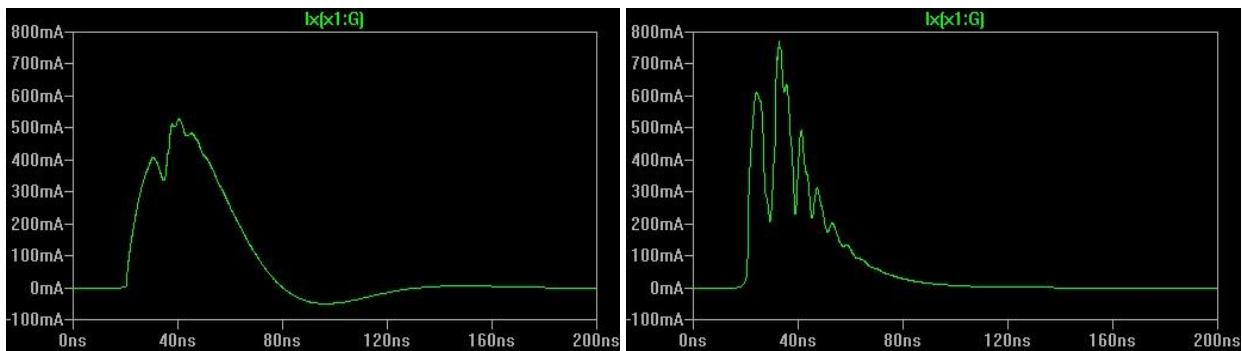


Figure 10: simulation showing internal V_{gs}

Finally, Figure 11 compares the current into the gate of the transistor with and without a ferrite bead in series (Z_g in Figures 9 and 10). The ferrite clearly opposes and damps high-frequency current in the gate loop, which is critical: V_{gs} only changes when there is current in C_{gs} .



(a)

(b)

Figure 11: gate current with (a) and without (b) a ferrite for Z_g

One final point to note regarding PCB layout is that separate ground planes are ideally used for the power and signal sections. These planes should be connected at a single point.

Off-state margin and negative gate voltage. The previous section analyzed the internal gate voltage of the actively switched transistor. Also of interest is the behavior of the opposite transistor which should be held off during the transient. Figure 12 shows a half bridge where the high-side transistor is switched and the low-side transistor carries the free-wheeling current. When Q_H turns on, the high dV/dt at the switching node (S) will induce current I_{GD} which charges C_{GD} of Q_L . Some of this current will flow in C_{GS} , raising the gate voltage. With a high enough ratio of C_{GD}/C_{GS} , V_{gs} could increase enough to turn on the low-side switch. However, in the cascode device this ratio is extremely low. For the TPH3006, for example, C_{GD} is 4.5pF while C_{GS} is 720pF at $V_{gs}=0$ and over 2000pF at the onset of turn-on.

A more valid concern than capacitive coupling through C_{GD} of the cascode pair is coupling through C_{GD_Si} of the low-voltage silicon FET. The drain-source voltage of the silicon FET, V_{ds_Si} in figure 12, only rises to $-V_{th}$ of the GaN HEMT, but will do so with high dV/dt . The ratio of C_{GD_Si}/C_{GS} in this case is significant.

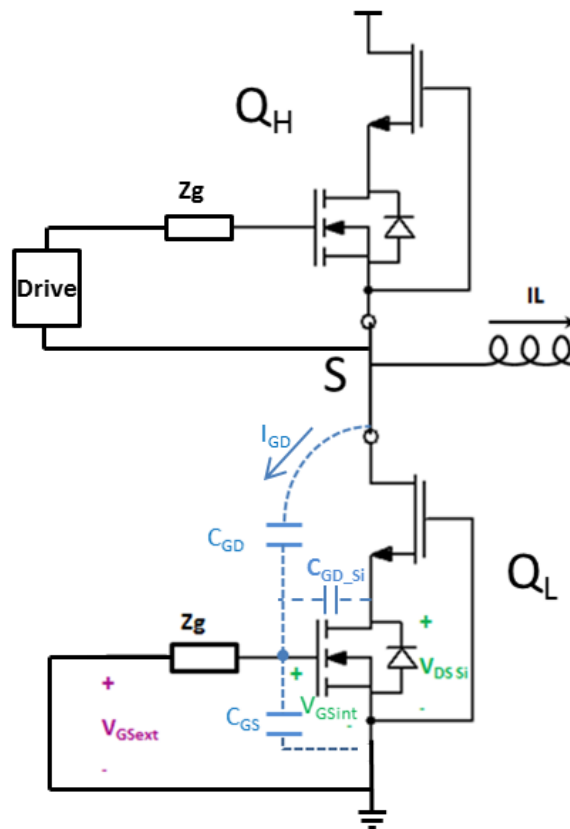


Figure 12: Capacitances of the off-state transistor: Q_H is actively switched, Q_L is off.

Figure 13 compares external gate waveforms for measured and simulated cases. The simulation also includes the internal V_{gs} of the silicon FET. It is seen that V_{gs} does rise quickly toward the threshold voltage when V_{ds_Si} changes. However, because the rise in V_{ds_Si} corresponds to turn-off of the GaN HEMT, any drain current induced in the silicon FET due to the rise in V_{gs} must first discharge the GaN gate before external current flows. Therefore a momentary turn-on of the silicon FET will not necessarily result in external drain current.

Renesas evaluation boards do not generally use a negative gate bias, and no excessive switching loss is observed. It is clear, nonetheless, that use of a small negative bias will improve the noise margin.

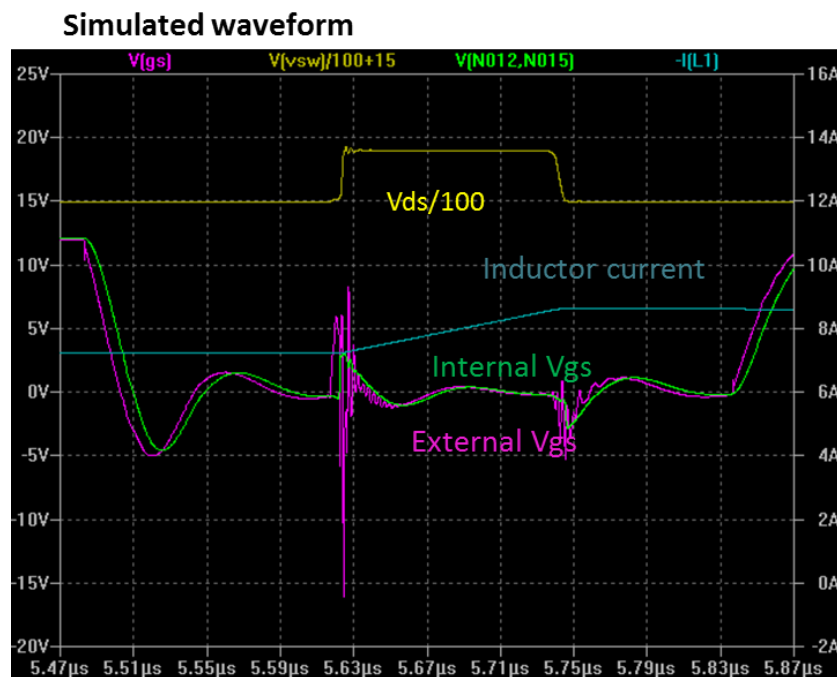
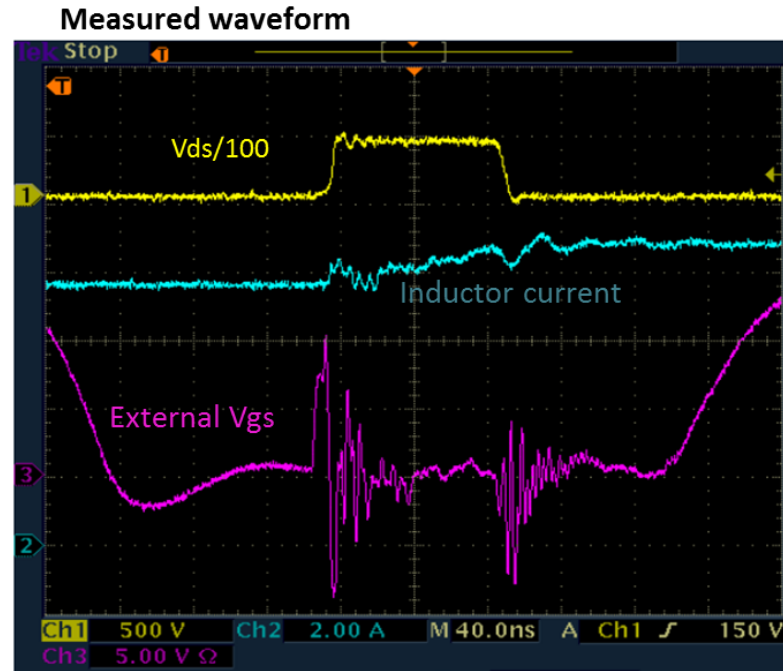


Figure 13: Measured and simulated waveforms for the off transistor (Q_L)..

3. Heat Sink connection. The heat sink should be connected to an AC ground. In the evaluation board of Figure 5 the heat sink is electrically connected to the negative supply, or ground plane. Both low-side and high-side transistors are insulated from the heat sink. For the low-side transistor the capacitance between tab and heat sink is not critical, since the tab of the TO-220 is connected to the source. This transistor could be mounted directly to the heat sink, but the possibility that load current could flow in the heat sink must be allowed for. If a reliable connection between tab and heat sink is

either not possible or not desirable, use of an insulator is necessary. For the high-side transistor, capacitance between the TO220 tab and the heat sink will add to switching loss, and so a thick and/or low permittivity insulator should be used.

Note: A Renesas device with a drain-tab connection, e.g. TPH3006PD, could be used for the high-side switch to eliminate this capacitance from the switching node. However, because the drain-tab configuration has a different internal interconnection compared to the source-tab configuration, the resonances which occur when one of each is used in a half bridge are more complicated. In the evaluation board, therefore, the combination of two source-tab devices was chosen as being more universally stable.

4. Gate drive and bootstrap supply: Because high slew rates on the order of 100V/ns are normal, the high-side gate-driver must have good common-mode transient immunity. Apart from that consideration, there are no special requirements for the hi/lo gate driver used with Renesas's GaN switches. As with any insulated-gate power transistor, the gate-drive current should be consistent with the desired turn-on time and total gate charge. The transistor is fully on with about +8V, gate to source. Since many gate-drive chips have an undervoltage protection threshold of 8 or 9V, Renesas evaluation boards often use 12V auxiliary supplies to avoid nuisance trips. As mentioned in section 2, use of a negative gate voltage in the off state is not mandatory, but is a viable option for increasing noise margin. Also mentioned in section 2, a series gate resistor is not generally as helpful as a small ferrite bead. Selecting a gate driver with a lower drive current can be appropriate for reducing di/dt . Drivers with 0.5A output current have been used with good result, for example.

The bootstrap, or floating, supply for the high-side gate drive comprises components R4, D1, C12, and C13 in Figure 5. The junction capacitance of D1 contributes directly to switching loss, and so a fast, low capacitance diode should be used. Resistor R4 is critical for limiting the inrush charging current; a value of 10-15 ohms works well. If an isolated DC-DC converter is used for the high-side supply, the isolation capacitance plays the same role as the junction capacitance of D1 in the bootstrap supply. Inductance in series with this capacitance will create an additional resonance which will be excited with each switching transient, so careful layout applies here. Use of a common-mode choke in the floating supply can be helpful.

5. **Probing:** In order to minimize inductance during measurement, the tip and the ground of the probe should be directly attached to the sensing points to minimize the sensing loop. For safe, reliable and accurate measurement, a scope probe tip may be directly soldered to the sensing point and a short ground wire soldered to the ground plane. Figure 14 indicates an alternative which does not require soldering the probe tip.

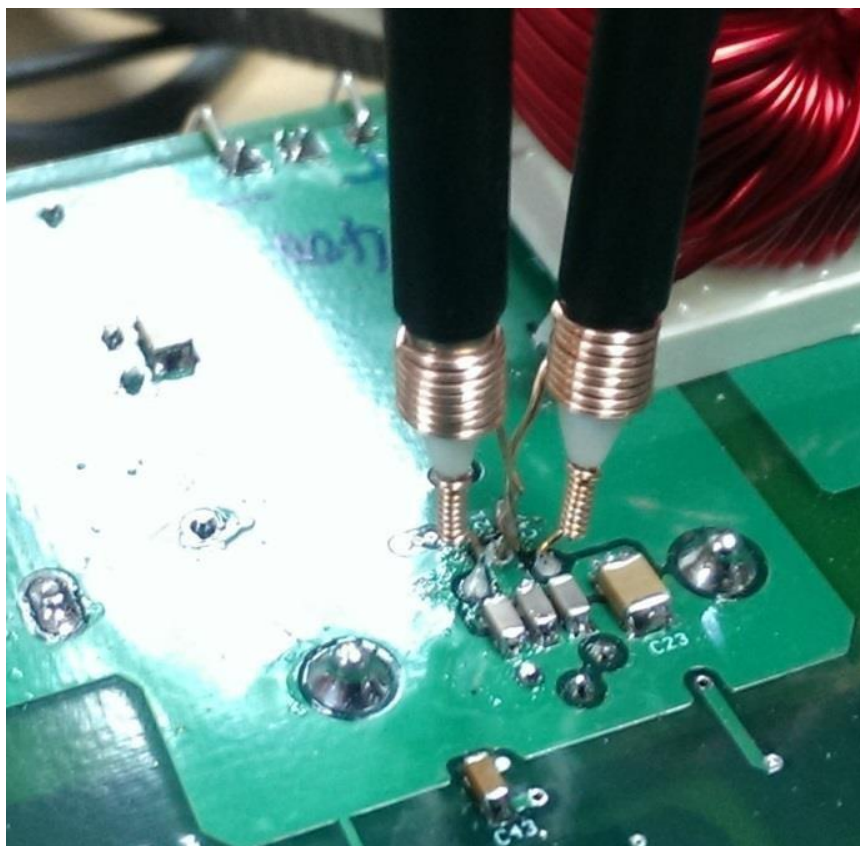


Fig. 14. Low-inductance probing of fast, high-voltage signals