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DESIGN OF PUSH-PULL TYPE SWITCHING REGULATOR (APPLICATIONS)

1. INTRODUCTION

Switching regulators can be made smaller in dimension plus more efficient than conventional series regulators. Thus, they are dominating in design applications of power supply systems.

In this material, we present the design of pulse width modulation type control circuits, giving an example of actual design for a push-pull switching regulator as the succeeding item to Technical Data Sheet "Design Of Push-Pull Type Switching Regulator (Basics)."

2. DESIGN OF CONTROL CIRCUIT

Figure 1 represents the block diagram of the control circuit of a push-pull switching regulator.

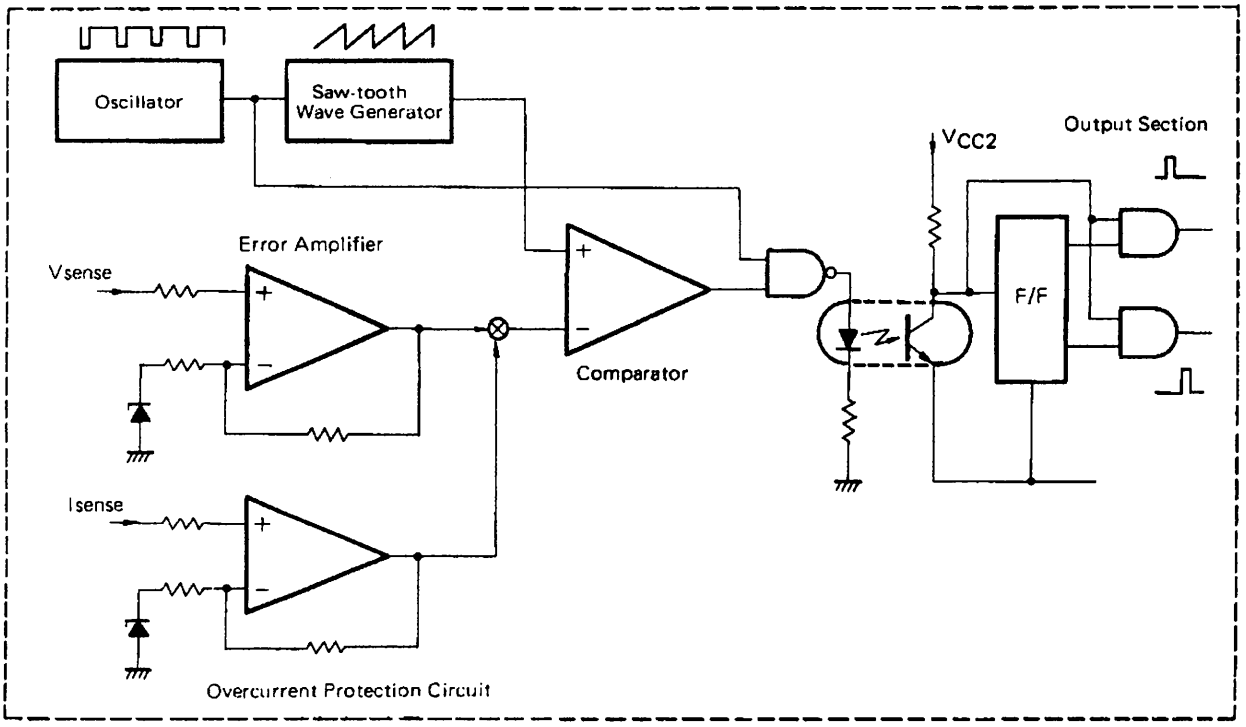


Figure 1. Block Diagram of Control Circuit

In this material, the switching regulator is composed of four circuits; a circuit which performs pulse width modulation in response to the fluctuation of input power or load for the stabilization of output power voltage, an isolator which transmits an isolated pulse width-modulated signal, a frequency divider circuit which operates two switching elements alternately and an additional circuit (overcurrent protection circuit).

The saw-tooth wave generator output signal which is synchronized to the oscillator frequency is applied to the (+) input terminal of the comparator where it is compared with the amplified error signal from the power source and converted into a signal which is pulse width-modulated in response to the output voltage fluctuation

of the power source. Because this output signal is often at a low level according to the status of error amplifier, it is AND'ed with the oscillator output signal with the specified quiescent time and further applied to the isolator.

In addition, the output signal of the overcurrent protection circuit is applied to the (--) input of comparator to prevent the collector current from increasing due to the short-circuiting of load, etc. The isolator uses the high speed photocoupler to transmit the signal which is pulse-modulated by approximately 40 kHz frequency. The light receiving side of the photocoupler divides the input signal into two, with a phase difference of 180°. by the two-phase clock circuit composed of a flip-flop and gates.

As explained above, the control circuit requires a logic IC in addition to linear IC. To minimize varieties of power source voltages, in this circuit design, CMOS is employed as a logic IC because of wide input voltage range and also because it can be used on a common line with the linear IC.

2-1 Oscillator

The oscillator determines the oscillation frequency of a switching regulator, as well as the maximum duty required for the elimination of ON-ON operation of the switching devices.

Figure 2 represents an astable multivibrator circuit composed of CMOS NAND gates and Figure 3, output waveform of the astable multivibrator.

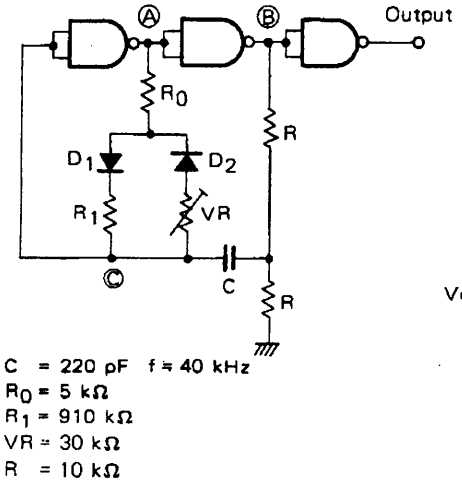


Figure 2. Block Diagram of Oscillator circuit Composed of NAND Gates

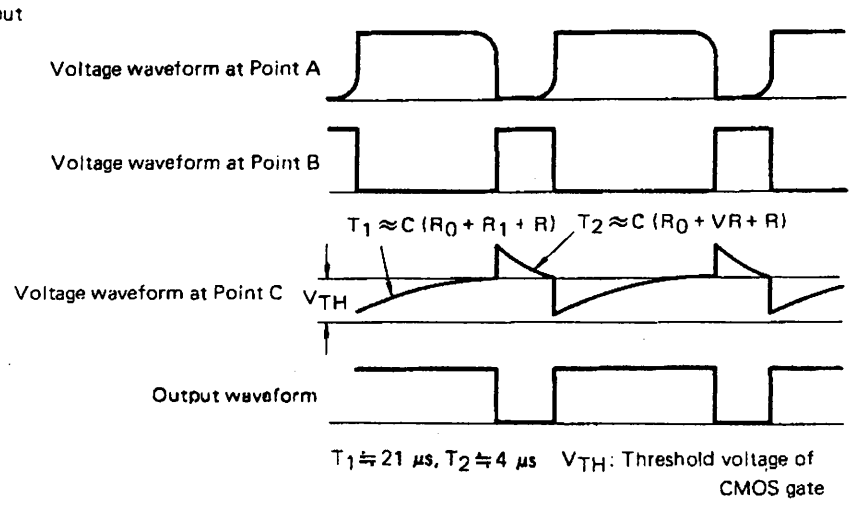


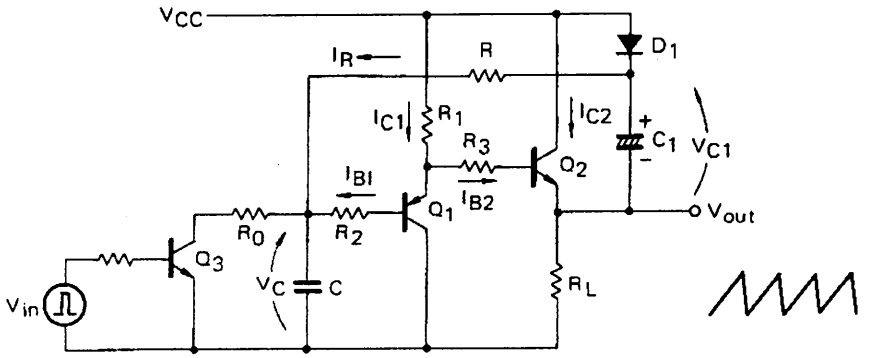
Figure 3. Waveform of Oscillator

Since the charging and discharging paths of timing capacitor C are changed by diodes D_1 and D_2 in response to the direction of the current, the resultant voltage at point C is a combination of two waveforms of different time constants as shown in Figure 3.

2-2 Saw-tooth Wave Generator

Since a saw-tooth wave generator has great influence over the linearity of input voltage and pulse width of the succeeding comparator circuit, the output waveform of the saw-tooth wave generator should be of excellent linearity.

For such a circuit as explained above, a bootstrap circuit composed of discrete components is shown in Figure 4.



C = 560 pF
C_1 = 1.5 μF
D_1: 1S953
Q_1: 2SA603
Q_2, Q_3: 2SC943

R_0 = 47 Ω
R_1 = 15 kΩ
R_2 = 100 Ω
R_3 = 47 Ω
R_L = 2 kΩ
R = 56 kΩ

V_{BE1}: Base to emitter voltage of Transistor Q_1
V_{BE2}: Base to emitter voltage of Transistor Q_2
V_C : Voltage across Capacitor C
V_{C1} : Voltage across Capacitor C_1

Figure 4. Saw-Tooth Wave Generator with Bootstrap Circuit

In Figure 4, suppose that the voltage across capacitor C is 0 V at the time t (=0). In this case, since the capacitor C is connected to the power source through diode D_1 and resistor R_L, voltage V_{C1} across capacitor C is, in equilibrium,

$$V_{C1} = V_{CC} - V_F \ (V) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

where

V_{CC}: Power source voltage of the circuit (V)

V_F : Forward voltage of diode D_1 (V)

Also, in this circuit, current I_R through feed back resistor R is

$$I_R = \frac{V_{C1} + V_{out} - V_C}{R} \ (A) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

as

$$V_{out} + V_{C1} - I_R \cdot R - V_C = 0 \ (V)$$

From

$$V_{out} = V_{E1} - R_3 \cdot I_{B2} - V_{BE2} \ (V)$$

$$V_{E1} = V_C + R_2 \cdot I_{B1} + V_{BE1} \ (V)$$

$$V_{out} = V_C + V_{BE1} - V_{BE2} + R_2 \cdot I_{B1} - R_3 \cdot I_{B2} \fallingdotseq V_C \ (V) \quad \ldots\ldots\ldots \quad (3)$$

as

$$V_{BE1} \fallingdotseq V_{BE2} \ (V)$$

$$R_2 \cdot I_{B1} \fallingdotseq R_3 \cdot I_{B2} \ll V_C \ (V)$$

Therefore, from equation (1), (2) and (3)

$$I_R \fallingdotseq \frac{V_{CC} - V_F}{R} \ (A) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

Thus, the current is constant regardless of output voltage V_{OUT}. And, therefore, the current through capacitor C is almost equal to I_R, if the base current of transistor Q_1 is disregarded.

$$V_C = \frac{1}{C}\int I_R \cdot dt = \frac{1}{C} I_R \cdot t \fallingdotseq \frac{(V_{CC} - V_F)}{CR} \cdot t \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (5)$$

Thus, output voltage V_{OUT} has the value in proportion to time t. On the other hand, charging voltage V_C of capacitor C is discharged through the resistor R_O when the transistor Q_3 turns on by the short pulse signal syncronized to the aforementioned oscillator signal.

Thus, saw-tooth waveforms can be obtained.

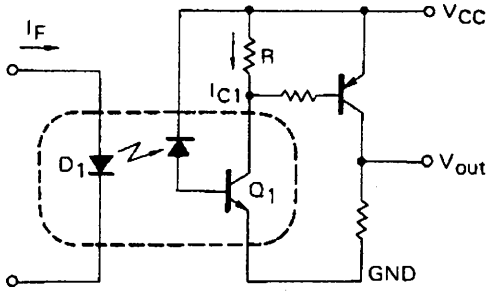
2-3 Pulse Width Modulator

The pulse width modulator requires a high speed comparator to perform the pulse width modulation with approximately 40 kHz. frequency.

In addition, to avoid the occurrence of erroneous operation caused by noise in input signal, a Schmitt trigger circuit having hysteresis to the input circuit is employed.

2-4 Isolator

As an isolator to transmit a pulse width-modulated signal to isolating the input circuit from the signal transmission path, a pulse transformer can be used in addition to its proper application to the base driving circuit. But the photocoupler is preferable to pulse transformer in insulation resistance and CMR. For actual application, however, a high speed photocoupler is necessary because conventional photocouplers are not satisfactory due to the insufficient response speed. Figure 5 represents the isolator circuit with high speed photocoupler.



I_F : Input current at the light emitting side (forward current of light emitting diode D_1)

I_{C1}: Collector current of transistor Q_1 of light receiving side. (I_{C1} = CTR x I_F, CTR: Current transfer ratio)

Figure 5. Isolator Circuit using High Speed Photocoupler

At the light receiving side of photocoupler, a low-resistance resistor is required at the collector of transistor Q_1 for its operation in the active region to avoid the degradation in response speed which is dependent on the storage time of transistor Q_1. In addition, due to the presence of coupling capacitance between input and output circuits erroneous operation may be caused by the outside noise. And such countermeasure as inserting a capacitor of small capacitance between the base and emitter of transistor Q_1, is required to eliminate them.

2-5 Two-Phase Clock Circuit

The two-phase clock circuit divides the signal which is pulse width-modulated by approximately 40 kHz frequency into two with difference in phase of 180° in order to make main switching devices operate alternately. Figure 6 represents the block diagram of two-phase clock circuit. In Figure 6, gates 1 and 2 are delay circuits to prevent the output signal from generating spikes by propagation delay time t_{pd} of flip-flop circuit. The delay time of approximately 75 ns can be obtained when the power source voltage V_{DD} is 10 V.

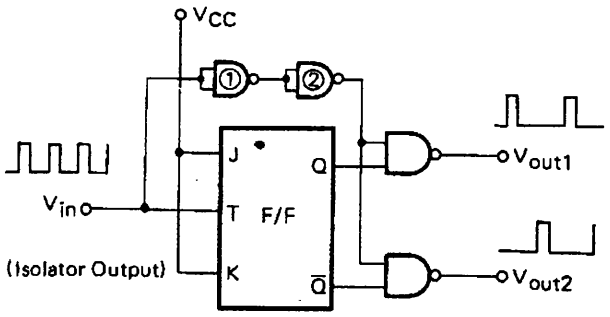
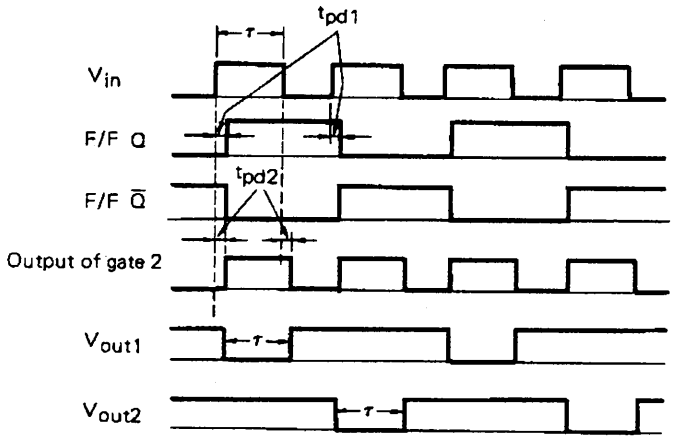


Figure 6. Two-Phase Clock Circuit

The clock terminal of J-K flip-flop is used to make the circuit as T flip-flop. Figure 7 represents the operating waveform of this circuit.



t_{pd1}: Propagation delay time of flip-flop
t_{pd2}: Propagation delay time by two NAND gates

Figure 7. Operating Waveform of Two-Phase Clock Circuit

3. EXAMPLE OF 5 V, 20 A OUTPUT SWITCHING REGULATOR

3-1 Specifications of Power Supply and Test result

Table 1 shows specifications of trial-manufactured power supply with the test results in the right column.

Table 1. Specifications of Switching Regulator and Test Results of Trial-manufactured Unit

Characteristic	Symbol	Specifications	Test Results
Input Voltage	v_{in}	100 V ±10 % (AC 50 Hz)	100 V ±10 %
Output Voltage	V_o	5 V ± 10 %	5 V ±10 %
Output Current	I_o	20 A	20 A
Ripple Voltage	V_{rip}	Within 20 mV	14 mV
Line Regulation		≦ ±0.25 %	±0.22 %
Load Regulation		≦ ±1 %	+0.9 %
Efficiency	η	> 70 %	76 %
Dimensions		–	130(H) x 125(W) x 197(D) mm^3

3-2 Schematic Diagram

Figure 8 represents the complete schematic diagram of 5 V, 20 A output switching regulator (push-pull type)

3-3 Design of Whole Blocks

(1) Rectifying and Smoothing Circuit of Primary Side

i) Rectifier

The input power P_{in} at rated output (P_O = 100 W) is approximately 140 VA if the efficiency η is assumed 70%.

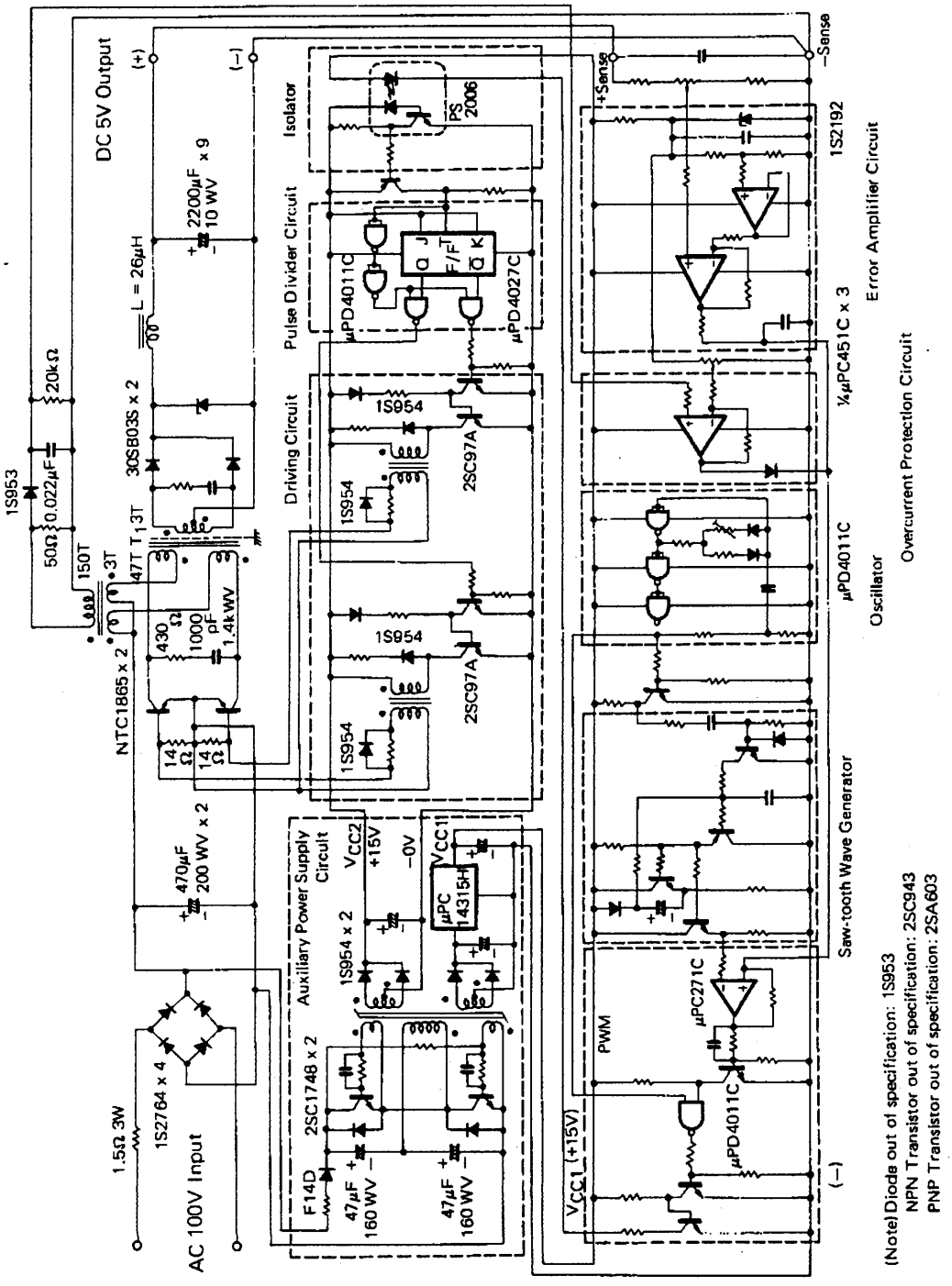


Figure 8. Schematic Diagram of 5 V, 20 A Output Switching Regulator (Push-Pull Type)

In this case, an average current of approximately 1.4 A runs every half cycle in the rectifier. However, the conducting angle becomes narrower and surge current becomes larger, as the smoothing capacitance increases to decrease ripple components of input voltage. In addition, since a maximum of $2\sqrt{2}$ times AC input voltage V_{in} is applied to the bridge rectifier, it should have reverse breakdown voltage of approximately 400 V when AC input is 100 V.

To comply with this requirement, NEC's 1S2764 is employed in this circuit, (V_{RRM} = 400 V, V_F = 1.0 V at I_F = 3.0 A)

Resistance R_S for preventing the rush current differs with the rectifier and capacitance of smoothing capacitor and shown in the characteristic curve of the rectifier. It is approximately 1.4 Ω for 1S2764 at C = 500 μF.

ii) Smoothing Capacitor

Capacitance C of the smoothing capacitor is dependent on the load and the ripple reducing rate. It can be simply obtained from the chart prepared by O. H. Schade. (Figure 9)

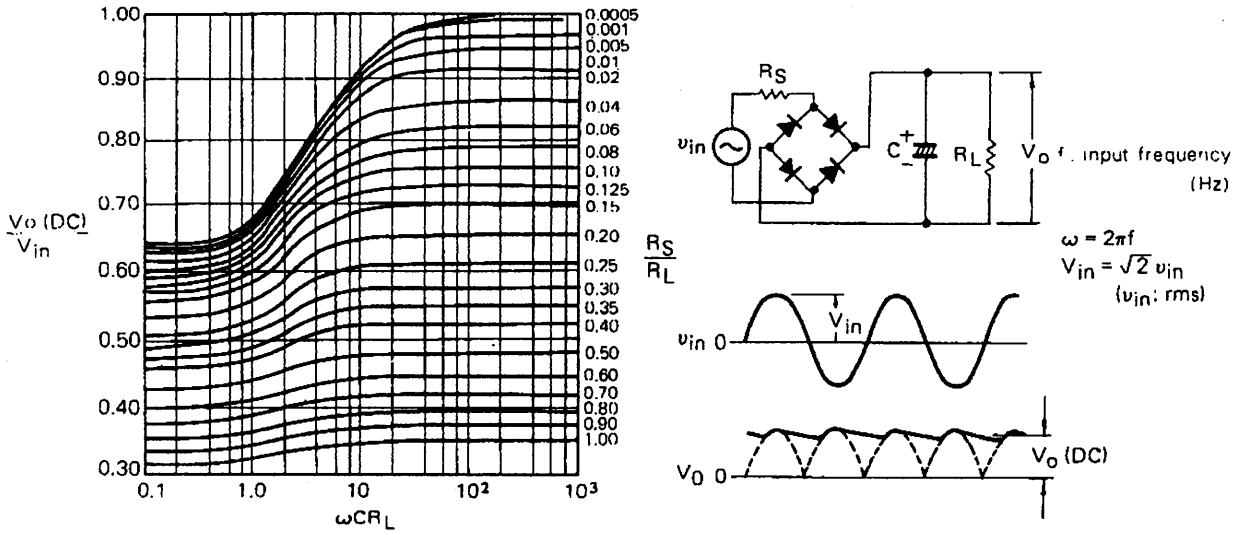


Figure 9. Chart for Circuit Constant of Full-Wave Rectifier Circuit

With input voltage V_{in} minimum and the load P_O maximum, and the smoothing output voltage V_O is set to 100 V (minimum value), from

$$v_{in(min.)} = 90 \text{ V}, \quad P_{in(max.)} = \frac{P_{O(max.)}}{\eta} = \frac{5.5 \times 20}{0.70} \fallingdotseq 157 \text{ (W)}$$

(Supposing efficiency is 70 %)

the peak value of output voltage is

$$V_{in(min.)} = \sqrt{2}\, v_{in(min.)} \fallingdotseq 127 \text{ (V)}$$

Therefore, the average output voltage is

$$V_{O(DC)} \geqq \frac{127 + 100}{2} \fallingdotseq 114 \text{ (V)}$$

Substituting the above results in the chart,

$$\frac{V_{O(DC)}}{V_{in(min.)}} \fallingdotseq 0.90 \qquad \frac{R_S}{R_L} \fallingdotseq \frac{1.4}{63.7} \fallingdotseq 0.022$$

as, $$R_{L(min.)} = \frac{(V_{O(min.)})^2}{P_{in(max.)}} \fallingdotseq 63.7 \ (\Omega)$$

thus,

$$\omega C R_L \geqq 20$$

therefore

$$C \geqq \frac{20}{\omega R_L} = \frac{20}{2\pi f R_L} \fallingdotseq \frac{20}{2\pi \times 50 \times 63.7} \fallingdotseq 9.99 \times 10^{-4} \ (F)$$

Therefore, two capacitors of 200 V, 470 μF are arranged in parallel (940 μF) in this circuit.

(2) Design of Transformer

i) Core

Use Tohoku Kinzoku's EI type ferrite core FEI40-3100B. The performances of this core are given in Table 2 below.

Table 2. Performances of Core FEI40-3100B (from Ferrite Core Manual "Cat. No. FR-17" of Tohoku Kinzoku)

Item	Symbol	Specifications
Cross Section	A_e	1.46 cm^2
Magnetic Path Length	l_e	7.59 cm
Induction Coefficient	AL	1 210 nH at t = 0.13 mm / 6 040 nH at t = 0*
DC Overlapping Characteristic	NI	≒20 AT at t = 0.13 mm / 1.5 AT at t = 0
Effective Saturated Magnetic Flux Density	Bms	0.52 T

* t: Core Gap

ii) Winding

a) Number of Turns of Primary Winding N_p

from

$$N_p = \frac{V_{in}}{4 \cdot B \cdot A_e \cdot f}$$

Where: $V_{in} = 130$ V, $B = 0.24$ T (= 0.24 wb/m^2), $f = 20$ kHz, $A_e = 1.46$ cm^2 (= 1.46×10^{-4} m^2)

$N_p \fallingdotseq 46.4 \fallingdotseq 47$ (turns)

b) Diameter of the wire of Primary Winding D_p

from

$$D_P = \sqrt{\frac{4 I_{in(av)}}{\delta \pi}} \qquad 2I_{in(av)} = \frac{P_{in}}{V_{o(DC)}} = \frac{157}{114} \fallingdotseq 1.38\ (A),\ \delta = 2\ A/mm^2$$

$$D_P \fallingdotseq \sqrt{\frac{4 \times \frac{1.38}{2}}{2 \times 10^6 \times 3.14}} \fallingdotseq 0.66\ (mm)$$

c) Number of Turns of Secondary Winding N_S

from

$$N_S = \frac{(V_O + V_F + I_O \cdot r_L) \cdot N_P \cdot T}{2\tau \cdot V_P}$$

where

$V_O = 5.5$ V, $V_F = 0.5$ V ($I_F = 20$ A), $r_L = 0$, $T = 50\ \mu s$, $\tau = 23\ \mu s$,
$N_P = 47$, $V_P = V_{in(DC)} = 100\ V_{min}$.

$N_S \fallingdotseq 3.06 \fallingdotseq 3$ (turns)

d) Shape of Secondary Winding

From the standpoint of skin effect, use wheel winding with a copper plate of 15 mm width and 0.3 mm thickness considering the bobbin shape of core.

e) Electrostatic Shield

Use alminum foil. Ground the foil to the case.

f) Core Gap and Inductance of Primary Side

Due to the difference in storage time of switching devices DC superimposed current flows through the circuit of primary side, so the core should have DC superimposed characteristics.

When designing, DC superimposed characteristic NI is set to 20 AT considering the margin for NI, from

$t = 0.13$ mm, $AL = 1\ 210$ nH

inductance L_p of primary side is

$$L_p = AL \cdot N_p^2 \cdot 10^{-9} = 1210 \times 47^2 \times 10^{-9} \fallingdotseq 2.67\ (mH)$$

(3) Selection of Switching Devices

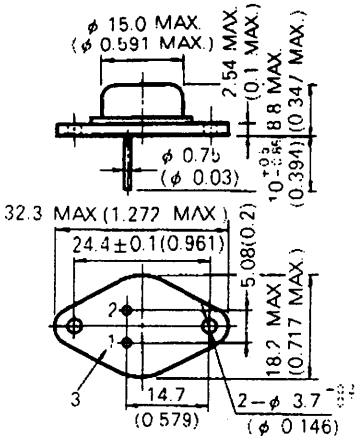
Prepare two transistors NTC1865 for switching devices to effectuate the push-pull operation at AC 100 V line, remembering that V_{CE} is 280 V and I_C is 2 A.

Table 3 represents a summary of the characteristics of transistor NTC1865.

Table 3. Characteristics of NTC1865

PACKAGE DIMENSIONS

in millimeters (inches)



1. Base
2. Emitter
3. Collector(Case)

EIAJ : TC-16, TB-23
JEDEC: TO-66
IEC : C13

FEATURES

- High speed switching.
- Low collector saturation voltage.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltages and Currents (Ta = 25 °C)

Collector to Emitter Sustaining Voltage	$V_{CEO(sus)}$	400	V
Collector to Emitter Sustaining Voltage	$V_{CE(sus)}$	450	V
Emitter to Base Voltage	V_{EBO}	7.0	V
Continuous Collector Current	$I_{C(DC)}$	7.0	A
Peak Collector Current	$I_{C(Pulse)}$*	15	A
Continuous Base Current	$I_{B(DC)}$	4.0	A
Maximum Power Dissipation (T_C = 25 °C)			
Total Power Dissipation	P_T	50	W
Maximum Temperature			
Junction Temperature	T_j	200	°C
Storage Temperature	T_{stg}	−65 to +200	°C

*Pulse PW ≦ 300 μs, duty cycle ≦ 10 %

ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Cutoff Current	I_{CEX}			100	μA	V_{CE} = 500 V, $V_{BE(OFF)}$ = −1.5 V
Emitter Cutoff Current	I_{EBO}			100	μA	V_{EB} = 5.0 V, I_C = 0
DC Current Gain	h_{FE1}	15		100		V_{CE} = 5.0 V, I_C = 3.0 A*
	h_{FE2}	10				V_{CE} = 5.0 V, I_C = 5.0 A*
Collector Saturation Voltage	$V_{CE(sat)}$			1.0	V	I_C = 5.0 A *
Base Saturation Voltage	$V_{BE(sat)}$			1.5	V	I_B = 1.0 A
Turn On Time	t_{on}			1.0	μs	I_C = 5.0 A, I_{B1} = −I_{B2} = 1.0 A
Storage Time	t_{stg}			2.0	μs	R_L = 30 Ω, V_{CC} ≃ 150 V
Fall Time	t_f			0.7	μs	

*Pulsed PW ≦ 350 μs, duty cycle ≦ 2 %

(4) Rectifying and Smoothing Circuit of Secondary Side

i) Selection of Rectifier Elements

Use 30 A schottky barrier diode 30SBO3S. Table 4 gives characteristics of this diode.

Table 4. Characteristics of 30SB03S

	Item	Symbol	Conditions	Standard
Maximum Rating	Repetitive Peak Reverse Voltage	V_{RRM}	—	30 V
	Forward Current	$I_{F(AV)}$	$T_C = 64$ °C, duty cycle ≦ 50 %	33 A
		$I_{F(RMS)}$	—	47 A
	Junction Temperature	T_j	—	100 °C
Charac-teristics	Repetitive Peak Reverse Current	I_{RRM}	$T_j = -40$ to $+100$ °C, $V_{RM}=V_{RRM}$	150 mA
	Forward Voltage	V_{FM}	$I_{FM} = 100$ A	0.8 V
	Thermal Resistance	$R_{th(j-c)}$	between Junction and Case, DC	1.4 °C/W

ii) Choke Coil

a) Inductance of Choke Coil

from

$$L \geqq \frac{(3.5 \sim 5) \cdot (V_S - V_O) \cdot V_O \cdot T}{I_{omax.} \cdot V_S}$$

where

$$V_S = \frac{N_S}{N_P} \cdot V_{in(DC)} = \frac{3}{47} \cdot 130 \fallingdotseq 8.3 \text{ V}, \qquad I_{omax.} = 20 \text{ A}, \; T = 50 \; \mu s$$

$$L \geqq \frac{3.5 \times (8.3 \cdots 4.5) \times 4.5 \times 50 \times 10^{-6}}{20 \times 8.3} \fallingdotseq 18 \; (\mu H)$$

b) Core and Number of Turns

Considering the applicable current and the required inductance, use core FEI40-3100B of Tohoku Kinzoku giving a gap of t = 1.8 mm under DC superimposed characteristic NI = 300 AT. (AL = 181 nH)

For winding, use a copper plate (t = 0.3 mm, W = 15 mm). In this case, the number of turns is N = 12 (turns).

Therefore

$$L = AL \cdot N^2 \cdot 10^{-9} = 181 \times 12^2 \times 10^{-9} \fallingdotseq 26 \; (\mu H)$$

c) Smoothing Capacitor

In normal cases, an electrolytic capacitor is used as a smoothing capacitor. However, a capacitor of low impedance which has excellent impedance Z_C for frequencies over 10 kHz is especially desirable. For this reason, Nippon Tsusin Kogyo's "Rawimpac" is applicable.

The impedance Z_C required by the capacitor can be obtained as follows:

from

$$Z_C = \frac{V_{rip.}}{V_S} \cdot \omega \cdot L \qquad Z_C \leqq 7.9 \times 10^{-3} \; (\Omega)$$

where

$$V_S \fallingdotseq 8.3\ V,\ V_{rip.} \leqq 20\ mV,\ \omega = 2\pi f,\qquad f = 20\ kHz,\ L = 26\ \mu H$$

To satisfy the above impedance requirement, use aluminum electrolytic capacitors (10 WV, 2 200 μF X 9 (19 800 μF)).

(5) Auxiliary Power Supply Circuit

Use self-running half-bridge type DC–DC converter shown in Figure 10. With such DC–DC converter, the voltage applied to the transistor can be smaller than push-pull type power source voltage.

i) Specifications

Input Voltage (V_{in}) : 100 ~ 150 V
Output Voltage (V_{O1}): 15 V (for stabilized output)
Output Voltage (V_{O2}): 15 V (for unstabilized output)
Output Current (I_{O1}) : 50 mA (for control circuit)
Output Current (I_{O2}) : 150 mA (for driver)
Frequency : 10 kHz

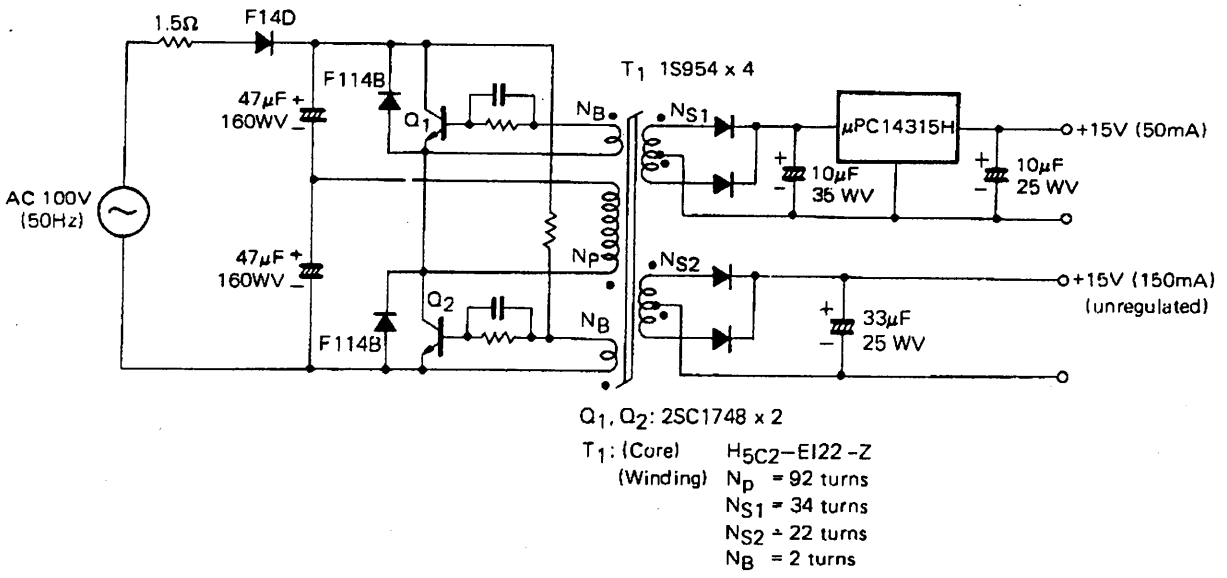


Figure 10. Schematic Diagram of Half-Bridge Type DC–DC Converter

ii) Applicable Transistor

As can be seen from the characteristics given above, the auxiliary power supply circuit requires power of approximately 3 W. As a result, a current of approximately 50 mA runs across the transistor. Therefore, use transistor 2SC1748. Table 5 presents characteristics of transistor 2SC1748.

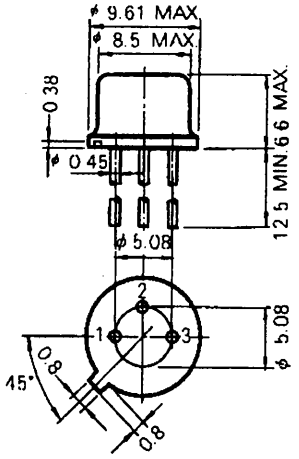
Table 5. Characteristics of 2SC1748

Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit
Collector to Base Voltage	V_{CBO}	300	V
Collector to Emitter Voltage	V_{CEO}	300	V
Emitter to Base Voltage	V_{EBO}	7.0	V
Collector Current (DC)	$I_{C(DC)}$	100	mA
Collector Current (pulse)	$I_{C(pulse)}$*	150	mA
Base Current (DC)	$I_{B(DC)}$	50	mA
Total Power Dissipation (Ta = 25 °C)	P_T	800	mW
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

* PW ≦ 10 ms, duty cycle ≦ 50 %

Package Dimensions (Unit:mm)



1. Emitter
2. Base
3. Collector (Case)

EIAJ : TC-5, TB-5B
JEDEC: TO-205MD (TO-39)
IEC : C4, B4B

Electrical Characteristics (Ta = 25 °C)

Characteristic	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Collector Cut-off Current	I_{CBO}	V_{CB} = 300 V, I_E = 0			1.0	μA
Emitter Cut-off Current	I_{EBO}	V_{EB} = 5.0 V, I_C = 0			100	nA
DC Current Gain	h_{FE}	V_{CE} = 2.0 V, I_C = 50 mA *	30	60	150	
Collector Saturation Voltage	$V_{CE(sat)}$	I_C = 50 mA, I_B = 5.0 mA *		0.12	1.0	V
Base Saturation Voltage	$V_{BE(sat)}$	I_C = 50 mA, I_B = 5.0 mA *		0.75	1.5	V
Gain-bandwidth Product	f_T	V_{CE} = 30 V, I_E = −10 mA		50		MHz
Collector Capacitance	C_{ob}	V_{CB} = 30 V, I_E = 0, f = 1.0 MHz		4.2		pF
Turn-on Time	t_{on}	I_C = 50 mA, I_{B1} = $-I_{B2}$ = 5.0 mA		0.3		μs
Storage Time	t_{stg}			3.5		μs
Turn-off Time	t_{off}			4.0		μs

* Pulsed PW ≦ 350 μs, duty cycle ≦ 2 %

iii) Design of Transformer for Converter

a) Type of Core

EI

Use core H5C2–EI22–Z of TDK for its rectangular hysterisis loop characteristic.

Effective area (A_e): 0.41 cm^2

Effective Saturation

Magnetic Flux Density (B_{ms}): 0.43 T (T_a = 25 °C)

Induction Factor (AL): 10 000 nH (at t = 0)

DC Superimposed Characteristics (NI): 0.9 AT (at t = 0)

b) Number of Turns and Diameter of Winding

Number of turns (N_p) of the primary winding is as follows:

from

$$Np = \frac{V_{in}}{4 \cdot B_{ms} \cdot A_e \cdot f}$$

$$Np = \frac{65}{4 \times 0.43 \times 0.41 \times 10^{-4} \times 10 \times 10^{3}} \fallingdotseq 92 \text{ turns}$$

Diameter of winding for the primary winding is as follows:
from

$$D_P \geqq \sqrt{\frac{4 I_{c(av)}}{\pi \delta}}, \quad I_{c(av)} = \frac{\frac{P_o}{7}}{V_{in}}$$

$$I_{c(av)} = \frac{\frac{3}{0.70}}{50} \fallingdotseq 86 \text{ mA} \quad (\text{supposing } \eta = 70\ \%)$$

therefore

$$D_P \geqq \sqrt{\frac{4 \times 86 \times 10^{-3}}{\pi \times 2 \times 10^{6}}} \fallingdotseq 0.23 \text{ mm}\phi$$

Numbers of turns (N_{S1} and N_{S2}) of the secondary winding are as follows:
from

$$N_{S1} = \frac{V_{S1}}{V_{in}} \cdot N_P, \quad V_S = V_{o1} + 2.5 + 0.7$$

$$N_{S1} = \frac{15 + 2.5 + 0.7}{50} \times 92 \fallingdotseq 34 \text{ turns}$$

and from

$$N_{S2} = \frac{V_{S2}}{V_{in}} \cdot N_P$$

$$N_{S2} = \frac{15}{65} \times 92 \fallingdotseq 22 \text{ turns}$$

Wire diameters (D_{S1} and D_{S2}) of the secondary winding are as follows:
from

$$D_{S1} \geqq \sqrt{\frac{4 I_{S1(av)}}{\pi \delta}}, \quad I_{S1(av)} = I_{o1} = 50 \text{ mA}$$

$$D_{S1} = \sqrt{\frac{4 \times 50 \times 10^{-3}}{\pi \times 2 \times 10^{6}}} \fallingdotseq 0.18 \text{ mm}\phi$$

and from

$$D_{S2} = \sqrt{\frac{4 I_{S2(av)}}{\pi \delta}}, \quad I_{S2(av)} = I_{o2} = 150 \text{ mA}$$

$$D_{S2} = \sqrt{\frac{4 \times 150 \times 10^{-3}}{\pi \times 2 \times 10^{6}}} \fallingdotseq 0.30 \text{ mm}\phi$$

c) Core Gap and Inductance

The core for a converter is used with saturated magnetic flux.

When fixing the EI core, the gap should be kept as small as possible to reduce the exciting current by striking the contacting surfaces to each other.

Inductance L_P of the primary winding is,

from

$$L_P = AL \cdot N_P^2 \cdot 10^{-9}$$

$$L_P = 10000 \times 92^2 \times 10^{-9} \fallingdotseq 85 \text{ (mH)}$$

Therefore, exciting current I_{PK} is

from

$$I_{PK} = \frac{V_{in}}{L_P} \cdot \tau$$

$$I_{PK} = \frac{65}{85 \times 10^{-3}} \times 50 \times 10^{-6} \fallingdotseq 38 \text{ mA}$$

(6) Base Driving Circuit

As shown in Figure 11, pulse transformer is used in base driving circuit for the current amplification.

i) Design of Transformer

a) Core

Use core H_{5A}–EI22–Z of TDK.

Effective Area (A_e): 0.41 cm^2

Magnetic Path Length (1_e): 4.42 cm

DC Superimposed Characteristics ($NI/1_e$): Approx. 2.5 A/cm

AL-Value (AL): 600 nH (at t = 60 μm, $\mu_{rev.} = 500$)

b) Base Current I_B

Base current I_B can be obtained in relation to the drive ratio ($I_{Cmax.}/I_B \fallingdotseq 5 \sim 10$) with the maximum collector current.

from $$\frac{P_O}{\eta} = \frac{\tau}{T} \cdot I_{Cmax.(av)} \cdot V_{in}$$

$$I_{Cmax.(av)} = \frac{P_O}{\eta} \cdot \frac{T}{\tau} \cdot \frac{1}{V_{in}} = \frac{110}{0.75} \cdot \frac{50}{44} \cdot \frac{1}{100} \fallingdotseq 1.67 \text{ (A)}$$

where

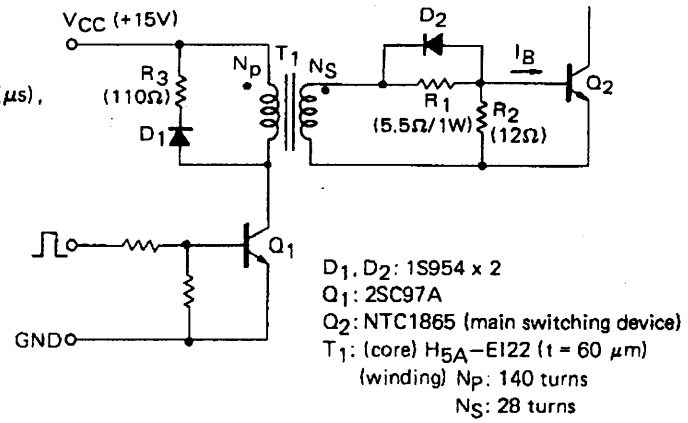
$P_O = V_O \times I_O = 5.5 \times 20 = 110$ (W),

$\eta = 75$ %, T = 50 μs, $\tau = 22 \times 2 = 44$ (μs),

$V_{in} = 100$ V (min.)

Therefore

$$I_B = \frac{I_{Cmax.}}{5} \fallingdotseq \frac{1.67}{5} \fallingdotseq 350 \text{ (mA)}$$



D_1, D_2: 1S954 x 2
Q_1: 2SC97A
Q_2: NTC1865 (main switching device)
T_1: (core) H_{5A}–EI22 (t = 60 μm)
(winding) N_P: 140 turns
N_S: 28 turns

Figure 11. Base Driving Circuit

c) Number of Turns and Diameter of Winding

The primary winding requires the maximum number of turns to make the loss caused by exciting current small. Therefore, it is represented as following.

$N_P = 140$ (turns)

The number of turns for the secondary winding is,

from

$$N_S = \frac{V_S}{V_{CC}} \cdot N_P, \quad N_S = 28 \text{ (turns)}$$

where

$V_S = 3$ V, and $V_{CC} = 15$ V

Diameters of Windings are as follows:

Diameter (D_p) of Primary Winding : 0.2 mm

Diameter (D_s) of Secondary Winding: 0.4 mm

(7) Overcurrent Sensing Circuit

According to the test result, details of the current transformer for the overcurrent detector circuit are as follows:

i) Applicable Core

H_{5C2} T14.5–20–7.5 of TDK

ii) Number of Turns and Diameter of Winding

N_p: 3 (turns)

N_s : 150 (turns)

D_p: 0.8 mm

D_s : 0.4 mm

iii) Sensing Sensitivity

With the component parts given above, the test results are as follows:

Detection Sensitivity: 1.64 V/A

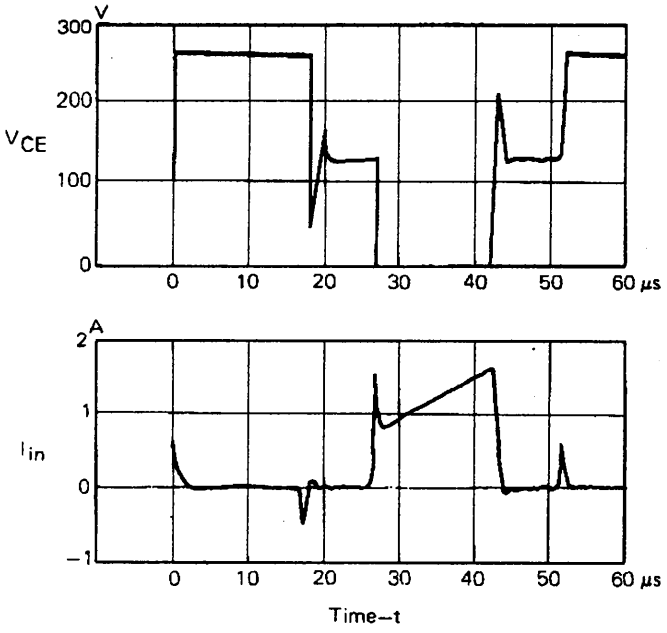
Sag (Droop: D) : 2.4 % (where $I_{in} = \sim 5$ A and $\tau = 20$ μs)

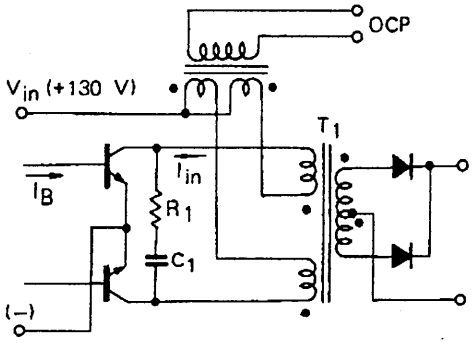
3-4 Operating Waveform

Figure 12 shows the operating waveform of the trial-manufactured switching regulator with actual loading.

The surge voltage applied to a transistor is due to the leakage inductance of transformer T_1. Thus, the surge absorbing circuit (C and R) is required to prevent the surge voltage from exceeding the breakdown voltage of the transistor.

In this circuit design, inductance L_p of the primary side of transformer T_1 is set to 2.67 mH. If a margin is left for the DC superimposed characteristics, gap t of transformer T_1 can be set to 40 μm ($L_p = 5$ mH).





R_1, C_1: Surge Absorption Circuit
R_1 = 430 Ω, 2 W
C_1 = 1 000 pF, 1.4 kWV

Conditions
Input Voltage : 100 V (AC 50 Hz)
Output Voltage: 5 V
Output Current: 20 A (full load)

Figure 12. Operating Waveforms of Switching Regulator

4. CONCLUSION

We have given general descriptions on examples of the switching regulator design. We are not able to touch on the design of the heat sink for lack of space.

For the trial-manufactured circuits in this technical data sheet, we have not finished the examinations of transient response and temperature characteristics. In addition, the circuit constants are not suited for mass-production of the circuit, due to the lack of consideration of the deviation and temperature characteristic of the component parts.

It is noted that we cannot take the responsibility for any claim or suit on the patent right regarding the circuit illustrated in this technical data sheet.

[redacted]

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