

RZ/N2L Power Requirements

Design of Power Supply Circuit for RZ/N2L using DA9083

Introduction

This document describes all the register default settings of the DA9083-31UUx for supplying power for the RZ/N2L MPU.

DA9083-31UUx's features and functionality are offered in a compact 36-lead WLCSP package (2.495 mm x 2.495 mm with a 0.4 mm pitch) to target small design solutions.

As an alternative, the RZ/N2L MPU can be supported by DA9080-61FCB2 which is a 32-lead UQFN package (5.0 mm x 5.0 mm with a 0.5 mm pitch).

Target Device

RZ/N2L

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Terms and Definitions

CH<x>	Channel <x>, where x = 1 to 4
DVC	Dynamic voltage control
LDO	Low drop out
OTP	One time programmable
STQFN	Sawn Type Quad flat-pack no-lead (package)
WLCSP	Wafer Level Chip Scale Package

1. References

- [1] DA9083_Datasheet, Renesas Electronics.
- [2] SLG46117_Datasheet, Renesas Electronics.
- [3] RZ/N2L Group Datasheet, Renesas Electronics.
- [4] AN-PM-192_DA9080_RZN2L-RZT2L-RZT2M, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

2. Power Requirements

For power-up, 1.1 V and 1.8 V power (i.e. VDD, VCC18, and AVCC) must be supplied first, then 3.3 V power (i.e. VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to a low level during the power-up.

For Power-down, 3.3 V power (i.e. VCC33) must go down first and then 1.1 V and 1.8 V power (i.e. VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 μ s.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

A stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when the reset signal (i.e. RES#) is driven high.

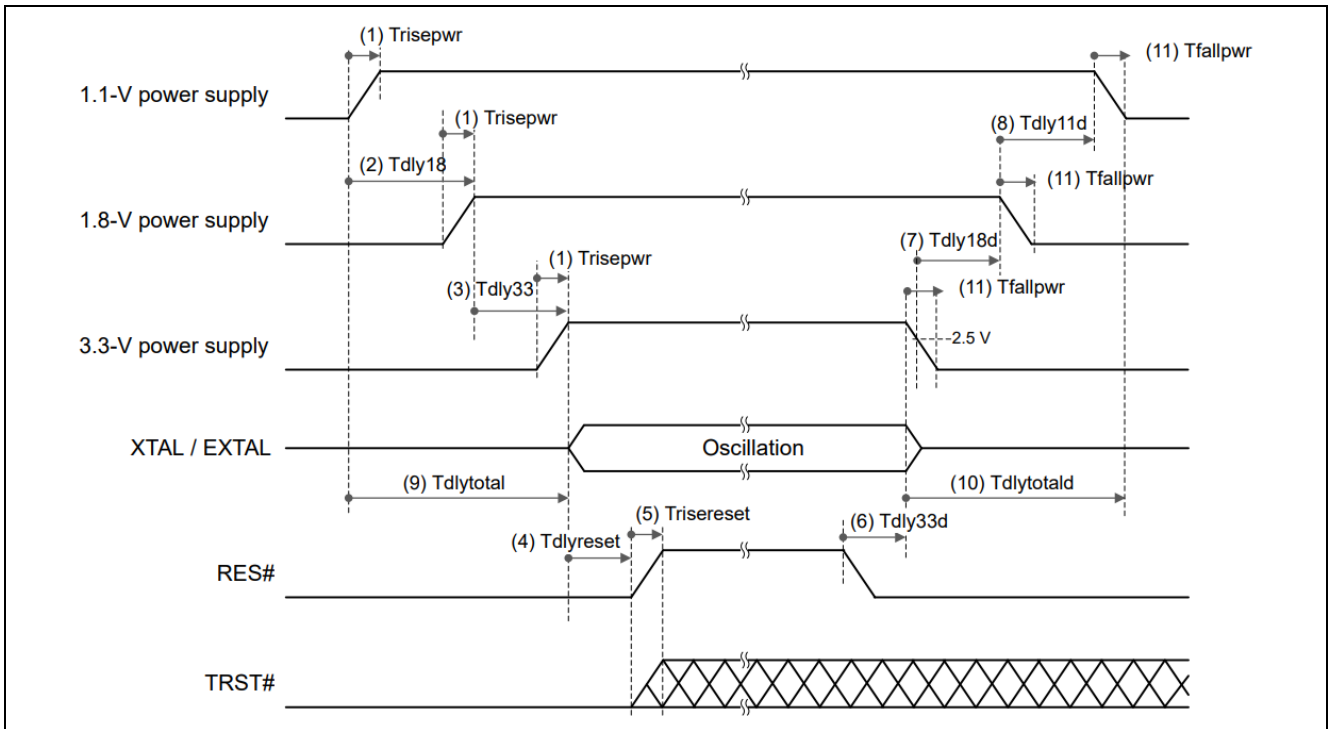


Figure 1: RZ/N2L MPU Power On/Off Sequence

3. Power Supply Tree Diagram

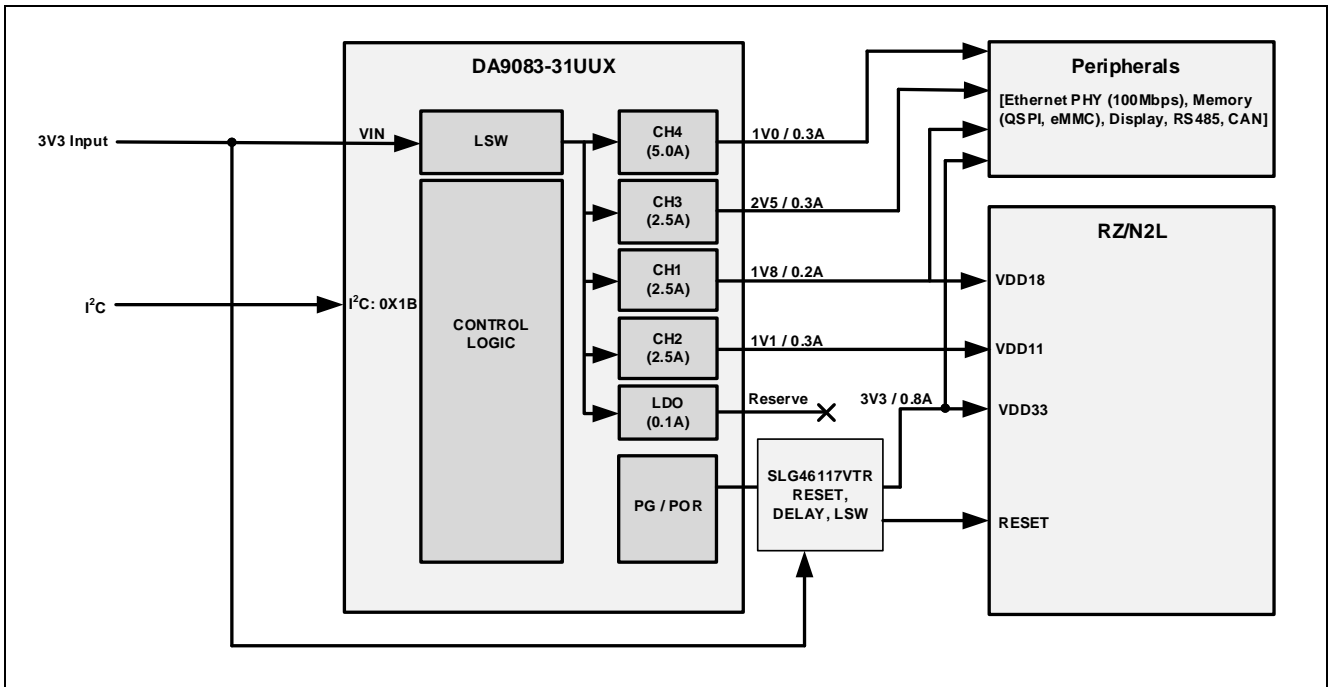


Figure 2: DA9083-31UUX, and SLG46117VTR – RZ/N2L Power Tree

4. Power On/Off Sequences

Ch1: Buck1 (1.8 V), Ch2: Buck2 (1.1 V), CH3: Buck3 (2.5 V), Ch4: Buck4 (1.0 V)

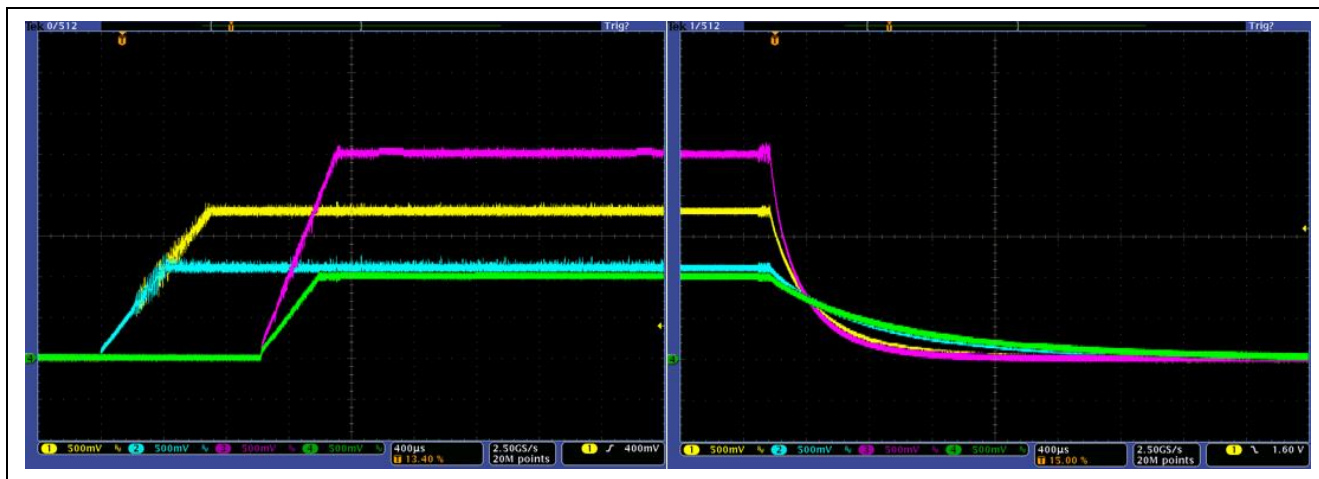


Figure 3: DA9083-31UUx Power On/Off Sequences

5. Variant Table and Ordering Information

Table 1: Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9083-31UUC	36 WLCSP	2.495 x 2.495 by 0.4 mm pitch	Tape & Reel	3000
DA9083-31UU6	36 WLCSP	2.495 x 2.495 by 0.4 mm pitch	Waffle Tray	500
SLG46117VTR	STQFN 14L	1.6 x 2.5 by 0.4 mm pitch	Tape and Reel	3000

6. Detailed Description

Table 2: Register Settings DA9083-31UUx

Register Address	Function	Default Value	Description
0x03	PMC_CH1_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x05	PMC_CH2_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x07	PMC_CH3_CFG_REG	0xEA	ILmax = 6 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x09	PMC_CH4_CFG_REG	0xAA	ILmax = 8.5 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x0B	PMC_LDO_SEL_REG	0xA0	VLDO = 1.80 V
0x0F	PMC_DCDCCTRL0_REG0	0x00	LSW enable, CH<x> enables and LDO enable controlled by the Sequencer
0x10	PMC_SLEEP_REG0	0x00	SLEEP settings not configured
0x11	PMC_DCDCCTRL1_REG	0x00	CH<x> operating in AUTO mode
0x12	PMC_DISCHARGE_REG0	0xFC	LSW, CH<x> and LDO discharge enabled

Register Address	Function	Default Value	Description
0x13	PMC_DCDCCTRL2_REG	0x00	CH<x> and LDO operating in Higher Power mode
0x14	PMC_CH1CH2_WAKEUP_TIME	0x11	CH1 = SLOT1, CH2 = SLOT1
0x15	PMC_CH3CH4_WAKEUP_TIME	0x33	CH3 = SLOT3, CH3 = SLOT3
0x16	PMC_LDO_WAKEUP_TIME	0x10	LDO = SLOT1
0x1B	PMC_IRQ_MASK0	0x00	No IRQ events masked
0x1C	PMC_IRQ_MASK1	0x00	No IRQ events masked
0x1D	PMC_IRQ_MASK2	0x00	No IRQ events masked
0x1E	PMC_VOUT_CH1	0xB4	VCH1 = 1.80 V
0x1F	PMC_VOUT_CH2	0x6E	VCH2 = 1.10 V
0x20	PMC_VOUT_CH3	0x7D	VCH3 = 2.50 V
0x21	PMC_VOUT_CH4	0x64	VCH4 = 1.00 V
0x4C	BUCK_BUCK_OPT_04	0x00	Divider mode disabled VCH1 range = 0.5 V to 1.9 V
0x4D	BUCK_BUCK_OPT_05	0x00	Divider mode disabled VCH2 range = 0.5 V to 1.9 V
0x4E	BUCK_BUCK_OPT_06	0x40	Divider mode enabled VCH3 range = 1.5 V to 2.7 V
0x4F	BUCK_BUCK_OPT_07	0x00	Divider mode disabled VCH4 range = 0.5 V to 1.9 V
0x62	OTP_CONFIG_ID	0x31	OTP variant number: DA9083-31UUx

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Aug 28, 2024	—	Initial version.
2.0	May 17, 2024	All	Updated to show support for RZ/N2L MPU. Used new template.

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