Renesas RX and RA Families

Design Guide for Main Clock Circuits and Sub-Clock Circuits

Introduction

This application note introduces recommended resonators for the RX and RA families along with the relevant resonator matching evaluation results, oscillation evaluation methods, and some recommendations on board design as information for the design of the main clock oscillation circuit and the sub-clock oscillation circuit.

Target Device

RX and RA families

Contents

1. Using the Application Note

This application note is intended for those who are considering how to select or evaluate an external resonator connected to RX and RA microcontroller (MCU) device families. Since it is difficult to select the optimal resonator yourself, we recommend that you ask the resonator manufacturer to perform the matching evaluation. For details, see each chapter.

- Chapter 2: This Chapter provides information on the external components connected to the RX and RA families clock systems.
- Chapter 3: This chapter introduces resonator manufacturers who have performed resonator matching evaluations with RX and RA and explains how to search for suitable resonators for RX and RA on their website (Tool). If you wish to select a resonator that has already been evaluated, refer to this chapter.
- Chapter 4: This chapter describes the resonator characteristics and provides information on the proposed components mounted on the board based on the evaluation. Refer to this chapter if you want to narrow down the resonator selection conditions.
- Chapter 5: This chapter describes how to select and evaluate external components to stabilize oscillation.
- Chapter 6: This chapter describes the key points of the board design. Read this chapter before designing a board.
- Chapter 7: This chapter describes the method for measuring clock frequency accuracy on MCU board products.

2. Connecting External Components

Most RX and RA MCUs support the use of a ceramic or crystal resonator as the main clock source, as shown in Figure 1. This should be connected between EXTAL and XTAL pins of the MCU. Note that for some MCU groups, the pin names EXTAL and XTAL may be replaced with X2 and X1. A crystal resonator can be used as the sub-clock source, which should be connected between XCIN and XCOUT pins of the MCU.

The frequency of the external resonator for the main clock source should be within the range specified as the oscillator frequency of the main clock oscillator of the MCU. The frequency of the external resonator for the sub-clock source must be exactly 32.768 kHz. For details, refer to "Electrical Characteristics" and "Clock Generation Circuit" in the MCU User's Manual: Hardware.

The damping register (R_d) and the load capacitors (C_{L1}, C_{L2}) are typically specified by the resonator manufacturer, and must be implemented as external components. When selecting external components, we recommend that you contact the resonator manufacturer for a matching evaluation. If you prefer to calculate suitable capacitances by yourself, refer to Chapter 5 "Oscillation Evaluation and Oscillation Circuit Constant Calculation Method".

Since RX and RA MCU have a built-in feedback resistor, it is not necessary to implement the feedback resistor (*) shown in Figure 1. However, if the resonator manufacturer recommends implementing the feedback resistor, follow the resonator manufacturer’s instructions.

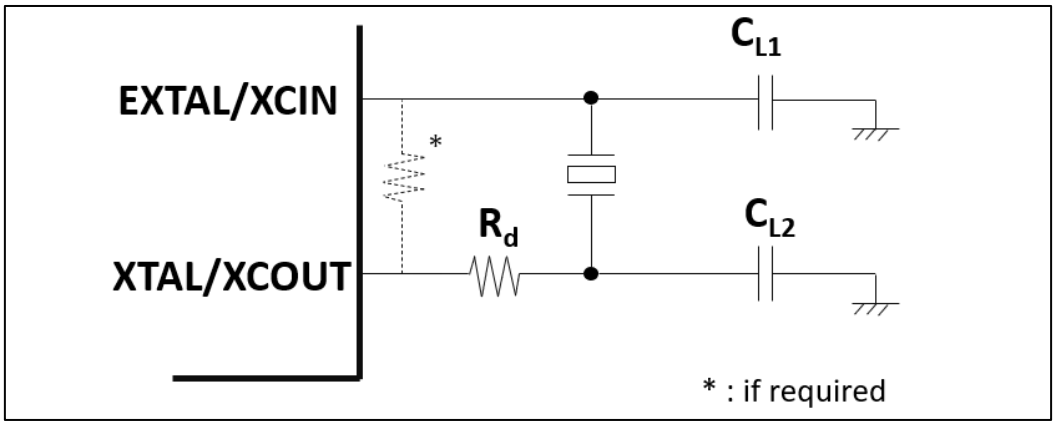

Figure 1. Connection Example of External Resonator

3. Introduction of resonator manufacturers that Renesas has requested matching evaluations from

Several resonator manufacturers have performed evaluations of the RX and RA family's oscillator circuits, and publish a list of suitable resonators for some of the RX or RA families. Table 1 shows some examples of resonators for which an evaluation has been performed. For the latest information, visit the resonator manufacturers' website.

If you cannot find the targeted MCU on the oscillator manufacturer's website :

Search for the target MCU from Table 2 and then Search the MCUs in the same group on the oscillator manufacturer's web.

Table 1. Example Resonator List with Matching Evaluated

Manufacturer	Resonator/Part Number	Oscillation frequency	Circuit-load capacitance (pF)	C_{L1} (pF)	C_{L2} (pF)	R_d (ohm)	MCU group name
Kyocera Corporation	CX3225CA12000D0PRTC2	12 MHz	6.49	10	10	4700	RX72T, RX66T
Murata Manufacturing	XRCGB24M000F3M26R0	24 MHz	6	8	8	0	RX72M, RX72N, RX66N, RX671
NIHON DEMPA KOGYO CO., LTD.	STD-MUA-9	32.768 kHz	9	12	12	0	RX660
Seiko Instruments Inc.	SSP-T7-F	32.768 kHz	12.5	22	22	0	RA2L1

The following shows how to search for a resonator matching the RX and RA families on the resonator manufacturers' website.

- Kyocera Corporation:

Search Page: Crystal Units vs. IC Matching Search

1) Select "Renesas Electronics" from the dropdown of IC Manufacturers.
2) Select the group-name from the dropdown of IC family.
   Ex.) IC family: RX72N
3) Press the search button. The corresponding data is displayed.

■ Murata Manufacturing Co., Ltd.

Search page: IC-Timing Device Search Tool

1) Select "Renesas Electronics" from the dropdown of IC manufacturers.

2) Select the group name from the dropdown of IC Part Numbers.

Ex.) IC Part Number: RX72N

3) Press the search button. The corresponding data is displayed.

■ NIHON DEMPA KOGYO CO., LTD.:

Search page: IC Matching Information

1) Select "Renesas Electronics" in Supplier Name checkboxes.

2) Click the PDF icon in the row whose Families/Series is the group you want to know about.

Ex) Select RX660.

The corresponding data is displayed.

■ Seiko Instruments Inc.:

Search page: IC Matching Information

1) Click the group name you want to know about. The corresponding data is displayed.

The matching parameters of the oscillator circuit published on the website of the resonator manufacturers are the experimental results of some samples under certain conditions, and Renesas do not guarantee them. Optimal parameters may be different for each user's actual system. Renesas recommends that users contact the resonator manufacturers for a matching evaluation of their specific system to determine the oscillator circuit parameters required.

The operating conditions of the MCU described on their website are used to stabilize the oscillation of their resonator in the evaluation and are not the recommended conditions by Renesas. For the recommended operating conditions for MCU, refer to "Electrical Characteristics" in MCU User's Manual: Hardware.

4. Matching evaluation results

This chapter shows the evaluation results from several resonator manufacturers. Table 3 through Table 15 and Figure 2 through show the drive capability setting of MCU, the specification of the resonator (Frequency, C_L), the parameters of external components mounted on the evaluation board (R_d, C_{L1}, C_{L2}), and the evaluation results (Negative R, recommended ESR, V_{oh} [1] and V_{ol} [1]).

Note that these results are based on experimentation under typical conditions with some samples and are not guaranteed under all conditions.

Table 2. The matching evaluation Group

Group	RX	RA
1	RX65N, RX651, RX671, RX66N, RX72N and RX72M	RA4M2, RA4M3, RA4E1, RA4E2 [2], RA4T1 [2], RA6M1, RA6M2, RA6M3, RA6M4, RA6M5, RA6T1, RA6T2 [3], RA6T3 [3], RA6E1 and RA6E2 [2]
2	RX26T [3], RX660, RX66T [3] and RX72T [3]	N/A
3	RX64M and RX71M	N/A
4	RX130, RX13T [3], RX230, RX231, RX23E-A [3] , RX23E-B, RX23T [3], RX23W, RX24T [3], and RX24U [3]	RA2A1, RA4M1 and RA4W1
5	RX111, RX110 and RX113	N/A
6	RX140	N/A
7	N/A	RA2E1 and RA2L1

1: V_{oh}, V_{ol} of the sub-clock cannot be measured when a probe is touched to the clock terminals, so there is no evaluation result.

2: 32-pin LQFP and QFN part numbers do not support their sub-clock oscillator function.

3: These groups do not include a sub-clock oscillator.

Table 3. Group 1, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
Setting = 8 MHz	8.0	8.0	0	8.0	8.0	-3760	750	2.60	-0.04
8 MHz < Setting ≦ 16 MHz	12	8.0	0	6.0	6.0	-2150	430	2.48	0.00
8 MHz < Setting ≦ 16 MHz	16	8.0	0	5.0	5.0	-1120	220	2.44	0.00
16 MHz < Setting ≦ 20 MHz	20	8.0	0	6.0	6.0	-1020	200	2.52	0.00
20 MHz < Setting ≦ 24 MHz	24	8.0	0	6.0	6.0	-1320	260	2.42	-0.04

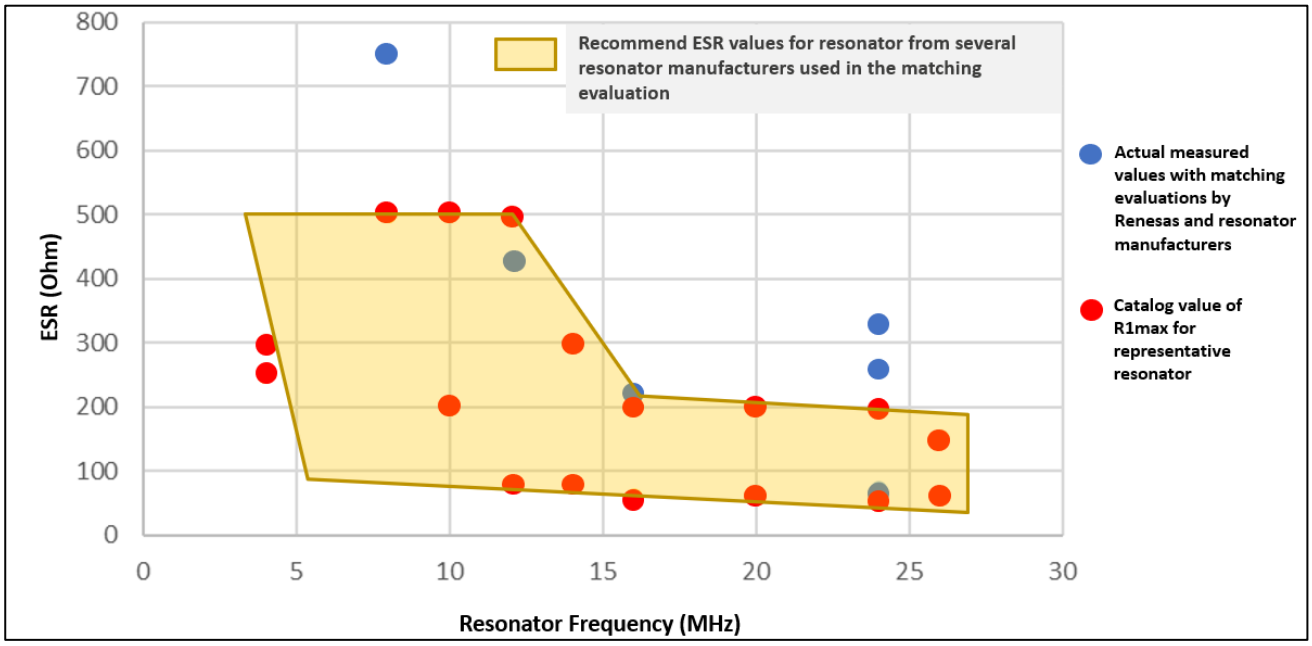

Figure 2. Group 1, Main clock: Resonator Frequency vs ESR max

Table 4. Group 1, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (kOhm)	Recommended ESR_max (kOhm)
Low C_L [6]	32	4.0	0	4.3	4.3	-510	100
	32	4.4	0	6.0	5.0	-340	60
	32	5.0	0	6.0	6.0	-370	70
	32	6.0	0	8.0	8.0	-240	40
Standard C_L [6]	32	7.0	0	12	12	-1250	250
	32	9.0	0	15	15	-840	160
	32	12.5	0	24	24	-430	80

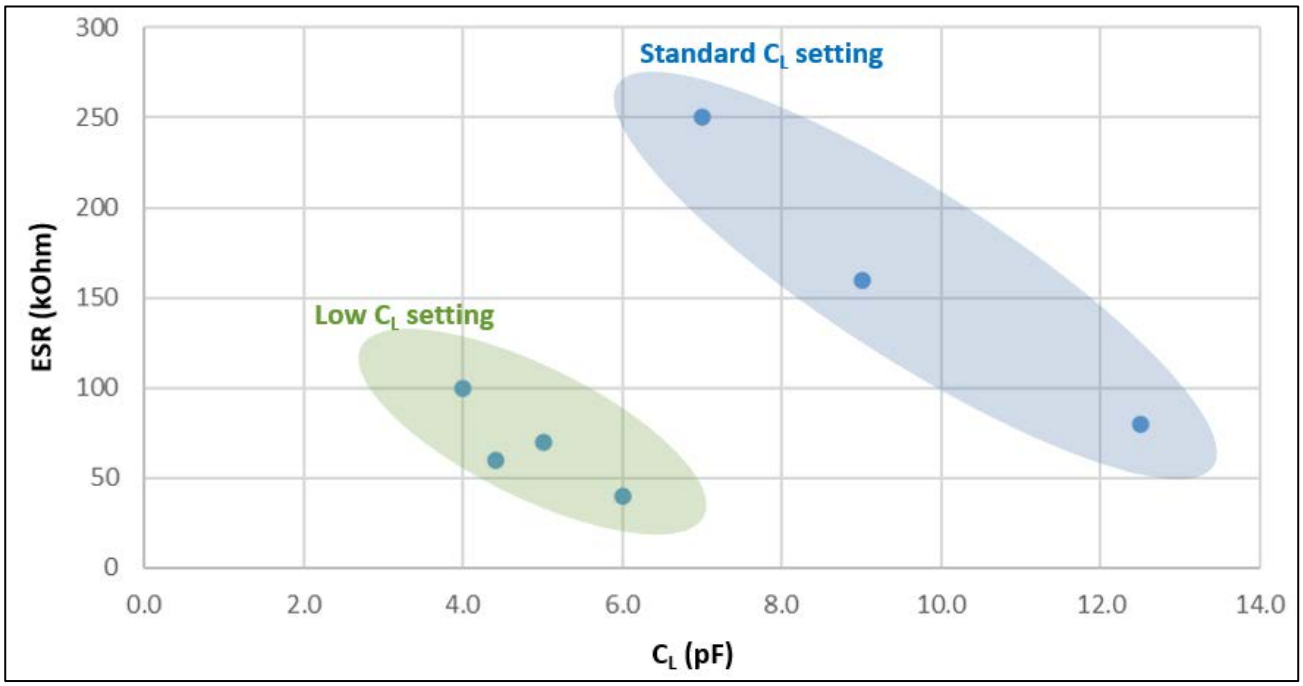

Figure 3. Group 1, Sub-clock: C_L vs ESR max

Table 5. Group 2, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
Setting = 8 MHz	8.0	8.0	4700	12	12	-1300	260	2.20	0.28
8 MHz < Setting ≦ 16 MHz	10	8.0	4700	12	12	-1150	230	2.24	0.24
	12	8.0	4700	10	10	-830	160	2.14	0.32
	16	8.0	3900	9.0	9.0	-440	80	2.00	0.48
16 MHz < Setting ≦ 20 MHz	20	8.0	3300	10	10	-240	40	1.92	0.52
20 MHz < Setting ≦ 24 MHz	24	8.0	2200	10	10	-200	40	1.88	0.52

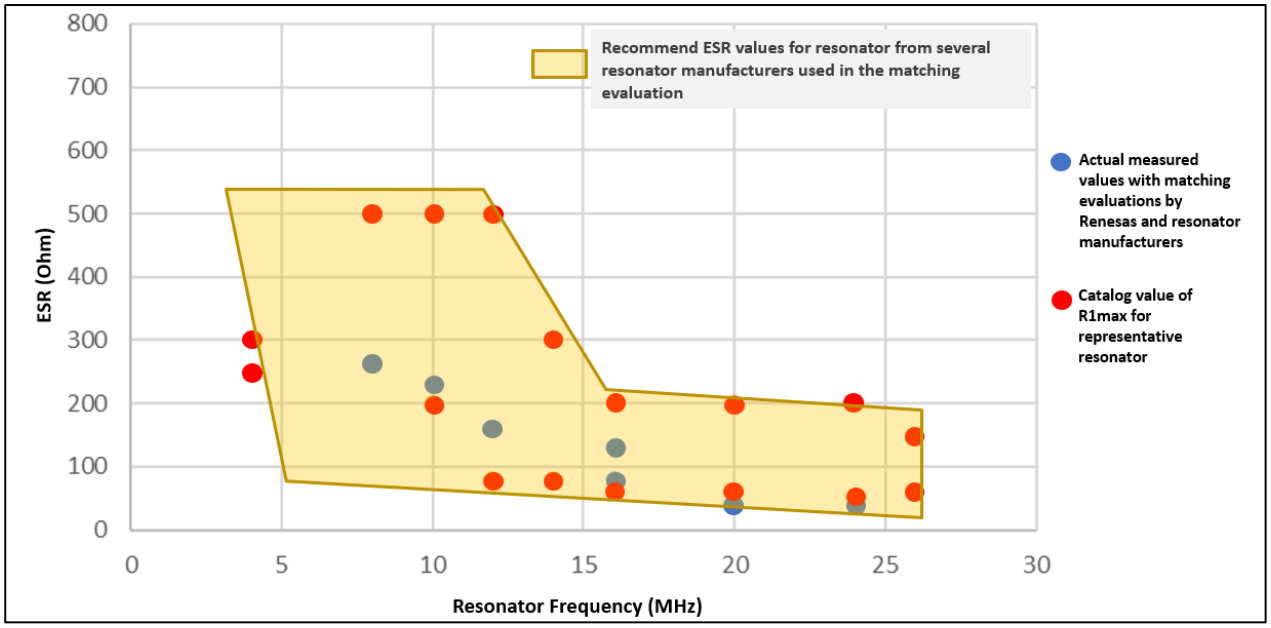

Figure 4. Group 2, Main clock: Resonator Frequency vs ESR max

Table 6. Group 2, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
Standard C_L [6]	32	7.0.	0	10	10	-930	180
	32	9.0	0	15	15	-540	100
	32	12.5	0	28	12	-310	60

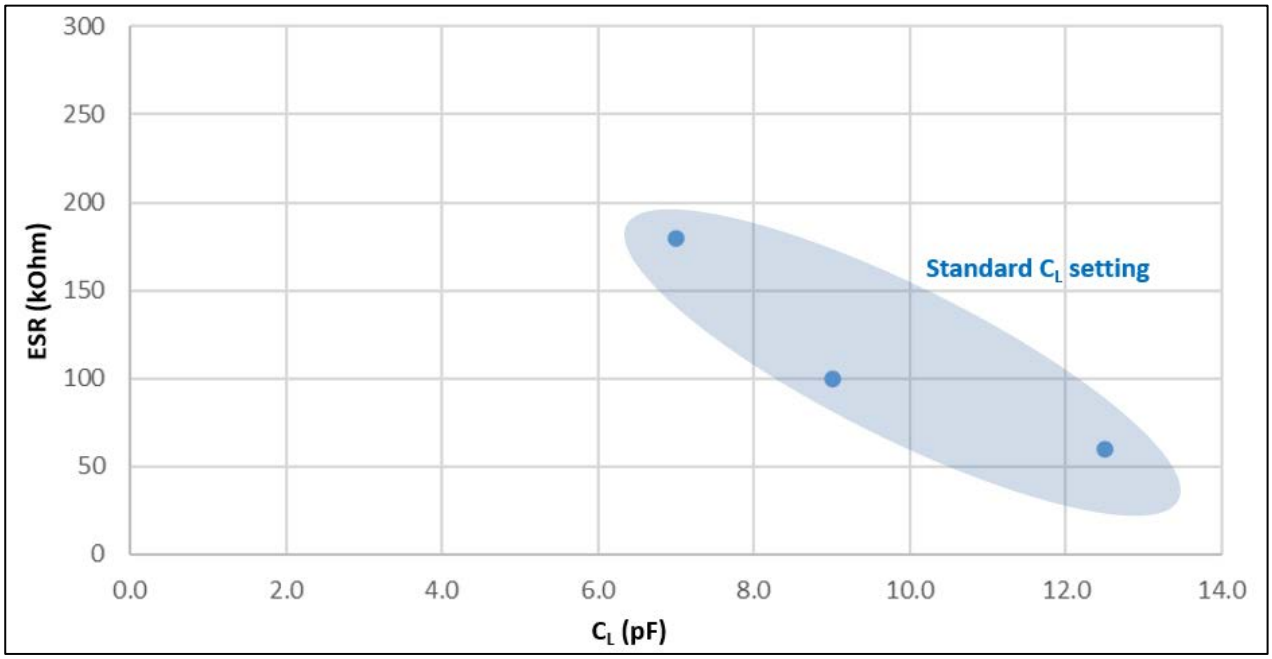

Figure 5. Group 2, Sub-clock: C_L vs ESR max

Table 7. Group 3 and Group 5, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
Setting = 8 MHz	8.0	8.0	0	8.0	8.0	-5760	1150	N/A	N/A
8 MHz < Setting ≦ 16 MHz	16	8.0	1000	7.0	7.0	-1520	300	N/A	N/A
16 MHz < Setting ≦ 20 MHz	20	8.0	1000	7.0	7.0	-1020	200	N/A	N/A
20 MHz < Setting ≦ 24 MHz	24	8.0	1000	7.0	7.0	-860	170	N/A	N/A

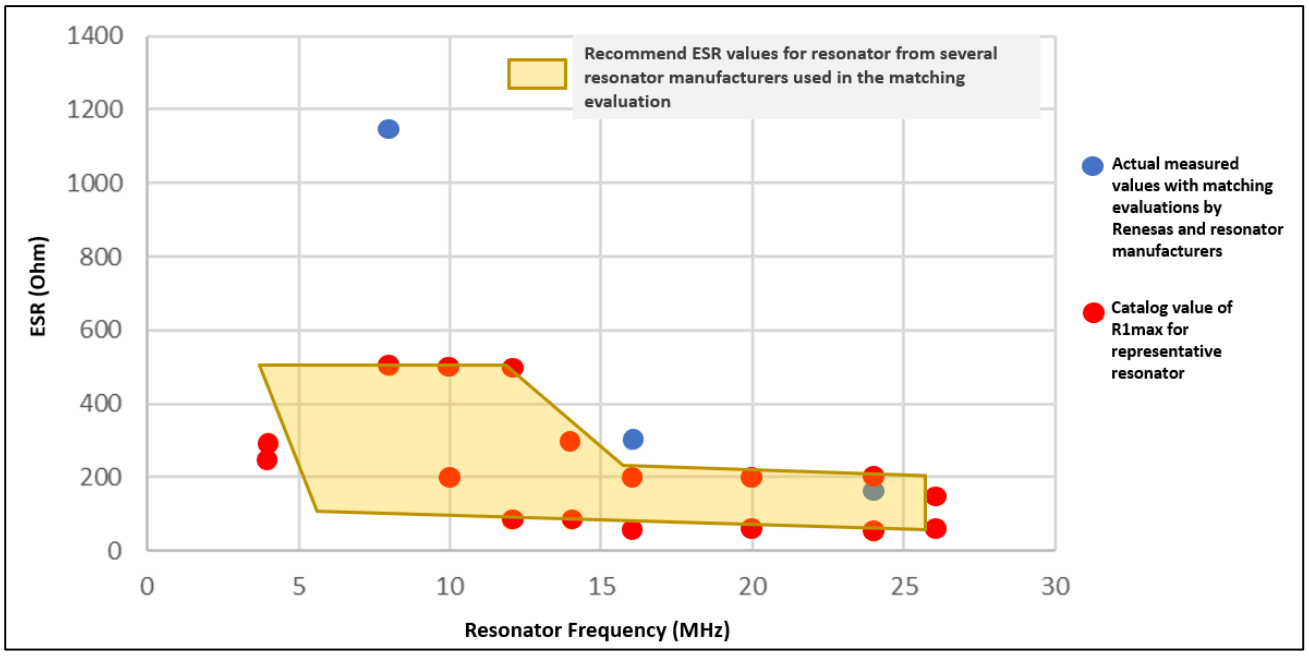

Figure 6. Group 3 and Group 5, Main clock: Resonator Frequency vs ESR max

Table 8. Group 3, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
C_L [6]	32	3.7	0	3.0	3.0	-430	80
	32	4.0	0	2.0	3.0	-570	110
Standard C_L [6]	32	7.0	0	9.0	9.0	-1000	200
	32	12.5	0	22	22	-350	70

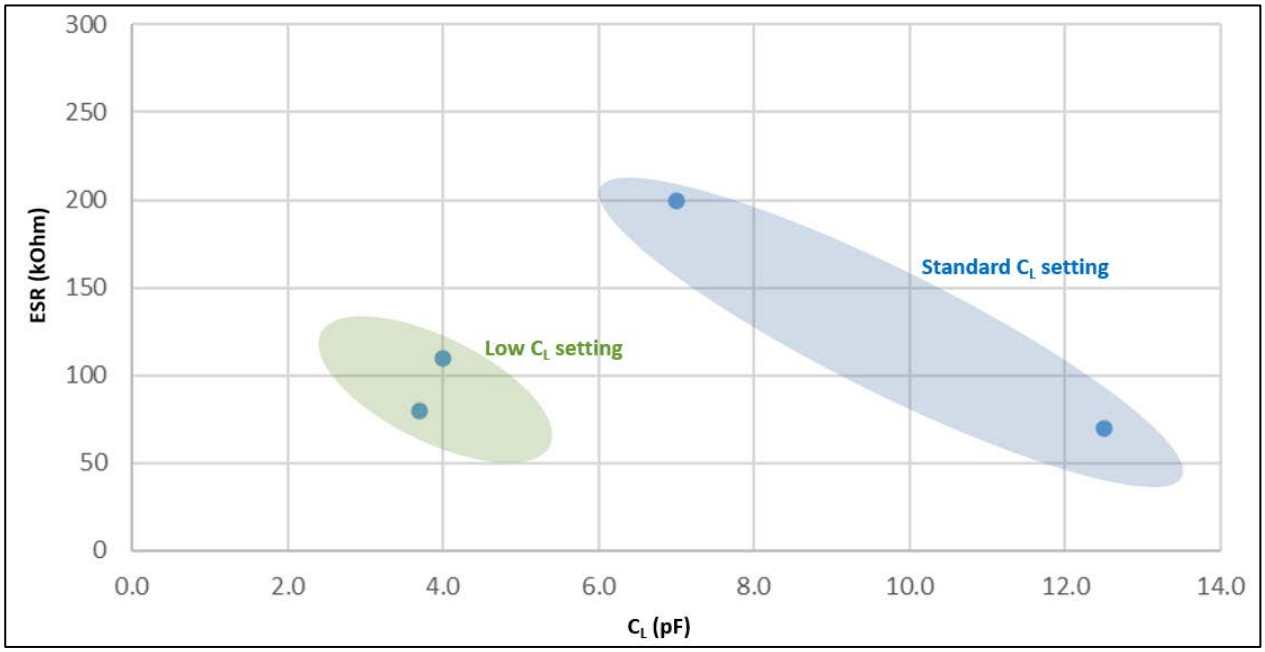

Figure 7. Group 3, Sub-clock: C_L vs ESR max

Table 9. Group 4, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
1 MHz ≦ Setting ≦ 10 MHz	4.0	8.0	0	8.0	8.0	-2500	500	N/A	N/A
	4.0	8.0	0	8.0	8.0	-2900	580	N/A	N/A
	8.0	8.0	0	10	10	-634	120	N/A	N/A
	8.0	8.0	0	6.0	6.0	-1171	230	N/A	N/A
10 MHz ≦ Setting ≦ 20 MHz	10	8.0	0	7.0	7.0	-810	160	N/A	N/A
	10	8.0	0	6.0	6.0	-1010	200	N/A	N/A
	12	8.0	0	9.0	9.0	-670	130	N/A	N/A
	16	8.0	0	9.0	9.0	-360	70	N/A	N/A
	20	8.0	0	9.0	9.0	-230	40	N/A	N/A

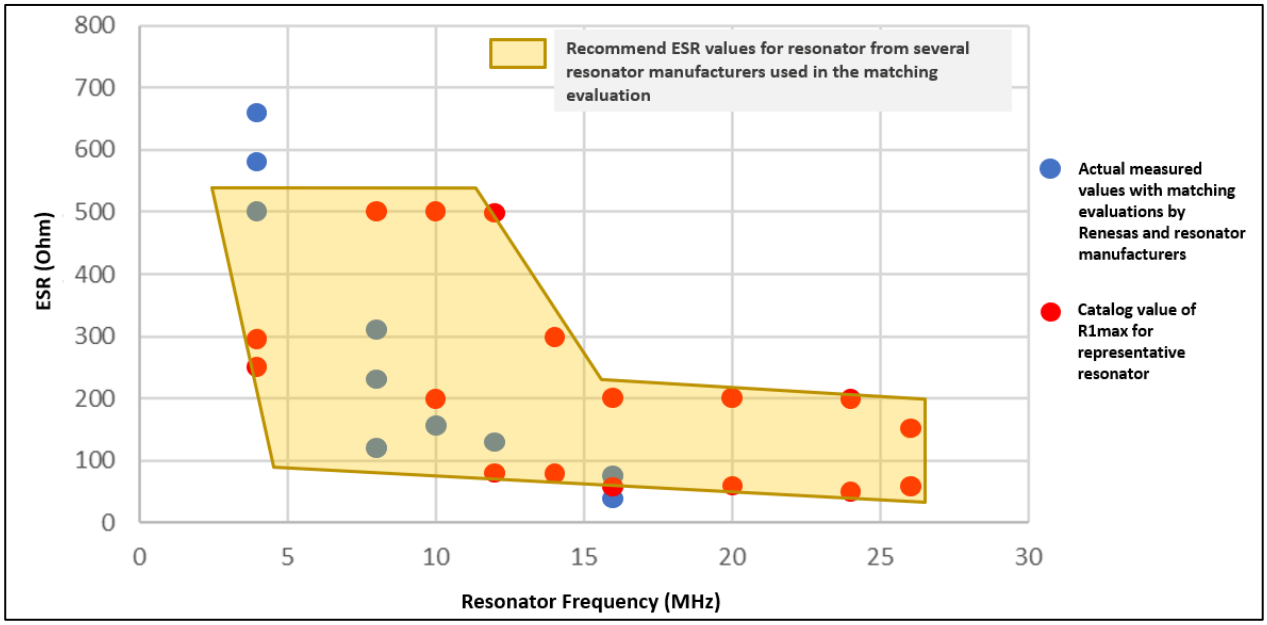

Figure 8. Group 4, Main clock: Resonator Frequency vs ESR max

Table 10. Group 4, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
Low C_L [6]	32	4.0	0	5.0	5.0	-2320	460
	32	6.0	0	9.0	9.0	-1060	210

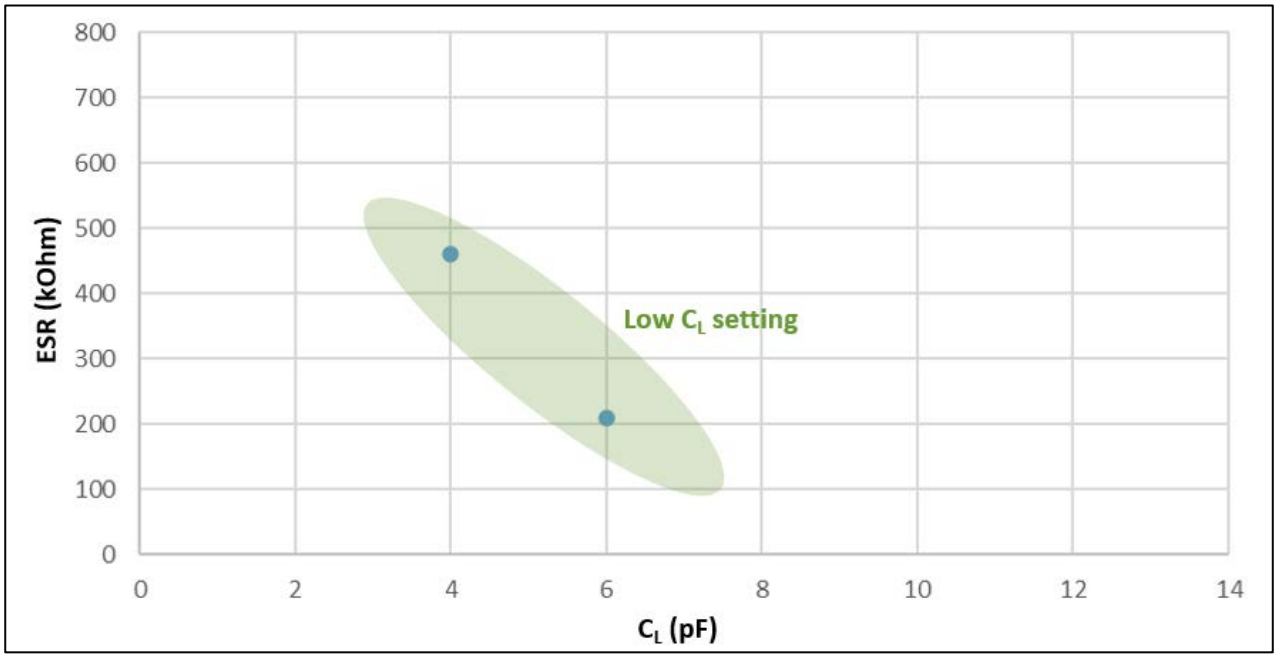

Figure 9. Group 4, Sub-clock: C_L vs ESR max

Table 11. Group 5, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
Low C_L (Low drive) [6]	32	3.7	0	4.0	4.0	-860	170
	32	4.4	0	5.0	6.0	-600	120
	32	6.0	0	9.0	9.0	-340	60
Low C_L (Medium drive) [6]	32	4.4	0	5.0	6.0	-1050	210
	32	6.0	0	9.0	9.0	-550	110
	32	7.0	0	10	12	-320	60
Low C_L (High drive) [6]	32	6.0	0	8.0	8.0	-740	140
	32	7.0	0	10	12	-450	90

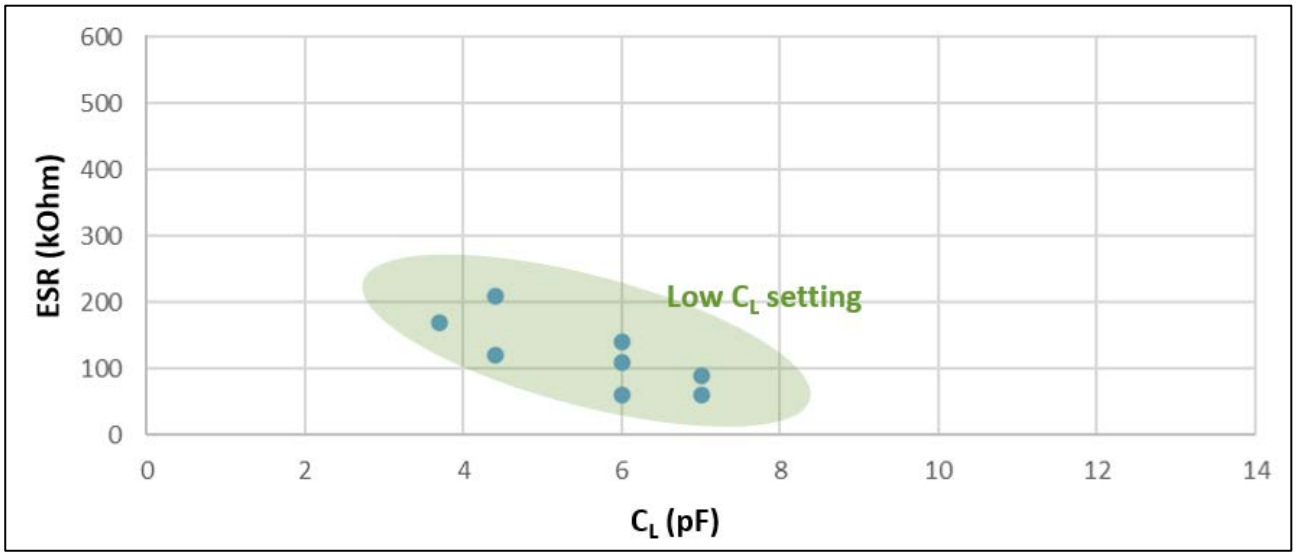

Figure 10. Group 5, Sub-clock: C_L vs ESR max

Table 12. Group 6, Main clock: Resonator Frequency vs ESR max

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
1 MHz ≦ Setting ≦ 10 MHz	8.0	6.0	330	5.0	5.0	-3440	680	1.58	0.02
10 MHz ≦ Setting ≦ 20 MHz	20	5.0	330	5.0	5.0	-1150	230	1.48	-0.04

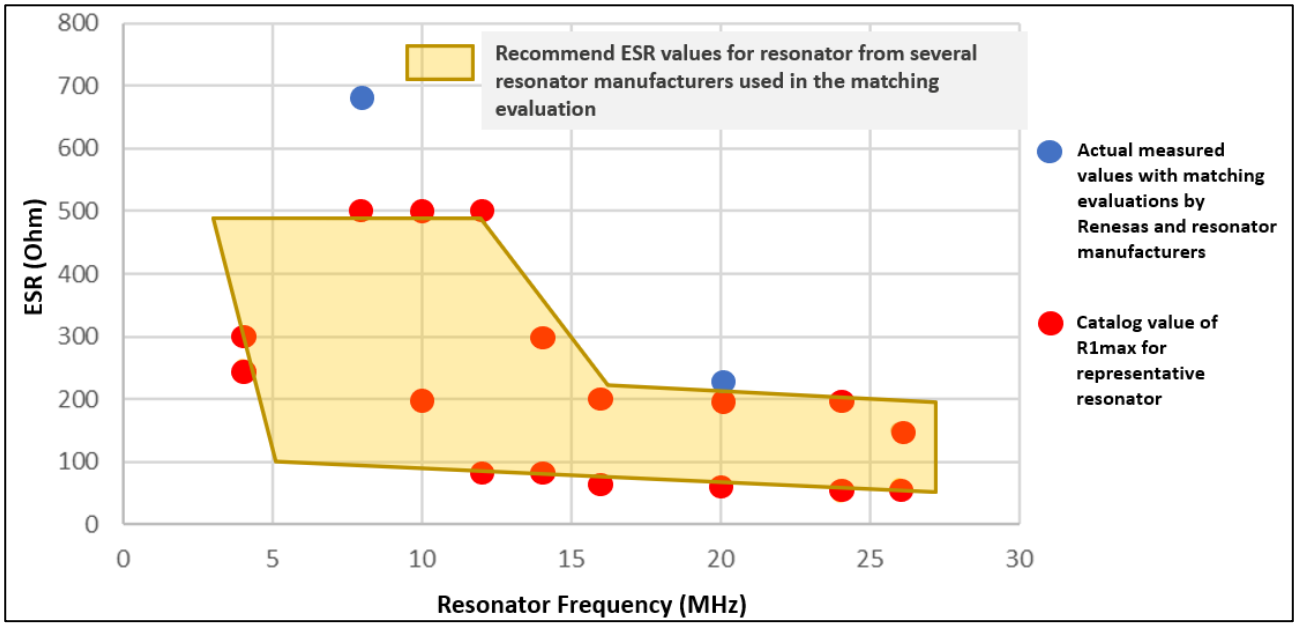

Figure 11. Group 6, Main clock: Resonator Frequency vs ESR max

Table 13. Group 6, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
Low C_L (Low drive) [6]	32	3.7	0	2.0	3.0	-340	60
	32	4.0	0	3.0	3.0	-300	60
	32	6.0	0	2.0	2.0	-290	50
Low C_L (Medium drive) [6]	32	6.0	0	7.0	7.0	-300	60
Low C_L (High drive) [6]	32	6.0	0	7.0	7.0	-610	120
	32	7.0	0	10	10	-590	110
	32	9.0	0	15	15	-350	70
Standard C_L [6]	32	6.0	0	7.0	7.0	-1340	260
	32	9.0	0	16	15	-760	150
	32	12.5	0	22	22	-420	80

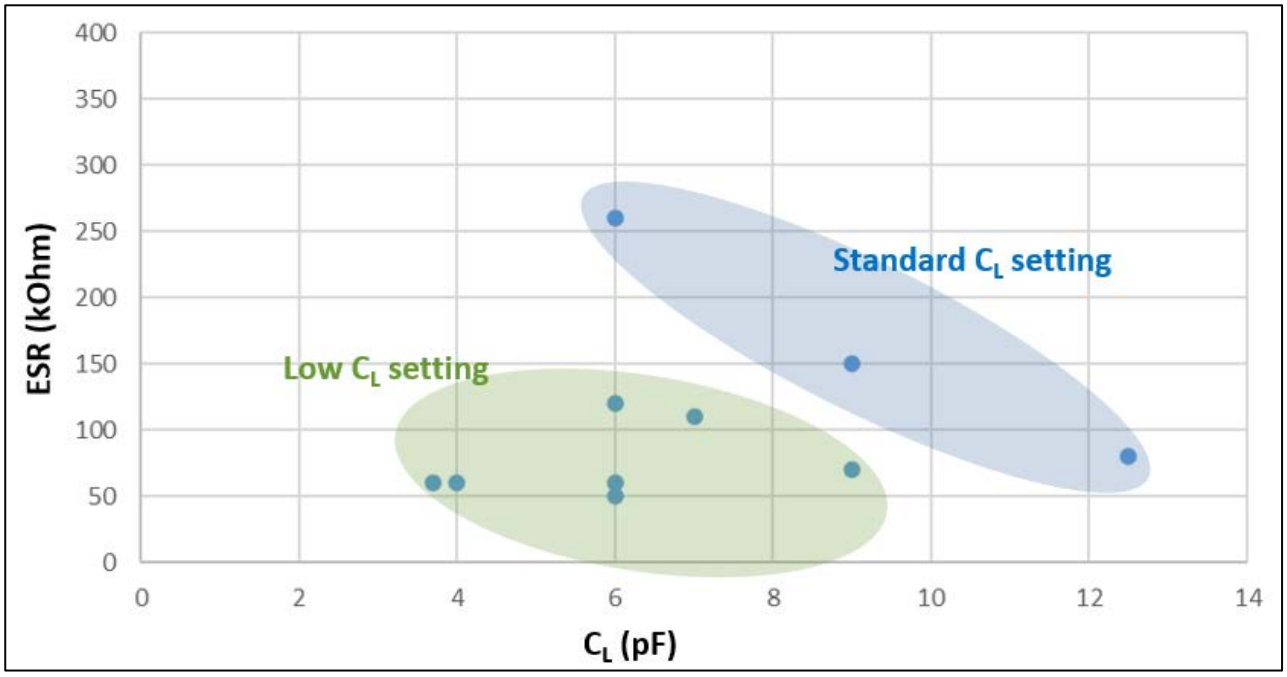

Figure 12. Group 6, Sub-clock: C_L vs ESR max

Table 14. Group 7, Main clock: Resonator Frequency vs ESR max

Main Clock Oscillator Driving Setting [4]	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V_{oh}	V_{ol}
1 MHz ≦ Setting ≦ 10 MHz	8.0	8.0	0	8.0	8.0	-2860	480	1.50	0.06
10 MHz ≦ Setting ≦ 20 MHz	12	8.0	0	8.0	8.0	-2060	410	1.54	-0.11
	16	8.0	0	8.0	8.0	-1246	240	1.56	-0.09
	20	5.0	470	4.0	4.0	-1360	270	1.53	-0.02

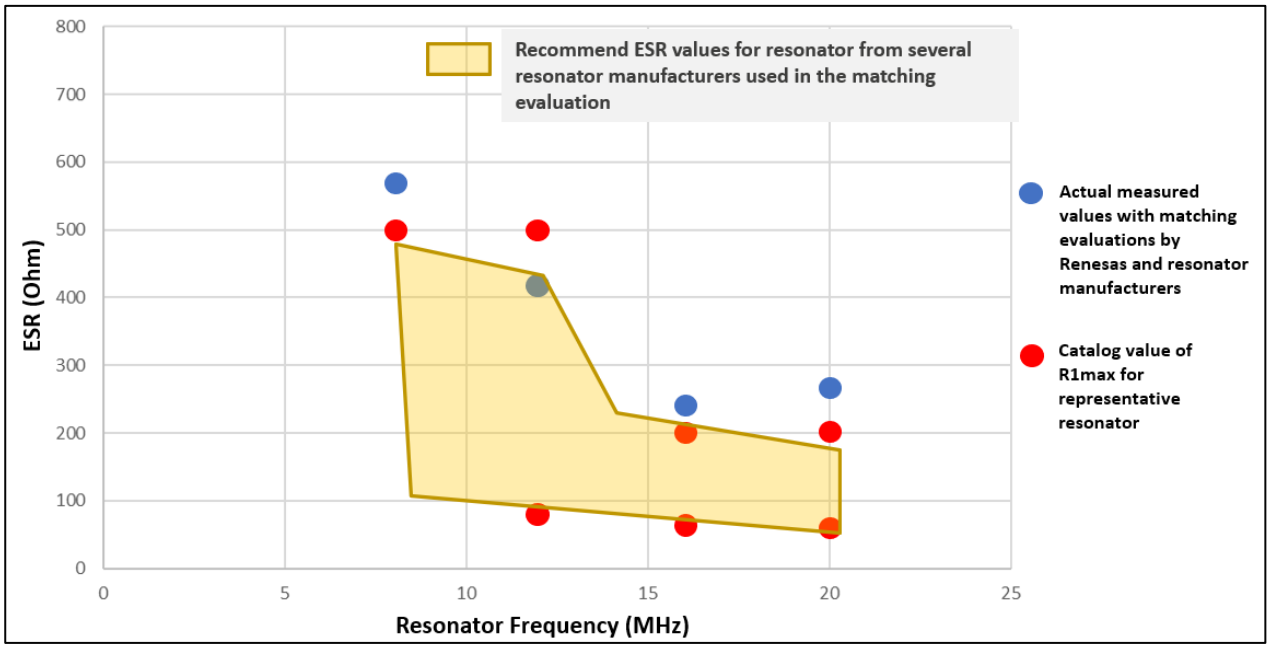

Figure 13. Group 7, Main clock: Resonator Frequency vs ESR max

Table 15. Group 7, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting [5]	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C_L (pF)	R_d (Ohm)	C_{L1} (pF)	C_{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (kOhm)
Low C_L (Low drive) [6]	32	4.0	0	4.0	4.0	-305	60
Low C_L (Medium drive) [6]	32	6.0	0	9.0	9.0	-384	70
Low C_L (High drive) [6]	32	7.0	0	10	12	-669	130
Standard C_L [6]	32	9.0	0	15	18	-672	120
	32	12.5	0	22	22	-452	80

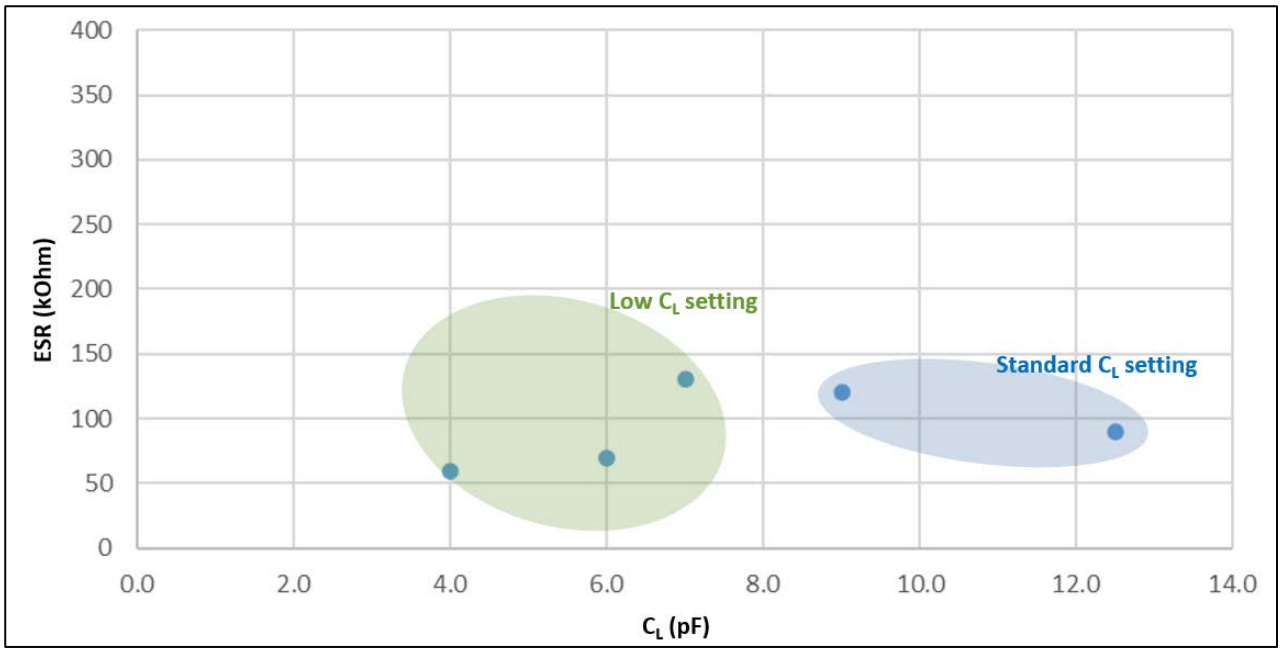

Figure 14. Group 7, Sub-clock: C_L vs ESR max

4: For the setting of the drive capability register of the main clock, refer to the "Clock Generation Circuit" chapter of the User's Manual: Hardware for both RX and RA.

Example:

RX66N: MODRV2[1:0] = b11 (Drive capability 8 MHz)
RA4E2: MODRV[1:0] = b11 (Drive capability 8 MHz)

5: Refer to the following chapter for setting of the sub-clock drive capability register.

RX: Real-time Clock in the User's Manual: Hardware
RA: Chapter "Clock Generator" in the User's Manual: Hardware

Example:

RX66N: RTCDV[2:0] = b110 (Standard C_L)

RA4E2: then SODRV[1] = b0 (Normal C_L)

6: The magnitude relationship between the drive capacity settings is as follows.

Notations used in this application note	Notations used in RX Family User's Manual	Notations used in RA Family User's Manual	Drive capability
Standard C_L	Standard C_L	Normal mode	4 (highest)
Low C_L (High drive)	Low C_L (High drive)	Low power mode 1	3
Low C_L (Medium drive)	Low C_L (Medium drive)	Low power mode 2	2
Low C_L (Low drive)	Low C_L (Low drive)	Low power mode 3	1 (minimum)

5. Oscillator matching evaluation method and oscillator circuit parameter calculation method

This chapter describes how to evaluate external components. The oscillation stability of the resonator is determined by whether the negative resistance or transconductance is sufficiently large relative to the ESR of the oscillator.

5.1 How to measure the negative resistance

To measure the negative resistance of the oscillator circuit, insert a resistor in series with the resonator as shown in , and check the maximum resistance of the resistor at which the oscillation of MCU clock output can be maintained. Use the FET probe (low capacitance, high impedance) when observing the MCU clock output waveform with an oscilloscope. It is recommended that the resistance of the series resistor be approximately five times ESR (equivalent series resistance) of the resonator.

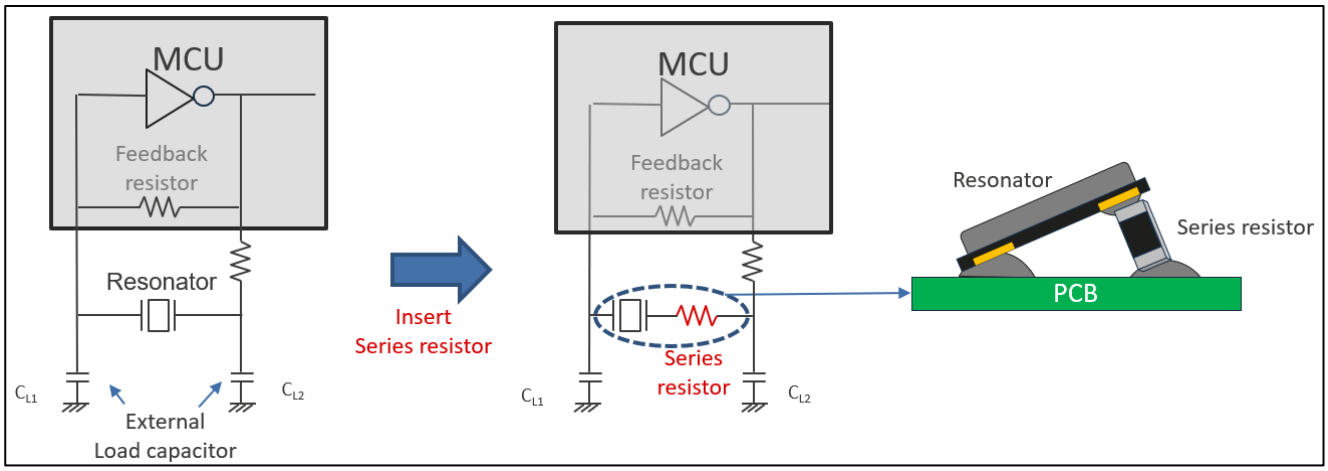

Figure 15. Measurement method of the negative resistance

5.2 Measurement method of oscillations' excitation power

The oscillations' excitation power (μW) is calculated from the oscillation current (I_{RMS}) measured by a current probe clamped to the resonator and the wire inserted between the circuit board as shown in , and the equivalent series resistance of the oscillator (R_{load}).

■ Oscillations excitation power = Rload * I_{RMS}^2 (μW)

If the excitation power exceeds the specification of the resonator, consider the following measures.

・Add a damping resistor on the board.
・Decrease the oscillator drive capability of MCU.
See Note 6 in Chapter 4 for information of the MCU's oscillator drive capability.

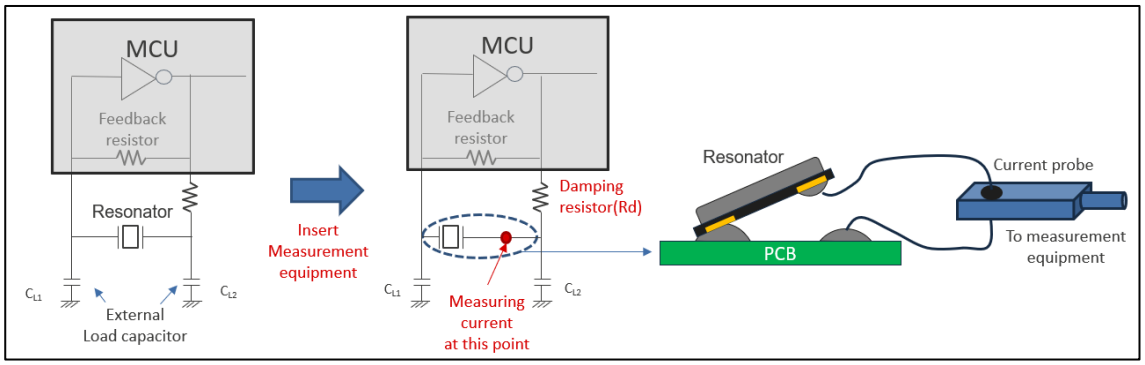

Figure 16. Measurement method of the oscillations excitation power

5.3 Measurement method of the oscillation amplitude voltage

Prepare a board with the selected external components according to Chapter 5.1 and Chapter 5.2. Connect a FET probe to XTAL/XCOUT and VSS of the MCU as shown in to measure the oscillation amplitude voltage. If the measured voltage exceeds the absolute maximum rating of the MCU, consider the following measures.

- Add a damping resistor on the board.
- Decrease the oscillator drive capability of the MCU.
  See Note 6 in Chapter 4 for information of the MCU's oscillator drive capability.

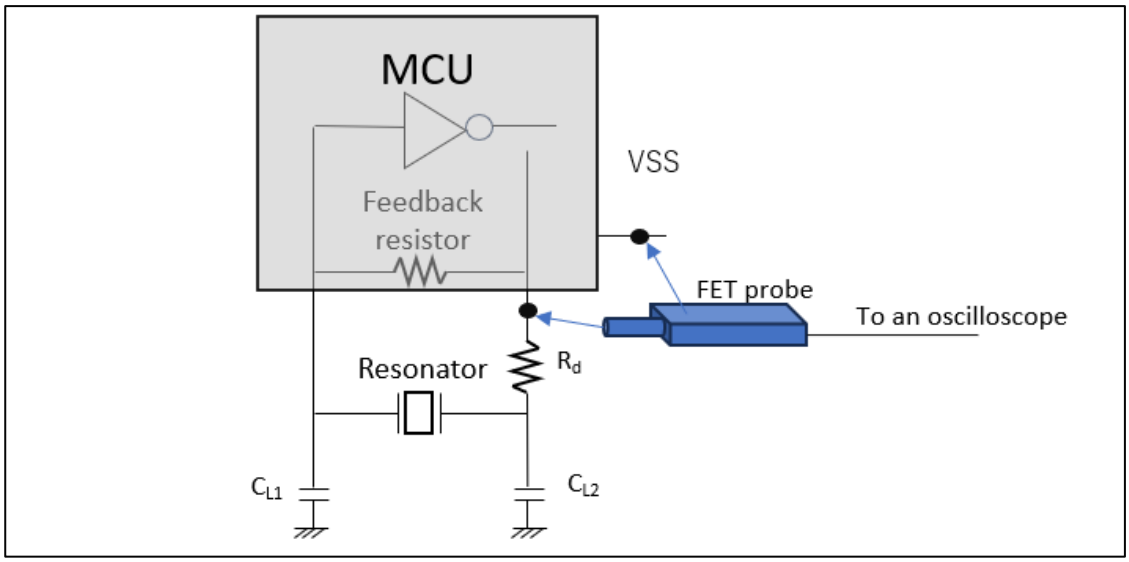

Figure 17. Oscillation Amplitude Voltage Measurement Method

5.4 How to determine the load capacitor values

In general, to determine the external load capacitance, adjust the capacitance in the actual experiment so that the oscillation frequency becomes the target value. If you want to estimate the external load capacitance without experimenting, follow the procedure below.

If you want to estimate the C_L of the load capacitor accurately, you must also consider the parasitic capacitance of the board, as shown in the (Exact Version). However, in this application note, to simplify the calculation, we use the formula in the (Simplified Version), where the parasitic capacitance value of the board is "zero". Other conditions are listed below.

- C_L: Use the resonator manufacturer's recommended value for the external load capacitor. For example, in this case we use C_L = 8 pF as a typical value.
- C_{L1} and C_{L2}: Assume them to the same value. (C_{L1} = C_{L2})
- C_{ps}: The typical MCU pin-to-pin capacitance is 1 pF. Use the actual measured value if you want to calculate it accurately.

Substituting these values into the equation shown in (Simplified version) gives capacitance of 14 pF for the external load capacitance, C_{L1} and C_{L2}.

■ $C_{L1} = C_{L2} = (C_L - C_{PS}) * 2 = (8 - 1) * 2 = 14$ pF

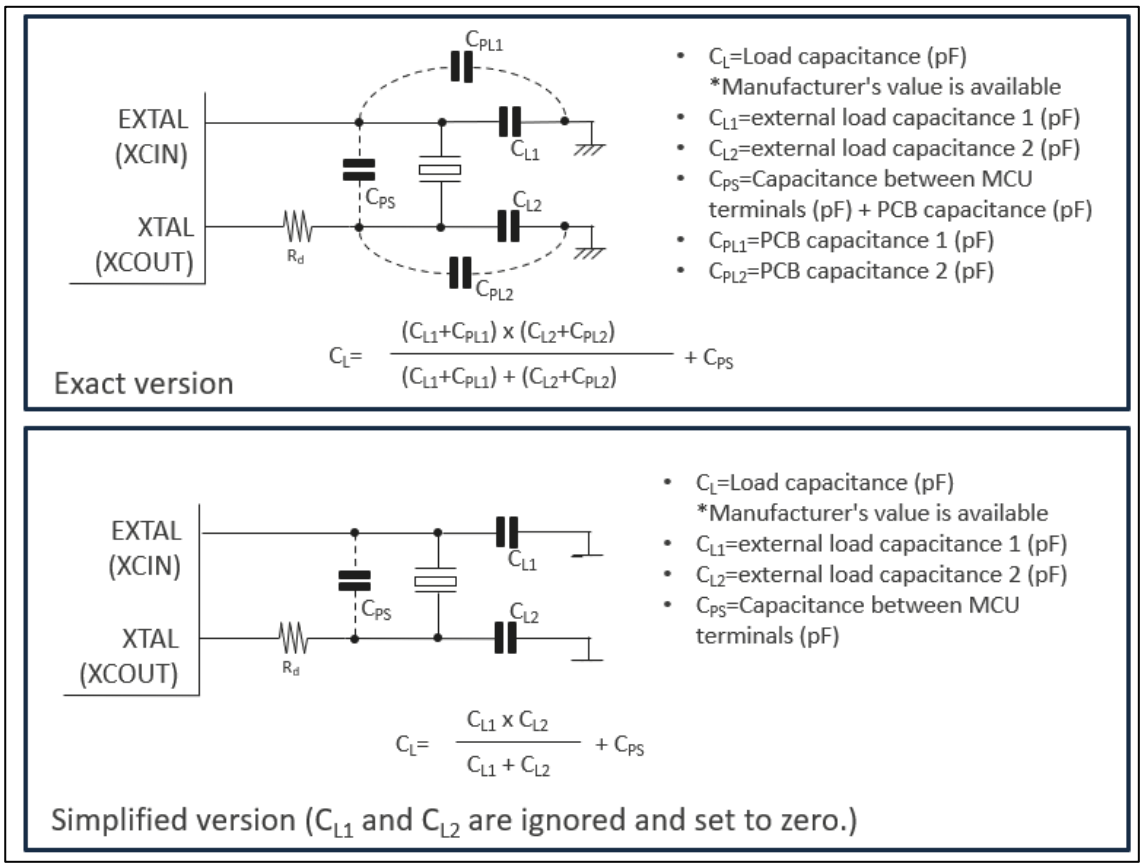

Figure 18. Formula for the External Load Capacity (C_{L1} and C_{L2})

5.5 Calculation method of transconductance

The transconductance (Gm) of the MCU oscillator can be calculated using the following equation. As R, C_{L1}, C_{L2} in this equation, use the matching evaluation results described in Chapter 4. The calculation result is a reference value and is not guaranteed.

■ $Gm = |R| * (\omega^2 \times C_{L1} \times C_{L2})$ * When the resistance of the damping register (R_d) is 0 Ohm

- R: Negative Resistance (Ohm)
- ω: Angular frequency (2π x frequency (Hz)) (rad/sec)
- C_{L1}, C_{L2}: External load capacitance (pF)

6. Board design recommendations

6.1 How to stabilize the oscillation

6.1.1 EXTAL/XCIN and XTAL/XCOUT Routing

(1) through (6) below describe recommendations for the EXTAL/XCIN and XTAL/XCOUT routing. through show examples of their traces.

(1) Do not cross the EXTAL/XCIN and XTAL/XCOUT wires with other signal wires.

(2) Do not connect any testing terminals to the EXTAL/XCIN and XTAL/XCOUT wires.

(3) Make the EXTAL/XCIN and XTAL/XCOUT wires width between 0.1 mm and 0.3 mm. The wires length from the MCU pins to the resonator pins should be within 10 mm as much as possible.

(4) The trace connected to the EXTAL/XCIN pin, and the trace connected to the XTAL/XCOUT pin should have as much space between them as possible (at least 0.3 mm).

(5) Connect the two external load capacitors with the shortest routing distance and connect the routing to the ground pattern on the component surface (hereafter referred to as ground shield. See chapter 6.1.2 for details). If there is no space near the MCU of the PCB and the external load capacitors cannot be placed near the MCU as shown in to , place them as shown in .

(6) To reduce the parasitic capacitance between the EXTAL/XCIN and XTAL/XCOUT, add a ground trace between the resonator and the MCU.

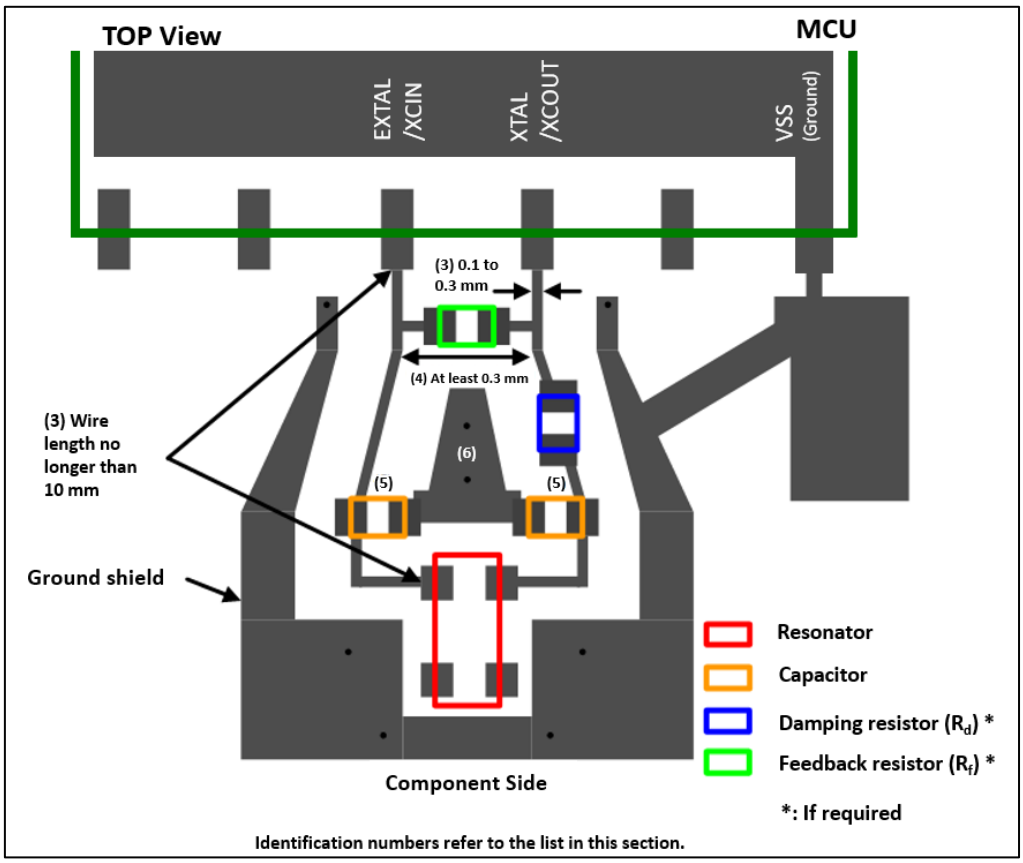

Figure 19. Example of the EXTAL/XCIN and XTAL/XCOUT Routing Pattern: LQFP Package

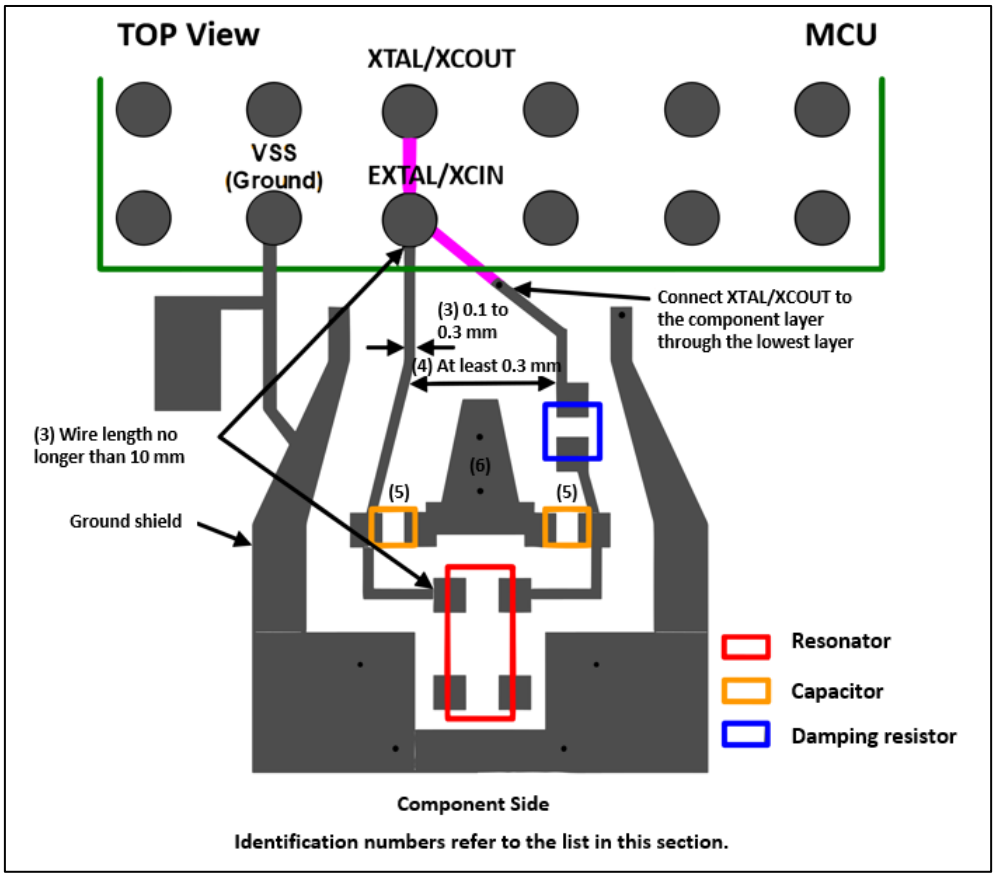

Figure 20. Example of the EXTAL/XCIN and XTAL/XCOUT Routing Pattern: LGA Package

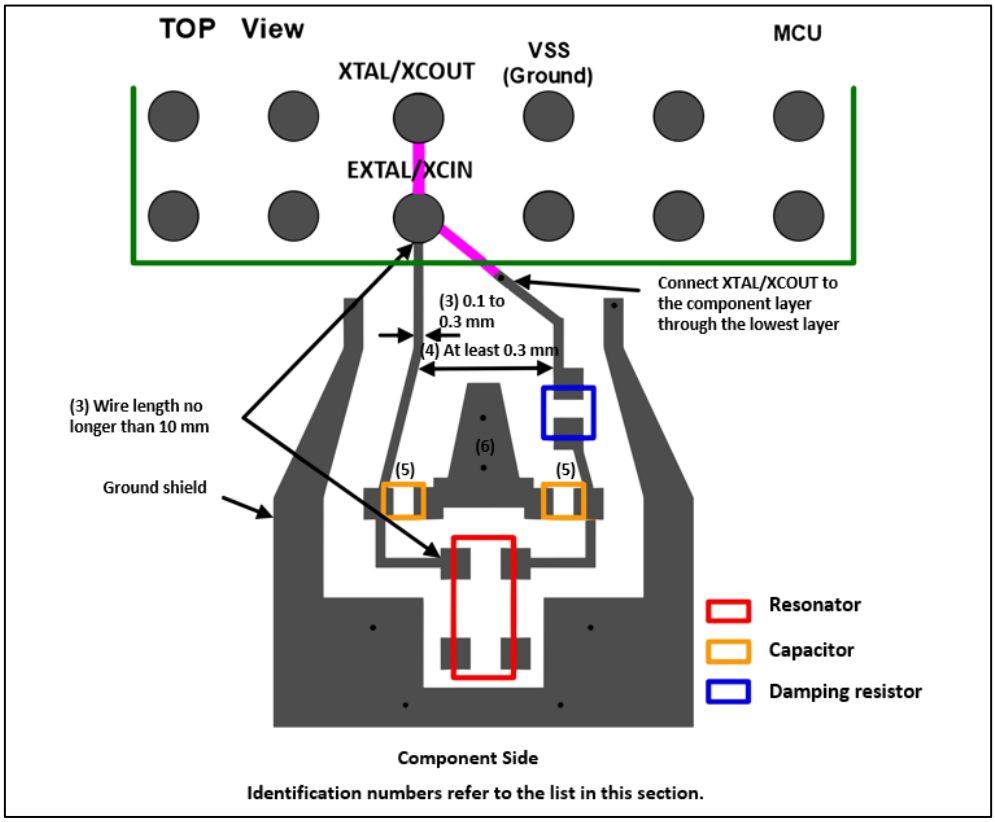

Figure 21. Example of the EXTAL/XCIN and XTAL/XCOUT Routing Pattern: BGA Package

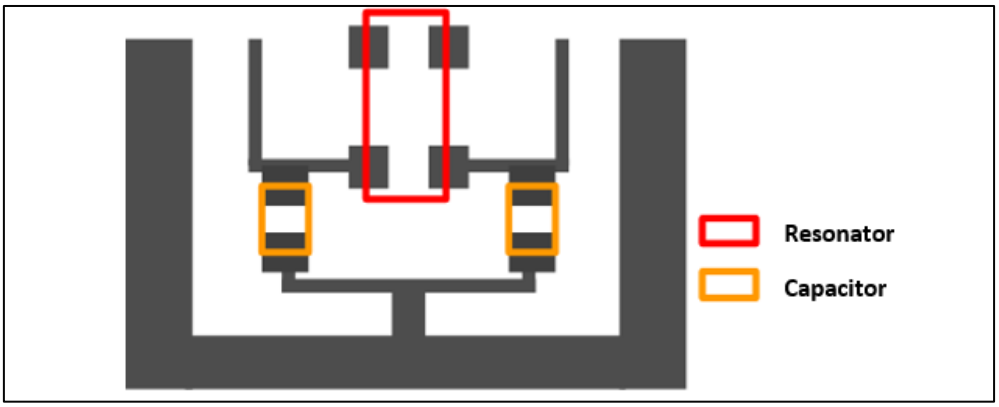

Figure 22. Pattern example when two external capacitors are difficult to place near MCU

6.1.2 Use a ground shield

Shield the resonator with a ground trace. (1) through (4) below describe the recommendations for the ground shield. through Figure 25 show trace examples for each package.

In addition, the ground shield of the main clock oscillator circuit and the sub-clock oscillator circuit should not be a continuous pattern as shown in . If the ground shield of the main clock oscillator and the ground shield of the sub-clock oscillator are directly connected, the output of the main clock oscillator may propagate as noise to the ground shield of the sub-clock and affect the oscillation of the sub-clock.

(1) Place the ground shield on the same layer as the resonator trace routing.

(2) Make the ground shield trace width at least 0.3 mm and leave a gap of 0.3 to 2.0 mm between the ground shield and other traces.

(3) Route the ground shield as close as possible to the VSS pin on the MCU and make sure that the trace width is at least 0.3 mm.

(4) To prevent current from flowing through the ground shield, branch the ground shield and the ground on the board near the VSS pin on the board.

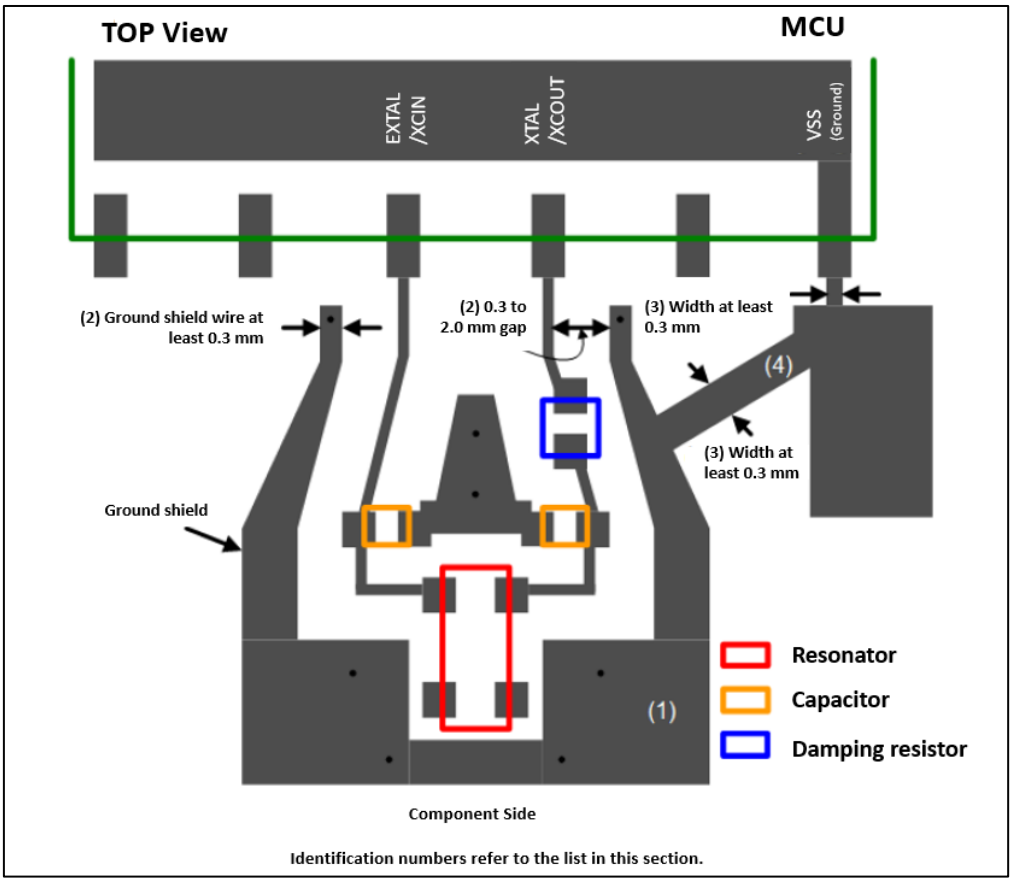

Figure 23. Example of the ground shield tracing: LQFP Package

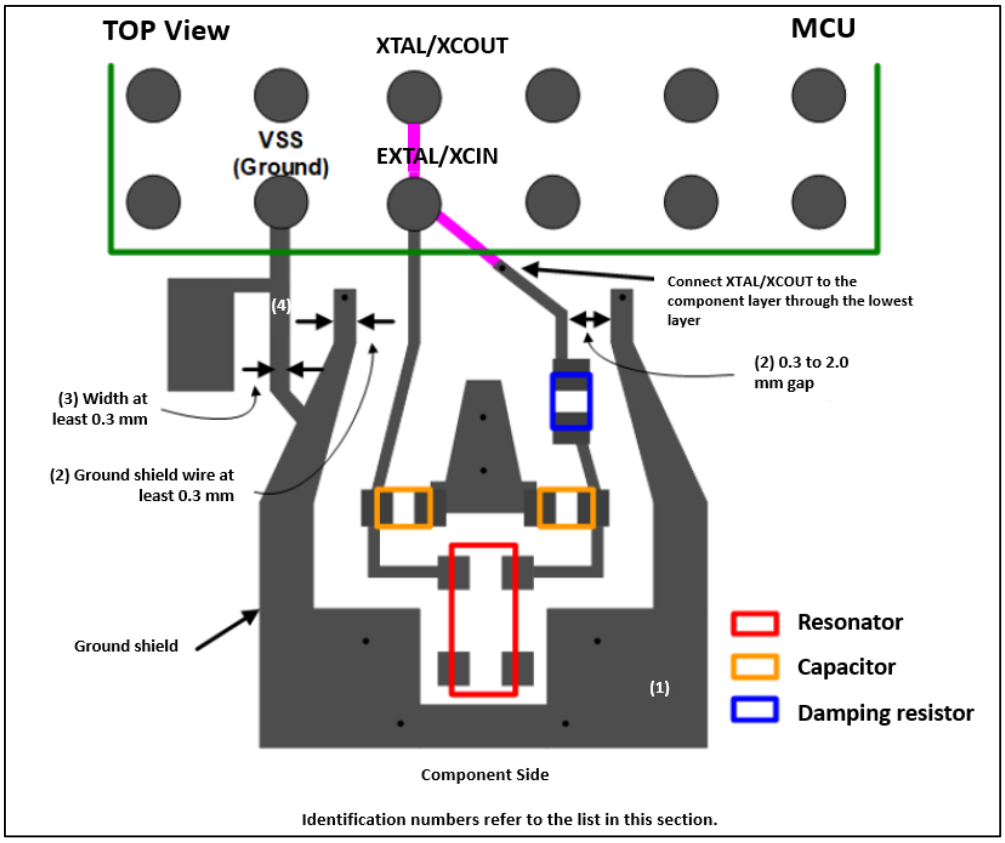

Figure 24. Example of the ground shield tracing: LGA Package

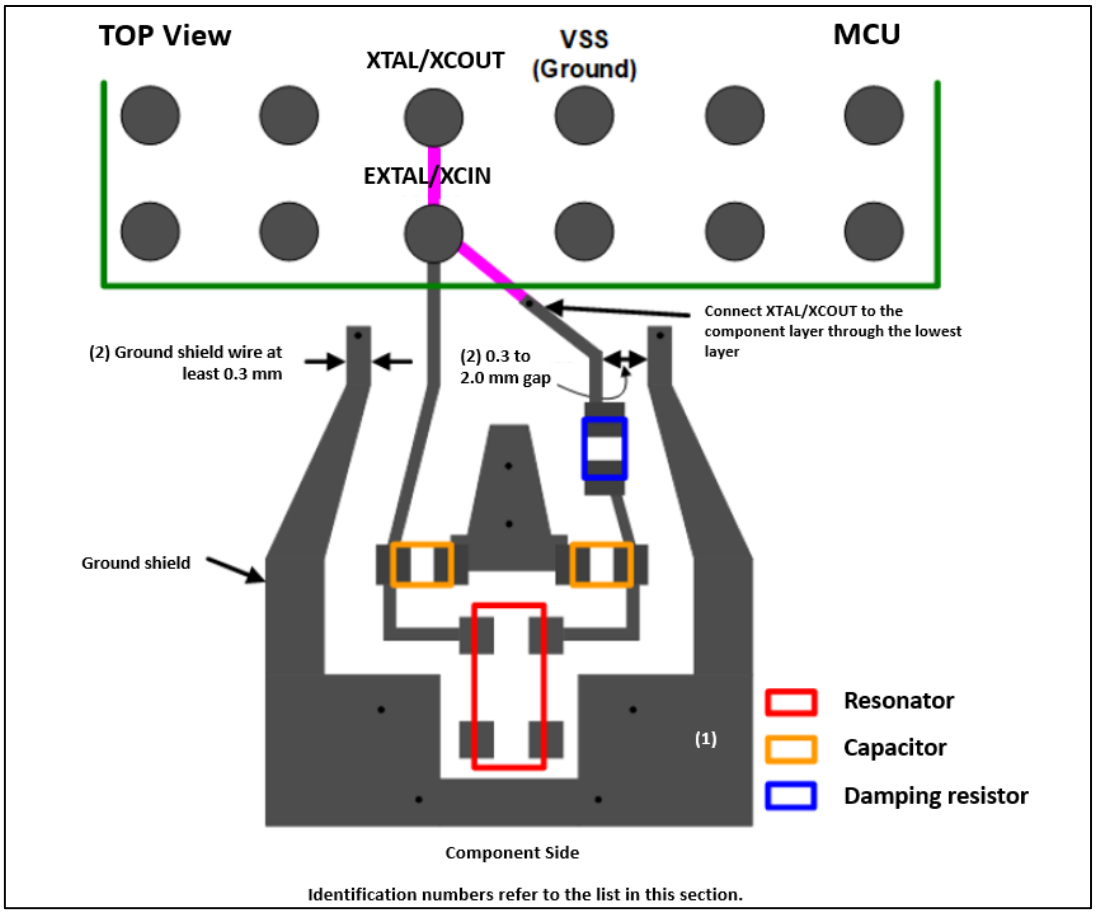

Figure 25. Example of the ground shield tracing: BGA Package

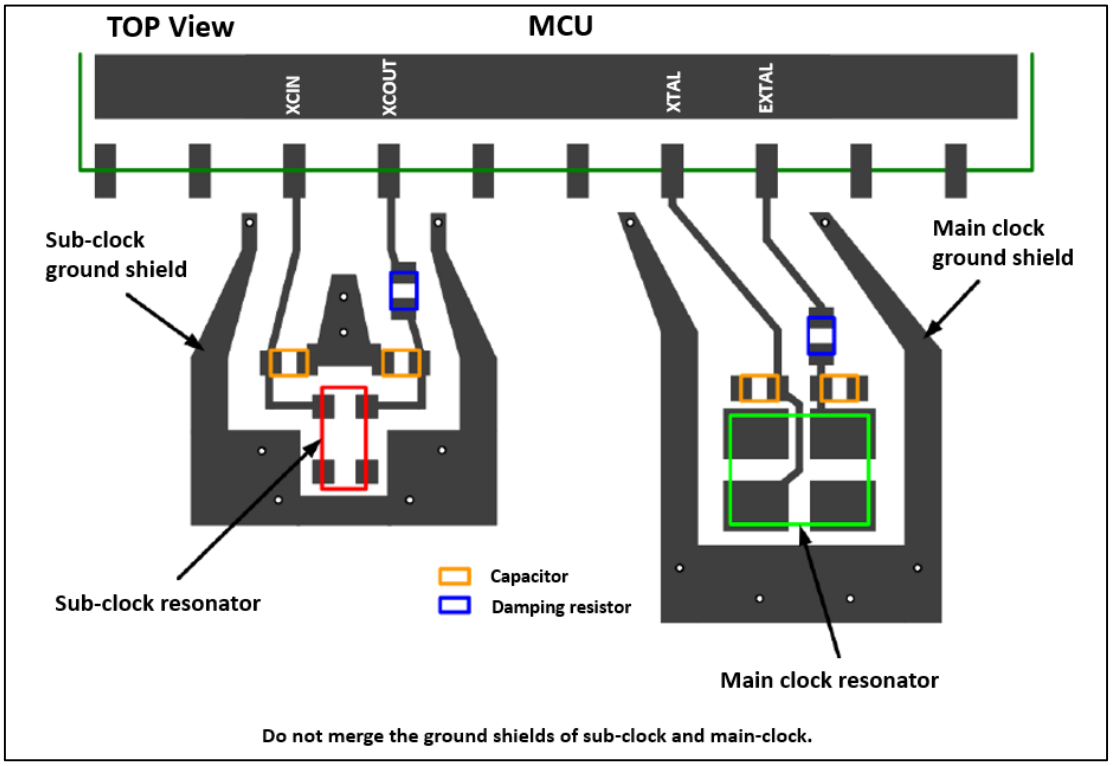

Figure 26. Example of the main clock and sub-clock ground shield configuration

6.1.3 Usage of a bottom-ground

6.1.3.1 Multilayer boards thicker than 1.2 mm

For multilayer boards thicker than 1.2 mm, place a ground pattern (hereafter referred to as bottom ground) on the solder surface of the resonator area (see Figure 27 through Figure 29).

The recommendations of the bottom ground are shown below. Figure 27 through Figure 29 show examples of patterns for each package.

(1) Do not place power supply, ground, or signal line patterns in the middle layer of the resonator area. The parasitic capacitance and crosstalk between layers may affect stable oscillation.

(2) Connect the ground shield termination on the component side to the bottom ground. If the termination is not connected to bottom ground and is an open end, there is a risk that the ground shield will become a noise source by acting as an antenna.

(3) Make the bottom ground at least 0.1 mm larger than the ground shield.

- Case of LQFP and LGA/BGA (whose VSS is placed in the outer column):

  Connect the bottom ground only to the ground shield on the component side.

  Do not connect the bottom ground directly to the VSS terminal, but connect it through the ground shield.

  Do not connect any ground other than the VSS pin to the bottom ground and the ground shield.

- Case of LQFP and LGA/BGA (whose VSS is placed in the inner column):

  Connect the bottom ground directly to the VSS pin.

  Do not connect any ground other than the VSS pin to the bottom ground and ground shield.

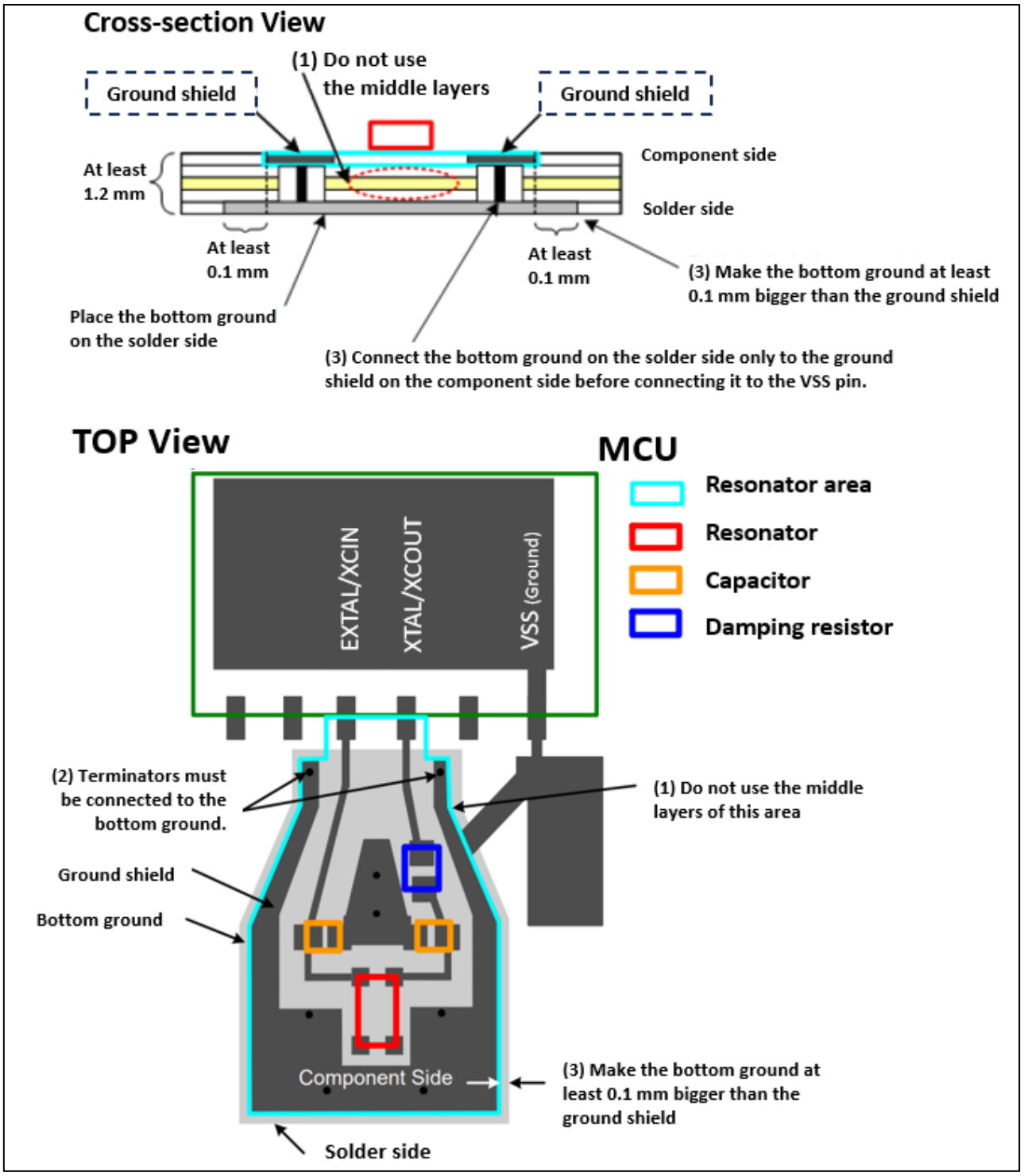

Figure 27. Routing example for a multilayer board thicker than 1.2 mm: LQFP Package

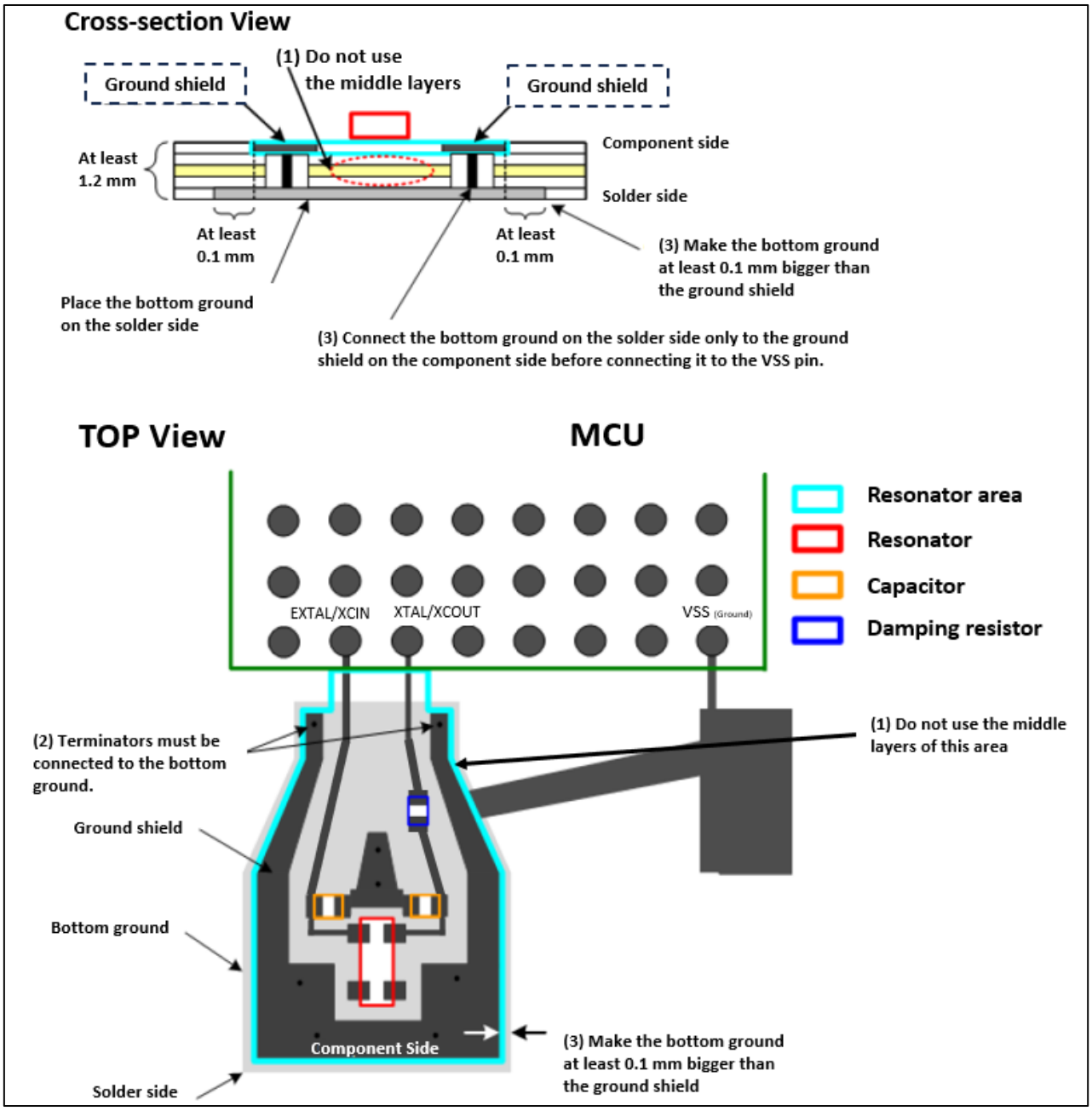

Figure 28. Routing example for a multilayered board thicker than 1.2 mm: LGA/BGA Package (VSS is placed in the outer column)

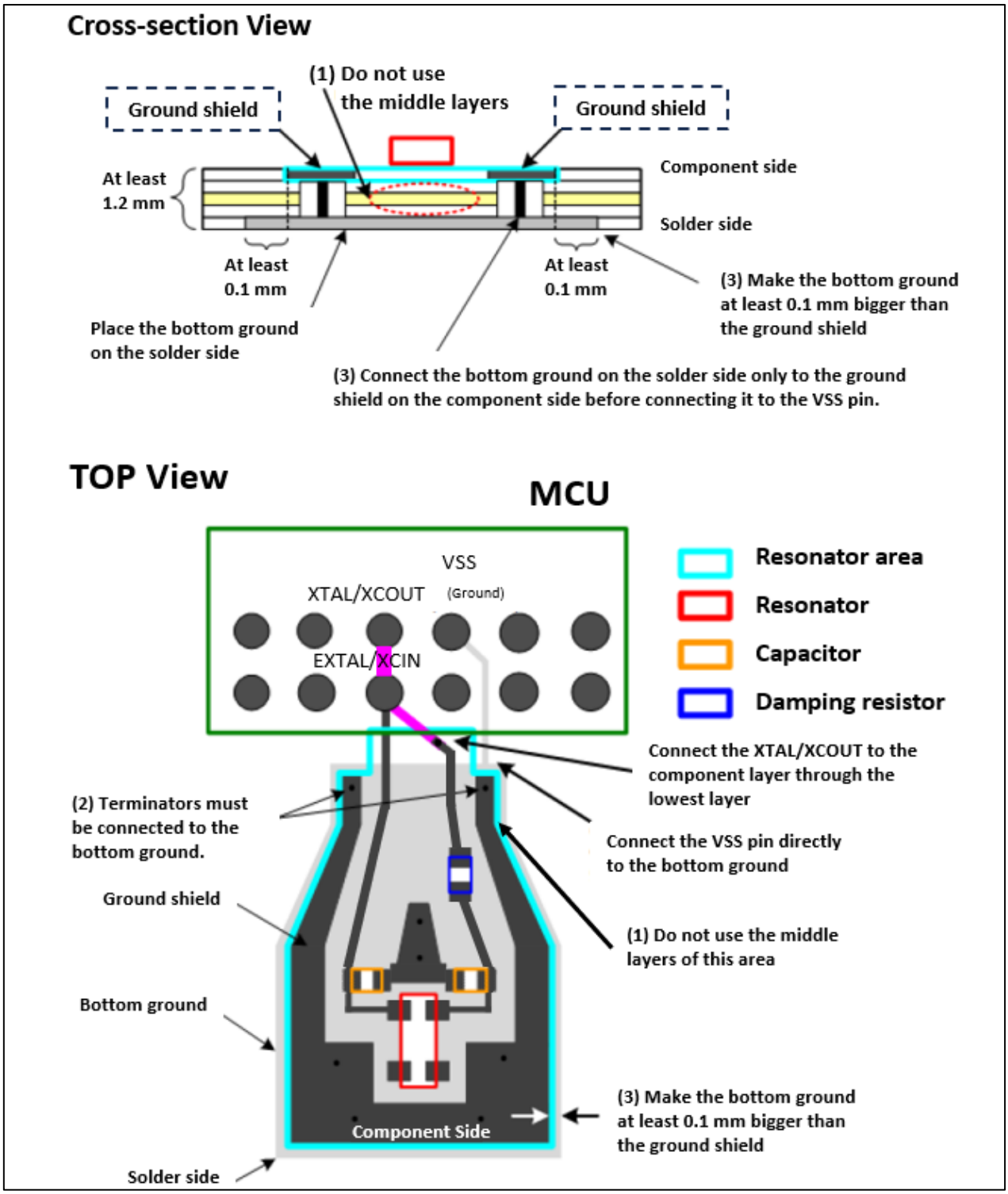

Figure 29. Routing example for a multilayered board thicker than 1.2 mm: LGA/BGA Package (VSS is placed in the inner column)

6.1.3.2 Multilayer boards thinner than 1.2 mm

The following are recommendations to consider when routing a multilayer board thinner than 1.2 mm. Figure 15 shows an example routing.

(1) Do not place power supply, ground, and signal line patterns in the middle layer of the resonator area. Do not place power, ground, or signal line patterns on the solder surface as well. The parasitic capacitance and crosstalk between the layers may interfere with stable oscillation.

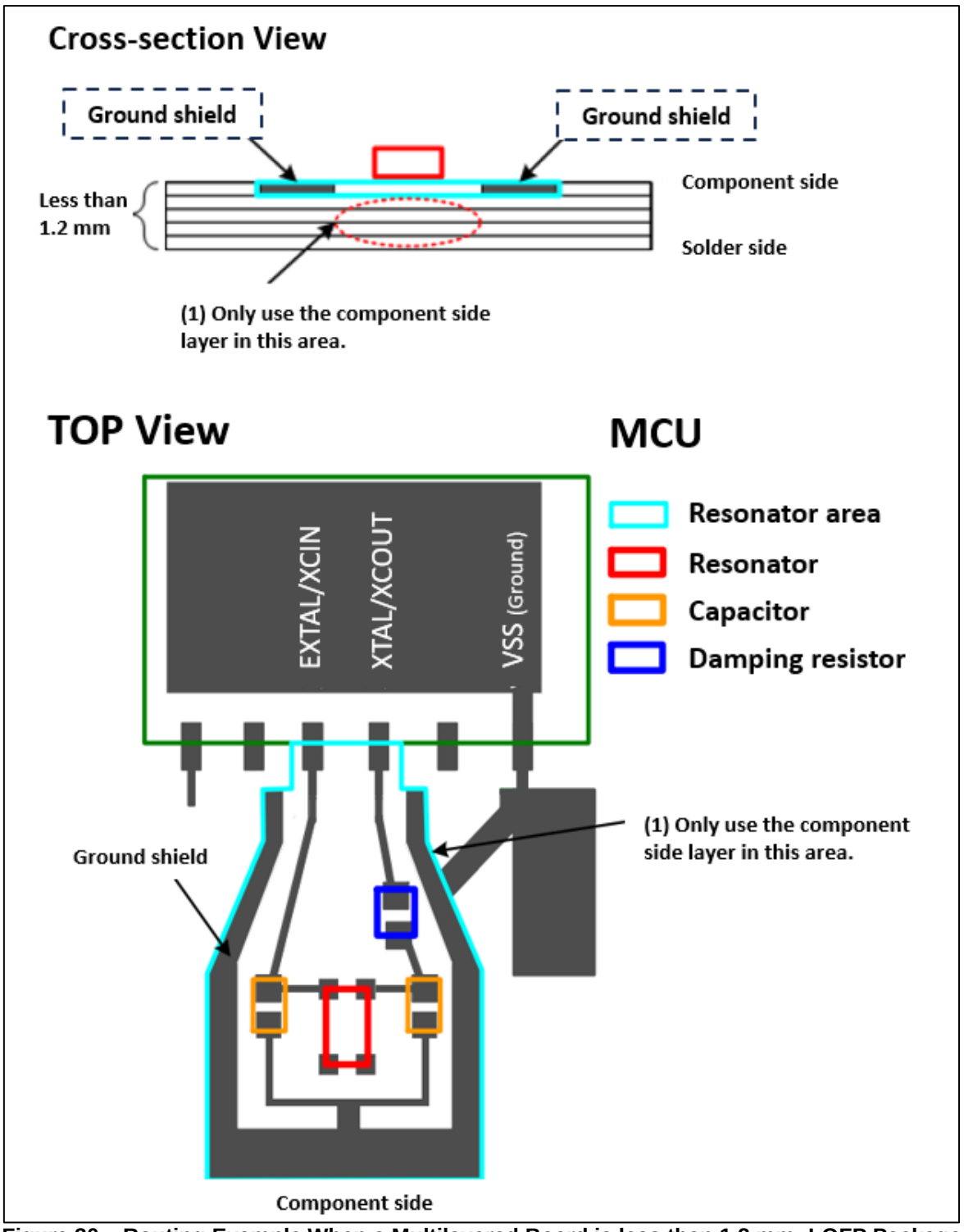

Figure 30. Routing Example When a Multilayered Board is less than 1.2 mm: LQFP Package

6.1.4 Other miscellaneous recommendations

The following are common recommendations for all packages. **Figure 31** also shows an LQFP pattern as an example.

(1) Do not place the EXTAL/XCIN and XTAL/XCOUT wires near traces with large current variations.
(2) Do not place the EXTAL/XCIN and XTAL/XCOUT wires in parallel with other signal wires, such as those for adjacent pins.
(3) Do not place the wires of the terminals adjacent to EXTAL/XCIN and XTAL/XCOUT in parallel with the EXTAL/XCIN and XTAL/XCOUT traces. Do not connect them directly to the outside of the MCU, but first route them through the bottom of the MCU and then bring them out from a location away from the EXTAL/XCIN and XTAL/XCOUT pins.
(4) Place the ground trace on the bottom side of the MCU and make this as large as possible.

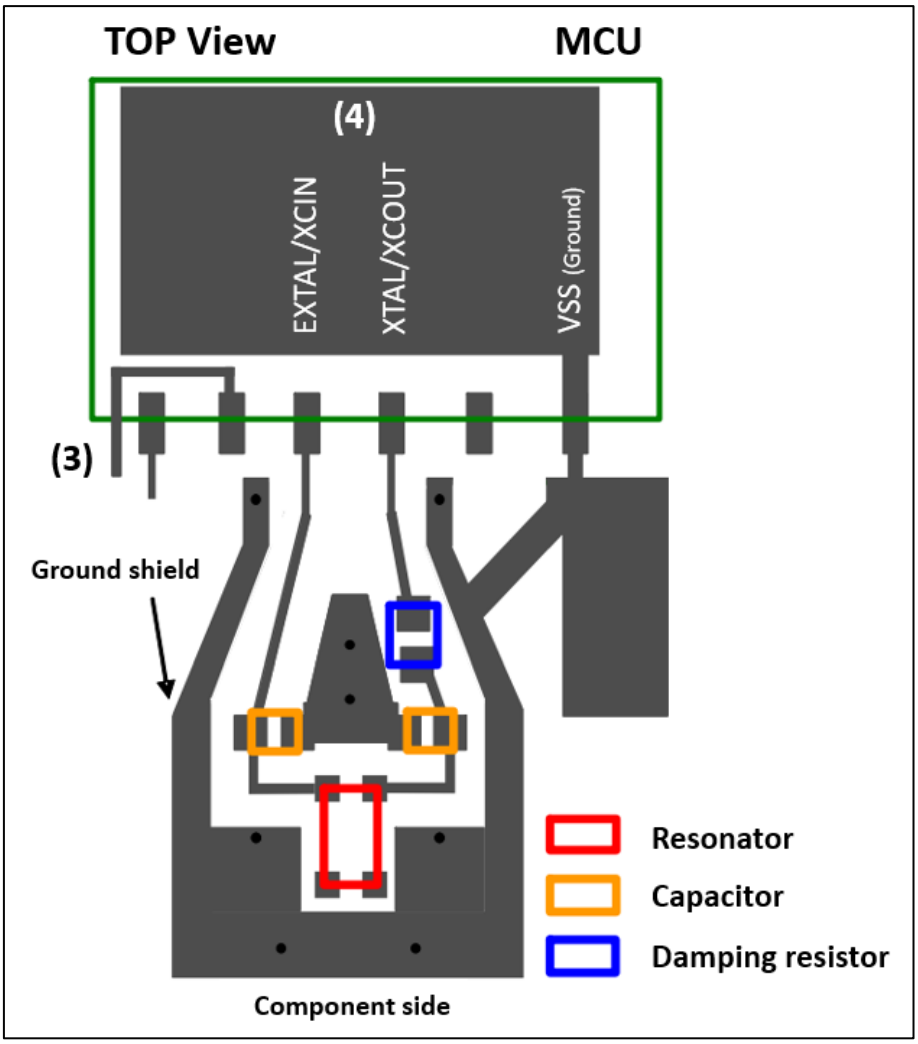

Figure 31. Example of Routing for Other Points: LQFP Package

6.2 Examples of patterns with a high risk of malfunction due to noise

Avoid the issues listed below in your PCB design as they may cause the resonator to oscillate incorrectly or may increase EMI. **Figure 32** shows some examples of incorrect patterns.

(1) The EXTAL/XCIN and XTAL/XCOUT wires cross other signal wires.
The MCU may malfunction due to crosstalk.
(2) Observation pins (test points) are attached to the EXTAL/XCIN and XTAL/XCOUT wires.
There is a risk of unstable oscillation due to impedance mismatch in the wiring and reflections in the oscillation waveform.

(3) The EXTAL/XCIN and XTAL/XCOUT wires are long.
Parasitic capacitance or inductance can cause oscillation instability and loss of accuracy. It is also a source of EMI.

(4) The ground shield does not cover the entire oscillation area, the wiring from the board ground is long or the wiring is thin.
The oscillating circuit is easily affected by noise.
There is a risk that the ground potential difference between the MCU and the external load capacitance may affect the accuracy of the oscillation frequency.

(5) The ground shield is not isolated from the board ground immediately adjacent to the VSS terminal.
The operating current of the MCU flows to the ground shield and may cause the resonator to malfunction.

(6) The power and ground patterns are located under the EXTAL/XCIN and XTAL/XCOUT wiring.
Oscillation in the resonator circuit may stop due to a lack of clock caused by parasitic capacitance, impedance and noise.

(7) Wires with high current flow are routed near the EXTAL/XCIN and XTAL/XCOUT wiring.
There is a risk that the resonator circuit will stop oscillating due to the effects of crosstalk.

(8) The distance between the EXTAL/XCIN and XTAL/XCOUT wiring, and the wiring of the adjacent terminals is close, and the parallel length is long.
There is a risk that the resonator circuit will stop oscillating due to the effects of crosstalk.

(9) Intermediate layers in the resonator area are used.
If there are ground and/or power supply layers in the intermediate layer, there is a risk that parasitic capacitance will affect the oscillation characteristics.
If signal lines are present, there is a risk of crosstalk causing the resonator circuit or signal lines to malfunction.

(10) The oscillation area is extremely close to the board edge.
Cause an increase in EMI radiated from the resonator circuit to the outside of the board.

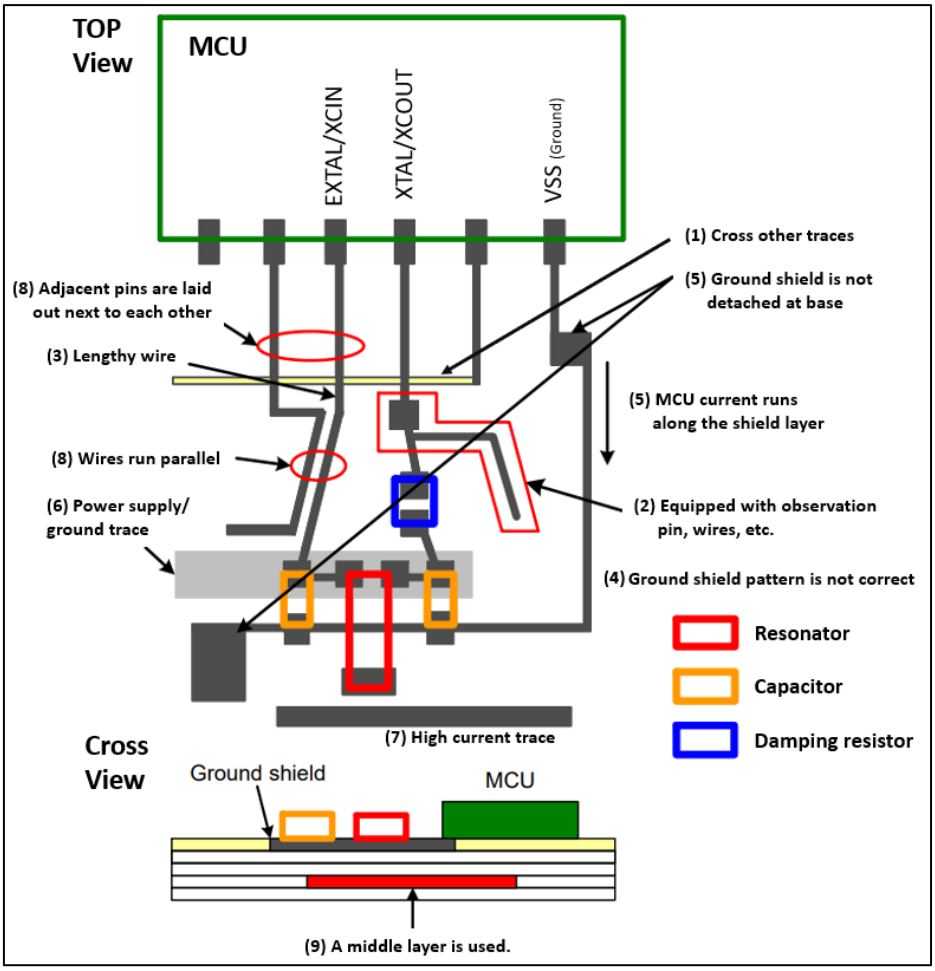

Figure 32. Example of a pattern with a high risk of malfunction due to noise

7. External Resonator Frequency Accuracy Measurement

As recommended by both resonator manufacturers and Renesas (in each MCU Hardware User's Manual), the correct implementation of the oscillator circuit includes 2 load capacitors (C_{L1} and C_{L2} in the diagram). Previous sections of this document cover capacitor selection. These capacitors directly influence the accuracy of the clock frequency. Loading capacitor values that are too high or too low can have a significant impact on the long-term accuracy of the clock, making the clock less reliable. The value of these capacitors is determined by a combination of the resonator device specification and the board layout, taking into account the stray capacitance of the PCB and the components in the clock path.

However, to correctly determine the accuracy of an oscillator circuit, the clock frequency must be measured on real hardware. Direct measurement of the oscillator circuit will almost definitely result in incorrect measurements. The typical value for the loading capacitors is in the range of 5 pF to 30 pF, and typical oscilloscope probe capacitance values are typically in the range of 5 pF to 15 pF. The additional capacitance of the probe is significant compared to the loading capacitor values and will skew the measurement, leading to incorrect results. The lowest value capacitance oscilloscope probes are still around 1.5 pF capacitance for very high precision probes, which would still potentially skew the measurement results.

The following is a suggested method for measuring clock frequency accuracy on MCU board products. This procedure eliminates potential measurement error due to capacitive loading added by the measurement probe.

7.1 Recommended Test Procedure

- One or more MCU boards for the device to be measured.
- Programming and emulation tools for the device to be measured.
- A frequency counter with at least 6-digit accuracy, with proper calibration

7.1.1 Test Method

1. Program the MCU to connect the clock crystal input for the sub-clock circuit to the CLKOUT pin of the MCU.
2. Connect the frequency counter to the CLKOUT pin of the MCU and an appropriate ground. DO NOT connect the frequency counter directly to the clock crystal circuit.
3. Configure the frequency counter to measure the frequency on the CLKOUT pin.
4. Allow the frequency counter to measure the frequency for several minutes. Record the measured frequency.

This procedure may be used for both sub-clock and main clock resonators. To see the effect of the loading capacitor values on clock crystal accuracy, the test can be repeated with different values for the loading capacitors. Select the values that provide the most accurate clock frequency for each clock.

It is also recommended to repeat the procedure on multiple boards of the same type to improve the validity of the measurements.

7.2 Frequency Accuracy Calculations

Frequency accuracy can be calculated using the following formulas:

f_m = measured frequency
f_s = ideal signal frequency
f_e = frequency error
f_a = frequency accuracy, typically expressed in parts per million (ppm) or parts per billion (ppb)

Frequency error can be expressed as

$$f_e = |f_s - f_m|$$

Frequency accuracy can be expressed as

$$f_a = \frac{f_e}{f_s} = \frac{|f_s - f_m|}{f_s}$$

To express frequency accuracy in parts per million:

$$f_{a(ppm)} = \frac{f_e}{f_s} \times 10^6$$

Frequency accuracy can also be expressed in deviation from actual time.

Deviation, in seconds per year, can be expressed as

$$\text{deviation} = 31{,}536{,}000\ seconds\ per\ year \times f_a$$

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.06.24	-	First edition
1.01	May.17.24	-	Added Chapter 7 and updated some minor points

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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