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Super Low Power Series

ΔΣ A/D Converter User's Guide

Contents

1. Basic Principles of the Delta Sigma Architecture

1.1 Successive-Approximation-Type A/D Converters and ΔΣ A/D Converters

1.1.1 Successive-Approximation-Type A/D Converters

An A/D converter of the successive-approximation type measures voltage by comparing the values of the analog voltage to be measured with a variable reference voltage generated by a D/A converter (DAC). The operation of an A/D converter of this type can be summarized as follows.

1. The analog voltage to be measured is compared with the DAC's output, which is used as a central value.
2. The DAC's output is either increased or decreased (according to whether the analog value to be measured was greater or smaller than the central value in the previous comparison) and again compared with the analog voltage.
3. The above step is repeated up to n + 1 times (resolution is assumed to be n bits) to complete the comparison.

This may be compared to measuring an object by using rulers with various lengths and determining which most closely matches the length of the object to be measured.

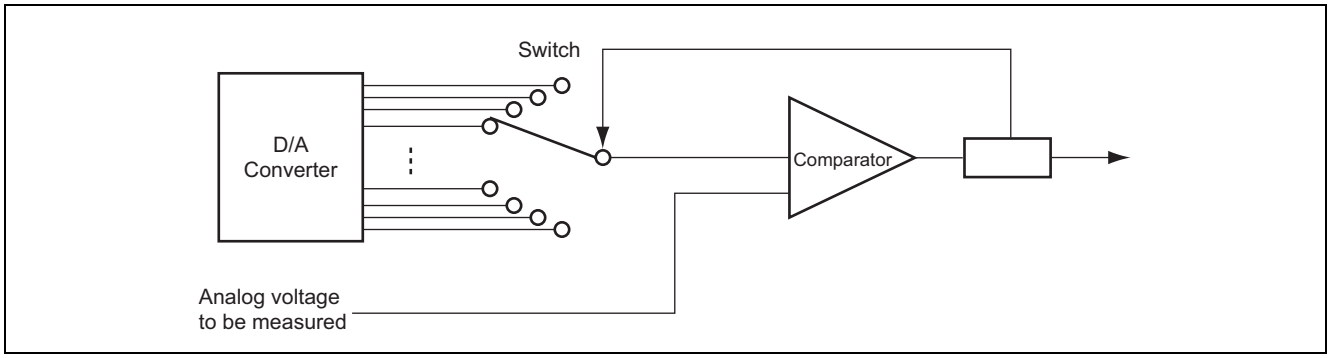


Figure 1.1 A/D Converter of the Successive-Approximation Type

1.1.2 ΔΣ-Type A/D Converter

In an A/D converter of the delta-sigma (ΔΣ) type, the voltage to be measured is sampled and integrated. It is then compared with a constant reference voltage and converted to digital values. This is similar to measuring the length of an object by counting the number of 1-cm units and then multiplying the result by 1 cm. Since this method of analog-to-digital conversion includes both differentiation and integration, it is called the delta-sigma (or sigma-delta) technique.

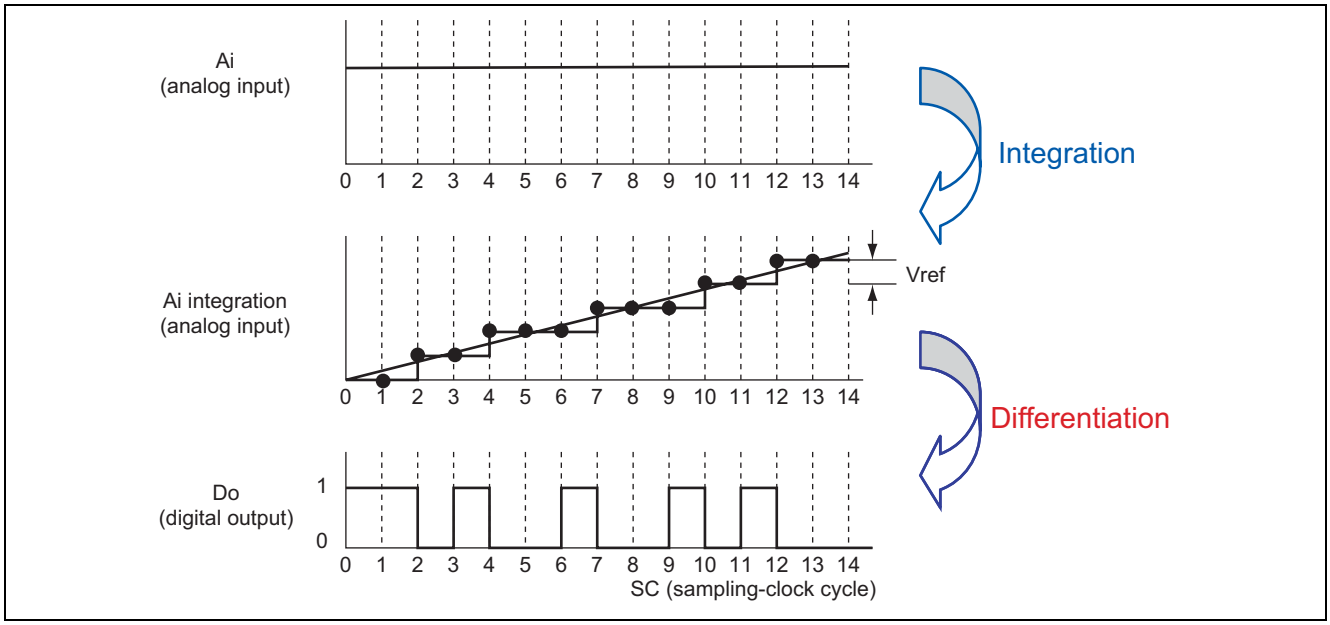


Figure 1.2 Principle of a ΔΣ-Type A/D Converter

1.2 Overview of the ΔΣ A/D Converter

1.2.1 Measurement of Direct Current Voltage

Let us suppose we are measuring a direct current (DC) voltage, and start by comparing the analog input (Ai) with an external reference voltage (Vref). Other relevant considerations are ignored for simplicity.

- When SC = 1, the digital output is 1 since the voltage being compared with the analog input was 0 V when SC = 0 and 0 < Ai. A voltage Vref is then added to the reference voltage for use in comparison on the next sampling clock (SC) cycle.
- When SC = 2, Vref is compared with Ai. The digital output is 0 since Vref > Ai. The same voltage value is thus used in the next round of measurement on the next SC cycle.
- When SC = 3, Vref is again compared with Ai. The digital output is 0 since Vref > Ai. The same voltage value is again to be used in the next round of measurement on the next SC cycle.

However many times the above procedure is repeated, the result will be a digital output made up of a single 1 for the first measurement and successive 0s for subsequent measurements, leaving the value of Ai unknown. Hence the next step is to integrate Ai. The slope of the waveform produced by integration represents Ai.

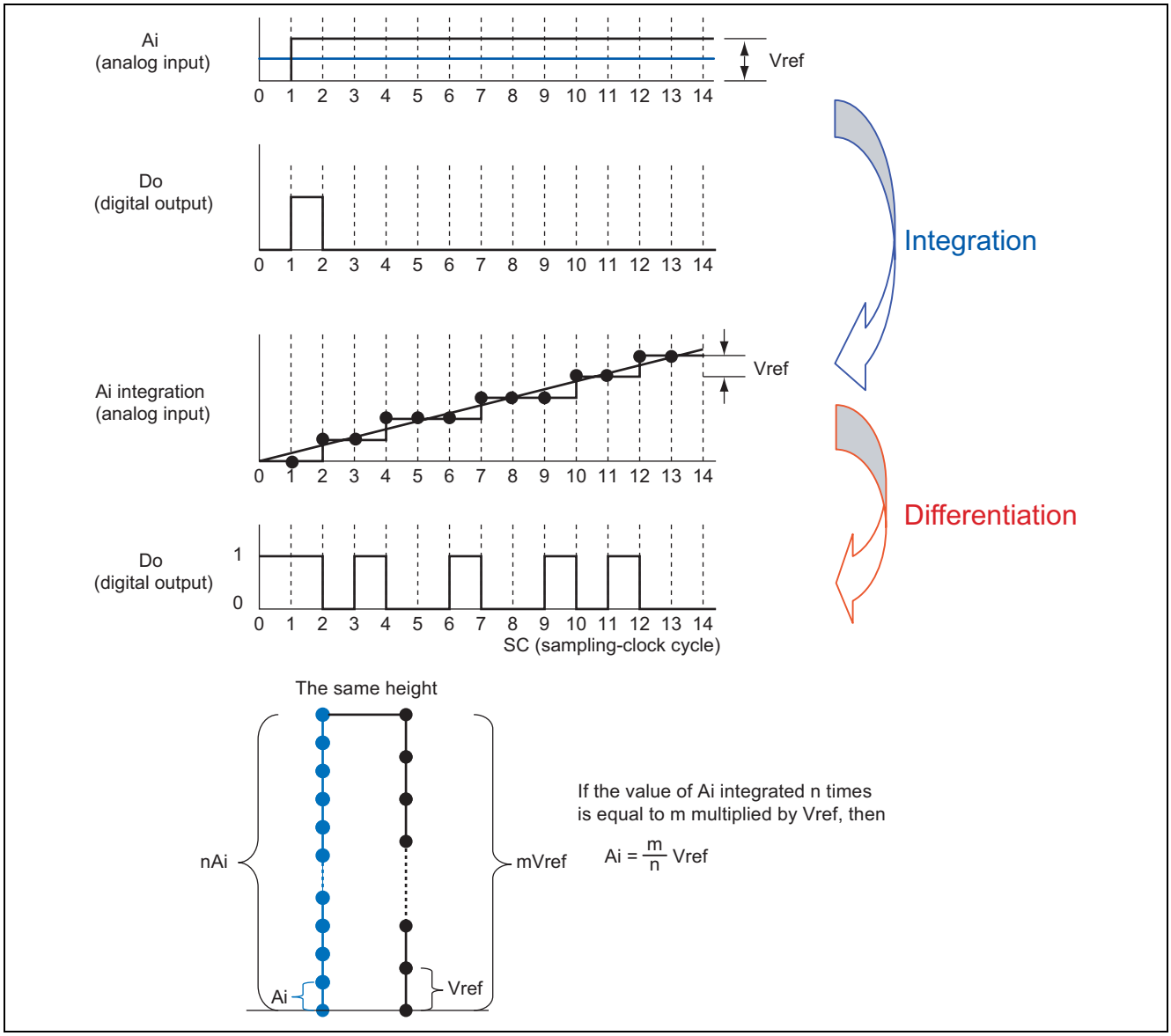


Figure 1.3 Comparison of the Integrated Value and Vref

Now, let us compare the integrated value with integer multiples of Vref as shown in figure 1.3.

- When SC = 1, Ai has only been integrated once and Vf remains at the same 0 V as it was before the integration. The digital output is 1 since Vf is less than or equal to Ai and therefore Vref is added to the above 0-V voltage for use in the next measurement.
- When SC = 2, Ai has been integrated twice. Vf is compared with 2Ai. The digital output is now 0 since Vref > 2Ai. The same voltage (Vref) is used in the next round of measurement.
- When SC = 3, Ai has been integrated three times. Vf (still at Vref) is compared with 3Ai. As we see in figure 1.3, the digital output is 1 since Vref < 3Ai. Vref is again added to the voltage for use in the next measurement (the result being 2Vref).
- When SC = 4, Ai has been integrated four times. Thus 2Vref is compared with 4Ai. In figure 1.3, the digital output is 0 since 2Vref > 4Ai. The same voltage (2Vref) is then used in the next round of measurement.

The above procedure is continued as required.
Ai is periodically integrated and the resulting slope represents Ai. This representation of Ai is compared with Vf to check the relation between the two values, with Vref being added to Vf as required. That is, Vf is compared with Ai represented as a slope. Each increase in Ai produced by integration is smaller than Vref. For example, while Vf is at Vref, this is compared with the integrated value of Ai until the latter has become greater. Another Vref unit is then added to Vf, which is again compared with the integral of Ai. We can see how the accuracy is improved with repeated sampling in this procedure. In other words, more samples correspond to greater accuracy.

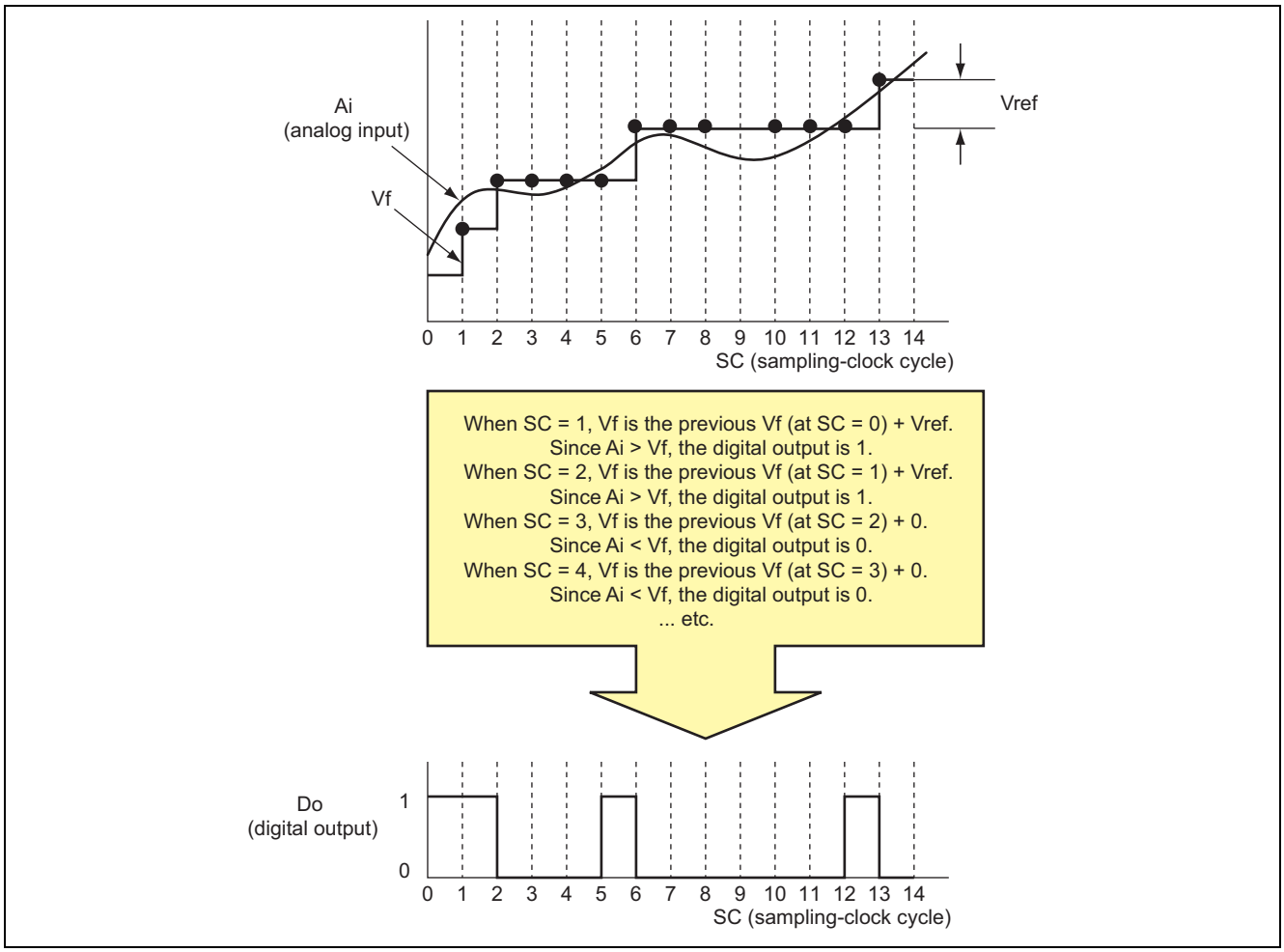


Figure 1.4 Analog Input to and Digital Output from the Δ Modulator

1.3 Advantages of the ΔΣ A/D Converter

1.3.1 Successive-Approximation-Type A/D Converter

- The speed of conversion is high and devices with lower resolutions are relatively cheap to implement.
- Obtaining N bits of resolution requires the inclusion of 2^n on-chip resistors. When the resistors are formed of silicon, the accuracy is limited due to manufacturing dispersal. This approach is thus not suitable for high resolution. This limitation led to the need for a new method.

1.3.2 ΔΣ-Type A/D Converter

- Converters of the ΔΣ type have lower conversion speeds than those of the successive-approximation type but higher conversion speeds than converters of the double-integrating type.
- This method is suitable for high resolution.

Table 1.1 Comparison of Characteristics of Successive Approximation and ΔΣ Converters

Item	Successive-Approximation Type	ΔΣ Type
Method	Sample and hold	Sampling
Module size	Large	Fitting
Conversion time	Fast (approximately 10 μs (H8S/2264)	Slow (32 μs or more) (H8/38086R)
High resolution	No	Yes
Frequency band	Without constraint	Depends on digital filter
Noise immunity	Low	High (noise shaping)

2. ΔΣ A/D Converter

2.1 Configuration

A ΔΣ A/D converter consists of one or more integrators, a delta modulator, and a digital filter. Analog input signals are modulated by the delta modulator into digital signals, the noise of which is then eliminated by the digital filter. The signal produced by digital filtering is taken as the measured data.

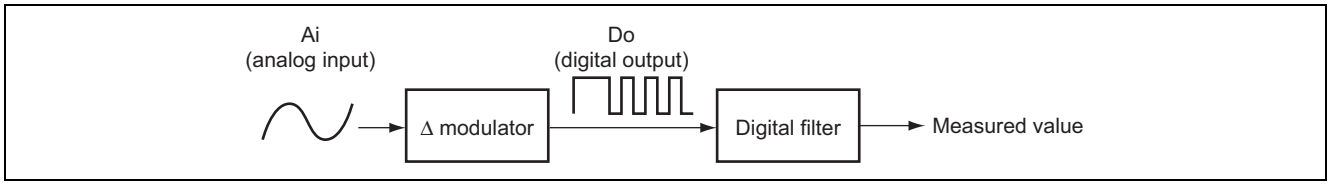


Figure 2.1 Configuration of a ΔΣ A/D Converter

2.2 Δ Modulator

The digital values output by the Δ modulator (see figure 2.2) are produced by comparing an analog input (Ai) with an integrator output (Vf). The flow of operations is as follows.

1. The adder determines the difference between the integrator's output (Vf), i.e. the result of D/A-conversion and integration of the digital output in the previous clock cycle, and the analog input signal (Ai).
2. The comparator compares the adder's output with 0 V, with the result that the comparator outputs a digital value of 1 if Ai > Vf or 0 if Ai < Vf.

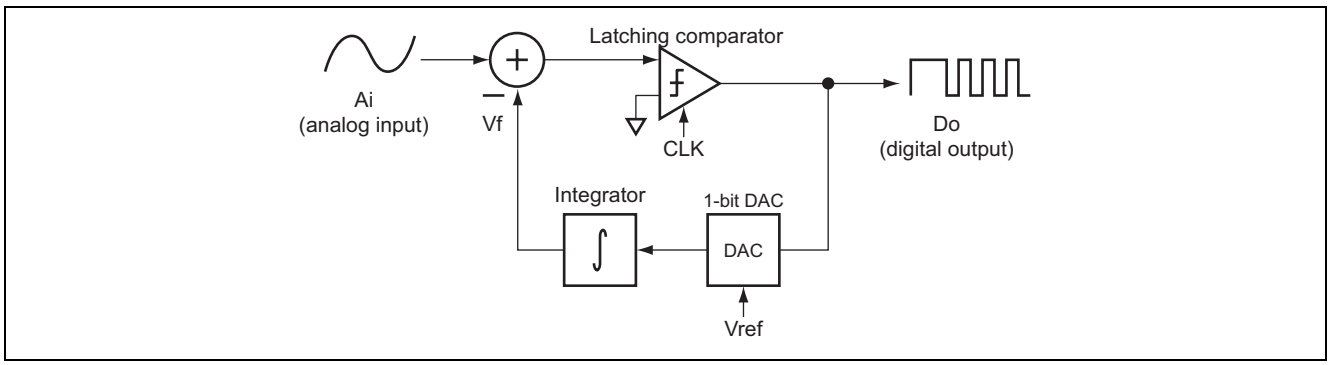


Figure 2.2 Δ Modulator

The above procedure is repeated to produce a stream of digital values that reflect the analog input. The operation of Δ modulator is summarized as follows:

[Conversion]

The analog input is differentiated to produce the digital output.

[Disadvantages]

1. Direct current voltages cannot be converted.
2. It is susceptible to slope overload* and high-frequency signals are difficult to be converted with accuracy.

Note: * Slope overload means the situation where the signal rapidly changes by large amounts, and the change is faster than the speed of integration.

[Countermeasure]

Integrate the analog input before it is input to the Δ modulator.

2.3 ΔΣ Modulator (Integrator + Δ Modulator)

In order to achieve conversion of direct current voltage, an integrator is added to the input circuit of the modulator. The unit that consists of a Δ modulator input circuit and an added integrator is called ΔΣ modulator. Since the two integrators have been gathered into a single one as shown by the equation below, the integrator follows the adder.

$$\int f1(x)dx + \int f2(x)dx$$
$$= \int (f1(x) + f2(x))\, dx$$
$$= \int f(x)dx$$

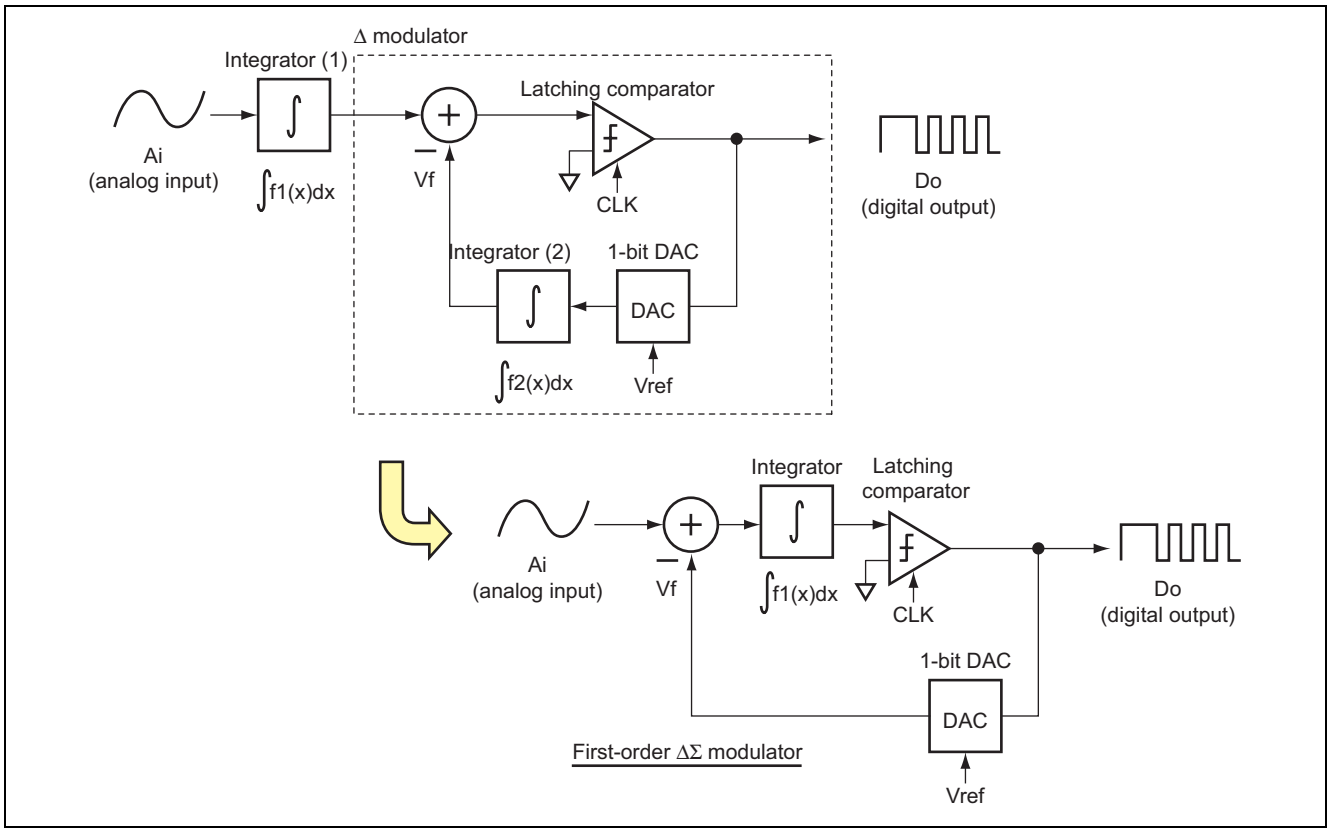


Figure 2.3 Input-Stage Integrator + Δ Modulator

2.4 First- and Second-Order ΔΣ Modulators

The first-order ΔΣ modulator has a single integrator while the second-order ΔΣ modulator has two. The second-order ΔΣ modulator has better performance in noise shaping than the first-order ΔΣ modulator.

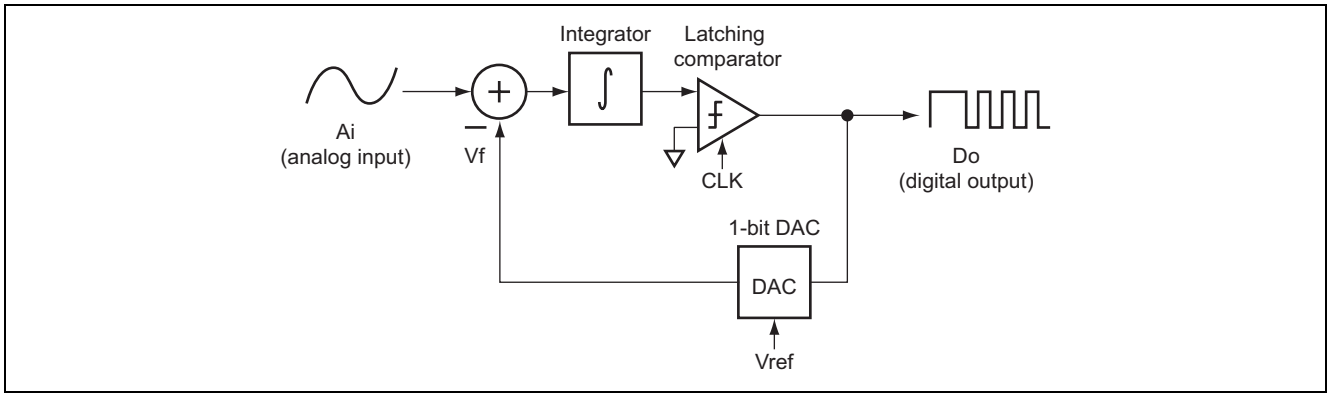


Figure 2.4 First-Order ΔΣ Modulator

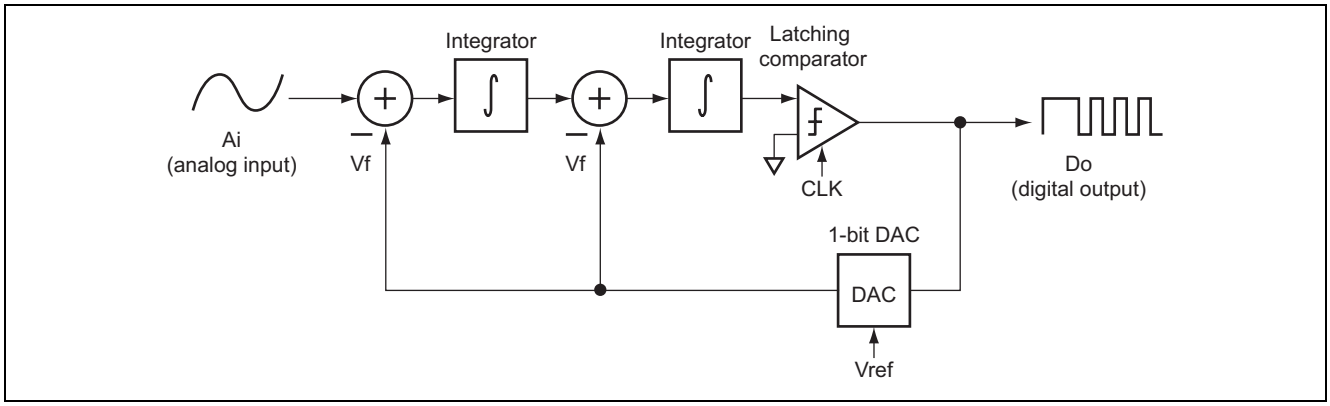


Figure 2.5 Second-Order ΔΣ Modulator

2.5 Second-Order ΔΣ A/D Converter

The operation of the second-order ΔΣ A/D converter is summarized as follows:

1. The analog input is integrated twice.
2. It is also differentiated twice, one in each of two differential loops.
   Although the differentiation is to be performed twice, the formulae have been expanded and consequently a single comparator is provided for the circuit.
3. The signal remains recoverable because differentiation and integration are the inverse transfer functions of each other. However, the above operation gives us a digital signal.
4. Digital filtering removes the noise introduced by sampling.

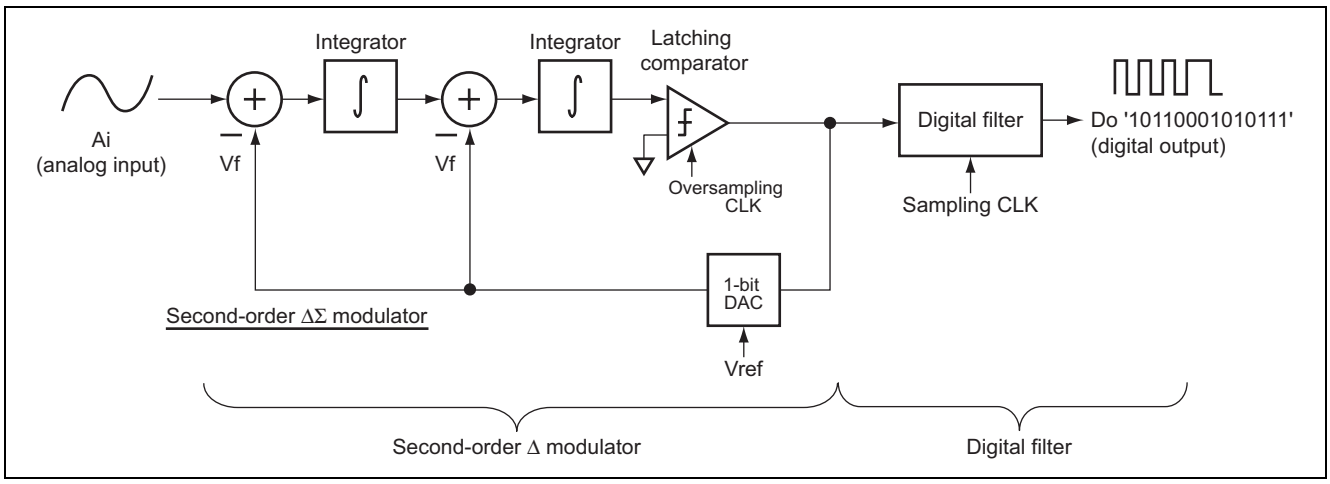


Figure 2.6 Second-Order ΔΣ A/D Converter

3. Filter

3.1 Digital Filter

The digital output of the ΔΣ modulator contains two types of noise generated by sampling: quantization error (figure 3.2) and aliasing noise (figure 3.3). This means that, by the calculation of digital values in real time, the interpolation and decimation are performed to reduce the noise components. Decimation refers to the conversion of a higher sampling frequency to a lower sampling frequency. The filter characteristics of a digital filter are expressed as an impulse response.

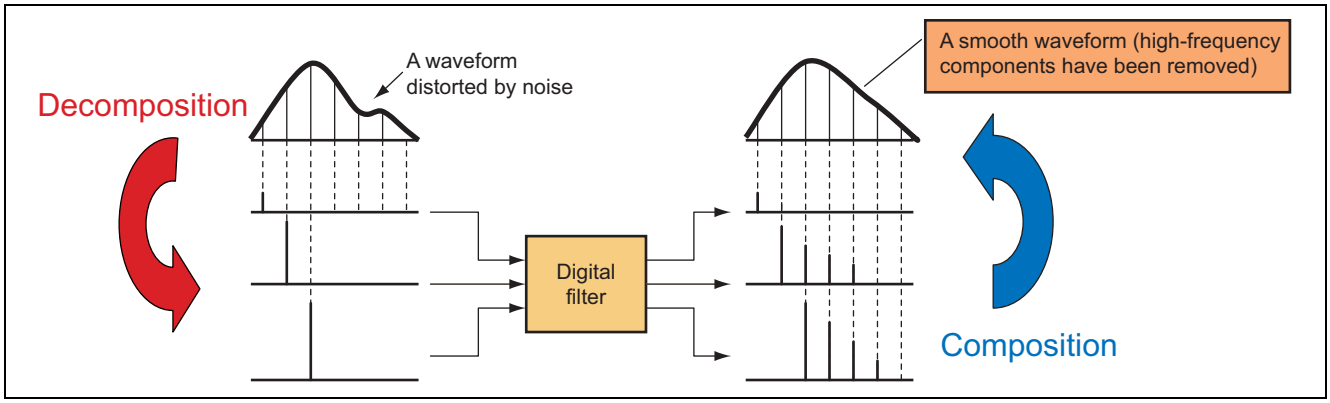


Figure 3.1 Digital Filter

3.2 Quantization Error

The quantization error is shown in the lower part of figure 3.2 as the sawtooth waveform.

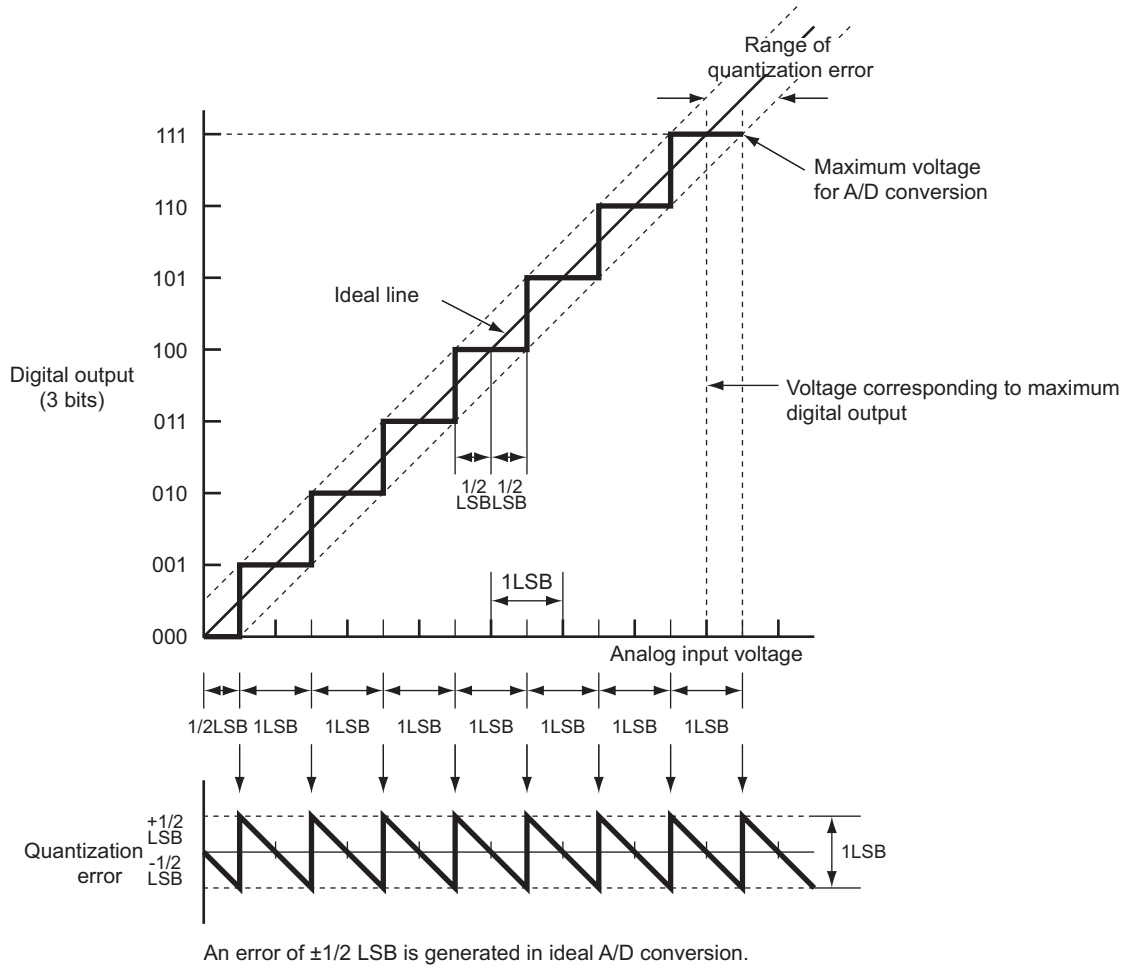


Figure 3.2 Quantization Error

3.3 Aliasing Noise

When analog signals f1 and f2 (f1 multiplied by 7) below are sampled at eight times the frequency of f1, the sampling points become identical with those that would be sampled from analog signal f2. The sampling points thus become a source for a component at frequency f2, and f2 is called the aliasing noise of f1 at the given sampling rate.

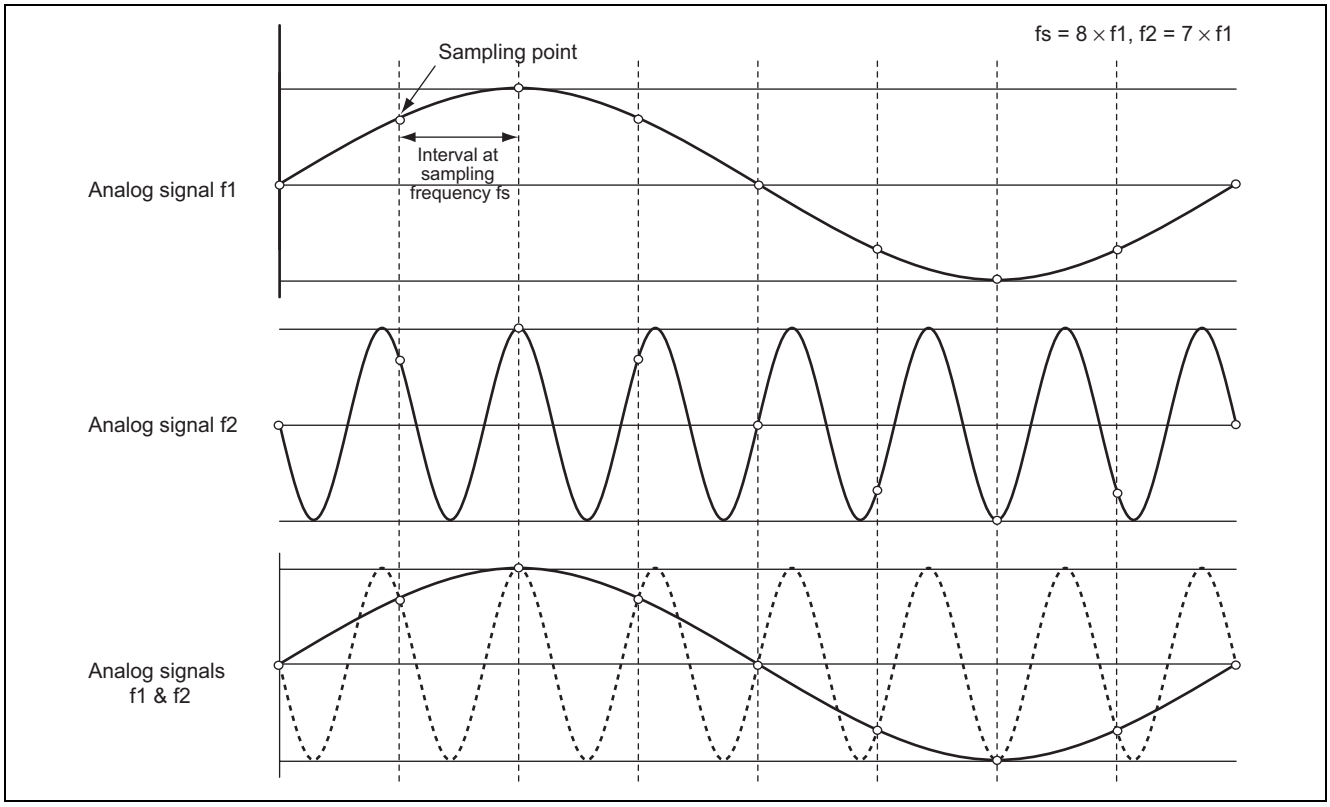


Figure 3.3 Aliasing Noise

3.4 Impulse Response

The impulse response is one way of analyzing signals in continuous (analog) systems. The impulse response of a system is the response the system generates in response to a unit impulse.

1. Decompose the continuous analog signal, which difficult to decompose as such, into impulses.
2. Given a transfer function h(t), the waveform in response to a single impulse is obtained by y(t) = h(t) * x(t).
3. By definition, the principle of superposition is valid in a linear system. Consequently, the superposition of the waveforms in response to the individual pulses represents the waveform in response to the overall input signal.

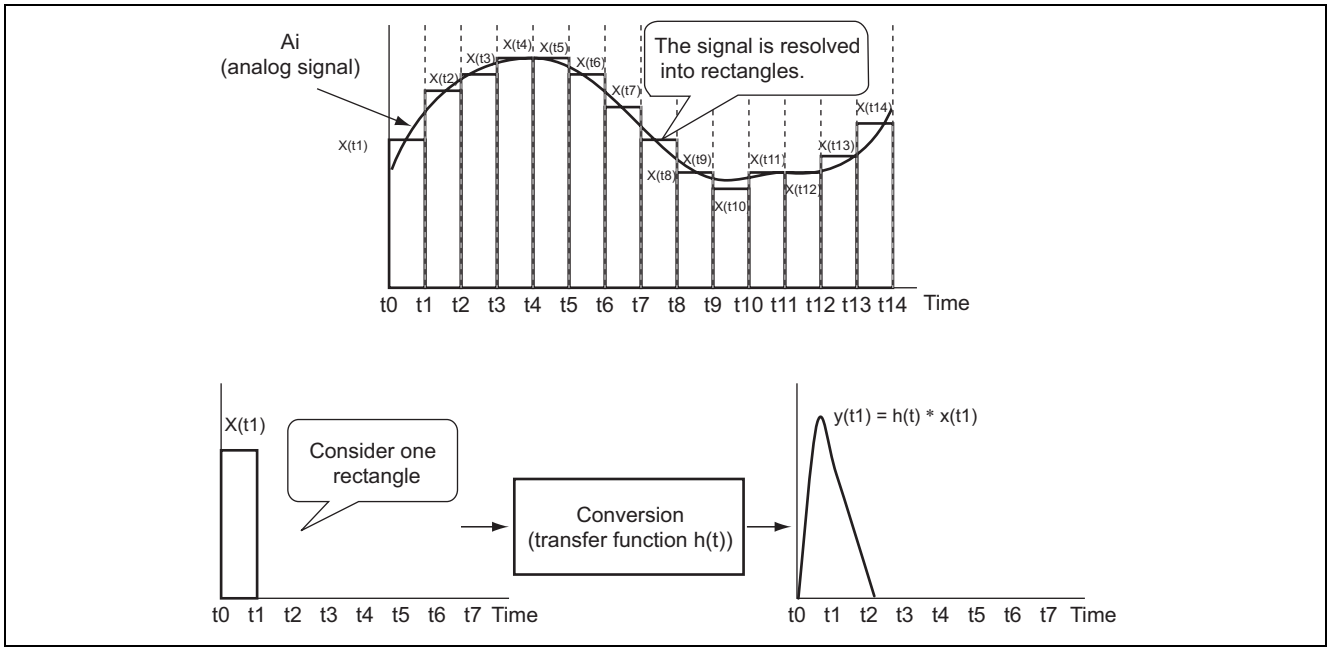


Figure 3.4 Impulse Responses

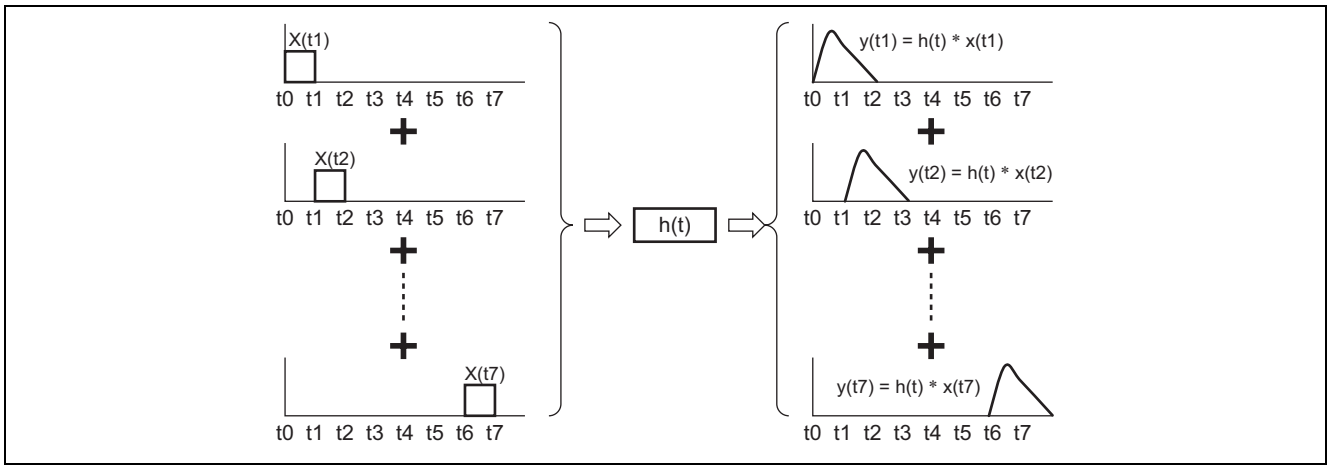


Figure 3.5 Definition of Superposition

3.5 Noise Reduction by Digital Filtering

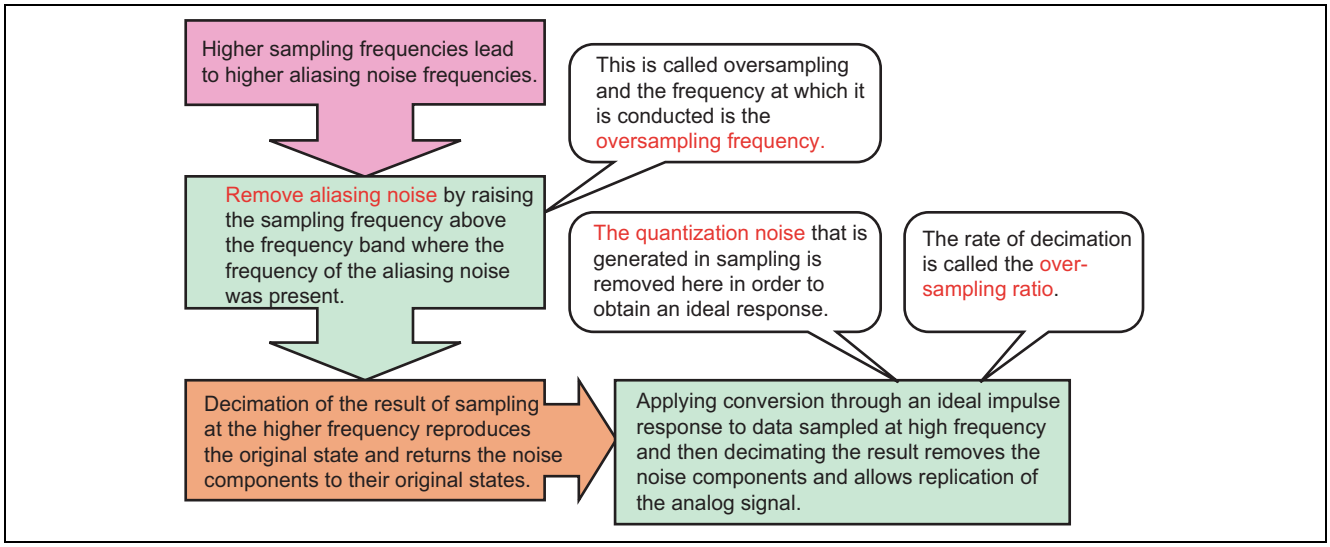


Figure 3.6 Procedure for Noise Reduction by Digital Filtering

3.6 Methods of Digital Filtering

The role of the digital filter is to reshape the samples so that they represent a stream of ideal impulse responses. This is achieved by multiplying the input impulses by a transfer function that synthesizes the ideal response. There are two ways to implement the multiplication required for the transfer function.

1. IIR (Infinite Impulse Response) Filter
   This is a method that combines an adder and a delay element to form a feedback loop. This kind of filter is referred to as an infinite impulse response filter because the output waveform in response to an impulse is dampened but continues indefinitely.

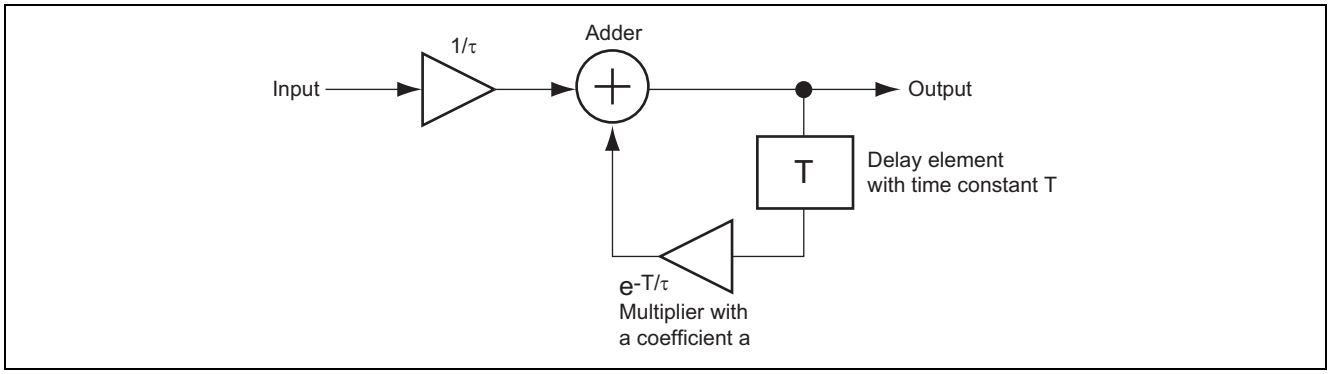


Figure 3.7 IIR (Infinite Impulse Response) Filter

2. FIR (Finite Impulse Response) Filter
   An FIR filter consists of taps on the respective bits of shift registers, multipliers on the taps, and an adder. The multipliers multiply the data from the taps by coefficients and the adder sums the input from the multipliers to produce the output. The coefficients, which are stored in ROM, are derived from the impulse response of an ideal filter. The H8/38086R ΔΣ A/D converter has an FIR filter.

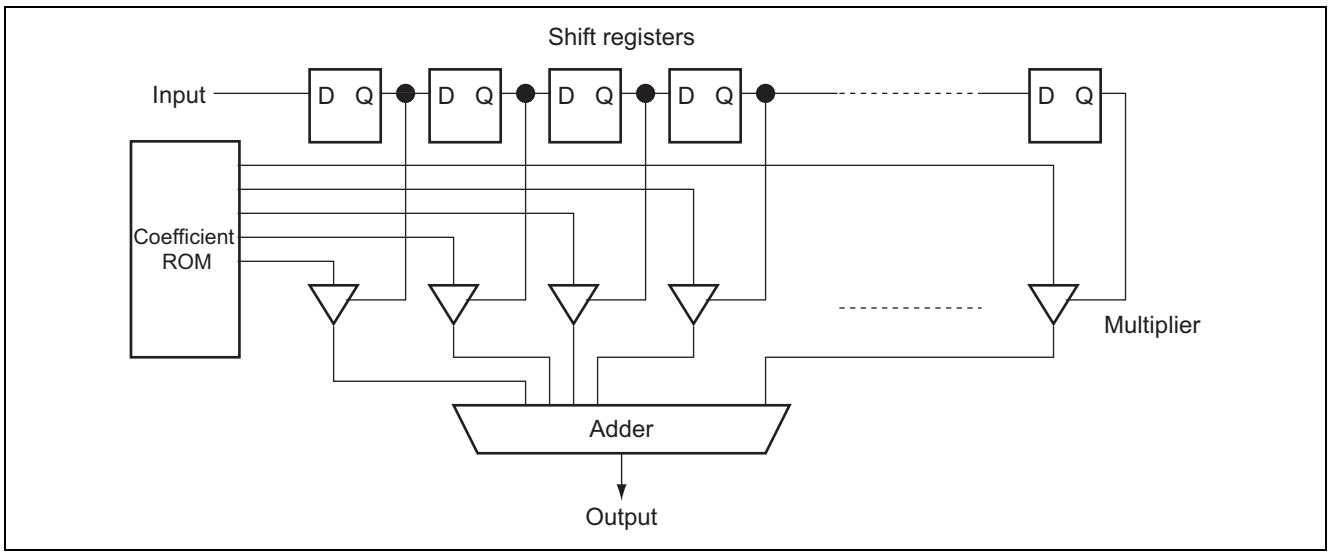


Figure 3.8 FIR (Finite Impulse Response) Filter

4. Errors and Methods of Correction

4.1 Errors in A/D Converter

4.1.1 Successive Approximation A/D Converter

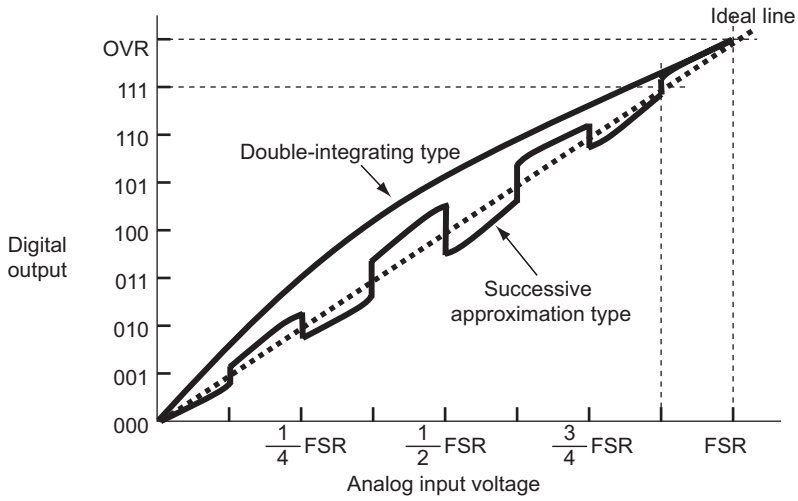
The output characteristics are subject to major errors at points where the values of large numbers of bits change, such as 1/2 FSR and 1/4 FSR. The dominant form of error is differential nonlinearity and the maximum error occurs at 1/2 FSR, where the values of all bits must be changed.

4.1.2 Double-Integrating A/D Converter

The output characteristic has no sharp changes. The dominant form of error is integral nonlinearity, which transcribes a smooth curve.

4.1.3 ΔΣ-Type A/D Converter

The error varies between the offset (OS) errors and full-scale (FS) error across the measurement range. The output characteristic is markedly linear and is very close to the ideal after the application of offset/full-scale error correction.



Note : FSR : Full-scale range (maximum input range)

Figure 4.1 Errors in Successive Approximation and Double-Integrating Type Converters

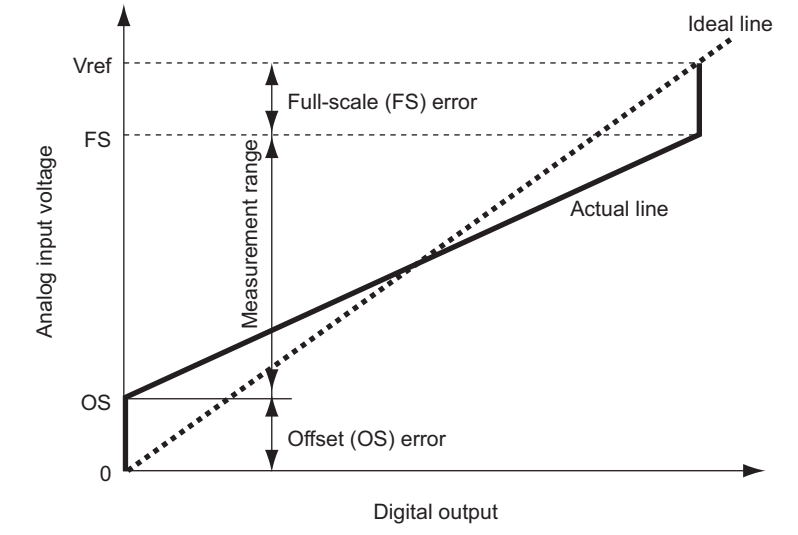


Figure 4.2 Errors in ΔΣ A/D Converters

4.1.4 Differential Nonlinearity Error

A differential nonlinearity error is depicted in figure 4.3 and refers to differences between the actual analog step size and the ideal value corresponding to one LSB (referred to simply as LSB in the figure below). When the step size is equal to the ideal for one LSB, the differential nonlinear error is zero. When the differential nonlinearity exceeds that for one LSB, the proportionality of output to input is reduced and code loss occurs, that is, the converter becomes incapable of producing one or more of the 2n codes for n bits of data.

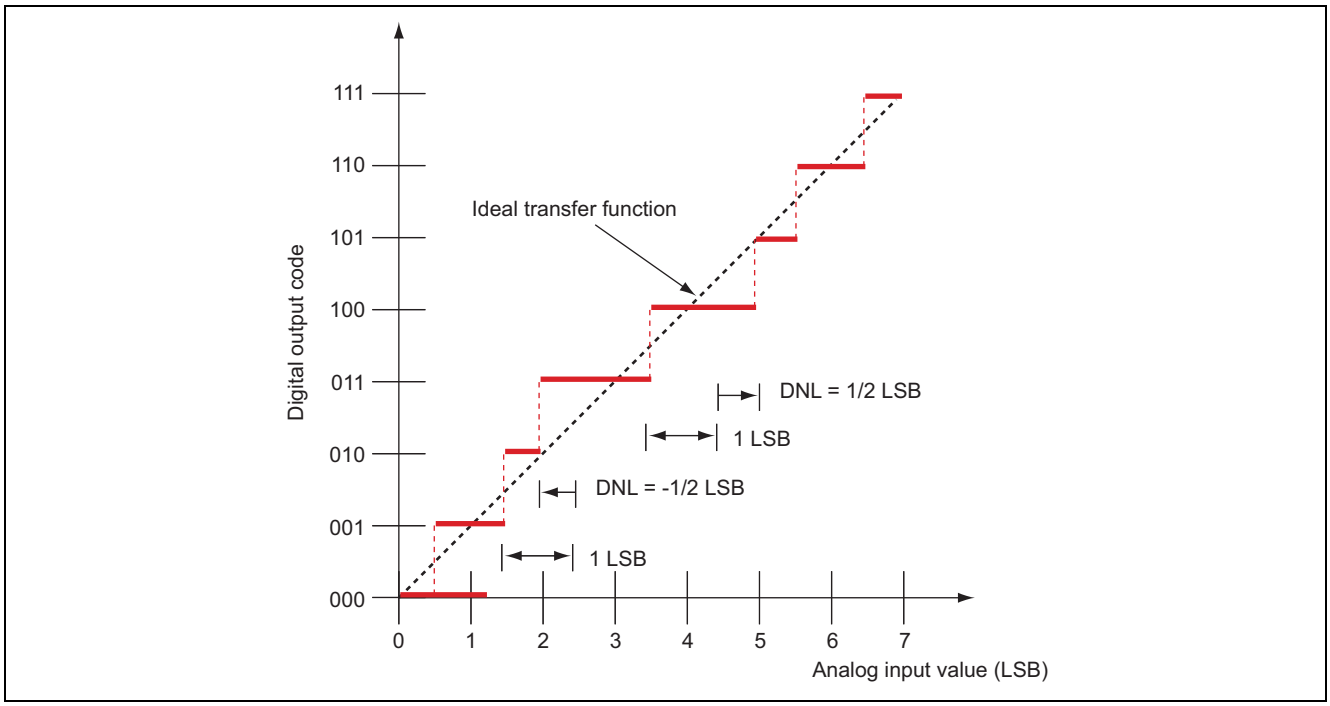


Figure 4.3 Differential Nonlinearity Error

4.1.5 Integral Nonlinearity Error

An integral nonlinearity error is the deviation of the actual result of conversion from the value given by the ideal line (see figure 4.4). Measurement of this deviation takes the form of measuring the changes from step to step.

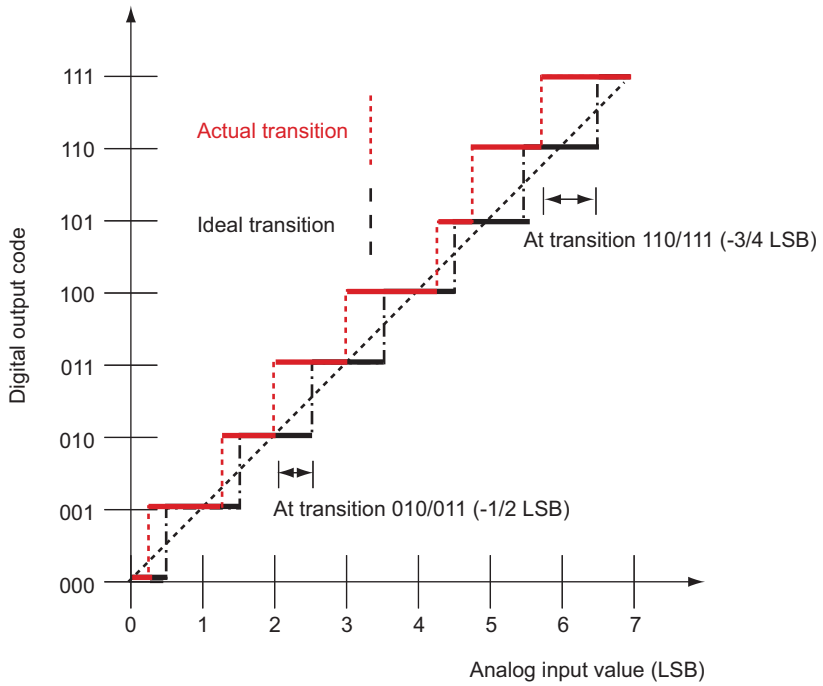


Figure 4.4 Integral Nonlinearity Error

4.2 Correction of Offset and Full-Scale Errors

4.2.1 Approach to Correction

Figure 4.5 shows the relation between digital values (ADDR values) and analog values (to be measured) of the ΔΣ A/D converter.

The response of an ideal A/D converter, shown as a dashed line in figure 5.5, is linear from the origin to the full-scale voltage. However, the actual relation is portrayed by the solid line from the offset (OS) error to the full-scale (FS) error. Consequently, offset/full-scale error correction should be applied to derive more accurate values from the measured digital values.

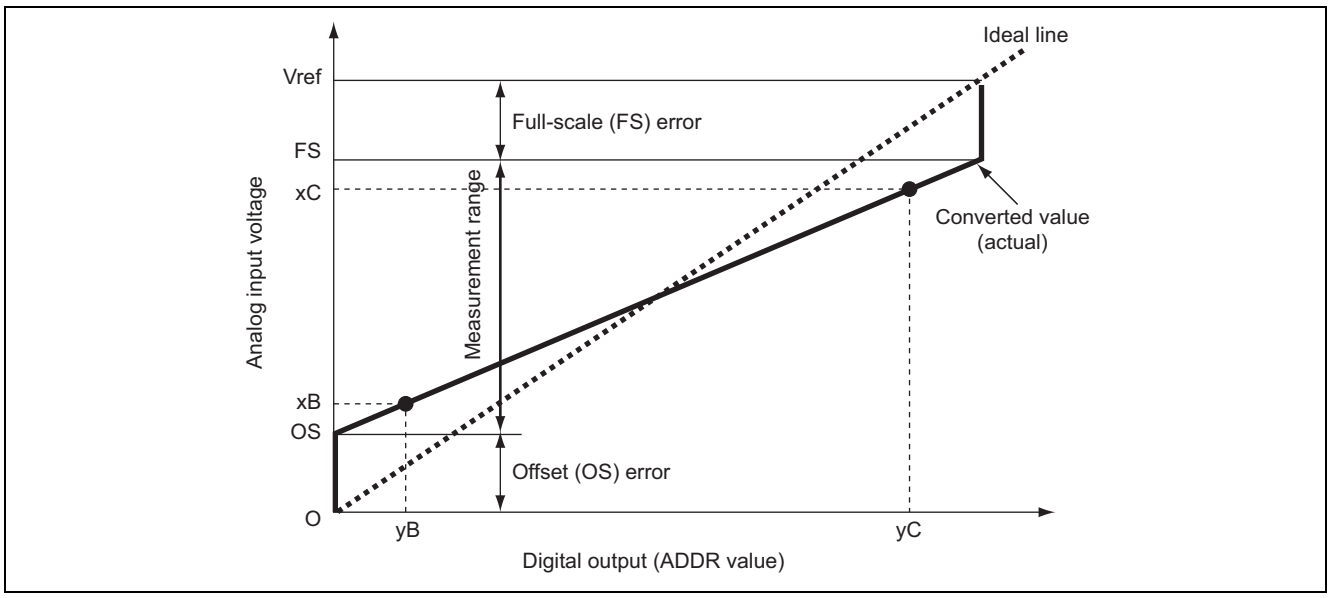


Figure 4.5 Relation of Analog Value (to be Measured) and Digital Value (ADDR Value)

The following equations describe the relations that define x and y values for the solid line.

lsb = (xC - xB) / (yC - yB) ···(1)
x = (xC - xB) / (yC - yB) * y + OS ···(2)
OS = xB - (xC - xB) / (yC - yB) * yB ···(3)

and from (1), (2), and (3), we have:

x = lsb * y + xB - lsb * yB = lsb * (y - yB) + xB

4.2.2 Correcting Offset and Full-Scale Errors

The procedure for offset/full-scale error correction is as follows.

1. Determine x and y values at the four points A, B, C, and D shown in figure 4.5.
2. Calculate the slope (lsb) by determining x and y values at points B and C.
3. Calculate the target value from the digital value (the value in ADDR).

Measured value = Slope (lsb) * (ADDR value – yB) + xB

4.3 Sample Program Code for Offset/Full-Scale Error Correction

An example of program code for offset/full-scale error correction is given below.

(1) Measurement Conditions

- Vcc = DVcc = 3.0 V
- Vss = 0 V
- Ain = 0 to 3.0 V
- Oversampling frequency = ϕ/32
- Conversion mode = Continuous mode
- PGA bypassed
- BGR = OFF

(2) Results of Two-Point Measurement

- xB = 12.838 mV
- yB = 26 (decimal)
- xC = 2924.092 mV
- yC = 16375 (decimal)
- Slope (lsb) = 0.17806924

(3) Sample Program

```
            .
            .
            .
c_data = correct(data);                          /* c_data = corrected data, data = ADDR value */
            .
            .
            .
 float correct (unsigned short y)
{
   const float lsb=0.17806924, yb=26, xb=12.838; /* slope, ADDR value of point B,              */
                                                 /*                  measured value of point B */
   return (lsb * ( y - yb ) + xb );              /* correction calculation                     */
}
```

5. Recommended Usage Conditions and Usage Notes

5.1 Recommended Condition 1: Programmable Gain Amplifier (PGA) Bypassed (with no Low-Pass Filtering Circuit)

5.1.1 Operating Conditions

(1) Register Settings

- PGA: Bypass mode
- Conversion mode: Wait mode
- Oversampling frequency (fovs): ϕ
- BGR circuit: Halted
- PB5/Vref/REF pin function: Vref input

(2) External Conditions

- Vcc = DVcc = 3.0 V
- Vref: External input 2.70 V
- fosc = 4 to 10 MHz
- Without low-pass filtering input circuit

Since the input impedance of the reference voltage (Vref) pin is approximately 20 kΩ, an input current will constantly flow.

Do not connect capacitive or resistive loads to the analog input pins.

5.1.2 External Circuit

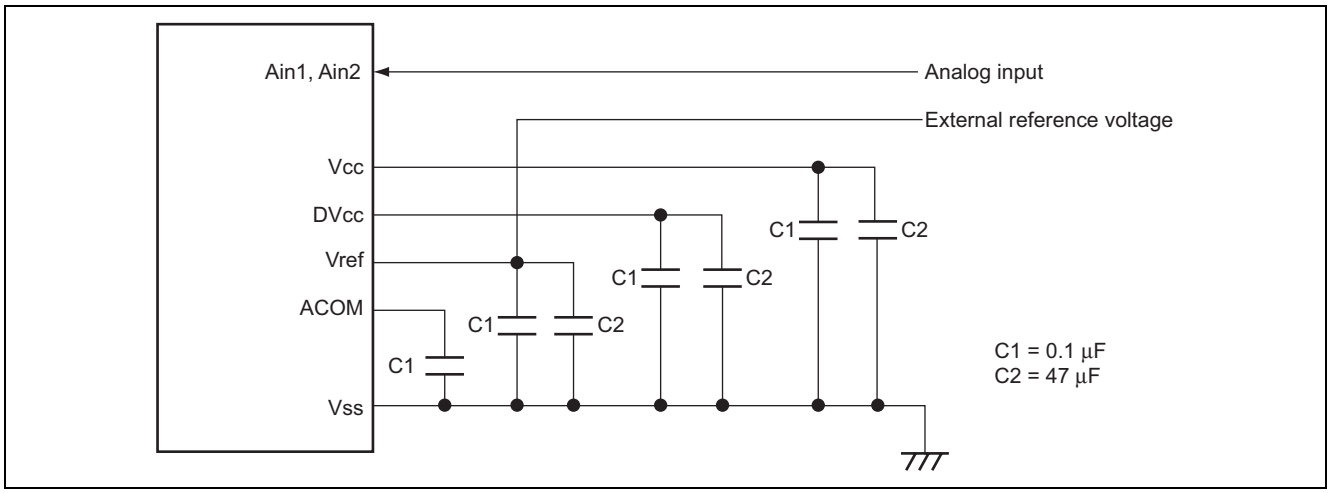


Figure 5.1 External Circuit (with no Low-Pass Filtering Circuit)

5.2 Recommended Condition 2: PGA = Gain 1 (with Low-Pass Filtering Circuit)

5.2.1 Operating Conditions

(1) Register Settings

- PGA: In use
- PGA gain selection: Set 1/3, 1, 2, or 4.
- Conversion mode: Wait mode
- Oversampling frequency (fovs): ϕ
- BGR circuit: Halted
- PB5/Vref/REF pin function: Vref input

(2) External Conditions

- Vcc = DVcc = 3.0 V
- Vref: External input 2.70 V
- fosc = 4 to 10 MHz
- With low-pass filtering circuit

Since the input impedance of the reference voltage (Vref) pin is approximately 20 kΩ, an input current will constantly flow.

5.2.2 External Circuit (Example for a Cutoff Frequency of 80 Hz)

Figure 5.2 shows an external circuit with the low-pass filtering circuit, for a cutoff frequency of 80 Hz.

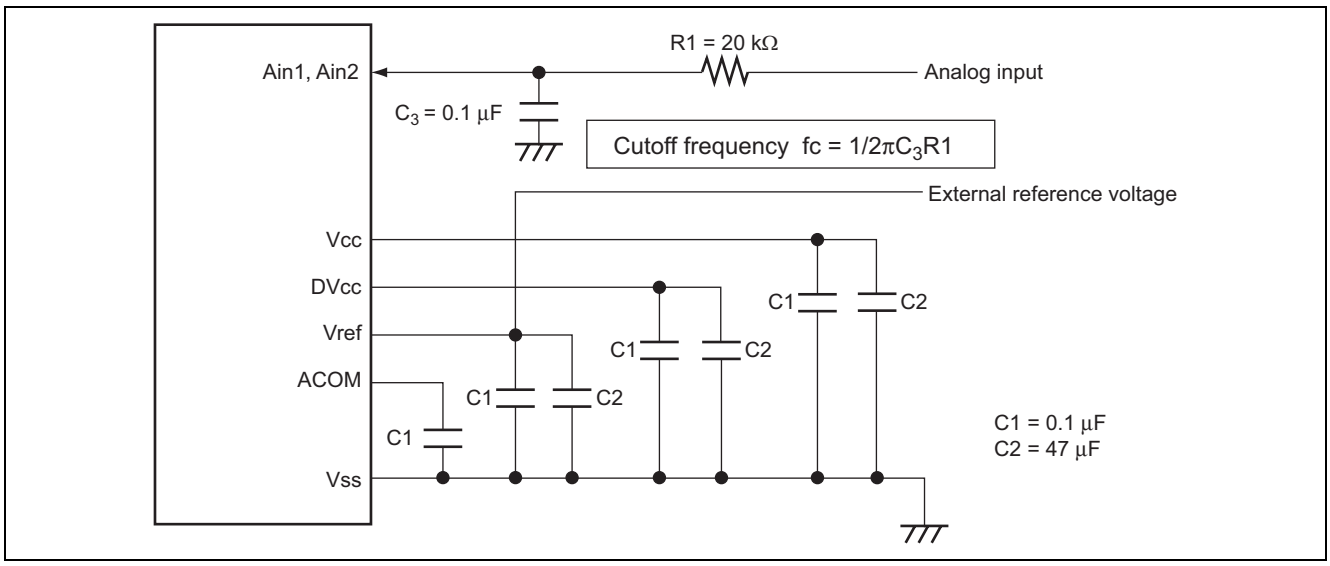


Figure 5.2 External Circuit (with Low-Pass Filtering Circuit)

5.3 Recommended Condition 3: PGA = Gain 1 (with the Internal Reference Voltage in Use)

5.3.1 Operating Conditions

(1) Register Settings

- PGA: In use
- PGA gain selection: Set 1/3, 1, 2, or 4.
- Conversion mode: Wait mode
- Oversampling frequency (fovs): ϕ
- BGR (bandgap reference) circuit: Running
- BGR output voltage trimming: Set an adjusted value of the BGR output voltage.
- PB5/Vref/REF pin function: REF output, with the internal reference voltage input to the reference voltage generation circuit.

(2) External Conditions

- Vcc = DVcc = 3.0 V
- Vref: On-chip BGR in use
- fosc = 4 to 10 MHz
- With low-pass filtering circuit

5.3.2 External Circuit (Example for a Cutoff Frequency of 80 Hz)

Figure 5.3 shows an external circuit with the internal reference voltage in use, for a cutoff frequency of 80 Hz.

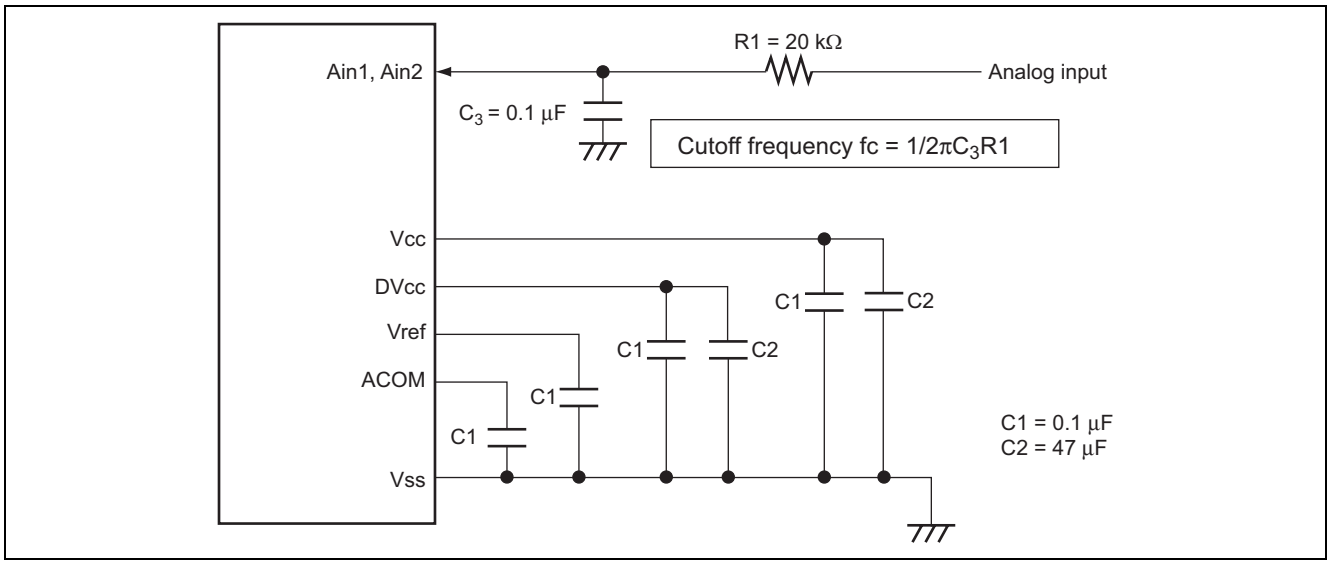


Figure 5.3 External Circuit (with the Internal Reference Voltage in Use)

5.4 Usage Notes

This subsection provides information on precautions to take to ensure accurate operation of the A/D converter.

5.4.1 Reduction of Internally Generated Noise

After the start of A/D conversion, place the chip in sleep mode to reduce noise generation by the CPU. As far as is possible, do not use any other peripheral functionality while A/D conversion is in progress.

5.4.2 Regarding the Oversampling Frequency

When the oversampling frequency has been divided, noise produced by peripheral I/O affects the converter. Consequently, do not use frequency division in normal A/D conversion.

5.4.3 Note on Large Potential Differences between the Input Pins (Ain1 and Ain2)

When the potential difference between input pins Ain1 and Ain2 is large, convergence on the voltage values can take time if measurement is attempted with switching between these two pins. In this case, discard the first value to be measured and use the data from the second measurement onwards.

5.4.4 Measurement when Power is Initially Supplied

Charging of the capacitor in the input circuit when power is initially supplied can take a little time. In this case, discard the first value to be measured and use the data from the second measurement onwards.

5.4.5 Averaging

Since errors in A/D conversion can be reduced by increasing the number of rounds of measurement and averaging the results, averaging across multiple rounds of measurement is strongly recommended where the extension of the processing time does not become a problem.

5.4.6 Treatment of the Internal Reference Voltage (REF)

(1) Adjustment of the Internal Reference Voltage

The internal reference value (typ.) is 1.17 V. Measure the value and, if necessary, adjust it before use. Adjustment of the output voltage is controlled by bits 2 to 0 in the BGR control register (BGRMR).

(2) External Use of the Internal Reference Voltage

The REF voltage output is incapable of driving sufficient current for external use. If the REF voltage is to be used externally, include an element that has a high input impedance (operational amplifier, etc.) to amplify the current.

5.4.7 Board Design

As a measure against noise, use a multilayered board having separate Vcc and GND layers and prevent the superposition of noise on input lines.

5.4.8 Input Impedance when the PGA is Bypassed

(1) When the PGA is in Use

Since the input impedance of the programmable gain amplifier is large, an analog filter (a circuit with time constant set by CR elements) can be used.

(2) When the PGA is Bypassed

When the A/D conversion time is 32 μs, each kΩ of input resistance produces a voltage drop of approximately 5.6 mV. Since this voltage is smaller with a longer conversion time, be sure to take this point into consideration as a worst-case condition in the design process.

5.4.9 External Reference Voltage (Vref) Settings

(1) How to Generate an External Reference Voltage from DVcc

The input impedance of the external reference voltage input (Vref) pin is 20 kΩ (typ.). To derive a Vref voltage supply from DVcc, the Vref voltage can be set to the value produced through voltage division by a resistor (R1) and the input impedance, as shown in the figure below. The value of the input impedance (20 kΩ) is only a typical value. Keep this in mind when selecting the resistor (R1).

(2) How to Suppress Supply Current

When supplying the Vref voltage from DVcc via R1, the current is DVcc/(Internal resistor + R1). While A/D conversion is not taking place, port (PB5) functionality (input) is selected for the Vref pin by clearing bits 3 and 2 in ADCR to 0. Cutting off this current path reduces current drawn.

External reference voltage (Vref) input = 0.2 to 0.9 DVcc

External reference voltage (Vref) input impedance = 20 kΩ

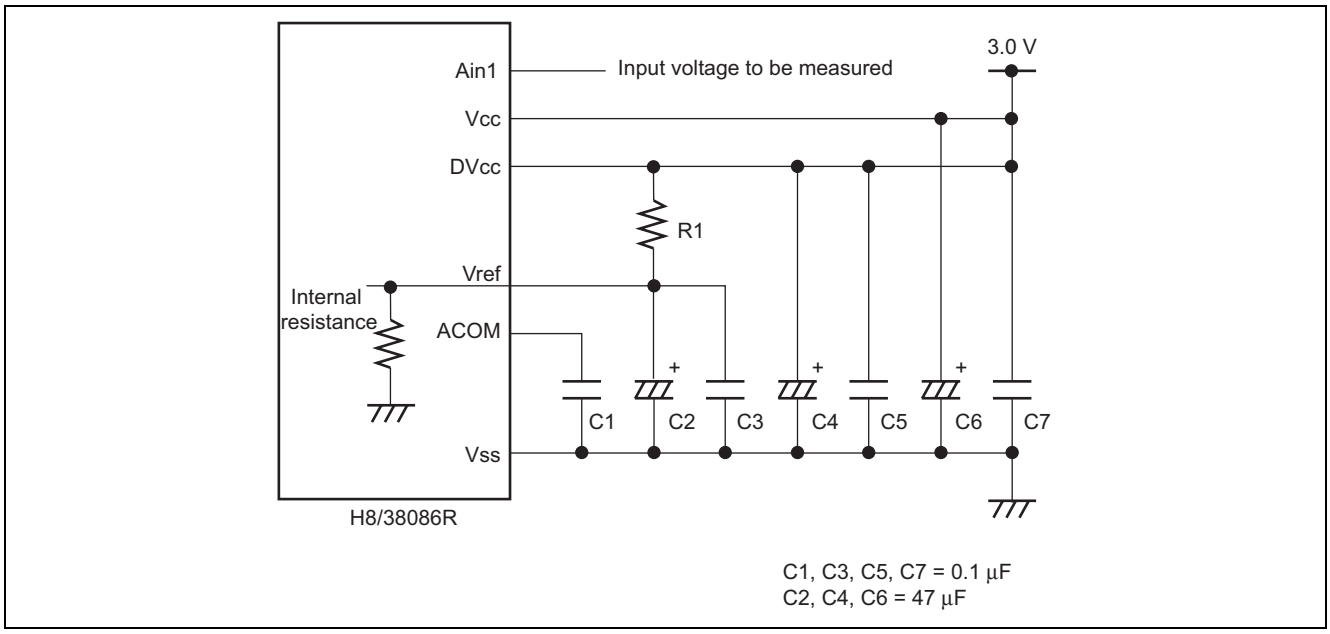


Figure 5.4 Measurement Circuit for the ΔΣ A/D Converter (Example)
(Divided Voltage from DVcc is Supplied as Vref Voltage)

6. Application Notes

6.1 Voltage Measurement Using the ΔΣ A/D Converter when an External Reference Voltage Used

6.1.1 Specifications

- As is shown in figure 6.1, the internal ΔΣ A/D converter of the H8/38086R is used to measure the voltage input to the Ain pin.
- An external input voltage provides the reference voltage for the ΔΣ A/D converter.
- The voltage on the Ain1 pin is measured, that is, converted from an analog level to a digital value, and the result of A/D conversion is stored in the internal RAM. A/D conversion is performed twice, with the result of the first conversion being discarded. Only the results of the second conversion are stored. Offset and full-scale errors in the 14-bit results of A/D conversion read-out from the A/D Data Register (ADDR) are corrected before the data is stored.
- A/D conversion is performed in the following operating mode: conversion is in the wait mode, the oversampling frequency is ϕ, and the programmable gain amplifier (PGA) is bypassed.
- The device is placed in sleep (high-speed) mode during A/D conversion, since this reduces the noise generated by the CPU and other modules. On generation of the A/D-conversion-complete interrupt, the device makes the transition from sleep mode to active (high-speed) mode; correction is applied and then the results of A/D conversion are stored in the internal RAM. The module-standby function is used to place all internal peripheral modules other than the ΔΣ A/D converter (i.e. the SCI modules, successive approximation A/D converter, timer F, RTC, TPU, IIC2, PWM, AEC, watchdog timer, and LCD controller/driver) in the module-standby mode.

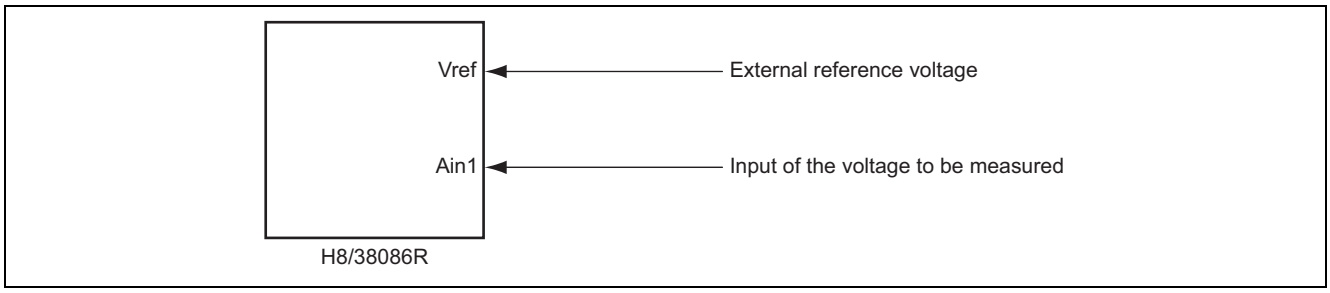


Figure 6.1 Configuration for Voltage Measurement by the ΔΣ A/D Converter (with an External Reference Voltage in Use)

6.1.2 ΔΣ A/D Converter Measurement Conditions

Figure 6.2 shows the measurement circuit for this sample task.

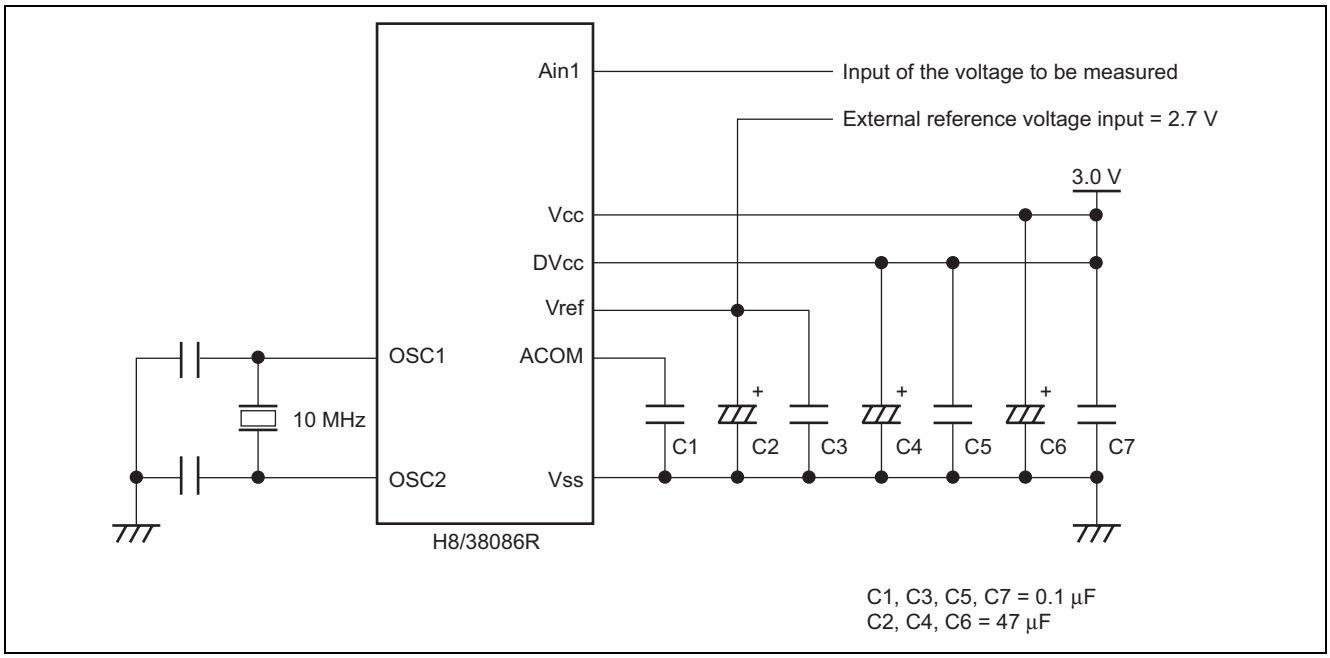


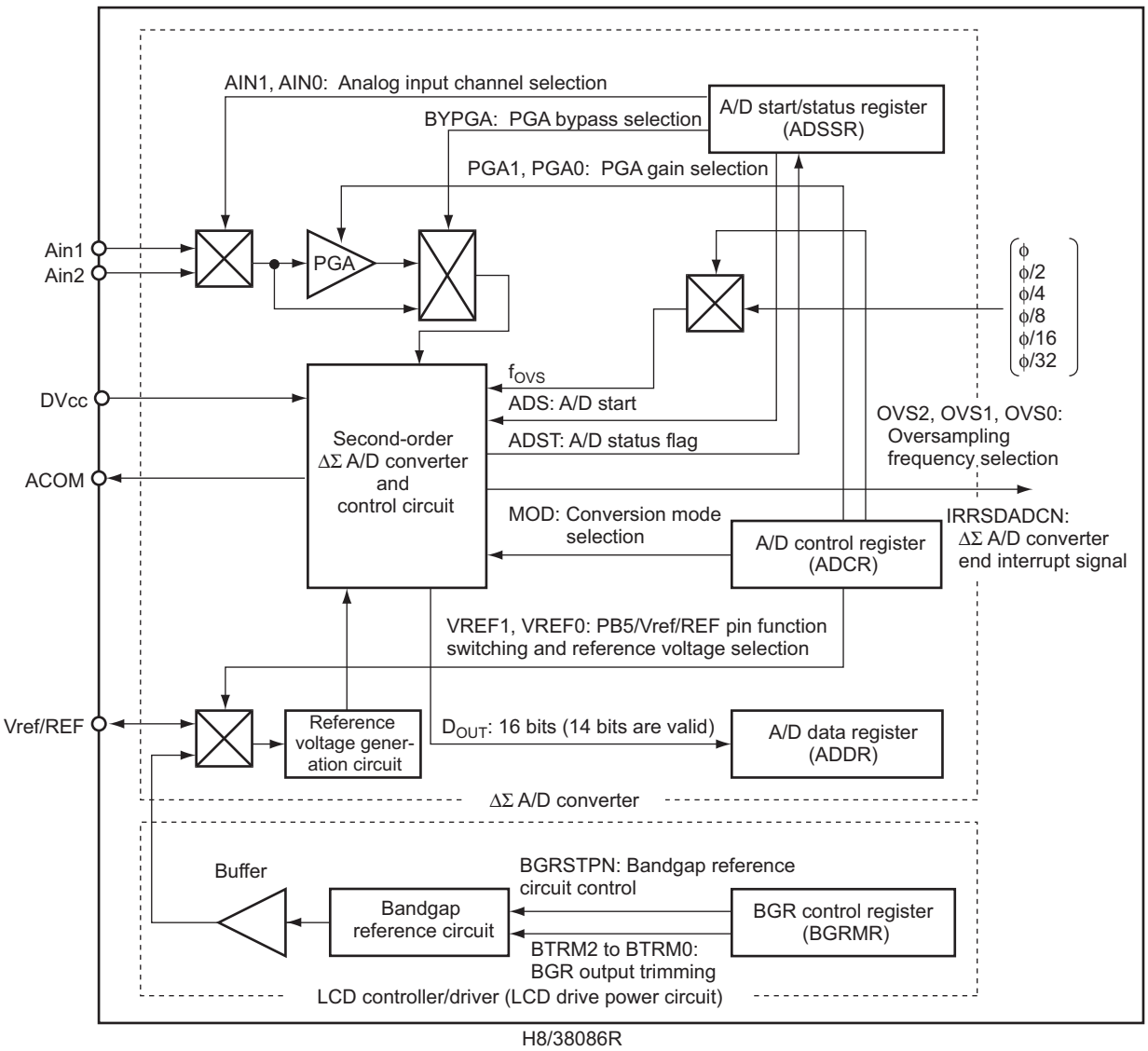
Figure 6.2 Circuit Allowing Measurement by the ΔΣ A/D Converter (with an External Reference Voltage in Use)

The following are the conditions of operation for voltage measurement by the ΔΣ A/D converter when an external voltage is in use.

- Vcc = 3.0 V
- DVcc = 3.0 V
- Vref = Externally input 2.7 V
- System clock frequency (ϕ) = 10 MHz
- Oversampling frequency (fovs) = ϕ
- PGA bypassed
- Conversion mode = Wait mode
- Input voltage range = 0.2 V to Vref (2.7 V)

6.1.3 Description of Functions Used

Figure 6.3 shows a block diagram of the ΔΣ A/D converter.



[Legend]
DVcc: ΔΣ A/D converter power supply pin
Ain1: Analog input pin 1
Ain2: Analog input pin 2
Vref: Reference voltage pin
REF: Internal reference voltage output pin
ACOM: Analog block voltage stabilization pin

Figure 6.3 Block Diagram of the ΔΣ A/D Converter

The characteristics and features of the ΔΣ A/D converter are described below.

(1) Features

- Resolution: 14 bits
- Number of input channels: 2
- Conversion method: Second-order ΔΣ, 320-times oversampling
- Conversion time: 32 μs per channel (in operation at 10 MHz)
- Number of interrupt sources: 1 (A/D conversion-complete interrupt request)
- Module standby mode for individual modules means that modules that are not in use can be placed in standby mode while ΔΣ A/D conversion is in progress.

(2) Input/Output Pins

The pins used with the ΔΣ A/D converter are described in table 6.1.

Table 6.1 ΔΣ A/D Converter Pins

Pin Name	Symbol	I/O	Function
Reference voltage pin	Vref	Input	External reference voltage input
Internal reference voltage output pin	REF	Output	Internal reference voltage output
Analog block voltage stabilization pin	ACOM	Output	Provides stabilization when connected to a capacitor with a value of 0.1 μF
Analog input pin 1	Ain1	Input	Analog input pin
Analog input pin 2	Ain2	Input	Analog input pin
ΔΣ A/D converter analog power supply pin	DVcc	Input	Power supply pin

(3) Internal Registers

The registers of the ΔΣ A/D converter are listed below.

- A/D Data Register (ADDR)
  ADDR is a 16-bit read-only register that holds the result of A/D conversion. ADDR is always readable by the CPU. The value in ADDR is undefined during A/D conversion. After conversion, the 14 higher-order bits of ADDR holds the fourteen bits of converted data. ADDR retains this data until the next round of conversion is started. The initial value in ADDR is undefined.
- BGR Control Register (BGRMR)
  BGRMR controls operation of the bandgap reference circuit (BGR) and is used to adjust the internal reference voltage (BGR output voltage) output on the REF pin.
- A/D Control Register (ADCR)
  ADCR is used to set the conversion mode, the multiplier for the PGA (programmable gain amplifier), the function of pin PB5/Vref/REF, the reference voltage, and the oversampling frequency.
- A/D Start/Status Register (ADSSR)
  ADSSR contains the A/D conversion status flag, and is used to select the analog input channel and the PGA bypass mode.

(4) ΔΣ A/D Converter

In the ΔΣ A/D converter, a ΔΣ modulator is applied to convert analog input voltages in the range determined by the voltage on the Vref pin to digital values with a resolution of 14 bits. The converter consists of an analog block, the main component of which is the ΔΣ modulator, and a digital block based on a digital filtering control circuit.
In the analog block, the voltages from analog input pins 1 and 2 (Ain1 and Ain2) are sampled at a frequency 320 times that of the conversion cycle (oversampling frequency), and then converted to a stream of 1-bit digital values by the second-order ΔΣ modulator. The result of this conversion process is passed through the decimation filter in the digital block, which produces the 14-bit unsigned binary output that is placed in the A/D Data Register (ADDR). In the ADDR, bit 13 is the MSB (most significant bit) and bit 0 the LSB (least significant bit).

(5) Conversion Modes of the ΔΣ A/D Converter

The ΔΣ A/D converter supports two conversion modes: wait mode and continuous mode.

(a) Wait Mode

In the wait mode, A/D conversion of the analog input on the specified channel is performed once in the following sequence.

1. When the ADS bit of the A/D Start/Status Register (ADSSR) is set to 1 by software, A/D conversion of the analog input on the specified channel starts.
2. On completion of A/D conversion, the result is transferred to the A/D Data Register (ADDR).
3. The A/D converter interrupt request flag (IRRSAD) of Interrupt Request Register 2 (IRR2) is set to 1. At this point, if the A/D Converter Interrupt Request Enable bit (IENSAD) of Interrupt Enable Register 2 (IENR2) is 1, an A/D conversion-complete interrupt request is also generated.
4. The ADST bit is held at 1 during A/D conversion and then automatically cleared to 0 when the conversion is finished. The A/D converter then enters the wait state.

(b) Continuous Mode

In the continuous mode, continuous A/D conversion of the analog input on the specified channel is performed in the following sequence.

1. When the MOD bit of the A/D Control Register (ADCR) is set to 1 by software, A/D conversion of the analog input on the specified channel starts.
2. On completion of A/D conversion, the result is transferred to the A/D Data Register (ADDR).
3. The A/D converter interrupt request flag (IRRSAD) of Interrupt Request Register 2 (IRR2) is set to 1. At this point, if the A/D Converter Interrupt Request Enable bit (IENSAD) of Interrupt Enable Register 2 (IENR2) is 1, an A/D conversion-complete interrupt request is also generated.
4. Steps 2 and 3 are repeated. The converter is taken out of the continuous mode by placing it in the watch mode, sub-active mode, sub-sleep mode, or standby mode, or by clearing the MOD bit of the ADCR register to 0.

(6) ΔΣ A/D Converter Registers and Modes of Operation

The states of the registers of the ΔΣ A/D converter in the various MCU operating modes and in module-standby mode are as listed in table 6.2.

Table 6.2 Operating Modes and the ΔΣ A/D Converter

Operating Mode	On a Reset	Active	Sleep	Watch	Sub-Active	Sub-Sleep	Standby	Module Standby
ADCR register	Reset	Operational	Retained	Retained	Retained	Retained	Retained	Retained
ADSSR register	Reset	Operational	Operational	Retained	Retained	Retained	Retained	Retained
ADDR register	Retained*	Operational	Operational	Retained	Retained	Retained	Retained	Retained
BGRMR register	Reset	Operational	Retained	Retained	Operational	Retained	Retained	Retained

Note: * The value is undefined after a power-on reset.

(7) Pin Assignments

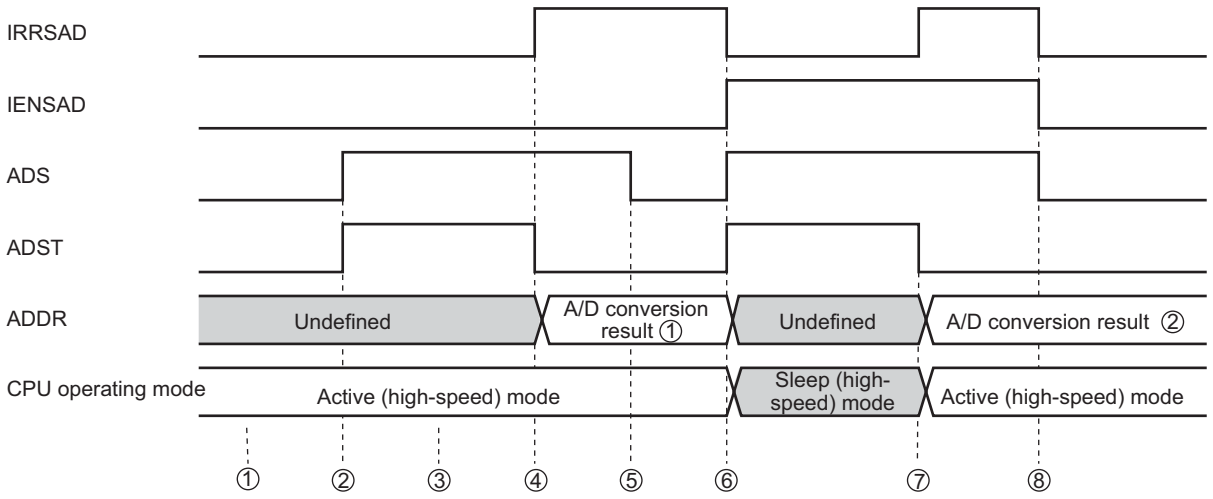
Pin assignments in this sample task are listed in table 6.3.

Table 6.3 Assignment of Functions

Pin Name	Description
Vref/REF	Vref, input for the external reference voltage at 2.7 VDC
DVcc	Input for the 3.0 VDC analog power supply for the ΔΣ A/D converter
Ain1	Analog input for the value to be measured
Ain2	Not used
ACOM	Analog-block voltage-stabilization pin for connection to a 0.1-μF capacitor

6.1.4 Principles of Operation

Figure 6.4 illustrates the principles of operation of ΔΣ A/D conversion in this sample task, for which the wait mode is used. Software polling is used to determine when the first round of A/D conversion has ended. On completion of the second round of A/D conversion, an interrupt is used to take the MCU out of the sleep (high-speed) mode.



① Initial settings for the ΔΣ A/D converter

Software processing	1. Set ADCR to H'04. (conversion mode: wait mode, oversampling frequency: ϕ, PB5/Vref/REF pin function: Vref input, reference voltage: external) 2. Set ADSSR to H'18 (analog input channel: Ain1, PGA bypassed)

② Start of the first round of A/D conversion

Hardware processing	Conversion by the ΔΣ A/D converter starts when the ADST bit of ADSSR is set to 1.
Software processing	Start A/D conversion by setting the ADS bit of ADSSR to 1.

③ Waiting for completion of the first round

Hardware processing	Conversion of the analog input to a digital value.
Software processing	Wait until the ADST bit of ADSSR becomes 0 (use software to poll the bit).

④ Completion of the first round

Hardware processing	Clearing the ADST bit of ADSSR to 0 and transferring the result of A/D conversion to ADDR.

⑤ Discarding the result of the first round

Software processing	Clear the ADS bit of ADSSR to 0.

⑥ Start of the second round of A/D conversion

Hardware processing	1. Conversion by the ΔΣ A/D converter starts when the ADST bit of ADSSR is set to 1. 2. Placing the MCU in the sleep (high-speed) mode.
Software processing	1. Start A/D conversion by setting the ADS bit of ADSSR to 1. 2. Clear the IRRSAD bit of IRR2 to 0 and set the IENSAD bit to 1 to enable the A/D conversion-complete interrupt. 3. Issue the sleep instruction to place the MCU in the sleep (high-speed) mode.

⑦ End of the second round

Hardware processing	1. Clearing the ADST bit of ADSSR to 0 and transferring the result of conversion to ADDR. 2. Taking the MCU out of the sleep (high-speed) mode and placing it in the active (high-speed) mode in response to an A/D conversion-complete interrupt request.

⑧ Reading of the result of the second round (A/D conversion-complete interrupt processing)

Software processing	1. Clear the IRRSAD and IENSAD bits of IRR2 to 0 to disable the A/D conversion-complete interrupt. 2. Clear the ADS bit of ADSSR to 0, read the result of A/D conversion from ADDR, and store it in the internal RAM.

Figure 6.4 Voltage Measurement by the ΔΣ A/D Converter with an External Reference Voltage

6.1.5 Description of Full-Scale/Offset Error Correction

Figure 6.5 shows the relation between digital values (ADDR values) and analog levels (to be measured) for the ΔΣ A/D converter.

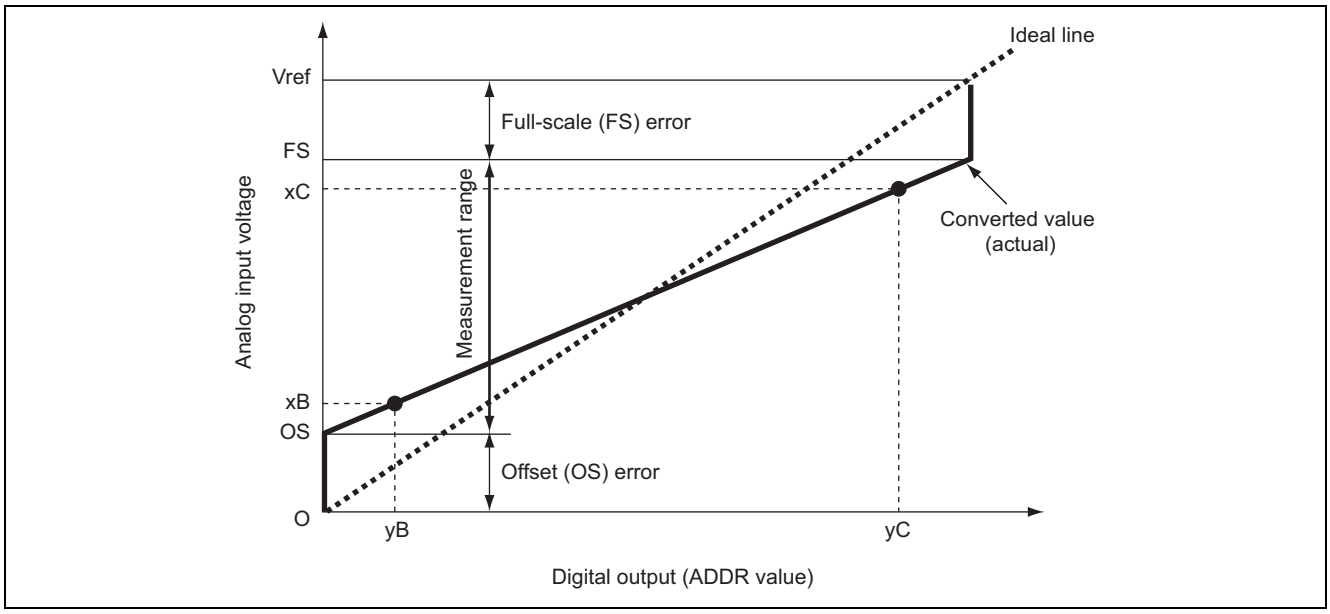


Figure 6.5 Relation between Analog Level (to be Measured) and Digital Values (in ADDR)

The following equations describe the relations that define x and y values for the solid line.

$$\text{Slope (lsb)} = (xC - xB) / (yC - yB) \quad \cdots(1)$$

$$\text{Target (x)} = (xC - xB) / (yC - yB) * y + OS \quad \cdots(2)$$

$$\text{Offset Error (OS)} = xB - (xC - xB) / (yC - yB) * yB \quad \cdots(3)$$

and from (1), (2), and (3), we have:

$$\text{Target value (x)} = lsb * y + xB - lsb * yB = lsb * (y - yB) + xB$$

A sample program for offset/full-scale error correction is given below.

```
        .
        .
        .
c_data = correct ( data ) ;                                  /* c_data  = corrected data,     */
                                                             /*              data = ADDR value */
        .
        .
        .
float correct ( unsigned short y )
{
    const float lsb = 0.1780692, yb = 1094, xb = 203.016 ; /* slope ( lsb ),                 */
                                                             /*   value of point B ( xB , yB ) */
    return ( lsb * ( y - yb ) + xb ) ;                       /* offset/full-scale              */
                                                             /*              error calculation */
}
```

The procedure for offset/full-scale error correction is as follows.

1. Determine values at the four points A, B, C, and D shown in figure 6.5.
2. Calculate the slope (ideal voltage step for 1 lsb) from the x and y values at points B and C.

   (Example) Results of two-point measurement
   xB = 203.016 mV
   yB = 1094 (decimal)
   xC = 2695.095 mV
   yC = 15089 (decimal)

   (Example) Calculation of the slope
   lsb = (xC – xB) / (yC – yB)
   = (2695.095 – 203.016) / (15089 – 1094)
   = 0.1780692

3. Set lsb to 0.1780692, xb to 203.016, and yb to 1094.
4. Use the above constants to calculate target values from the results of A/D conversion (values in ADDR).

   (Example) Target value = Slope * (ADDR value – yb) + xB

6.1.6 Description of Software

(1) Internal Register Usage

The following tables describe the internal registers usage in this sample task.

- A/D Data Register (ADDR) Address: H'F062

Table 6.4 A/D Data Register (ADDR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
15	ADD13	Undefined	R	This 16-bit read-only register holds the results of A/D conversion. On completion of a round of conversion, the 14 higher-order bits hold the 14 bits of A/D-converted data. Values in ADDR during A/D conversion are undefined.	—
14	ADD12				
13	ADD11				
12	ADD10				
11	ADD9				
10	ADD8				
9	ADD7				
8	ADD6				
7	ADD5				
6	ADD4				
5	ADD3				
4	ADD2				
3	ADD1				
2	ADD0				
1	—	Undefined	—	—	—
0	—	Undefined	—	—	—

- A/D Control Register (ADCR) Address: H'F060

Table 6.5 A/D Control Register (ADCR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	MOD	0	R/W	Conversion Mode Selection This bit selects the conversion mode. When MOD = 1, A/D conversion proceeds regardless of the value of the ADS bit in the ADSSR register. 0: Wait mode 1: Continuous mode	0
6	OVS2	0	R/W	Oversampling Frequency Selection	0
5	OVS1	0	R/W	These bits select the oversampling frequency.	0
4	OVS0	0	R/W	000: ϕ 001: ϕ/2 010: ϕ/4 011: ϕ/8 100: ϕ/16 101: ϕ/32 11x: Setting prohibited	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	VREF1	0	R/W	PB5/Vref/REF Pin Function Switch and Reference Voltage Selection The setting here determines whether the PB5/Vref/REF pin is used as the PB5 pin, Vref pin, or REF pin. The setting also determines whether the reference voltage for the ΔΣ A/D converter is an external reference voltage (Vref) or the internal reference voltage (REF). Note, however, that when REF is to be used, the BGRSTPN bit of BGRMR must be set to 1 to start operation of BGR (bandgap reference circuit) before these bits are set. 00: The pin functions as the PB5 input pin. 01: The pin functions as the Vref input pin, so the reference-voltage generation circuit is an external reference voltage (Vref). 10: The pin functions as the REF output pin. 11: The pin functions as the REF output pin, and the reference voltage input to the reference-voltage generation circuit is the internal reference voltage (REF). Setting B'11 causes the REF pin to output the internal reference voltage (REF), which is also input to the reference-voltage generation circuit in the ΔΣ A/D converter. Set these bits to B'11 to use the internal reference voltage (REF) in converter operation.	0
2	VREF0	0	R/W		1
1	PGA1	0	R/W	PGA Gain Selection	0
0	PGA0	0	R/W	These bits specify multiplication of the analog input voltage by a multiplier in the range from 1/3 to 4. 00: x1 01: x2 10: x4 11: x1/3	0

[Legend]
x: Don't care

- A/D Start/Status Register (ADSSR) Address: H'F061

Table 6.6 A/D Start/Status Register (ADSSR)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	ADS	0	R/W	A/D Conversion Start In the wait mode (the MOD bit of ADCR is 0), setting this bit to 1 starts A/D conversion.	1
6	ADST	0	R	A/D Status Flag In the wait mode (the MOD bit of ADCR is 0), this bit can be read to determine the state of A/D conversion. 0: The converter is idle. 1: A/D conversion is in progress.	—
5	AIN1	0	R/W	Analog Input Channel Selection	0
4	AIN0	0		These bits select the analog input channel. 00: Deselected 01: Ain1 10: Ain2 11: Deselected	1
3	BYPGA	0	R/W	PGA Bypass Selection This bit selects whether the analog data is input via the PGA or directly to the second-order ΔΣ A/D converter. 0: Input analog data via the PGA. 1: Input analog data to the second-order ΔΣ A/D converter.	1
2	—	0	—	Reserved (these bits cannot be modified)	—
1	—	0	—		—
0	—	0	—		—

- Interrupt Enable Register 2 (IENR2) Address: H'FFF4

Table 6.7 Interrupt Enable Register 2 (IENR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
5	IENSAD	0	R/W	ΔΣ A/D Converter Interrupt Request Enable Setting this bit to 1 enables ΔΣ A/D converter interrupt requests. 0: Disables ΔΣ A/D converter interrupt requests 1: Enables ΔΣ A/D converter interrupt requests	1

- Interrupt Request Register 2 (IRR2) Address: H'FFF7

Table 6.8 Interrupt Request Register 2 (IRR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
5	IRRSAD	0	R/(W)*	ΔΣ A/D Converter Interrupt Request Flag [Setting condition] Completion of ΔΣ A/D conversion [Clearing condition] Writing of 0	0

Note: * Only 0 can be written to clear the flag.

- System Control Register 1 (SYSCR1) Address: H'FFF0

Table 6.9 System Control Register 1 (SYSCR1)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	SSBY	0	R/W	Software Standby This bit selects the target mode for the transition made when the SLEEP instruction is executed. 0: The transition is to the sleep mode or the sub-sleep mode. 1: The transition is to the standby mode or the watch mode.	0
3	LSON	0	R/W	Low-Speed On Flag This bit selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the clock to drive CPU operations after the system is taken out of the watch mode. 0: The system clock (ϕ) drives CPU operations. 1: The subclock (ϕ_{SUB}) drives CPU operations.	0

- System Control Register 2 (SYSCR2) Address: H'FFF1

Table 6.10 System Control Register 2 (SYSCR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	DTON	0	R/W	Direct Transfer On Flag Along with the MSON bit described below and the SSBY, TMA3, and LSON bits in SYSCR1, this bit selects the target mode for transitions after execution of the SLEEP instruction.	0
2	MSON	0	R/W	Middle Speed On Flag This bit selects the active (high-speed) mode or the active (middle-speed) mode for operation of the system after it is taken out of the standby, watch, or sleep mode.	0

- Clock Stop Register 1 (CKSTPR1) Address: H'FFFA

Table 6.11 Clock Stop Register 1 (CKSTPR1)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	S4CKSTP	1	R/W*[1]	SCI4 Module Standby Setting this bit to 0 places SCI4 on standby. 0: Places SCI4 in the module standby mode. 1: Takes SCI4 out of the module standby mode.	1
6	S31CKSTP	1	R/W	SCI3_1 Module Standby*[2] Setting this bit to 0 places SCI3_1 on standby. 0: Places SCI3_1 in the module standby mode. 1: Takes SCI3_1 out of the module standby mode.	0
5	S32CKSTP	1	R/W	SCI3_2 Module Standby*[2] Setting this bit to 0 places SCI3_2 on standby. 0: Places SCI3_2 in the module standby mode. 1: Takes SCI3_2 out of the module standby mode.	0
4	ADCKSTP	1	R/W	A/D Converter Module Standby Setting this bit to 0 places the A/D converter on standby. 0: Places the A/D converter in the module standby mode. 1: Takes the A/D converter out of the module standby mode.	0
3	DADCKSTP	1	R/W	ΔΣ A/D Converter Module Standby Setting this bit to 0 places the ΔΣ A/D converter on standby. 0: Places the ΔΣ A/D converter in the module standby mode. 1: Takes the ΔΣ A/D converter out of the module standby mode.	1
2	TFCKSTP	1	R/W	Timer F Module Standby Setting this bit to 0 places timer F on standby. 0: Places timer F in the module standby mode. 1: Takes timer F out of the module standby mode.	0
1	FROMCKSTP	1	R/W	Flash Memory Module Standby Setting this bit to 0 places the flash memory on standby. 0: Places the flash memory in the module standby mode. 1: Takes the flash memory out of the module standby mode.	1

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
0	RTCCKTP	1	R/W	RTC Module Standby Setting this bit to 0 places the RTC on standby. 0: Places the RTC in the module standby mode. 1: Takes the RTC out of the module standby mode.	0

Notes: 1. In the masked ROM version, this is a reserved bit; writing here is prohibited and values read are undefined.
2. When SCI3 is placed in the module standby mode, all of its registers are reset.

- Clock Stop Register 2 (CKSTPR2) Address: H'FFFB

Table 6.12 Clock Stop Register (CKSTPR2)

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
7	ADBCKSTP	1	R/W	Address Break Module Standby Setting this bit to 0 places the address break module on standby. 0: Places the address break module in the module standby mode. 1: Takes the address break module out of the module standby mode.	1
6	TPUCKSTP	1	R/W	TPU Module Standby Setting this bit to 0 places the TPU on standby. 0: Places the TPU in the module standby mode. 1: Takes the TPU out of the module standby mode.	0
5	IICCKSTP	1	R/W	IIC2 Module Standby Setting this bit to 0 places IIC2 on standby. 0: Places IIC2 in the module standby mode. 1: Takes IIC2 out of the module standby mode.	0
4	PW2CKSTP	1	R/W	PWM2 Module Standby Setting this bit to 0 places PWM2 on standby. 0: Places PWM2 in the module standby mode. 1: Takes PWM2 out of the module standby mode.	0

Bit	Bit Name	Initial Value	R/W	Function	Setting Value
3	AECCKSTP	1	R/W	Asynchronous Event Counter Module Standby Setting this bit to 0 places the asynchronous event counter on standby. 0: Places the asynchronous event counter in the module standby mode. 1: Takes the asynchronous event counter out of the module standby mode.	0
2	WDCKSTP	1	R/W*	Watchdog Timer Module Standby Setting this bit to 0 places the watchdog timer on standby. 0: Places the watchdog timer in the module standby mode. 1: Takes the watchdog timer out of the module standby mode.	0
1	PW1CKSTP	1	R/W	PWM1 Module Standby Setting this bit to 0 places PWM1 on standby. 0: Places PWM1 in the module standby mode. 1: Takes PWM1 out of the module standby mode.	0
0	LDCKSTP	1	R/W	LCD Controller/Driver Module Standby Setting this bit to 0 places the LCD controller/driver on standby. 0: Places the LCD controller/driver in the module standby mode. 1: Takes the LCD controller/driver out of the module standby mode.	0

Note: * WDCKSTP is only valid if WDON of TCSRWD1 is cleared (0). Although WDCKSTP will be cleared if this is attempted while WDON is set to 1 (the watchdog timer is operating), the watchdog timer will not enter the module standby mode but instead continues watchdog operation. In this case, WDCKSTP becomes effective as soon as the software terminates watchdog operation by clearing WDON, at which time the watchdog timer is placed in the module standby mode.

(2) Description of Modules

Table 6.13 describes the modules of this sample task.

Table 6.13 List of Modules

Module Name	Function
`main( )`	Main Routine Performs initial setting of the ΔΣ A/D converter, waits for completion of the first round of ΔΣ A/D conversion, enables ΔΣ A/D conversion-complete interrupt requests, and issues the function call to place the system in the sleep (high-speed) mode.
`int_dsadc( )`	ΔΣ A/D Converter Interrupt Processing Routine Clears the ΔΣ A/D converter interrupt request flag, disables ΔΣ A/D converter interrupt requests, and stores the result of A/D conversion in the internal RAM.
`correct ( )`	Offset/Full-Scale Error Correction Routine Applies offset/full-scale error correction to the results of ΔΣ A/D conversion.

(3) RAM Usage

Table 6.14 describes RAM usage in this sample task.

Table 6.14 RAM Usage

Label Name	Function	Data Size	Address	Used In
`c_data`	14-bit result of ΔΣ A/D conversion (lower 14 bits) after offset/full-scale correction	float	H'F780	main( ) int_dsadc( ) correct( )

(4) Linkage Address Specifications

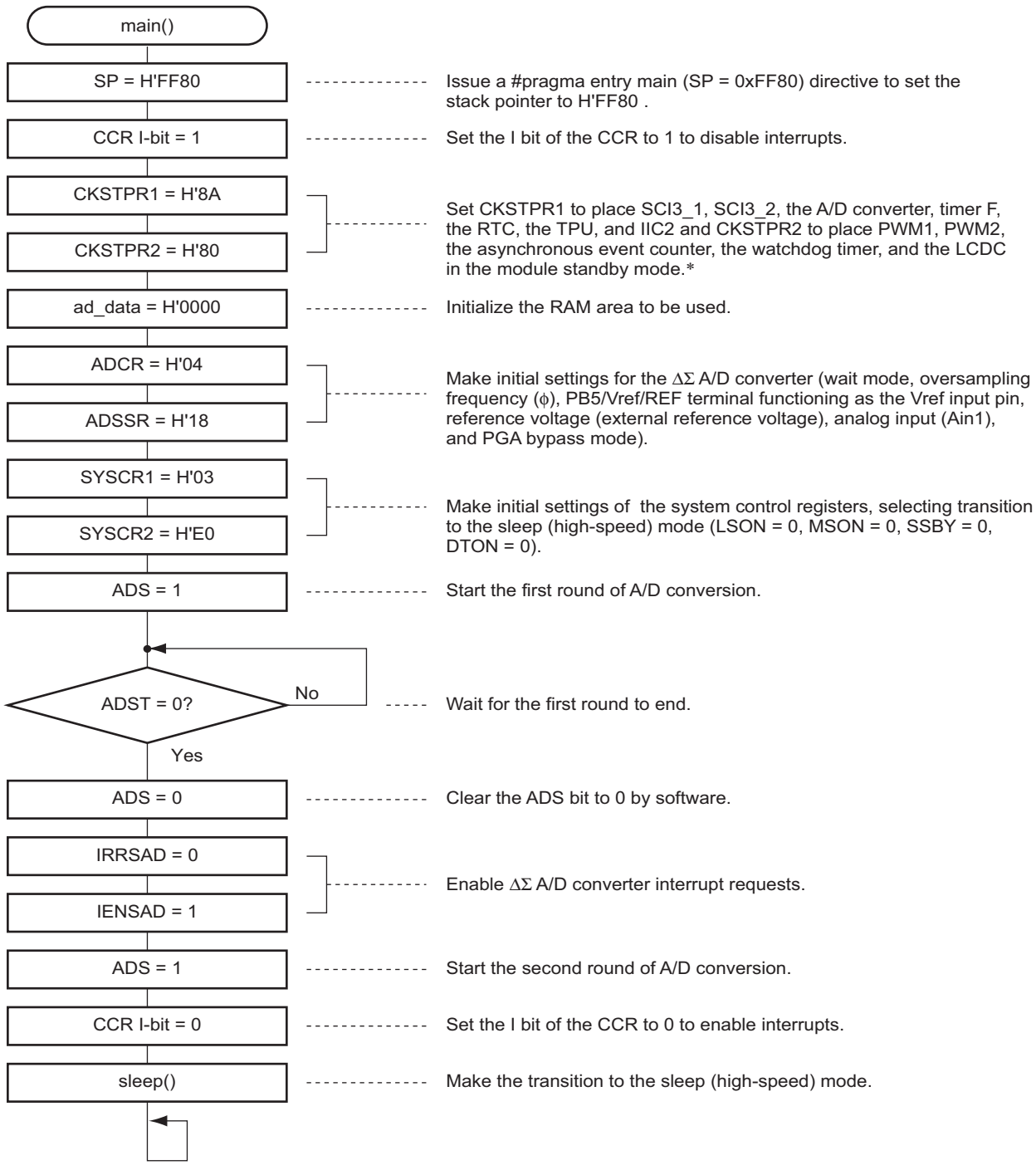
Table 6.15 provides a description of the linkage addresses specified in this sample task.

Table 6.15 Linkage Addresses

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

6.1.7 Flowcharts

(1) Main Routine



Note: * In this sample task, all internal peripheral modules other than SCI4, the flash memory module, address break, and ΔΣ A/D converter are placed in the module standby mode. The user should write 1 to the corresponding bits in the clock stop registers to take other required peripheral modules out of the module standby mode.

Figure 6.6 Main Routine Flowchart

(2) ΔΣ A/D Converter Interrupt Processing Routine

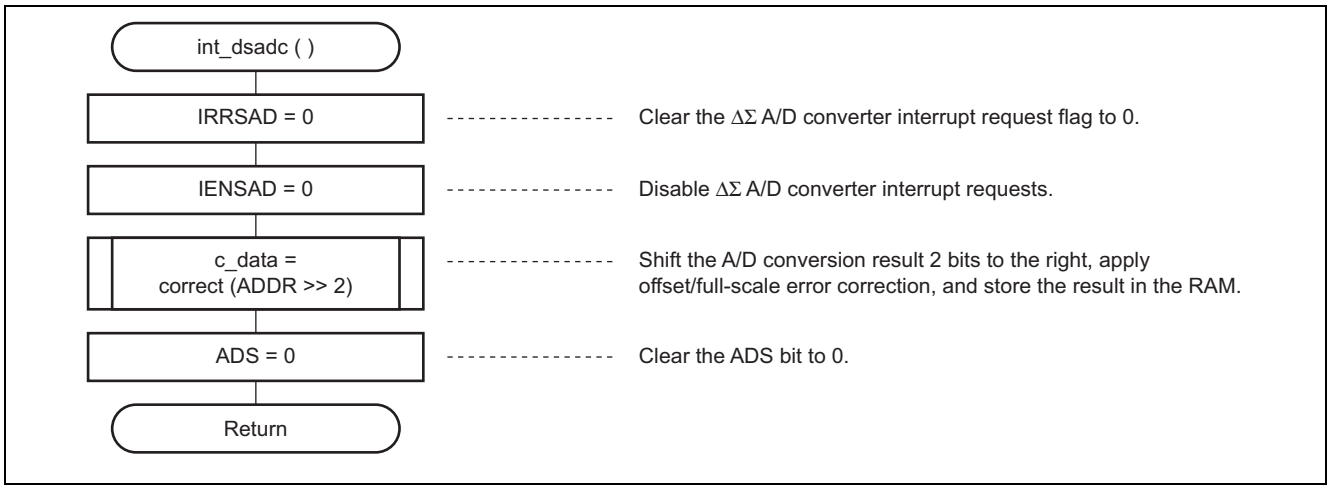


Figure 6.7 ΔΣ A/D Converter Interrupt Processing Routine

(3) Offset/Full-Scale Error Correction Routine

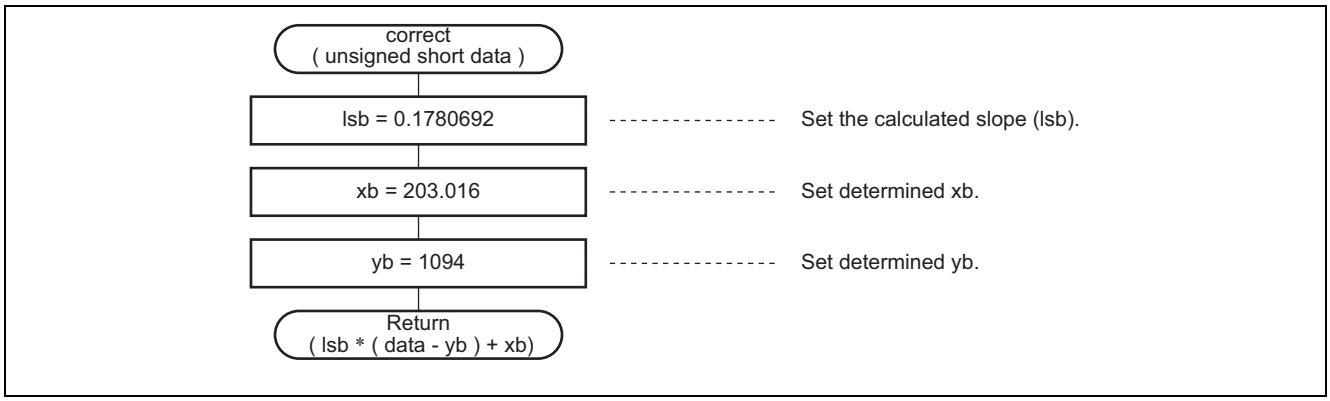


Figure 6.8 Offset/Full-Scale Error Correction Routine

6.1.8 Program Listing

```
#include <machine.h>
struct BIT {
    unsigned char b7:1;        /* Bit-7 */
    unsigned char b6:1;        /* Bit-6 */
    unsigned char b5:1;        /* Bit-5 */
    unsigned char b4:1;        /* Bit-4 */
    unsigned char b3:1;        /* Bit-3 */
    unsigned char b2:1;        /* Bit-2 */
    unsigned char b1:1;        /* Bit-1 */
    unsigned char b0:1;        /* Bit-0 */
};
/************************************************************************************************/
/* Internal I/O register symbol definition                                                      */
/************************************************************************************************/
#define ADCR      *(volatile unsigned char *)0xF060  /* A/D control register                    */
#define ADSSR     *(volatile unsigned char *)0xF061  /* A/D start/status register               */
#define ADSSR_BIT (*(struct BIT *)&ADSSR)
#define ADS       ADSSR_BIT.b7                       /* A/D start                               */
#define ADST      ADSSR_BIT.b6                       /* A/D status flag                         */
#define ADDR      *(volatile unsigned short *)0xF062 /* A/D data register                       */
#define SYSCR1    *(volatile unsigned char *)0xFFF0  /* System control register 1               */
#define SYSCR2    *(volatile unsigned char *)0xFFF1  /* System control register 2               */
#define IENR2     *(volatile unsigned char *)0xFFF4  /* Interrupt enable register 2             */
#define IENR2_BIT (*(struct BIT *)&IENR2)
#define IENSAD    IENR2_BIT.b5                       /* Delta-sigma ADC interrupt               */
                                                     /*                          request enable */
#define IRR2      *(volatile unsigned char *)0xFFF7  /* Interrupt request register 2            */
#define IRR2_BIT  (*(struct BIT *)&IRR2)
#define IRRSAD    IRR2_BIT.b5                        /* Delta-sigma ADC interrupt request flag  */
#define CKSTPR1   *(volatile unsigned char *)0xFFFA  /* Clock stop register 1                   */
#define CKSTPR2   *(volatile unsigned char *)0xFFFB  /* Clock stop register 2                   */
/************************************************************************************************/
/* Interrupt function definition                                                                */
/************************************************************************************************/
#pragma interrupt (int_dsadc)              /* Delta-sigma ADC interrupt                         */
/************************************************************************************************/
/* Function definition                                                                          */
/************************************************************************************************/
void main(void);                           /* Main routine                                      */
void int_dsadc(void);                      /* Delta-sigma ADC interrupt routine                 */
float correct(unsigned short data);        /* Data correct routine                              */
/************************************************************************************************/
/* User RAM area symbol definition                                                              */
/************************************************************************************************/
float c_data;                              /* A/D result data store                             */
/************************************************************************************************/
/* Vector table                                                                                 */
/************************************************************************************************/
#pragma section VECT
void (*const vect_tbl[])(void) = {
    main,                                  /* H'0000 : No.00 : Reset                            */
    main,                                  /* H'0002 : No.01 : System reserve                   */
    main,                                  /* H'0004 : No.02 : System reserve                   */
    main,                                  /* H'0006 : No.03 : NMI                              */
    main,                                  /* H'0008 : No.04 : System reserve                   */
```

```
    main,                           /* H'000A : No.05 : Address break                  */
    main,                           /* H'000C : No.06 : IRQ0                           */
    main,                           /* H'000E : No.07 : IRQ1                           */
    main,                           /* H'0010 : No.08 : IRQAEC                         */
    main,                           /* H'0012 : No.09 : IRQ3                           */
    main,                           /* H'0014 : No.10 : IRQ4                           */
    main,                           /* H'0016 : No.11 : WKP0                           */
    main,                           /* H'0018 : No.12 : WKP1                           */
    main,                           /* H'001A : No.13 : WKP2                           */
    main,                           /* H'001C : No.14 : WKP3                           */
    main,                           /* H'001E : No.15 : WKP4                           */
    main,                           /* H'0020 : No.16 : WKP5                           */
    main,                           /* H'0022 : No.17 : WKP6                           */
    main,                           /* H'0024 : No.18 : WKP7                           */
    main,                           /* H'0026 : No.19 : RTC - 0.25sec overflow         */
    main,                           /* H'0028 : No.20 : RTC - 0.5sec overflow          */
    main,                           /* H'002A : No.21 : RTC - second periodic overflow */
    main,                           /* H'002C : No.22 : RTC - minute periodic overflow */
    main,                           /* H'002E : No.23 : RTC - hour periodic overflow   */
    main,                           /* H'0030 : No.24 : RTC - day periodic overflow    */
    main,                           /* H'0032 : No.25 : RTC - week periodic overflow   */
    main,                           /* H'0034 : No.26 : RTC - free-run overflow        */
    main,                           /* H'0036 : No.27 : WDT                            */
    main,                           /* H'0038 : No.28 : AEC                            */
    main,                           /* H'003A : No.29 : TPU_1 - TG1A                   */
    main,                           /* H'003C : No.30 : TPU_1 - TG1B                   */
    main,                           /* H'003E : No.31 : TPU_1 - TCI1V                  */
    main,                           /* H'0040 : No.32 : TPU_2 - TG2A                   */
    main,                           /* H'0042 : No.33 : TPU_2 - TG2B                   */
    main,                           /* H'0044 : No.34 : TPU_2 - TCI2V                  */
    main,                           /* H'0046 : No.35 : Timer FL                       */
    main,                           /* H'0048 : No.36 : Timer FH                       */
    main,                           /* H'004A : No.37 : SCI4                           */
    main,                           /* H'004C : No.38 : SCI3_1                         */
    main,                           /* H'004E : No.39 : SCI3_2                         */
    main,                           /* H'0050 : No.40 : IIC2                           */
    int_dsadc,                      /* H'0052 : No.41 : Delta-sigma ADC                */
    main,                           /* H'0054 : No.42 : 10-bit ADC                     */
    main                            /* H'0056 : No.43 : Direct transition              */
};
#pragma entry main(sp = 0xFF80)     /* SP = H'FF80                                     */
#pragma section
```

```
/************************************************************************************************/
/* Main routine                                                                                 */
/************************************************************************************************/
void main(void) {
    set_ccr(0x80);                          /* CCR I-bit = 1                                    */
    CKSTPR1 = 0x8A;                         /* Module standby mode set                          */
    CKSTPR2 = 0x80;
    c_data = 0x00000000;                    /* Used RAM area initialize                         */
    ADCR = 0x04;                            /* Delta-sigma ADC initialize                       */
    ADSSR = 0x18;
    SYSCR1 = 0x03;                          /* SSBY = 0, LSON = 0                               */
    SYSCR2 = 0xE0;                          /* DTON = 0, MSON = 0                               */
    ADS = 1;                                /* A/D conversion start (1st)                       */
    while (ADST == 1);                      /* A/D conversion end ?                             */
    ADS = 0;
    IRRSAD = 0;                             /* Delta-sigma ADC interrupt enable                 */
    IENSAD = 1;
    ADS = 1;                                /* A/D conversion start (2nd)                       */
    set_imask_ccr(0);                       /* CCR I-bit = 0                                    */
    sleep();                                /* Active-H mode  -> Sleep-H mode                   */
    while(1);
}
/************************************************************************************************/
/* Delta-sigma ADC interrupt routine                                                            */
/************************************************************************************************/
void int_dsadc(void) {
    IRRSAD = 0;                             /* Interrupt request flag clear to 0                */
    IENSAD = 0;                             /* Delta-sigma ADC interrupt disable                */
    c_data = correct(ADDR >> 2);            /* A/D result data store                            */
    ADS = 0;                                /* A/D start = 0                                    */
}
/************************************************************************************************/
/* Data correction routine                                                                      */
/************************************************************************************************/
float correct(unsigned short data) {
    const float lsb=0.1780692, xb=203.016, yb=1094;   /* lsb, (xB,yB) set                       */
    return (lsb * (data - yb) + xb);
}
```

7. Characteristics Data

1. The characteristics data was gathered from a limited number of samples under a limited range of conditions. Therefore, all data given below is for general reference only, and the characteristics are not guaranteed. The data are provided for reference by the user in defining his/her own conditions of usage.
2. Remember that offset/full-scale error correction is easily applied. For details, see section 4, Errors and Methods of Correction.
3. If you cannot find data that corresponds with your conditions, we recommended that you refer to the data for the most similar conditions.
4. The characteristics data may include conditions that go beyond the guaranteed range of safe operation.

7.1 Measured Parameter Dependences of Error Components

- Measurement conditions

1. Common conditions

   Microcomputer operating mode: high-speed active mode (all modules other than the ΔΣ A/D on standby)
   ΔΣ A/D operating mode: wait mode, analog input pin: Ain1
2. External circuit

   Power is supplied to Vcc, AVcc, DVcc and Vref by a battery box.

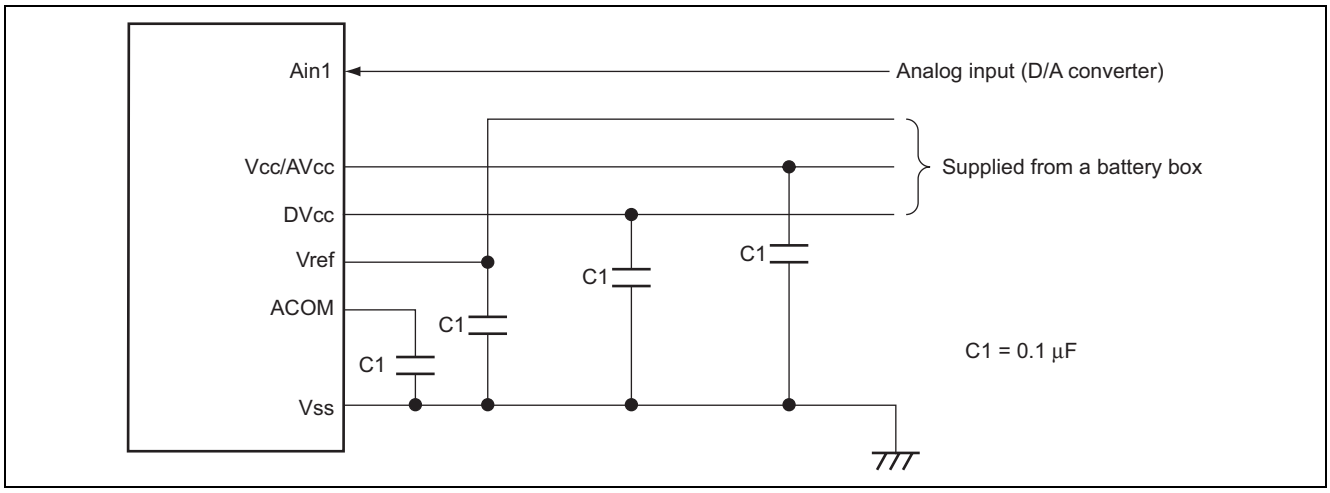


Figure 7.1 Parameter Measurement Circuit

7.1.1 Flash ROM Version

Graphs of the dependences of the integral error, differential error, offset error and full-scale error on the parameters listed in the table below are given after the table.

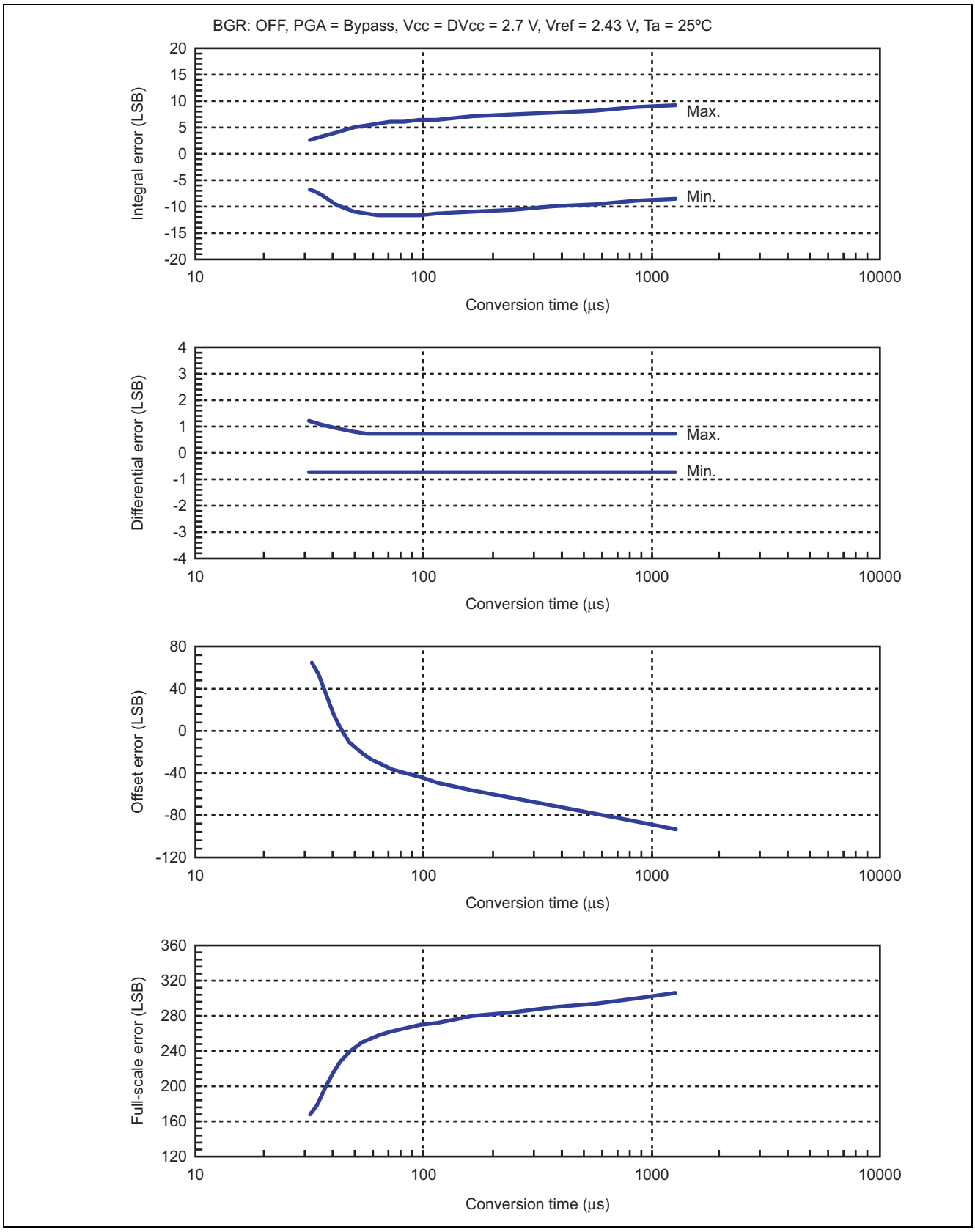
Table 7.1 Conditions in Parameter-Dependence Measurement (Flash ROM Version)

	Measurement Conditions						
Graph Name	**BGR**	**Vcc (V)**	**DVcc (V)**	**Vref (V)**	**Ta (°C)**	**PGA**	**Conversion Time (μs)**
Conversion time dependence 1	OFF	2.7	2.7	2.43	25	Bypassed	—
Conversion time dependence 2	OFF	3.0	3.0	2.70	25	Bypassed	—
Conversion time dependence 3	OFF	3.0	3.0	2.70	25	1/3	—
Conversion time dependence 4	OFF	3.6	3.6	3.24	25	1	—
Conversion time dependence 5	OFF	3.0	3.0	2.70	25	1	—
Conversion time dependence 6	OFF	2.2	2.2	1.98	25	1	—
Conversion time dependence 7	OFF	3.0	3.0	2.70	25	2	—
Conversion time dependence 8	OFF	2.7	2.7	2.43	25	2	—
Conversion time dependence 9	OFF	3.0	3.0	2.70	25	4	—
Conversion time dependence 10	OFF	2.7	2.7	2.43	25	4	—
Conversion time dependence 11	OFF	3.0	3.0	2.70	25	1/3	—
Conversion time dependence 12	ON	3.0	3.0	2.70	25	Bypassed	—
Conversion time dependence 13	ON	3.6	3.6	3.24	55	Bypassed	—
Conversion time dependence 14	ON	3.0	3.0	2.70	25	1	—
Conversion time dependence 15	ON	3.6	3.6	3.24	55	1	—
Conversion time dependence 16	ON	3.0	3.0	2.70	25	1/3	—
Temperature dependence 1	OFF	2.2	2.2	1.89	—	Bypassed	64
Temperature dependence 2	OFF	3.0	3.0	2.70	—	Bypassed	160
Temperature dependence 3	OFF	2.7	2.7	2.43	—	Bypassed	64
Temperature dependence 4	OFF	2.2	2.2	1.98	—	1	64
Temperature dependence 5	OFF	3.0	3.0	2.70	—	1	32
Temperature dependence 6	OFF	3.0	3.0	2.70	—	2	64
Temperature dependence 7	OFF	2.7	2.7	2.43	—	2	64
Temperature dependence 8	OFF	2.2	2.2	1.98	—	2	64
Temperature dependence 9	OFF	2.7	2.7	2.43	—	4	64
Temperature dependence 10	OFF	3.0	3.0	2.70	—	4	32
Temperature dependence 11	OFF	2.2	2.2	1.98	—	4	64
Temperature dependence 12	OFF	3.0	3.0	2.70	—	1/3	64
Temperature dependence 13	OFF	2.2	2.2	1.98	—	1/3	64
Temperature dependence 14	ON	2.2	2.2	1.98	—	Bypassed	64
Temperature dependence 15	ON	2.2	2.2	1.98	—	Bypassed	1280
Temperature dependence 16	ON	3.0	3.0	2.70	—	Bypassed	32
Temperature dependence 17	ON	3.0	3.0	2.70	—	1	32
Temperature dependence 18	ON	2.2	2.2	1.98	—	1/3	64
Temperature dependence 19	ON	2.2	2.2	1.98	—	1/3	1280
Temperature dependence 20	ON	3.0	3.0	2.70	—	1/3	32

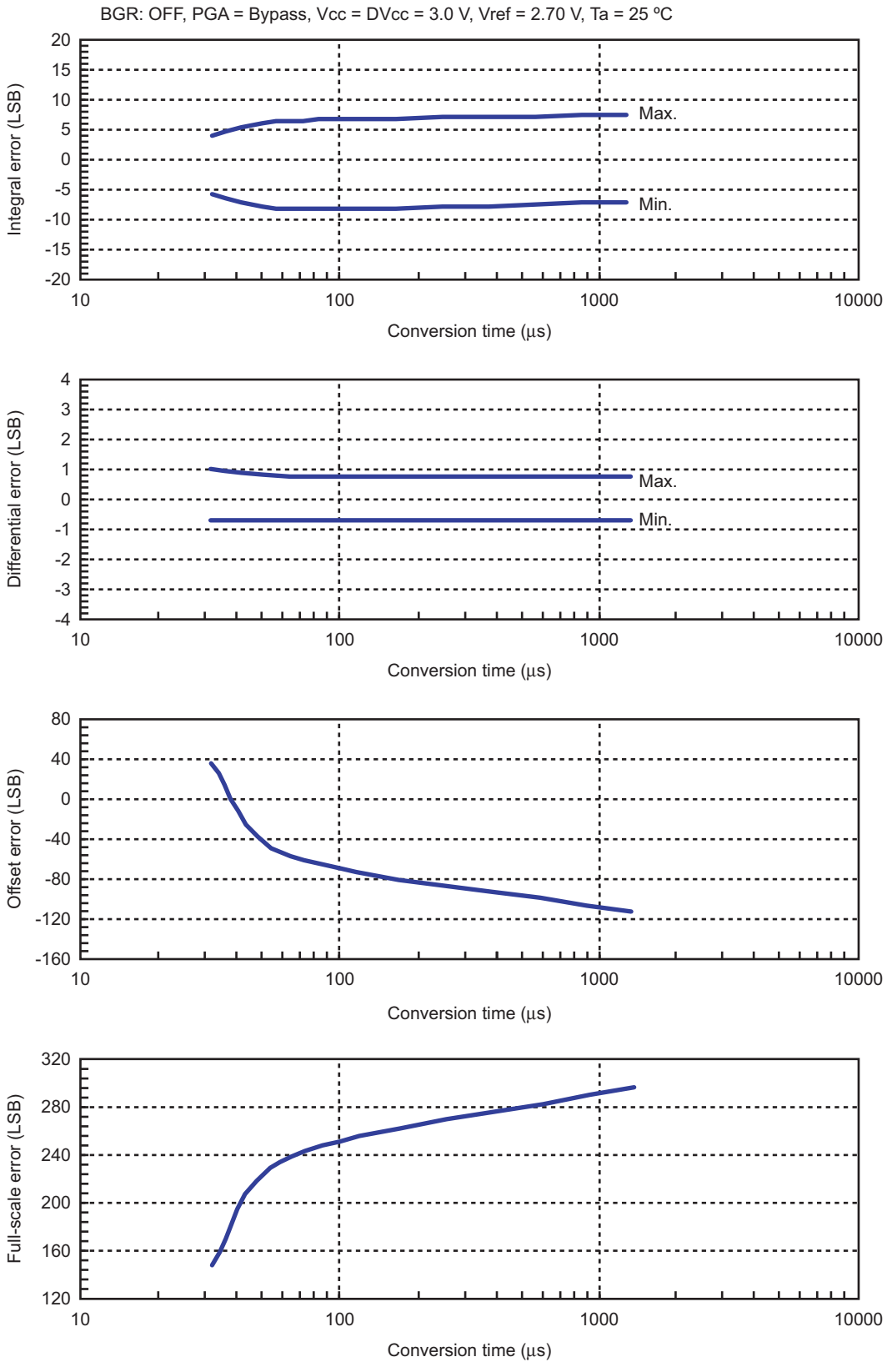
	Measurement Conditions						
Graph Name	BGR	Vcc (V)	DVcc (V)	Vref (V)	Ta (°C)	PGA	Conversion Time (μs)
DVcc dependence 1	OFF	—	—	—	25	Bypassed	32
DVcc dependence 2	OFF	—	—	—	25	Bypassed	64
DVcc dependence 3	OFF	—	—	—	25	Bypassed	1280
DVcc dependence 4	OFF	—	—	—	25	1	32
DVcc dependence 5	OFF	—	—	—	25	1	64
DVcc dependence 6	OFF	—	—	—	25	1	1280
DVcc dependence 7	OFF	—	—	—	25	2	32
DVcc dependence 8	OFF	—	—	—	25	2	64
DVcc dependence 9	OFF	—	—	—	25	2	1280
DVcc dependence 10	OFF	—	—	—	25	4	32
DVcc dependence 11	OFF	—	—	—	25	4	64
DVcc dependence 12	OFF	—	—	—	25	4	1280
DVcc dependence 13	OFF	—	—	—	25	1/3	1280
PGA dependence 1	OFF	2.2	2.2	1.98	25	—	64
PGA dependence 2	OFF	2.2	2.2	1.98	25	—	1280
PGA dependence 3	OFF	3.0	3.0	2.70	25	—	32
PGA dependence 4	OFF	3.0	3.0	2.70	25	—	64
PGA dependence 5	OFF	3.0	3.0	2.70	25	—	1280
PGA dependence 6	OFF	3.6	3.6	3.24	25	—	32
PGA dependence 7	OFF	3.6	3.6	3.24	25	—	1280

(1) Dependences on Conversion Time

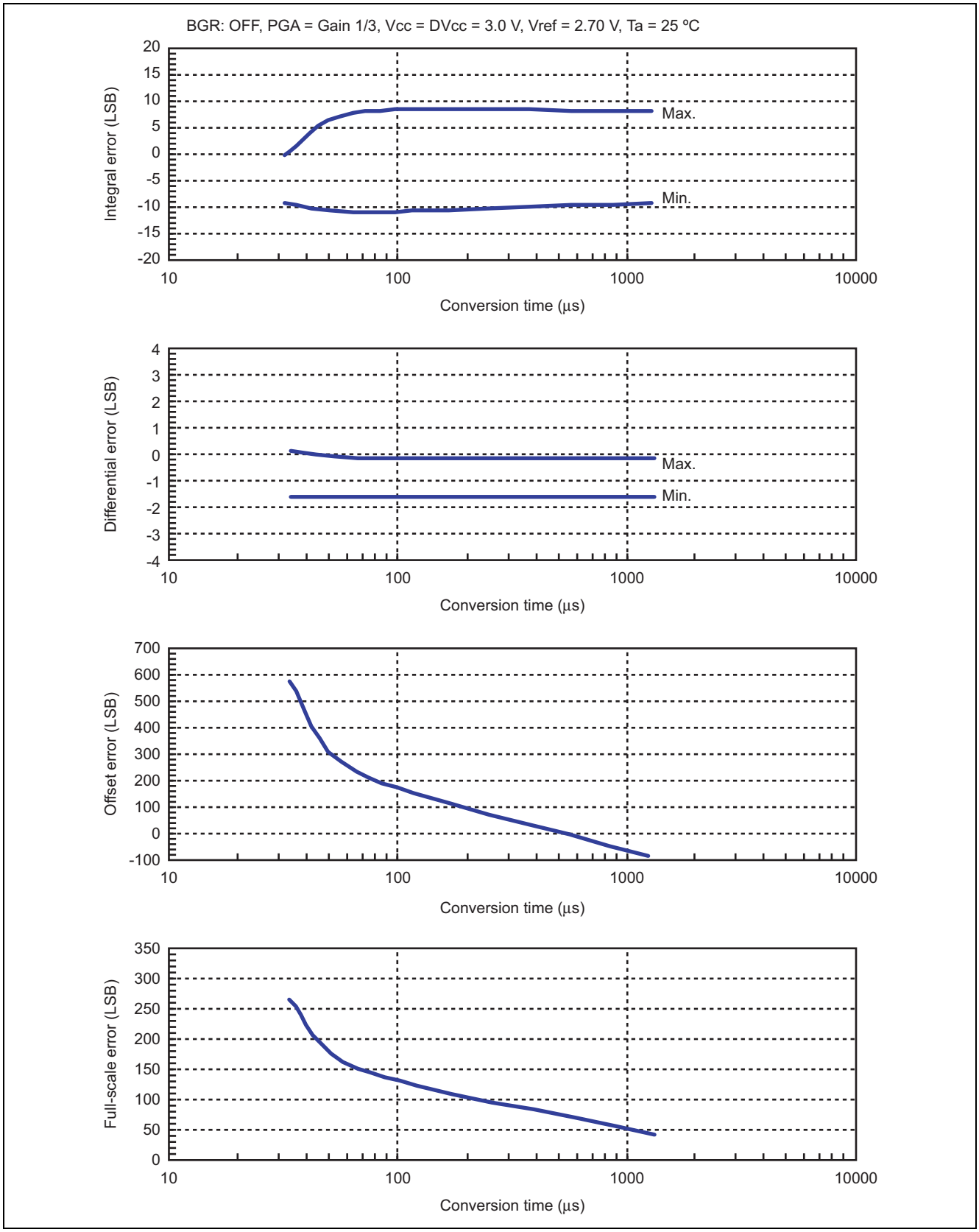
- Conversion time dependence 1



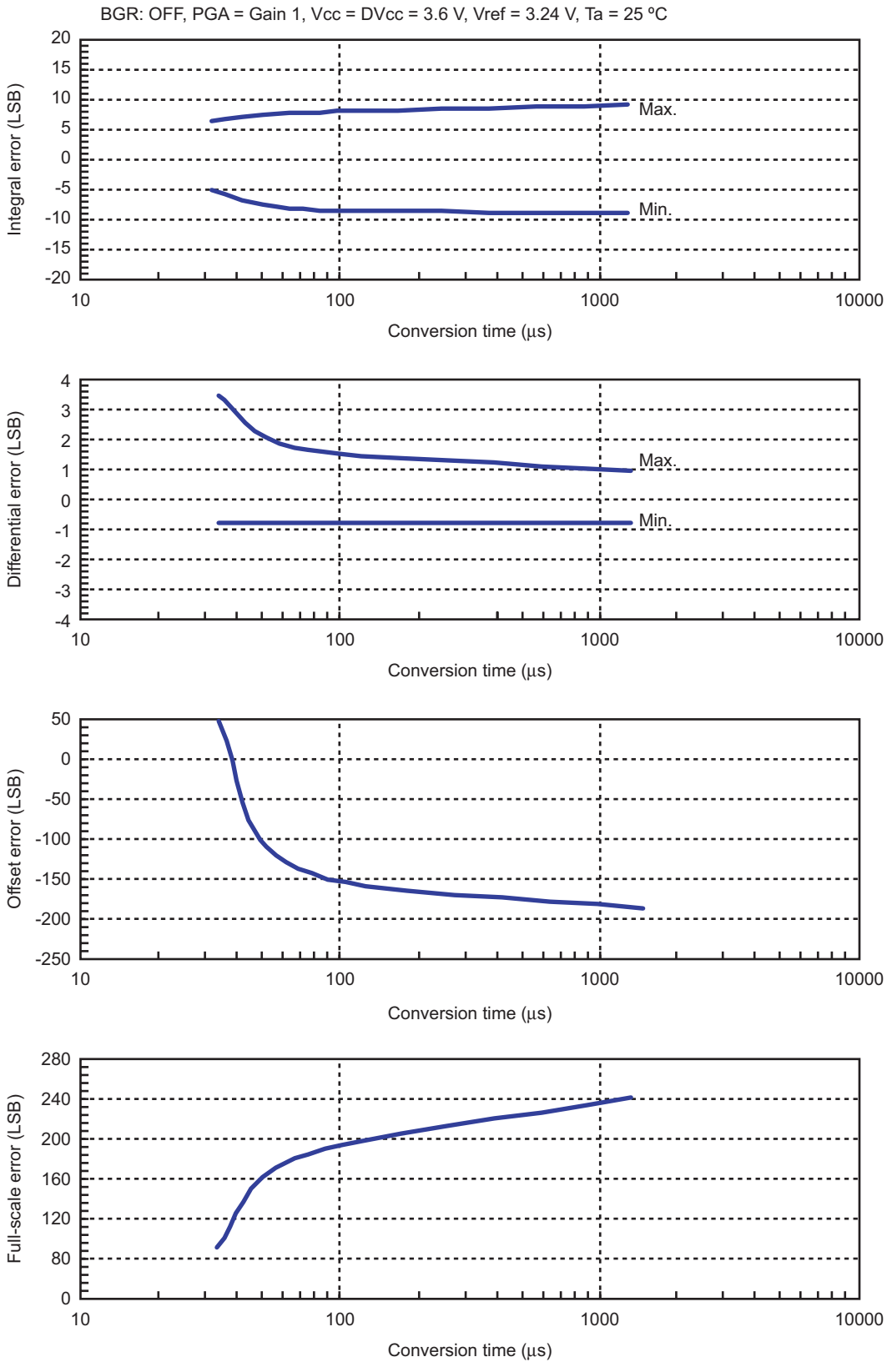
- Conversion time dependence 2



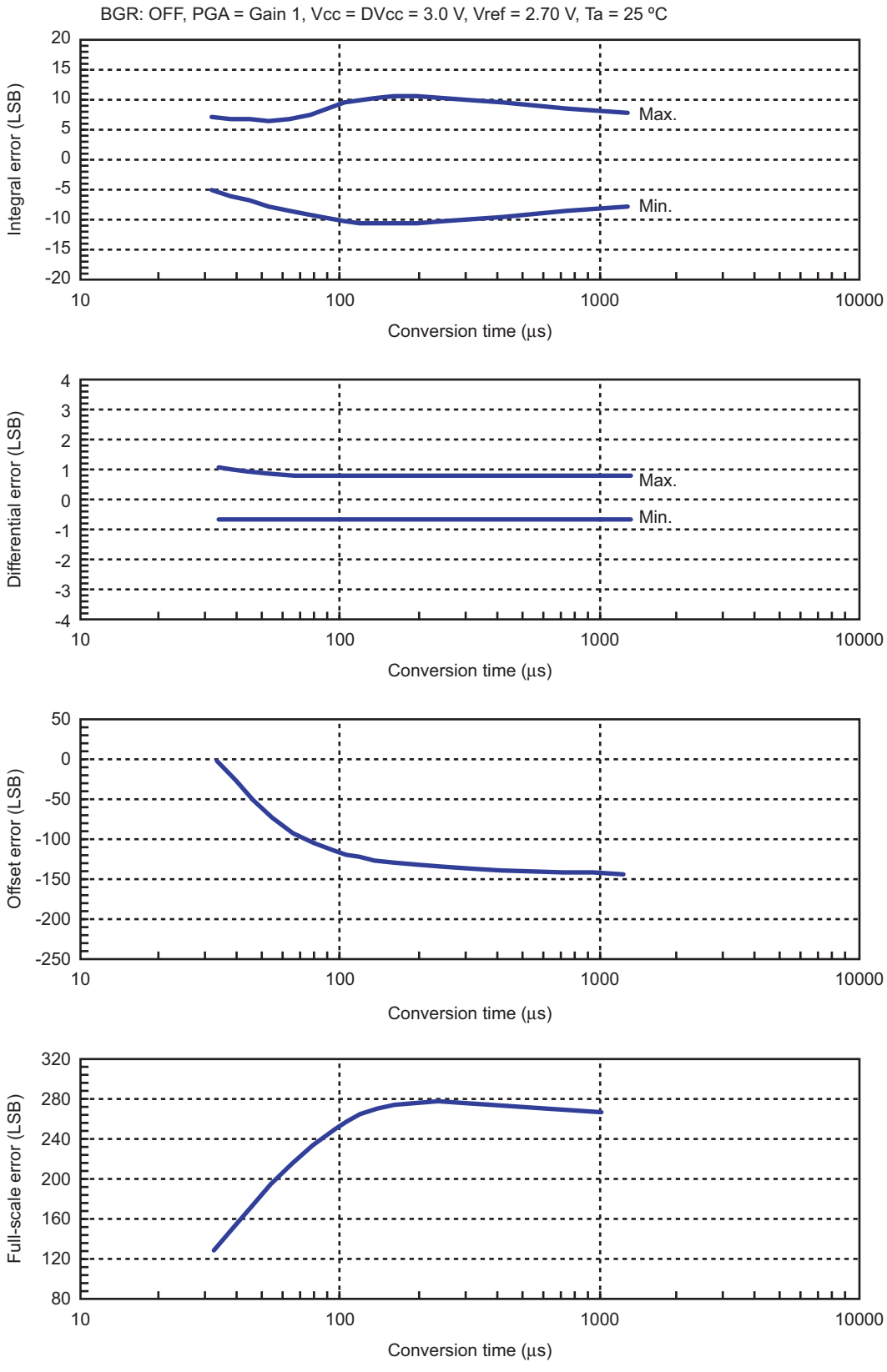
- Conversion time dependence 3



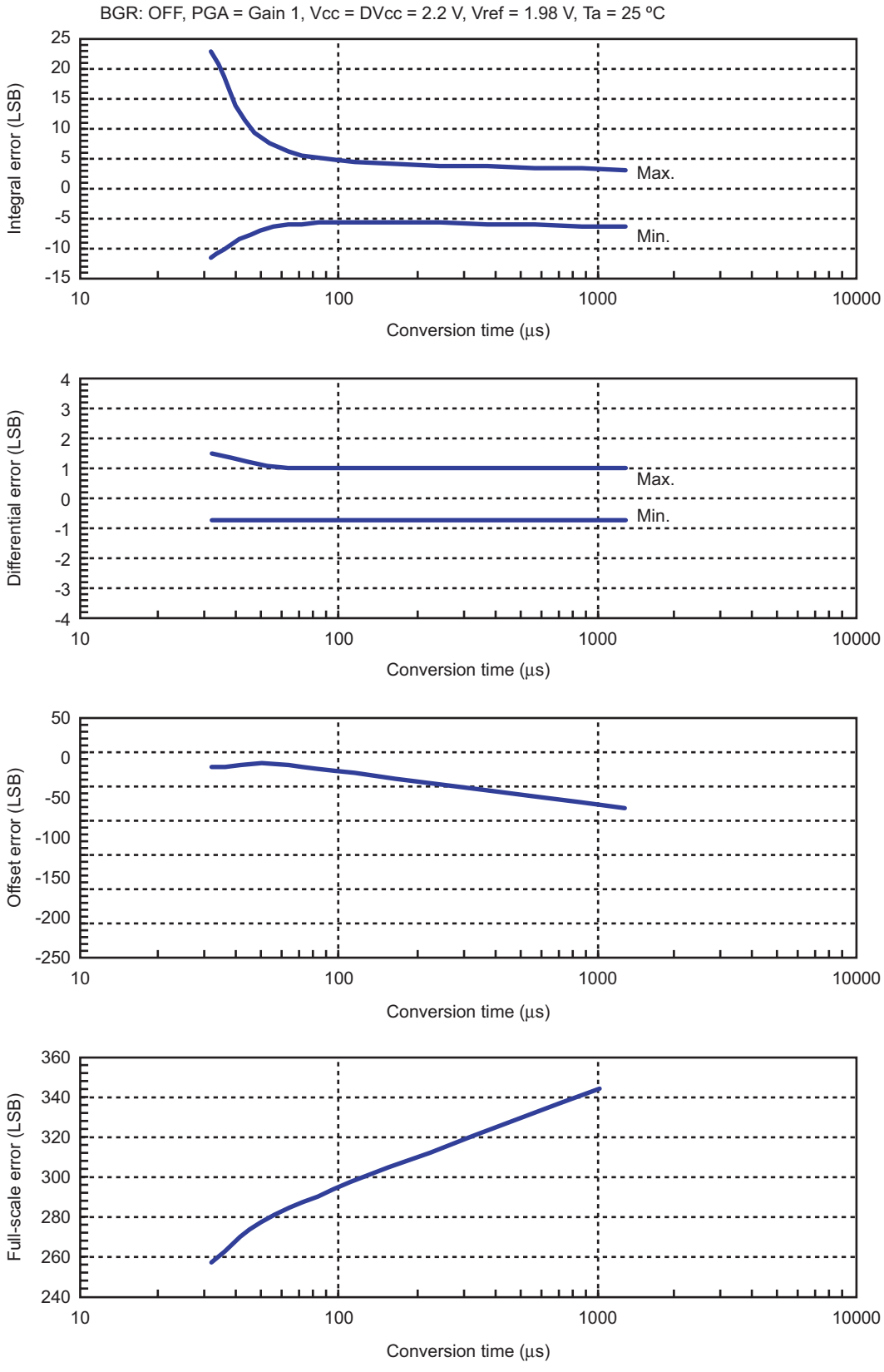
- Conversion time dependence 4



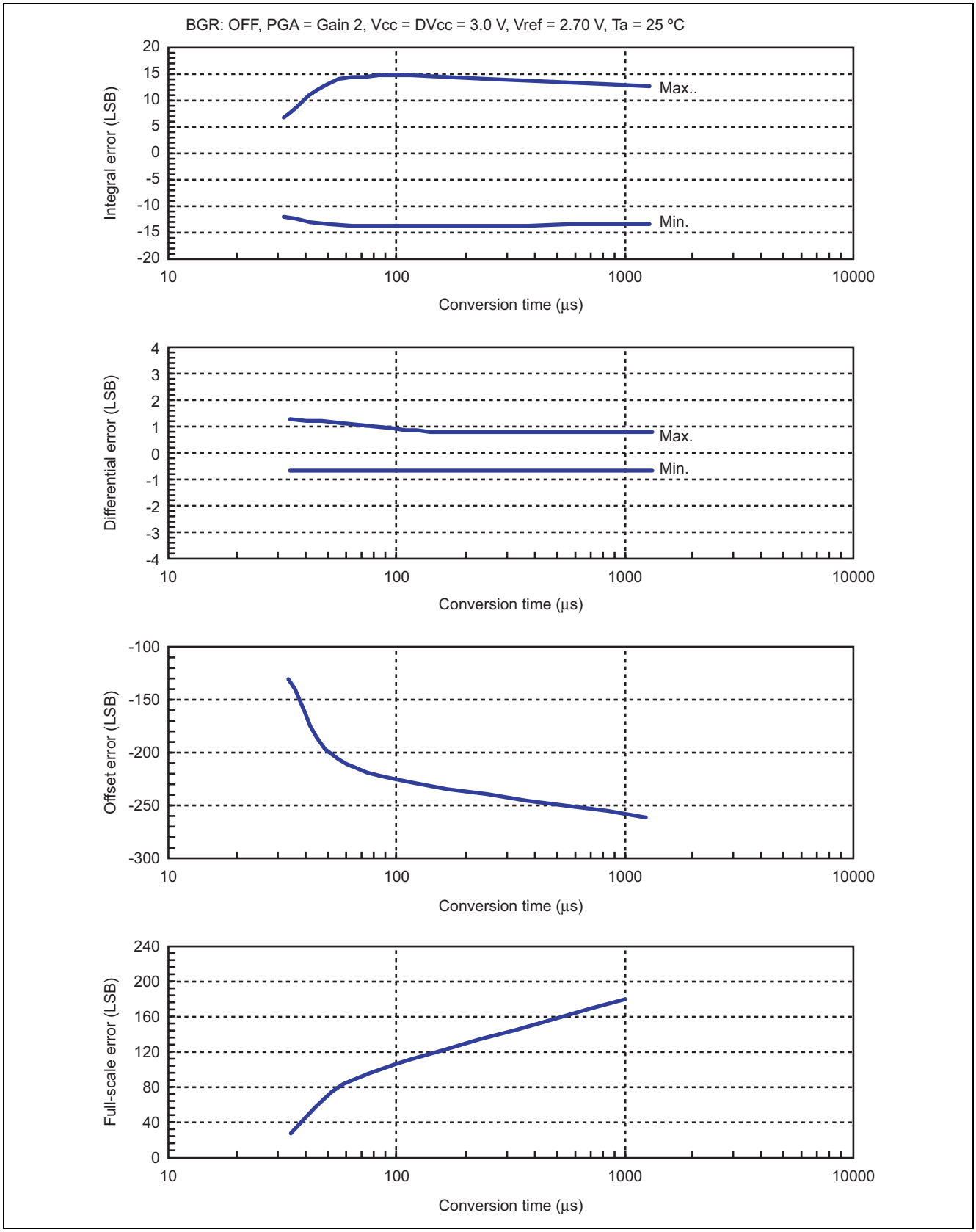
- Conversion time dependence 5



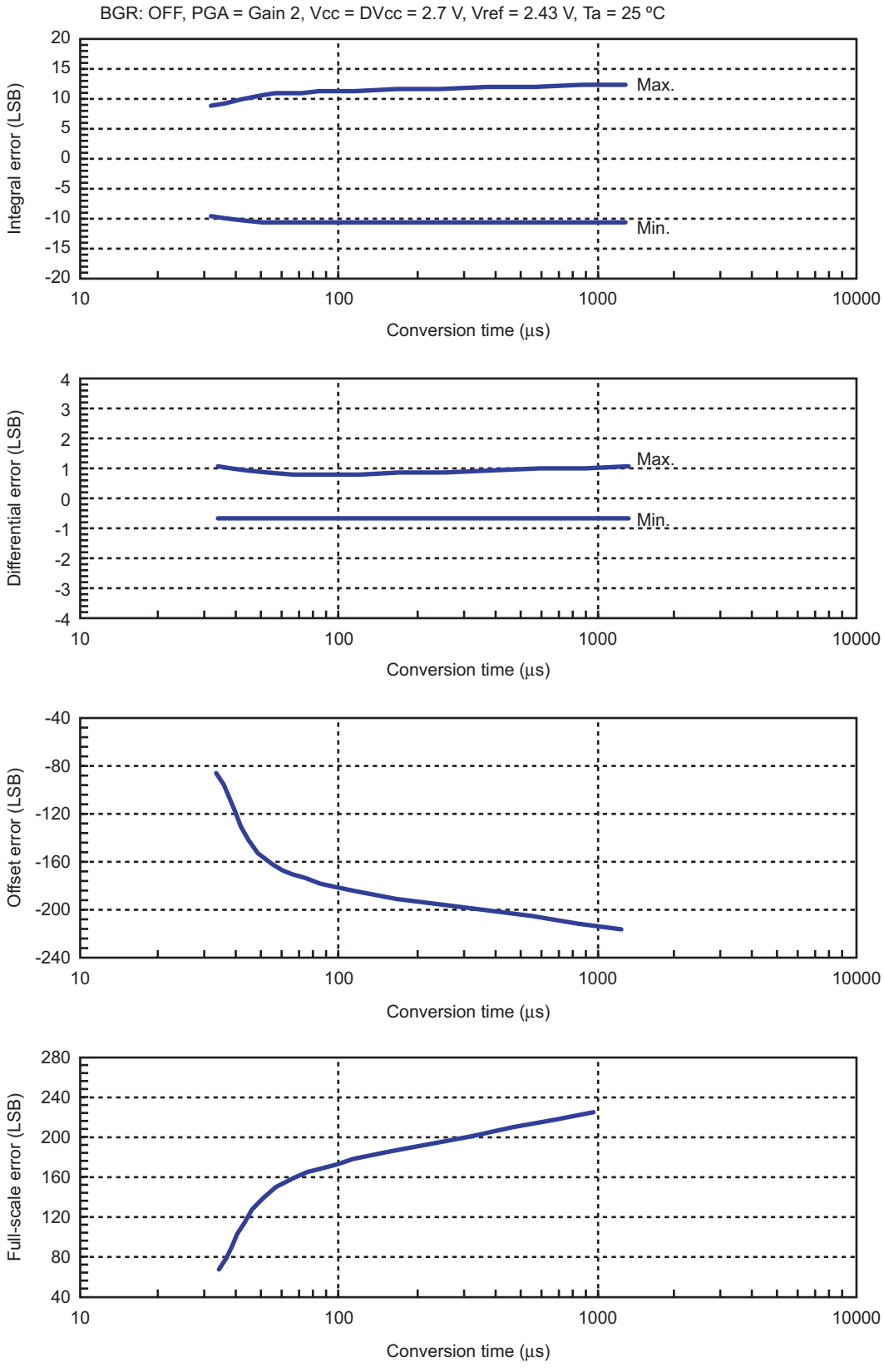
- Conversion time dependence 6



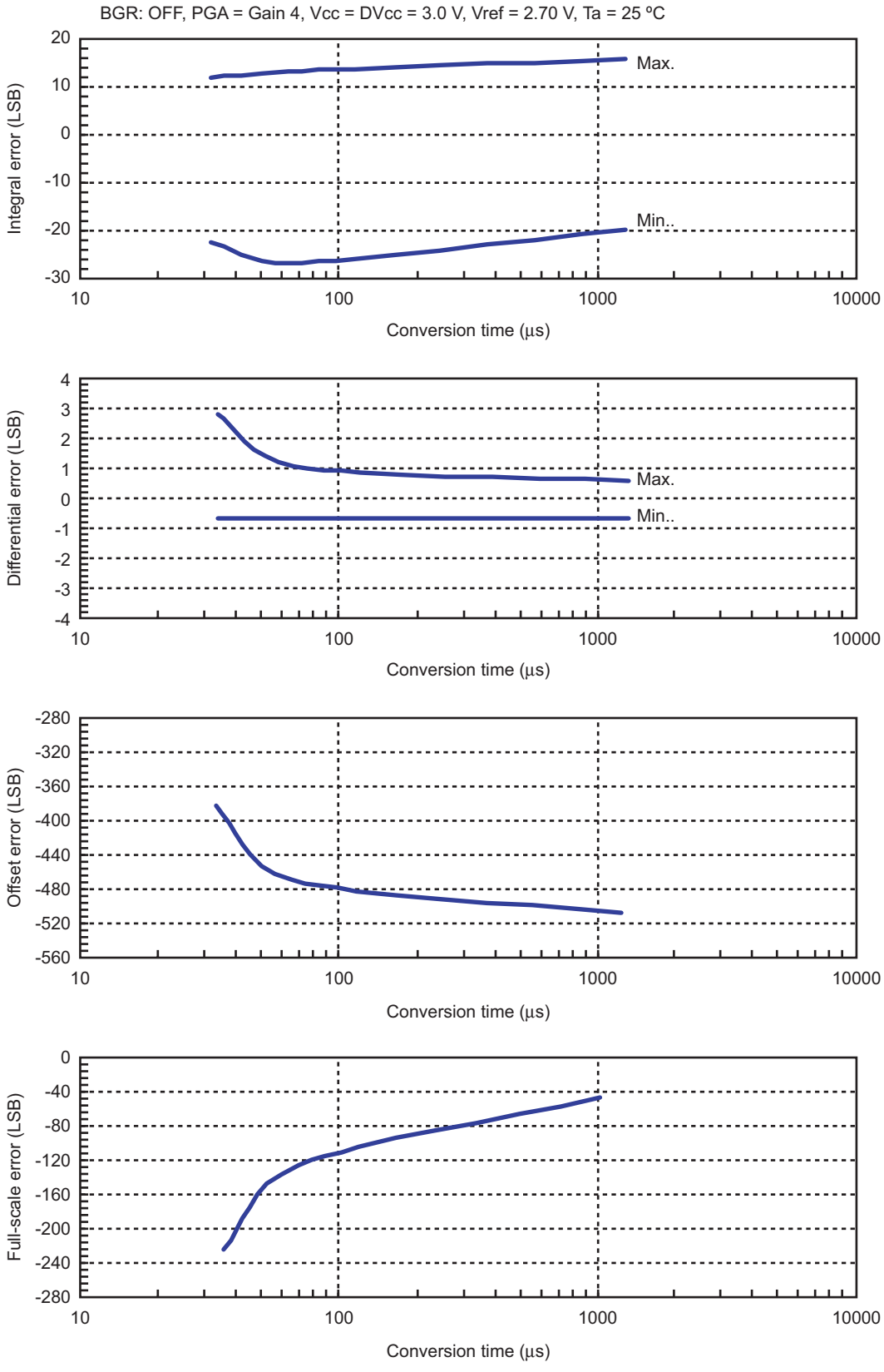
- Conversion time dependence 7



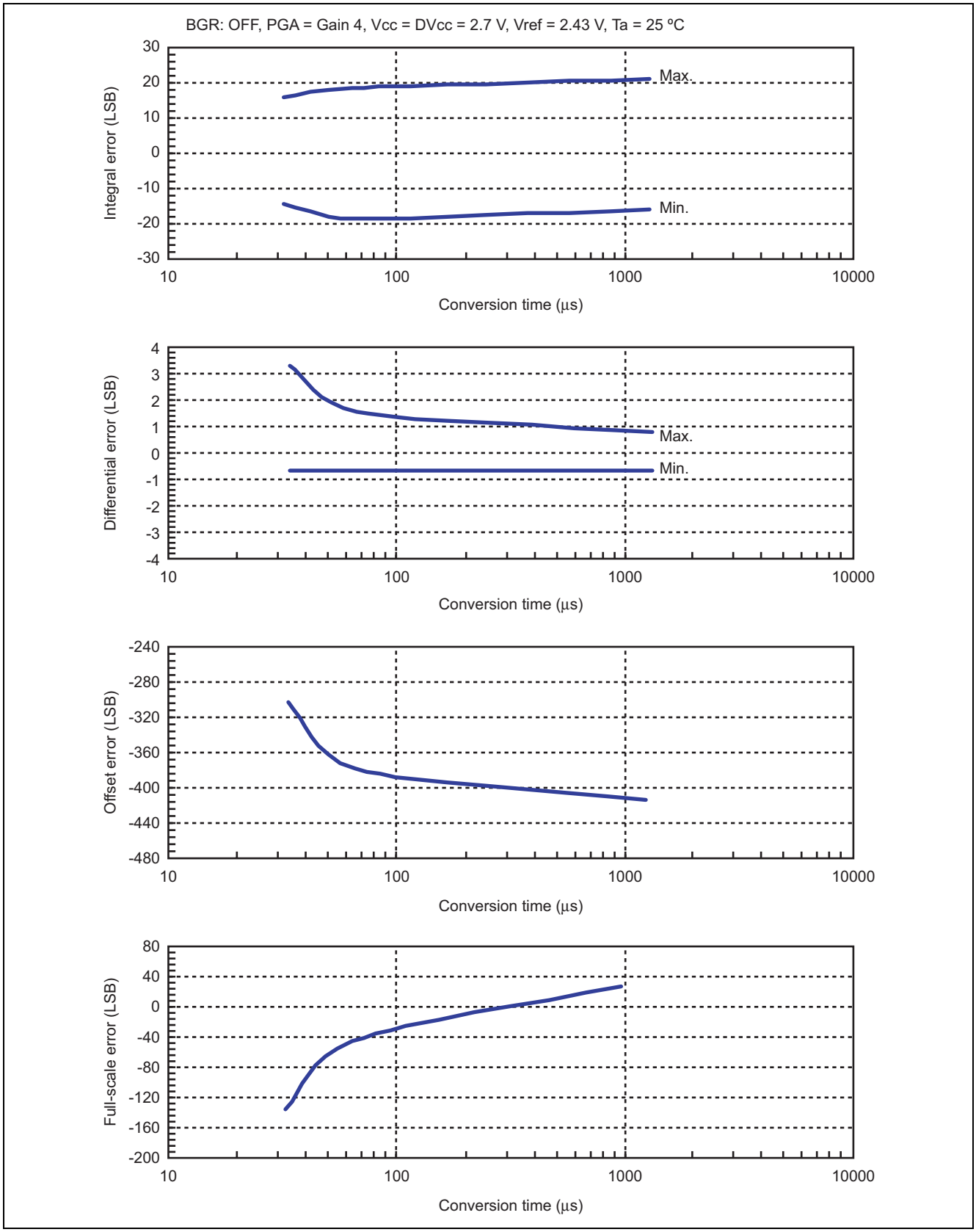
- Conversion time dependence 8



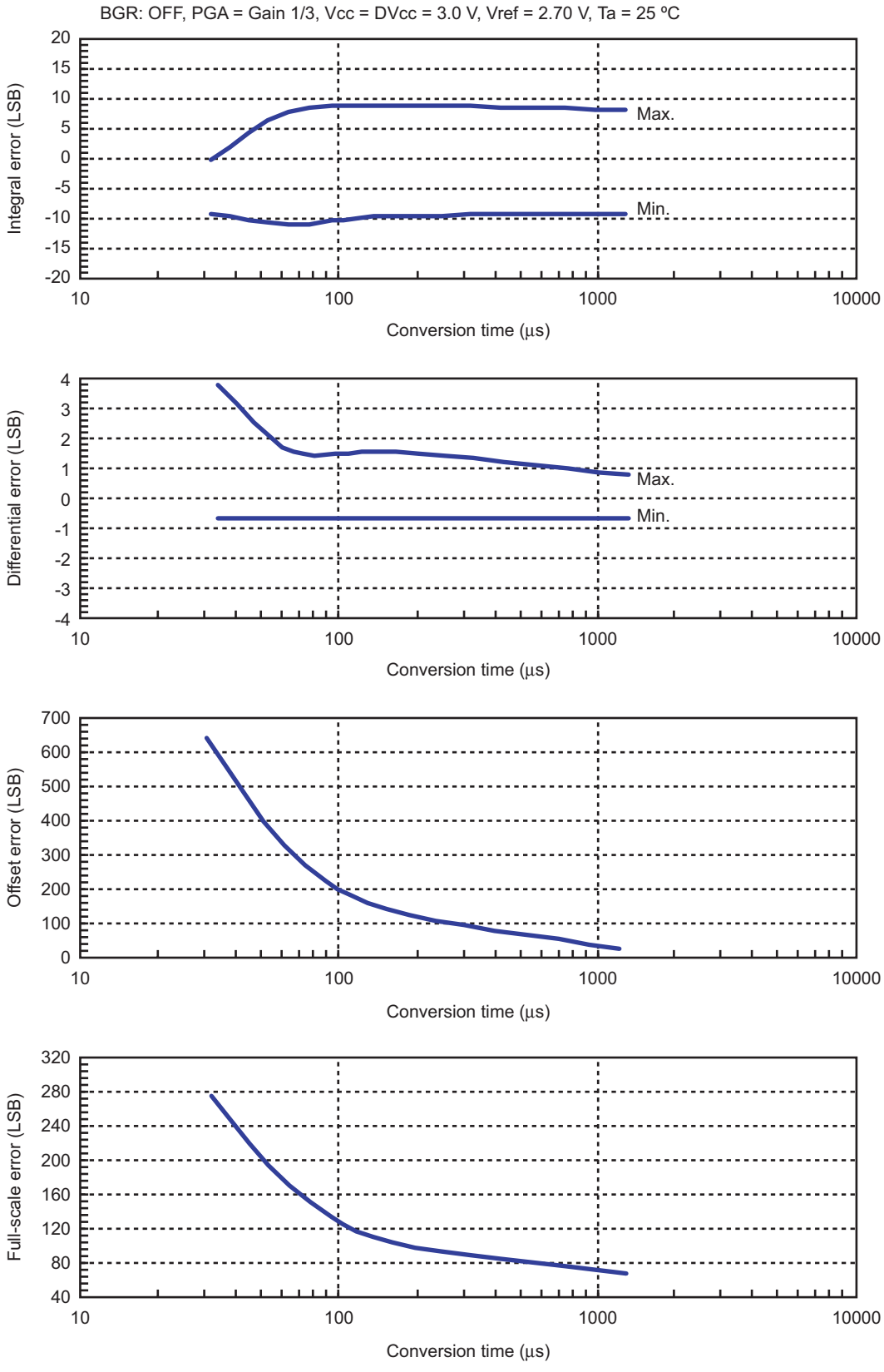
- Conversion time dependence 9



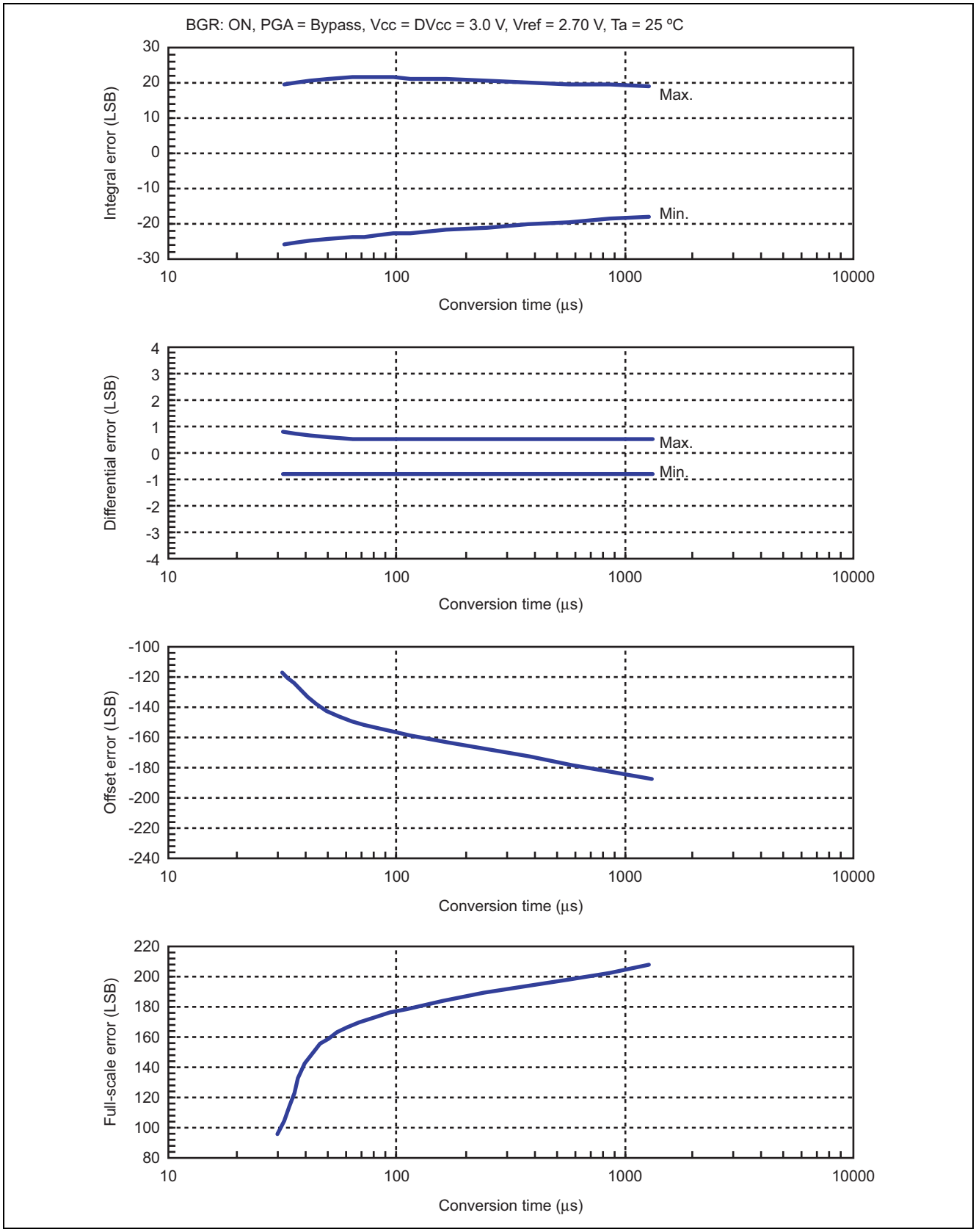
- Conversion time dependence 10



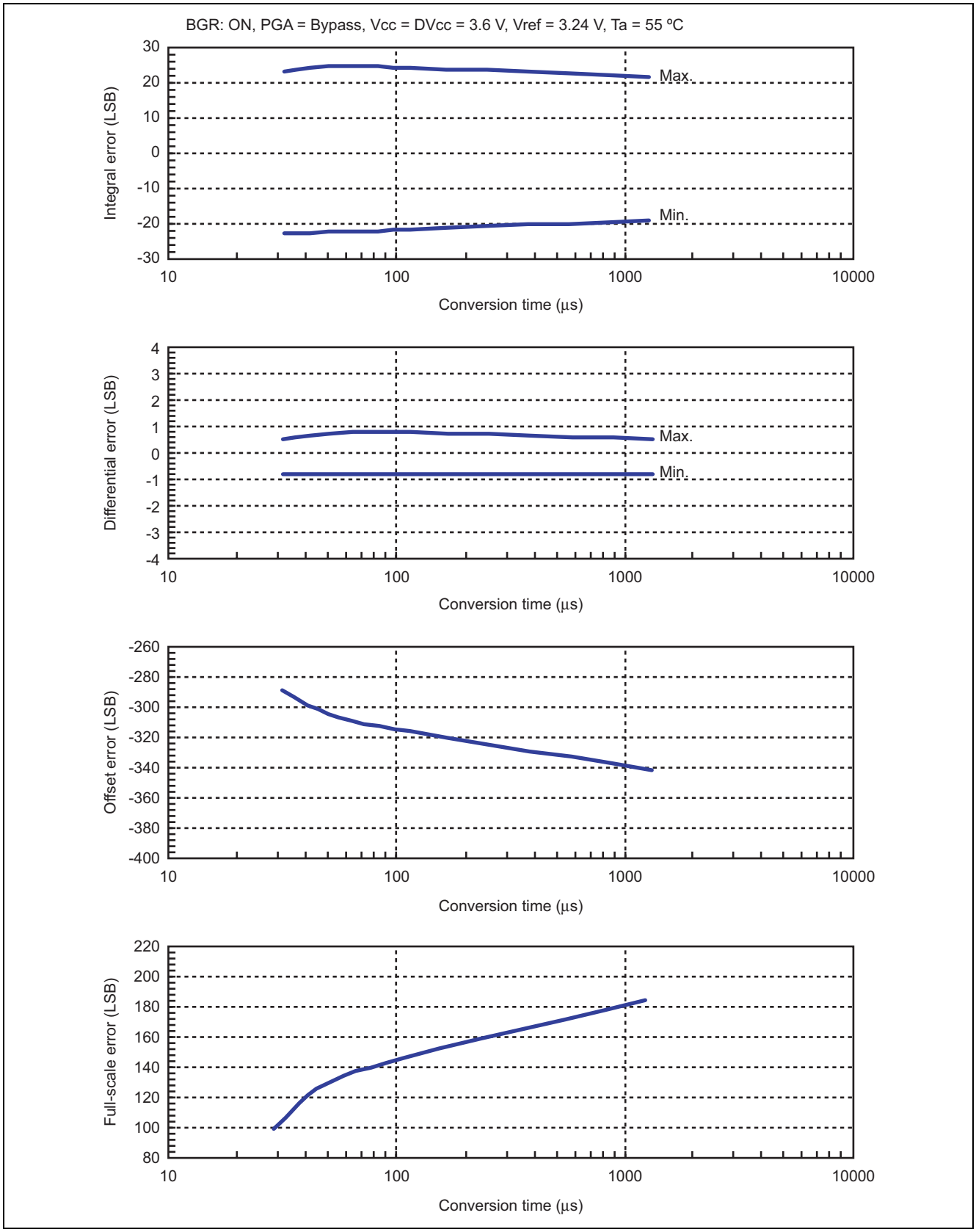
- Conversion time dependence 11



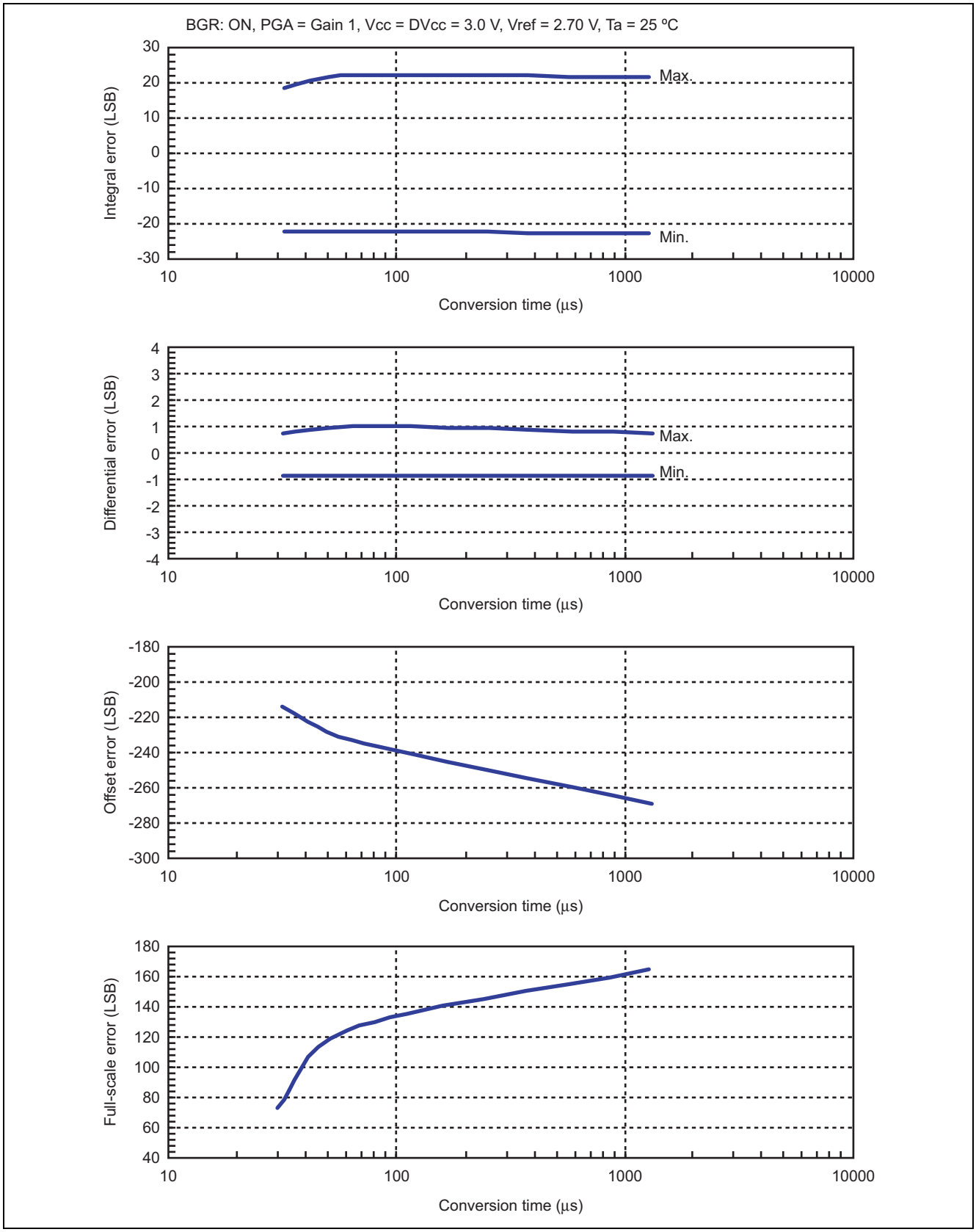
- Conversion time dependence 12



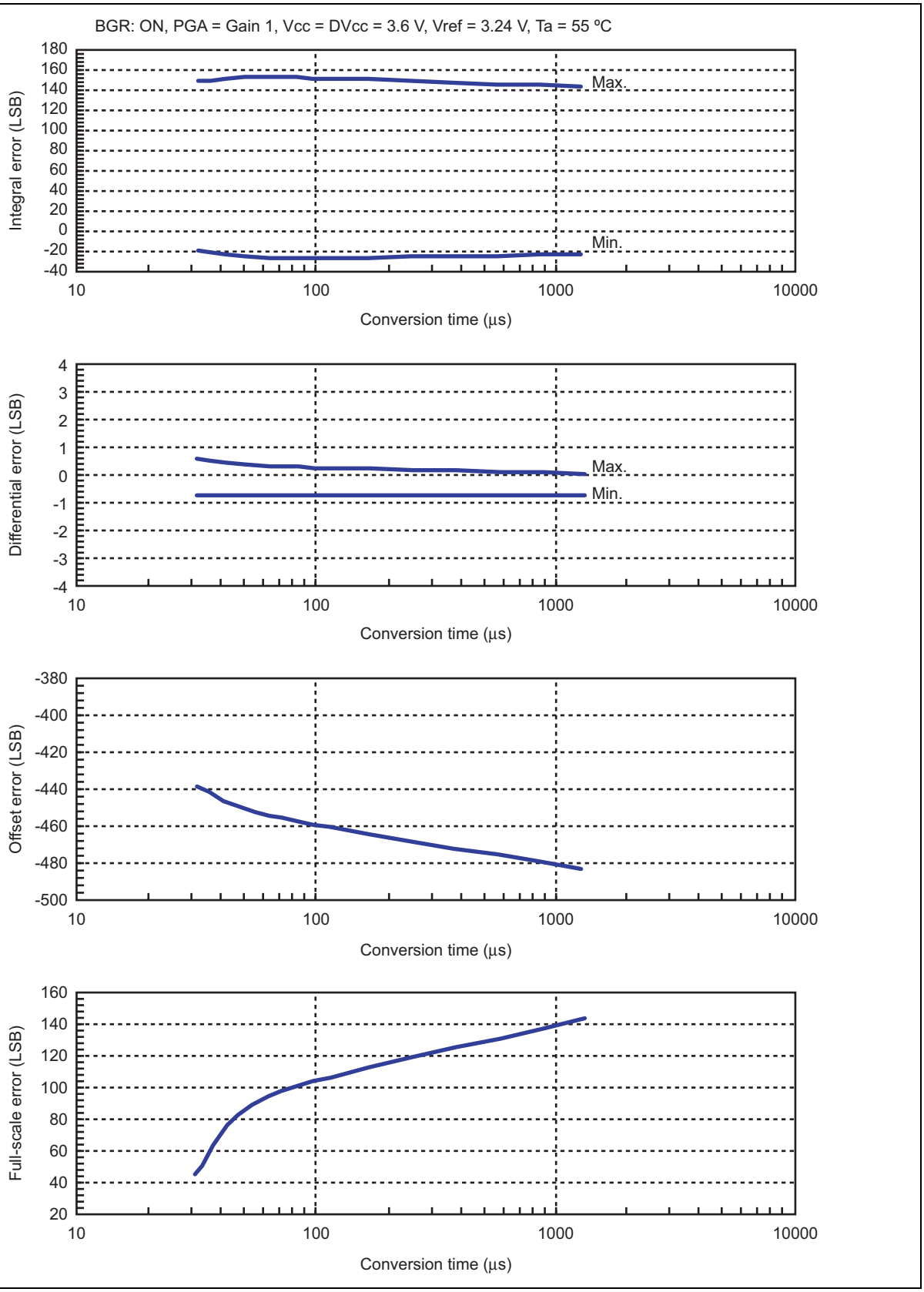
- Conversion time dependence 13



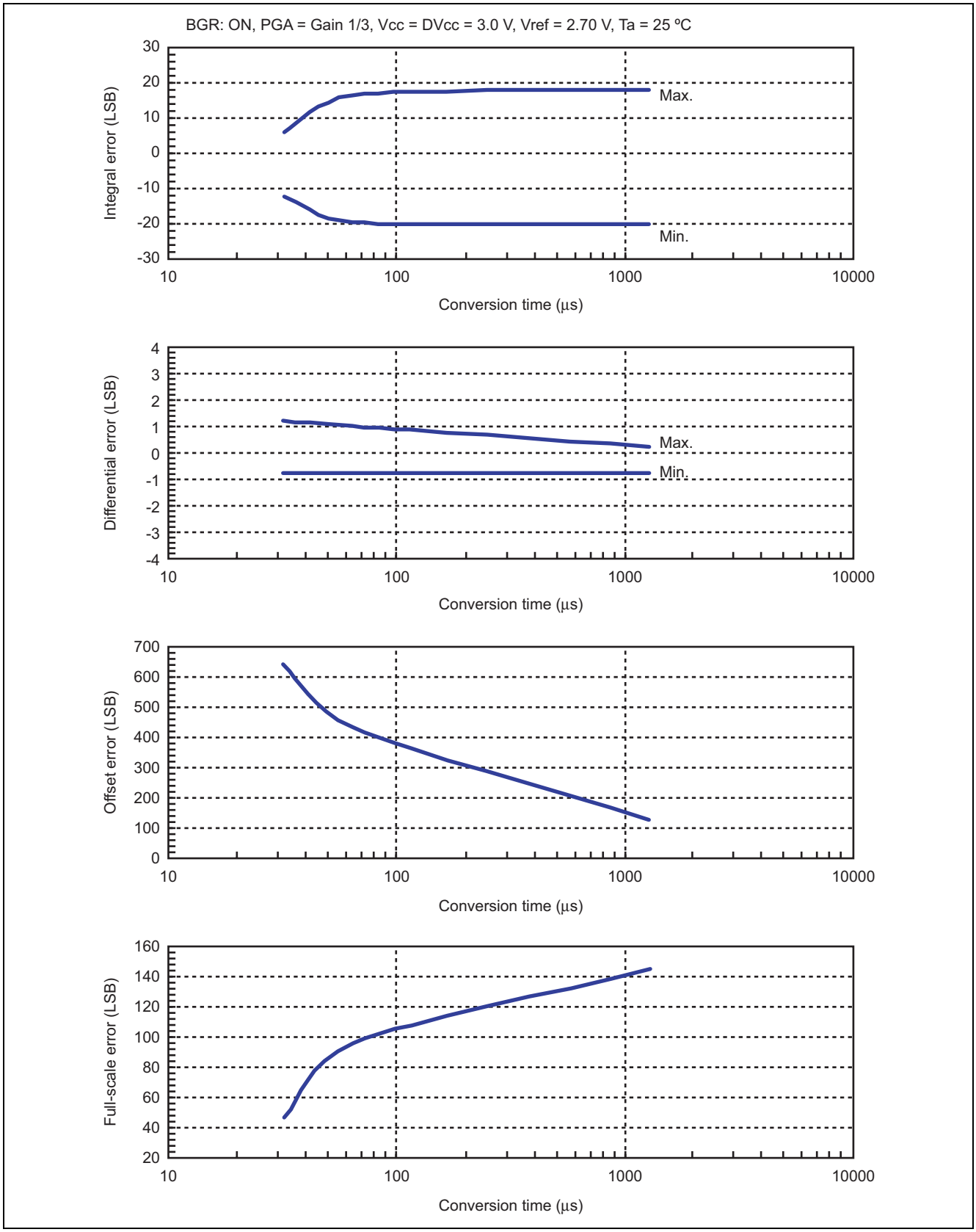
- Conversion time dependence 14



- Conversion time dependence 15

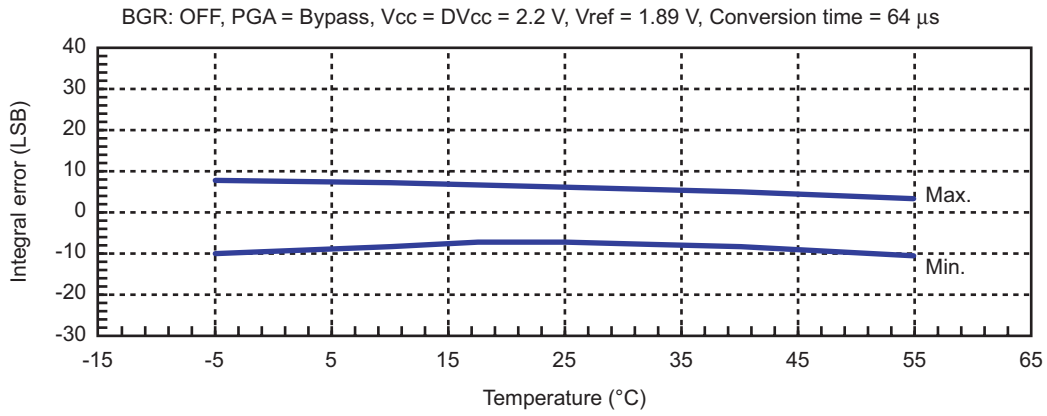


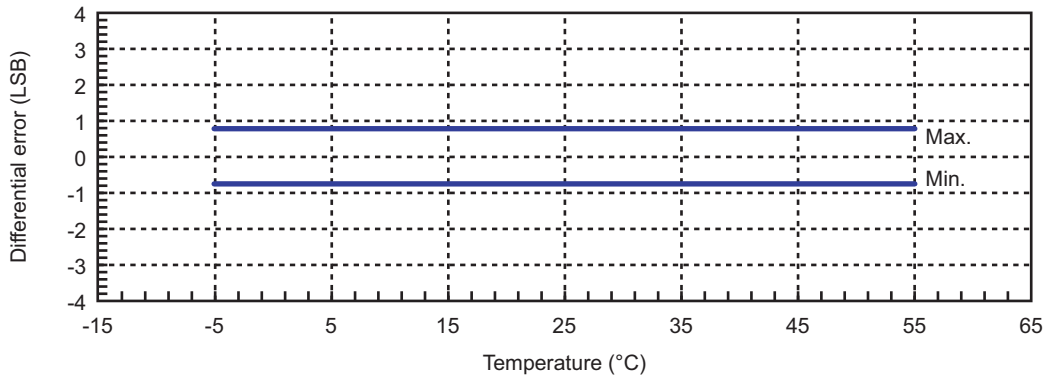
- Conversion time dependence 16

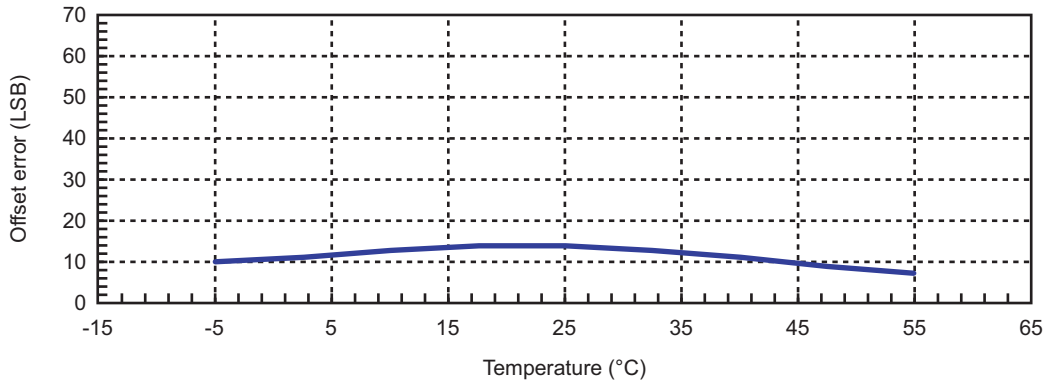


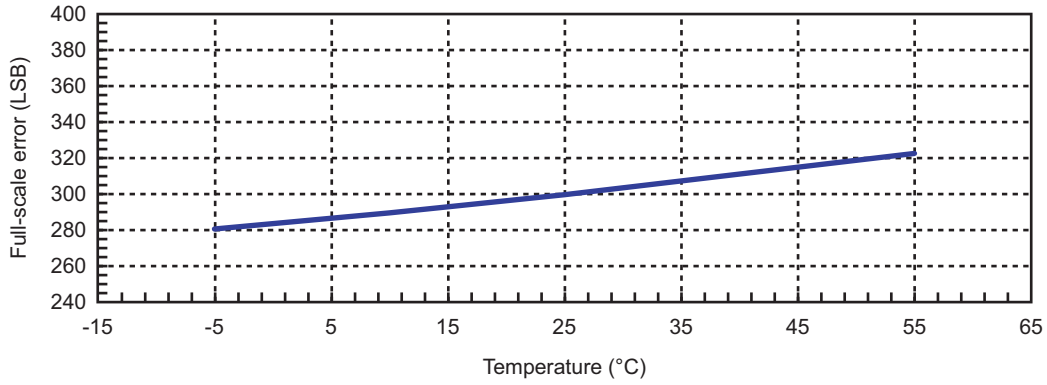
(2) Dependences on Temperature

- Temperature dependence 1

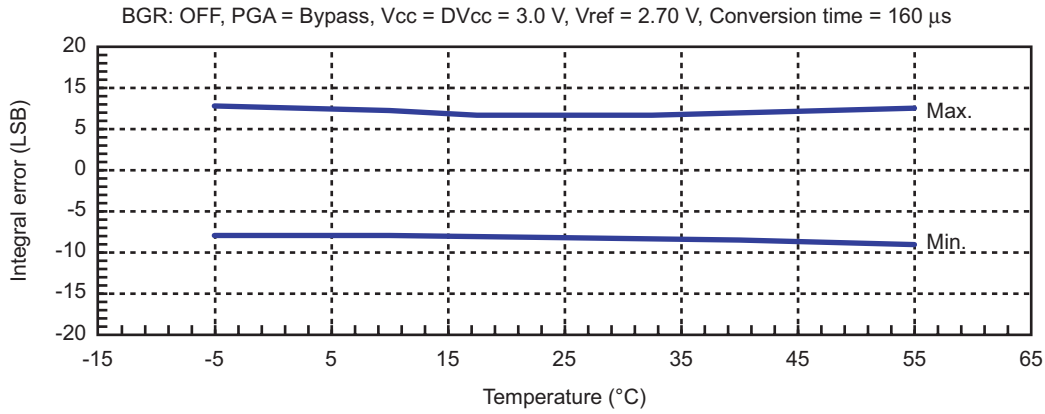


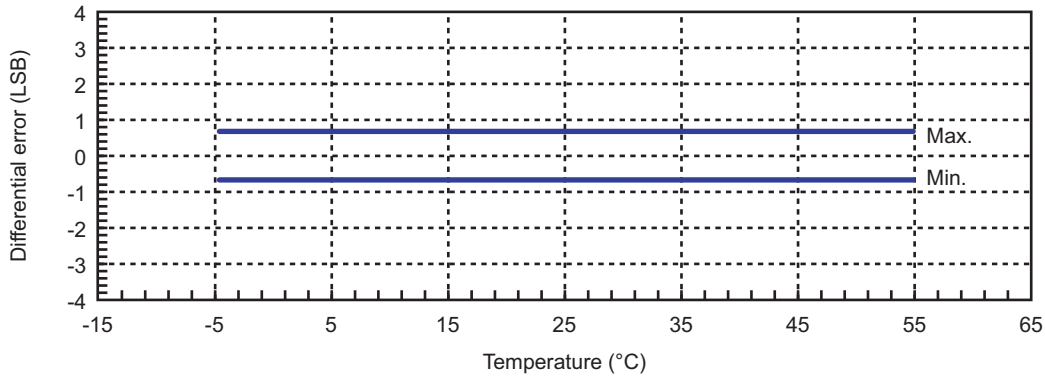


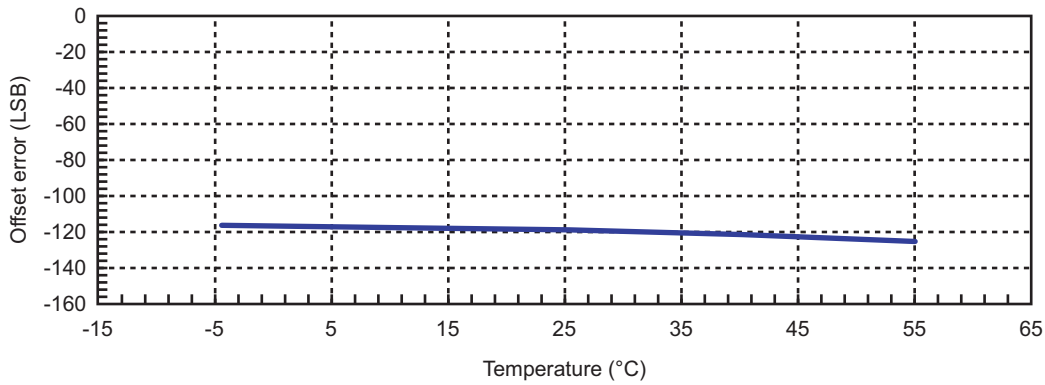


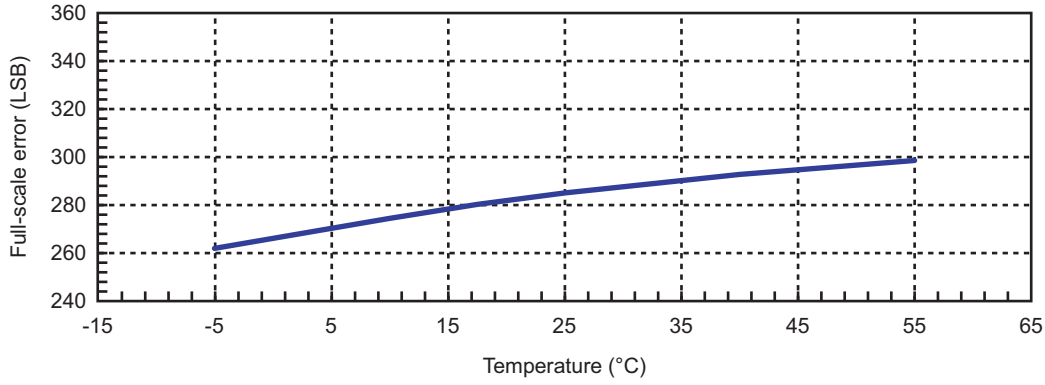


- Temperature dependence 2

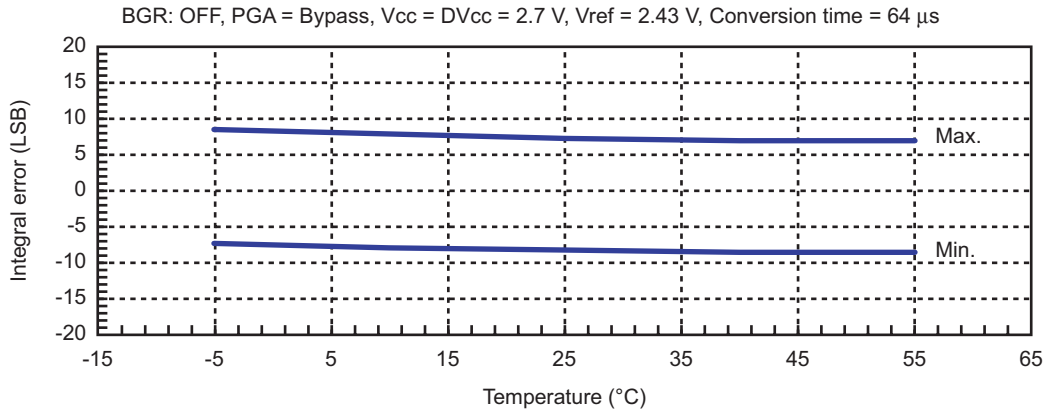


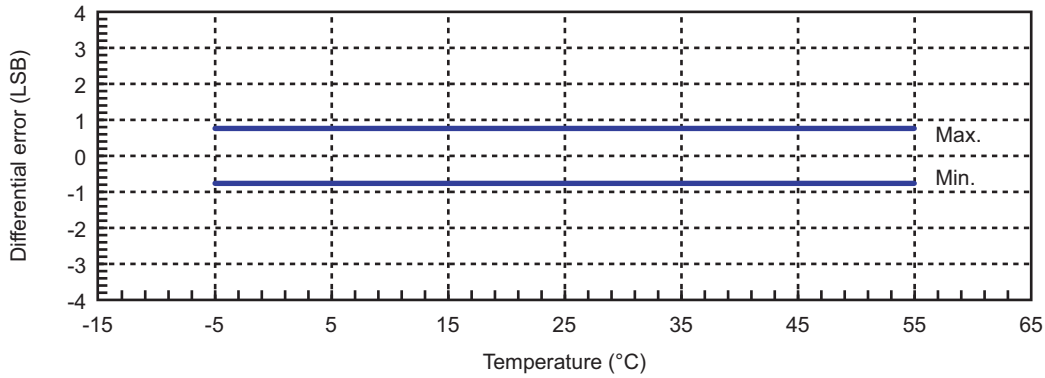


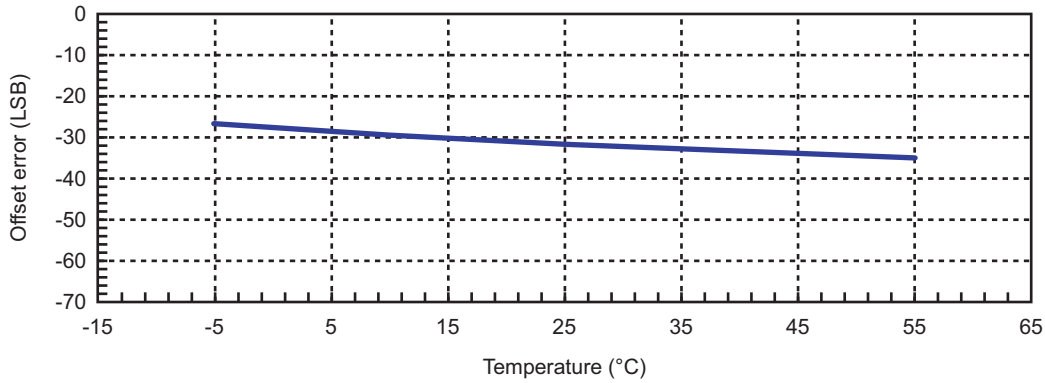


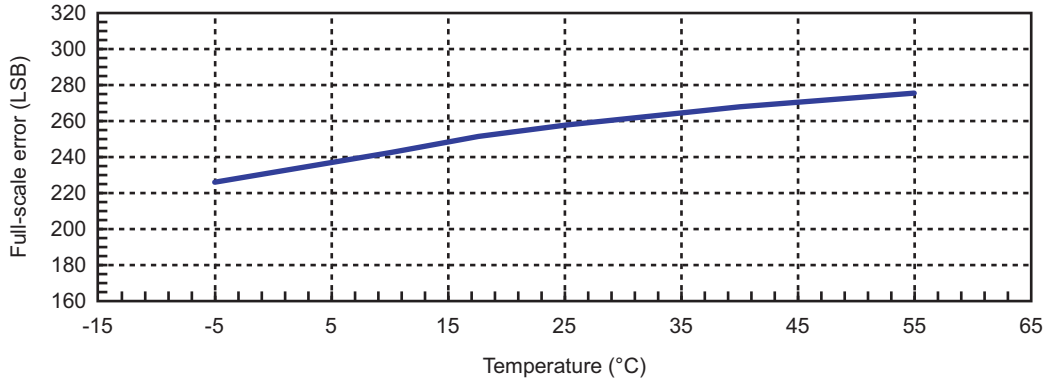


- Temperature dependence 3

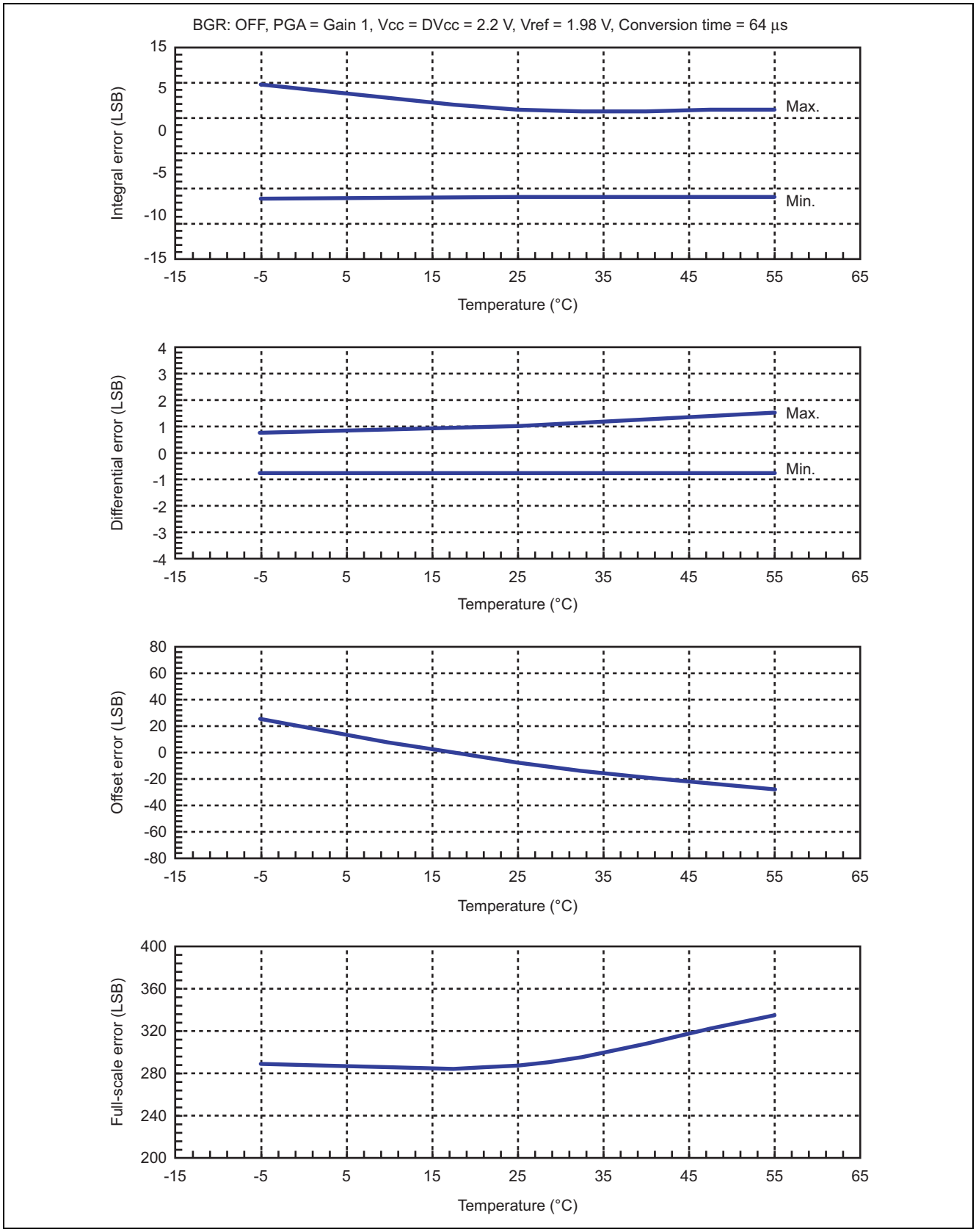




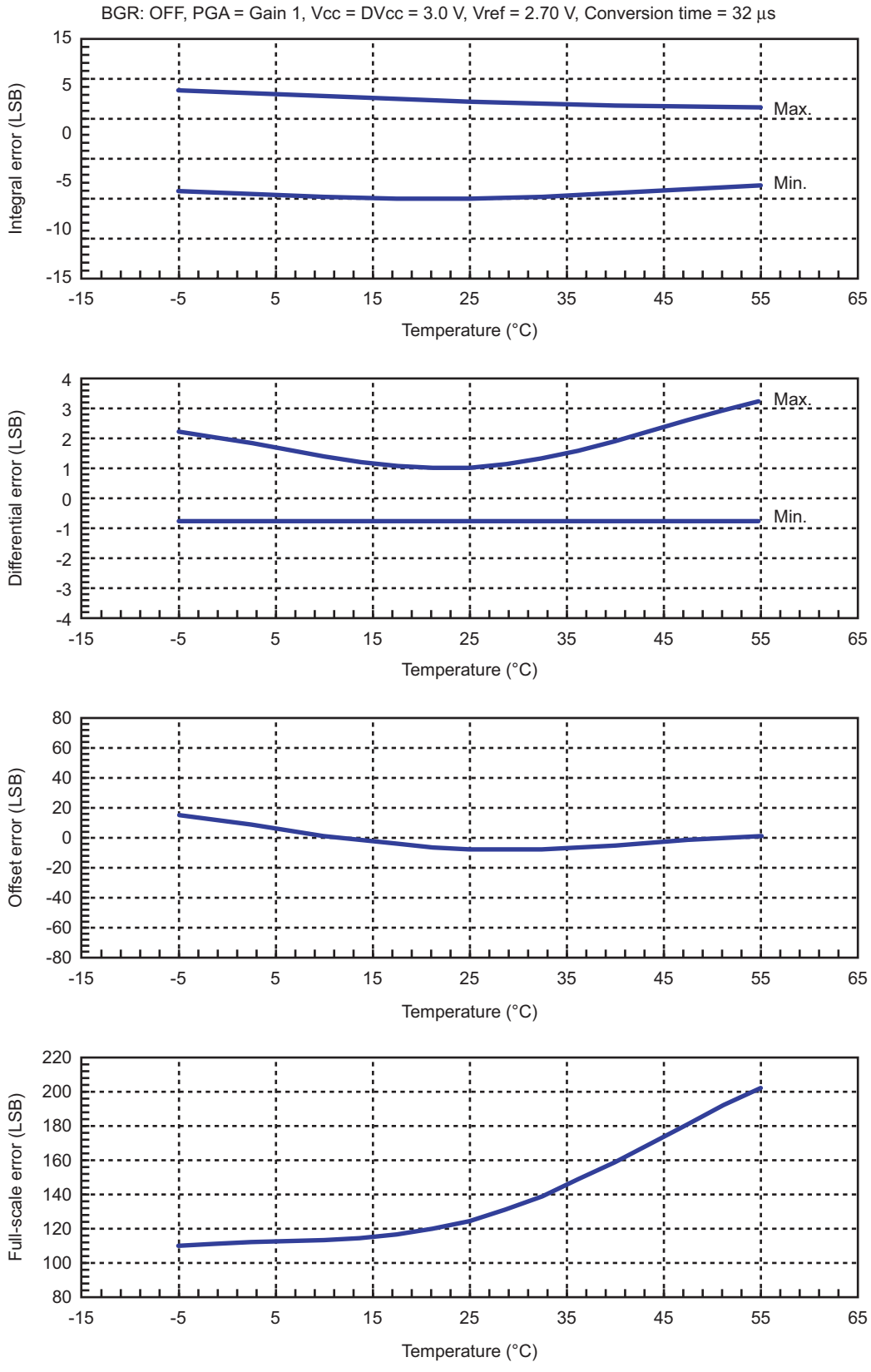




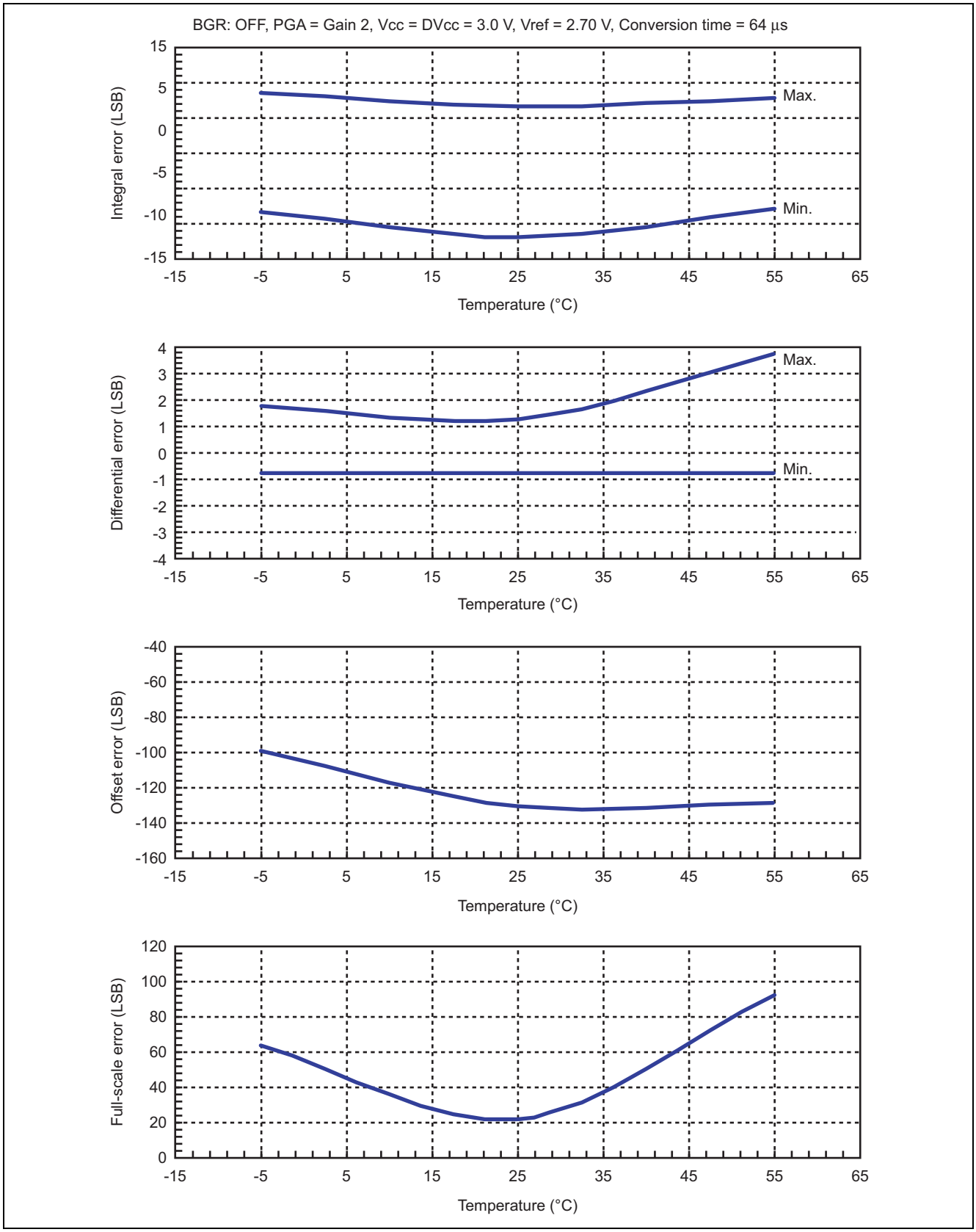
- Temperature dependence 4



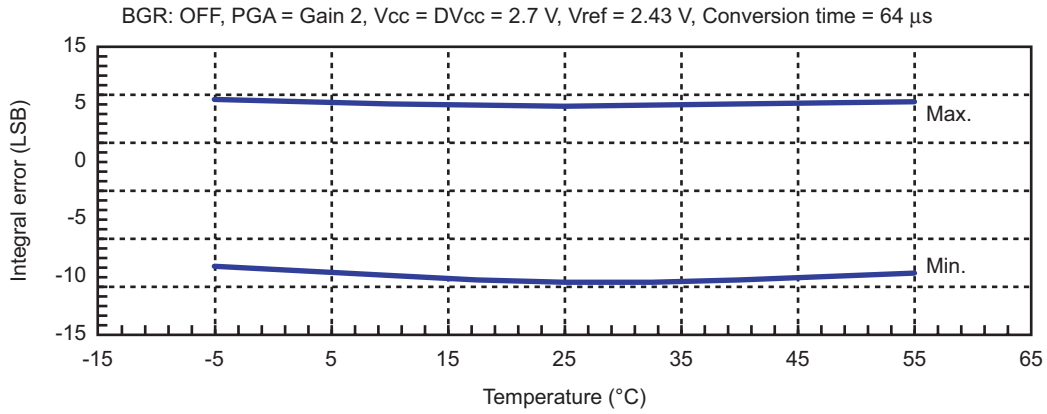
- Temperature dependence 5

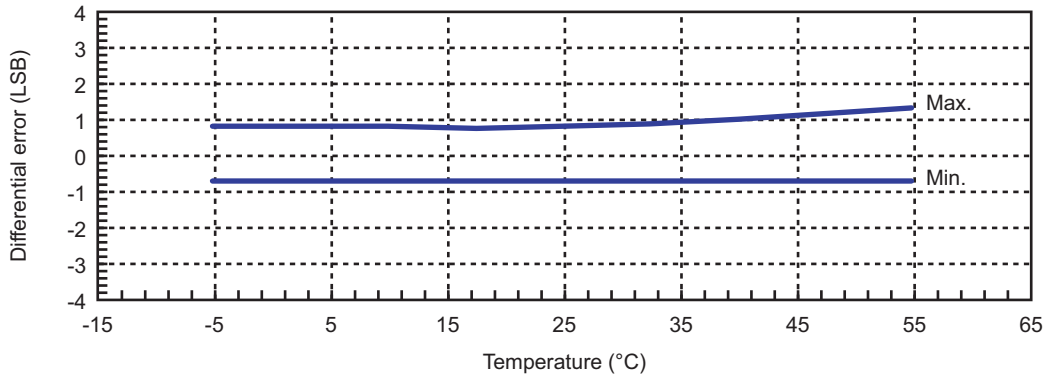


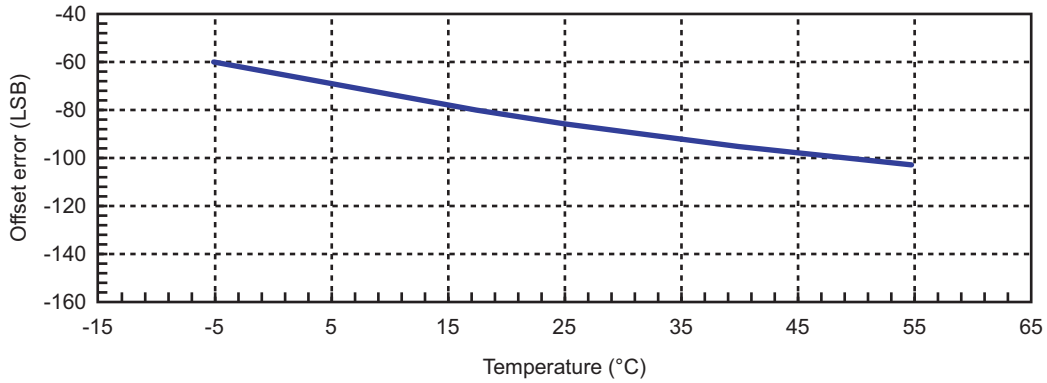
- Temperature dependence 6

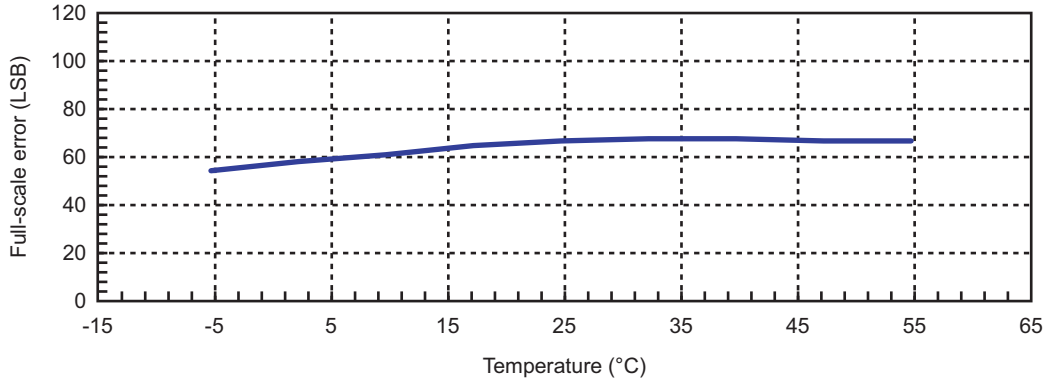


- Temperature dependence 7

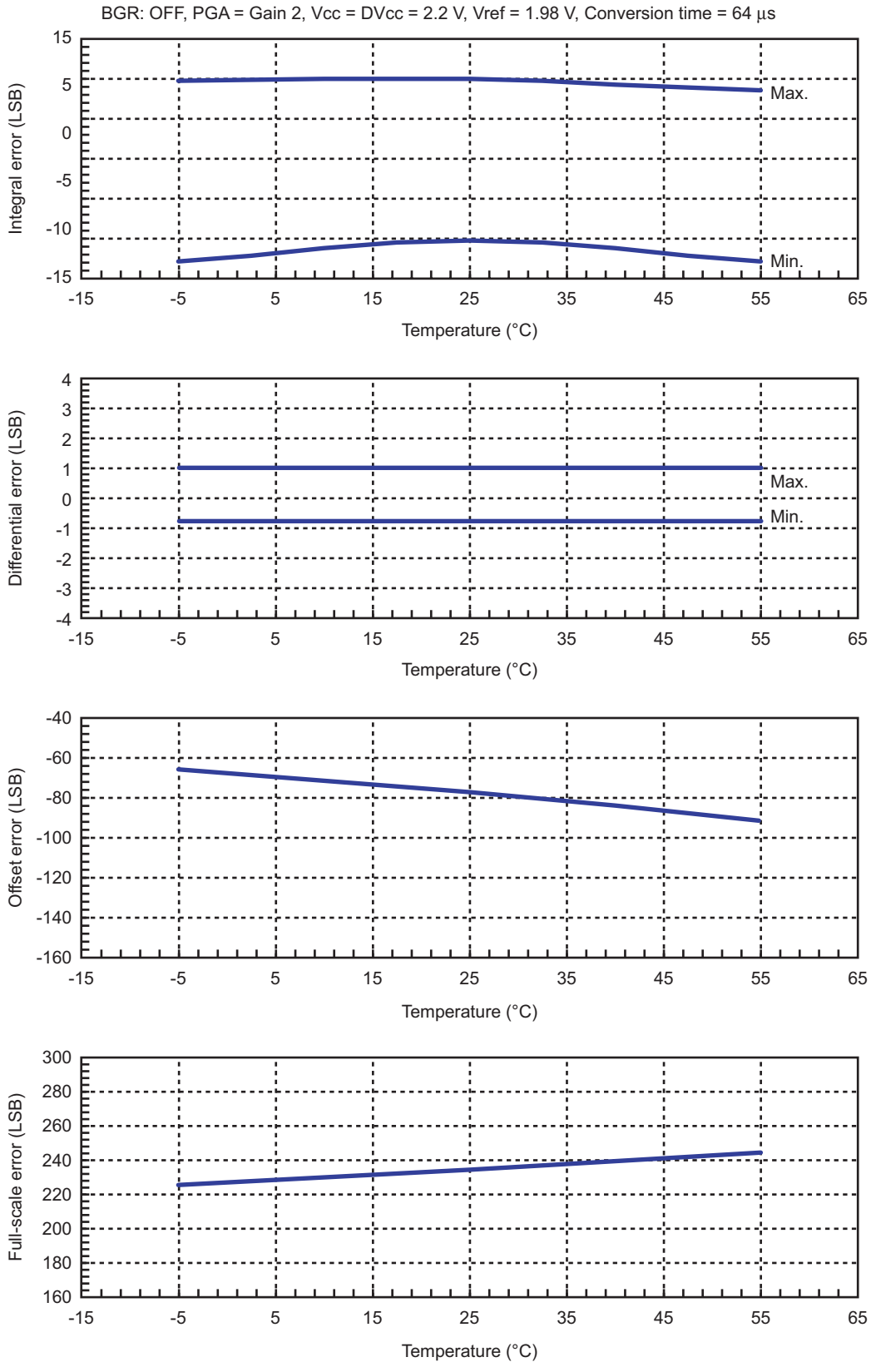




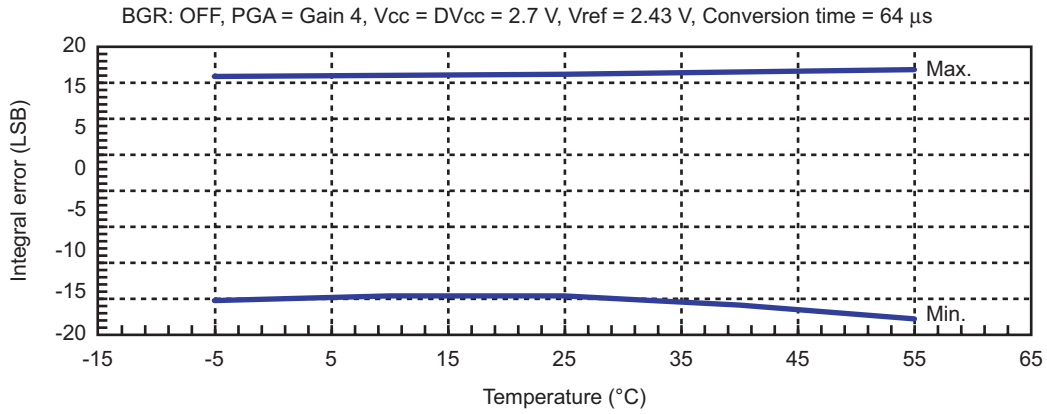


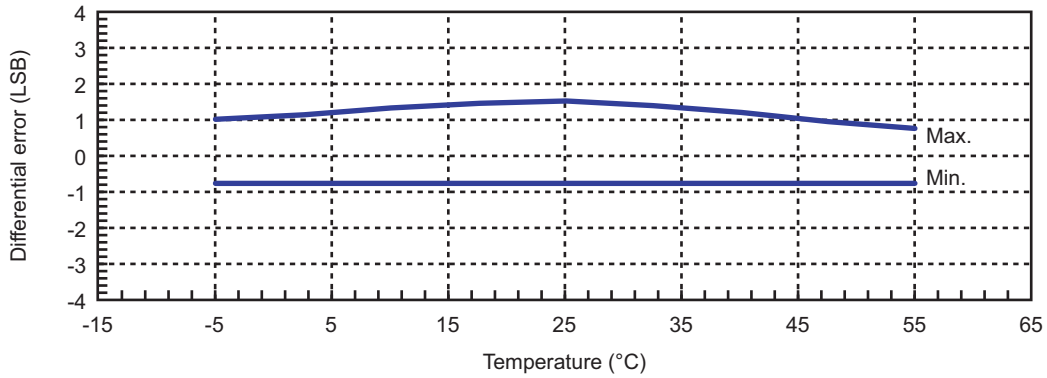


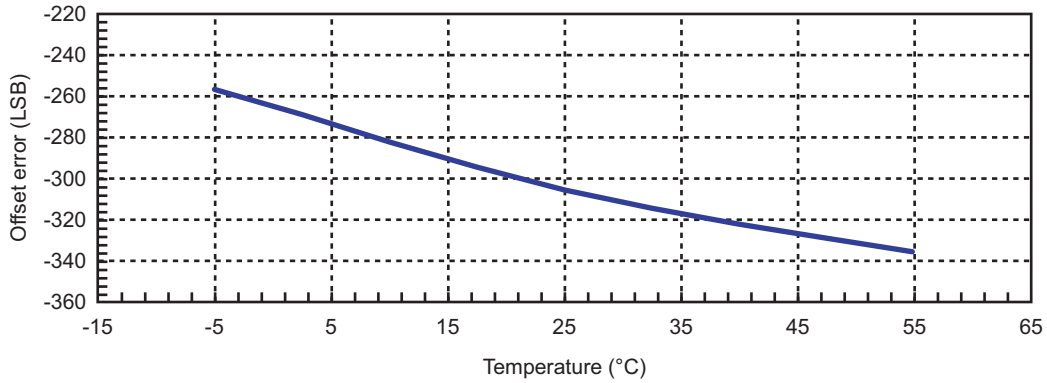
- Temperature dependence 8

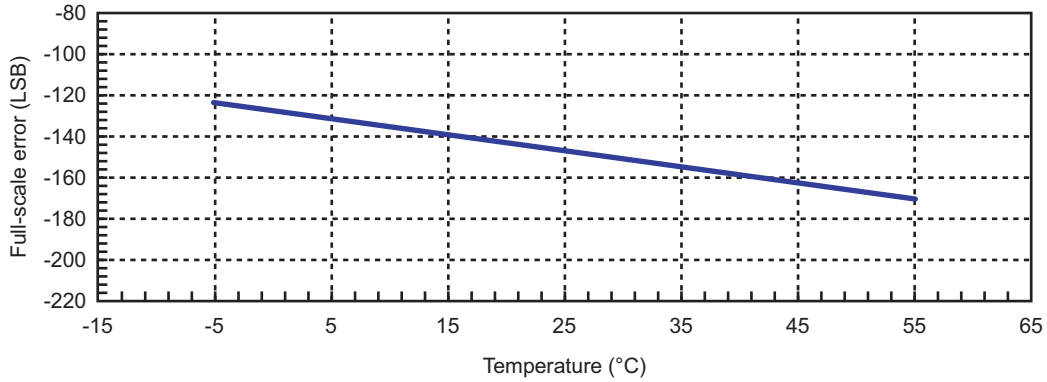


- Temperature dependence 9

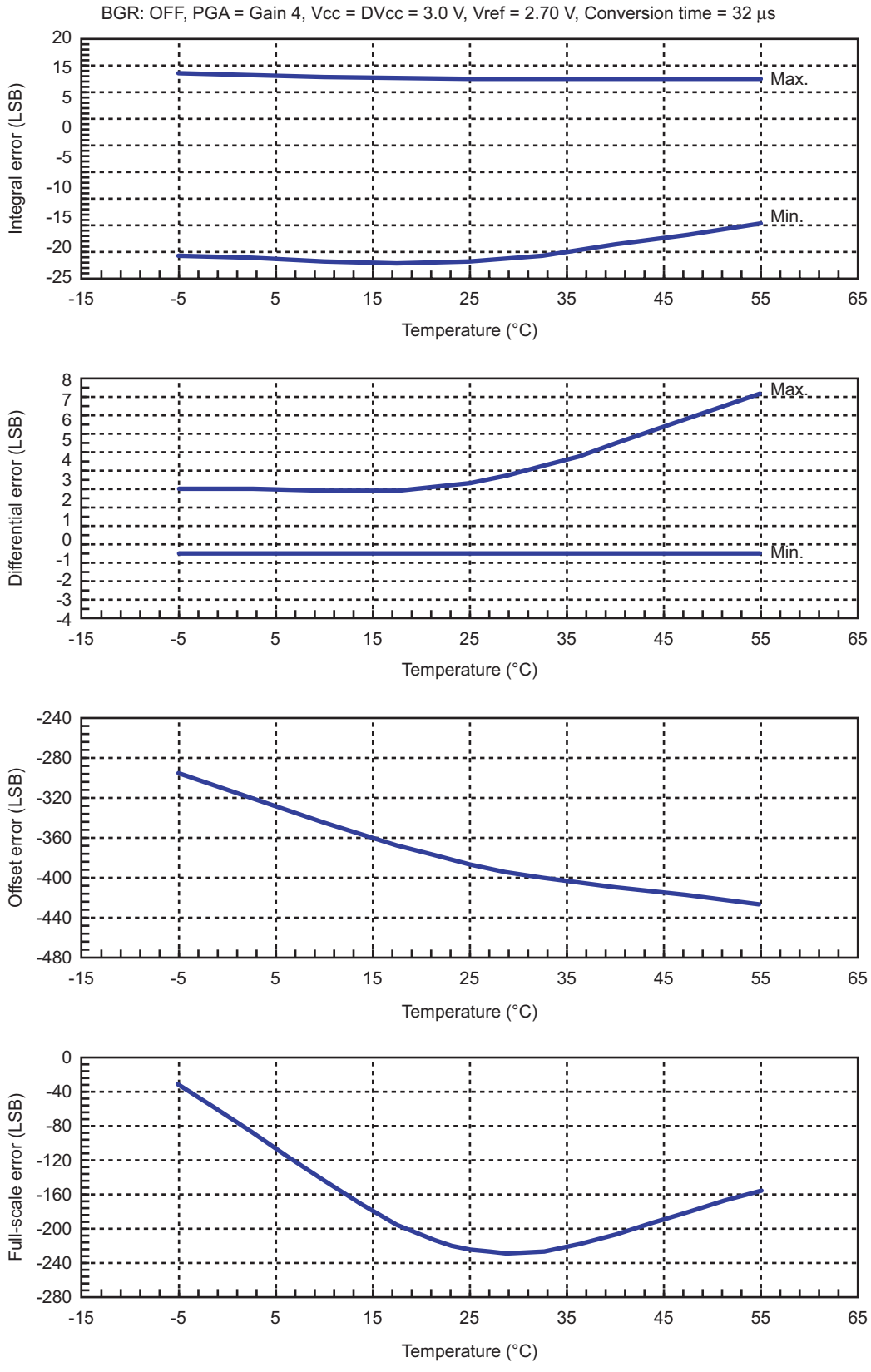




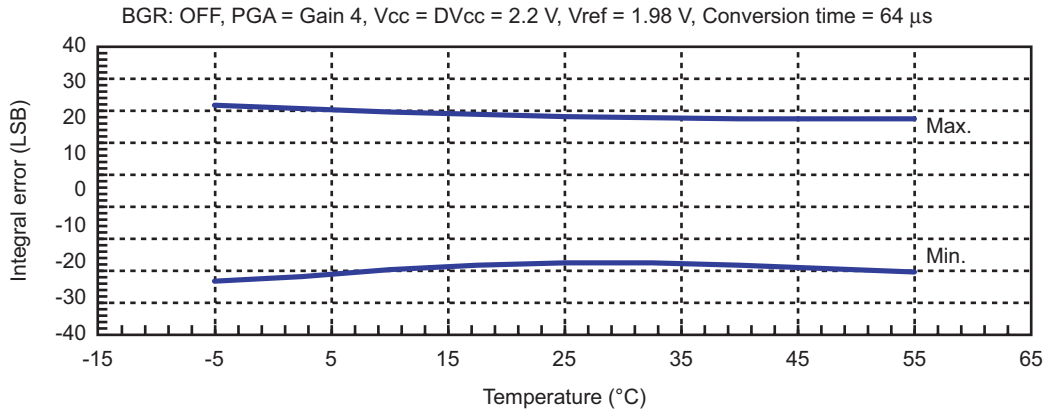


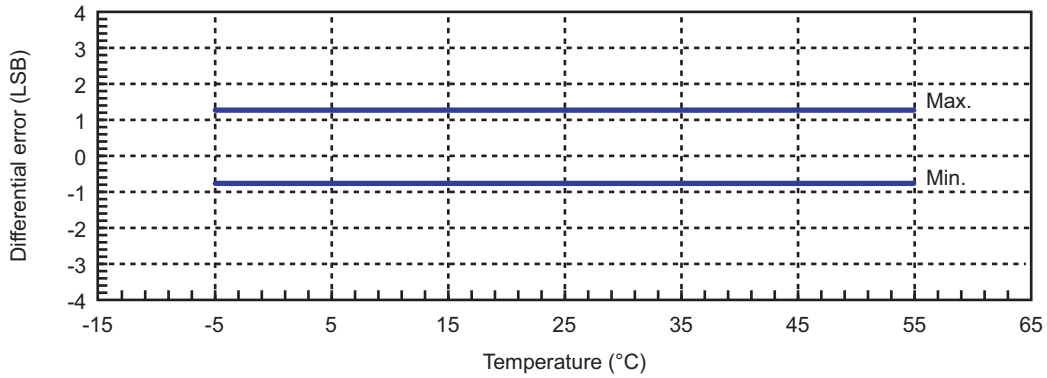


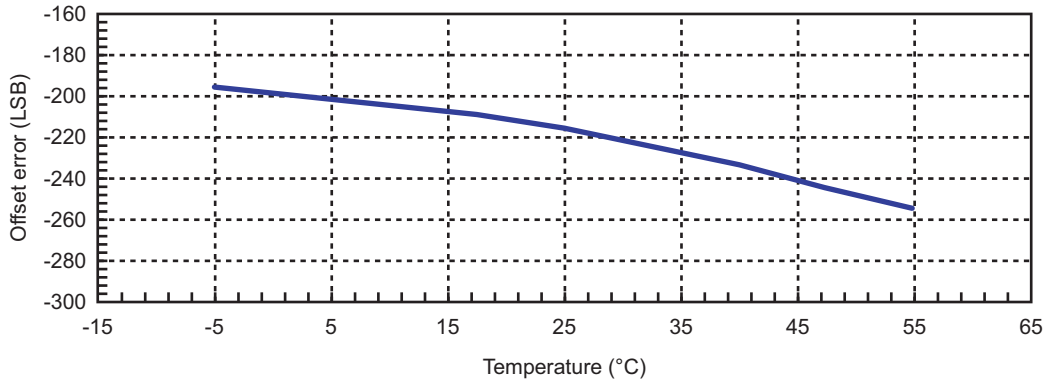
- Temperature dependence 10

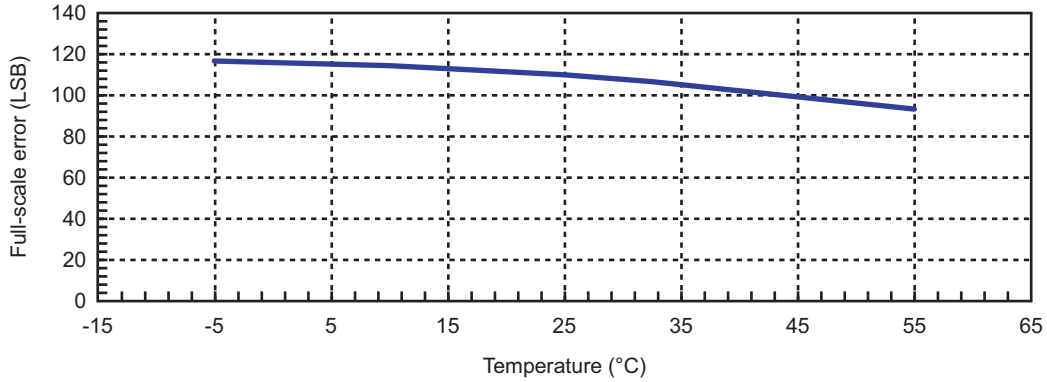


- Temperature dependence 11

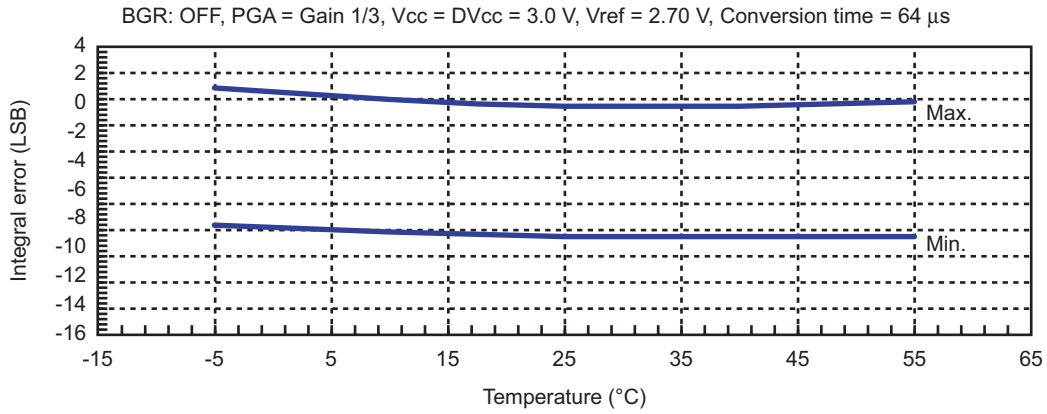


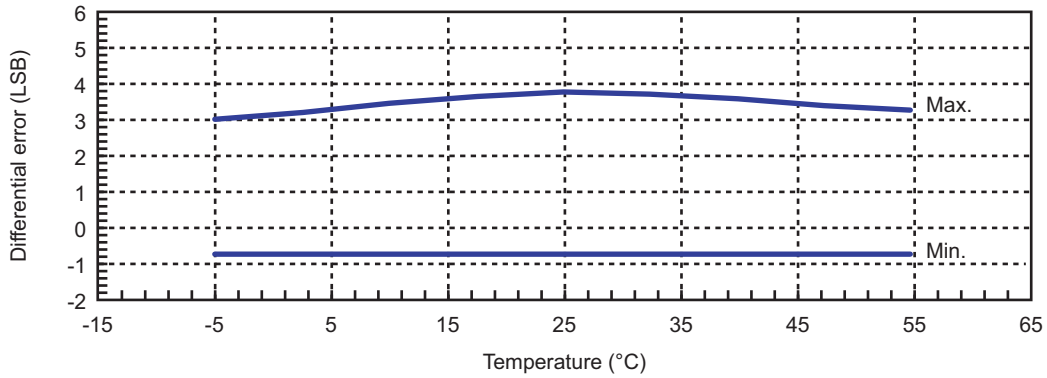


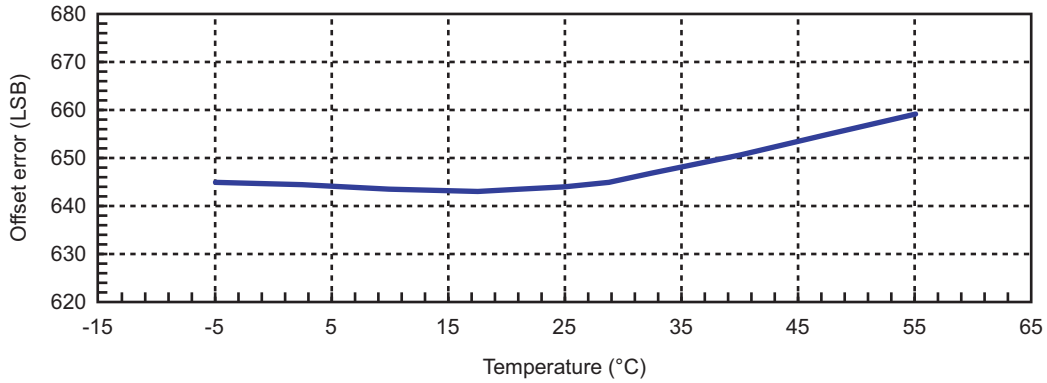


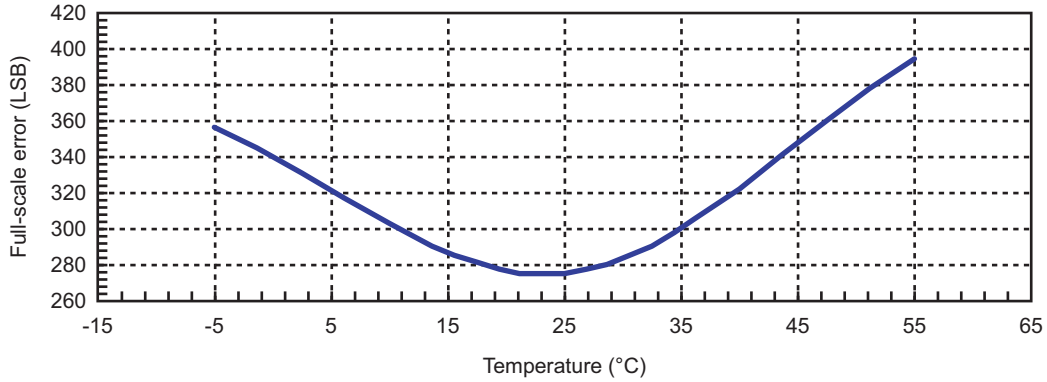


- Temperature dependence 12

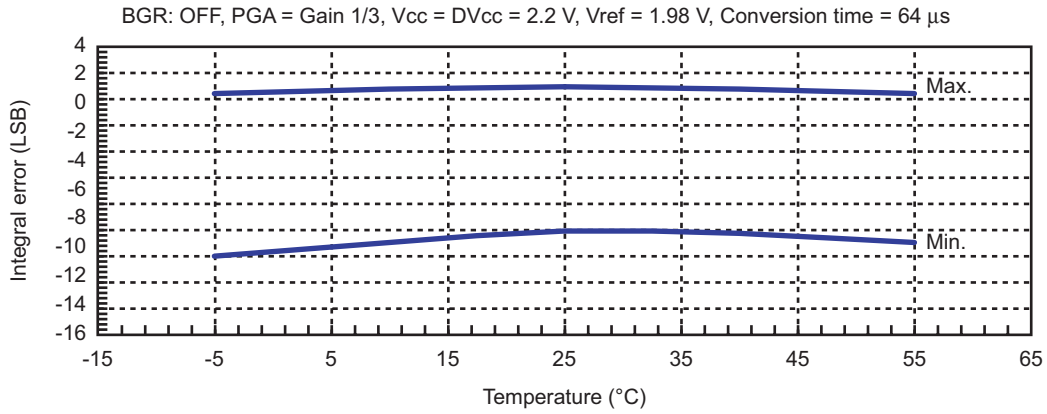


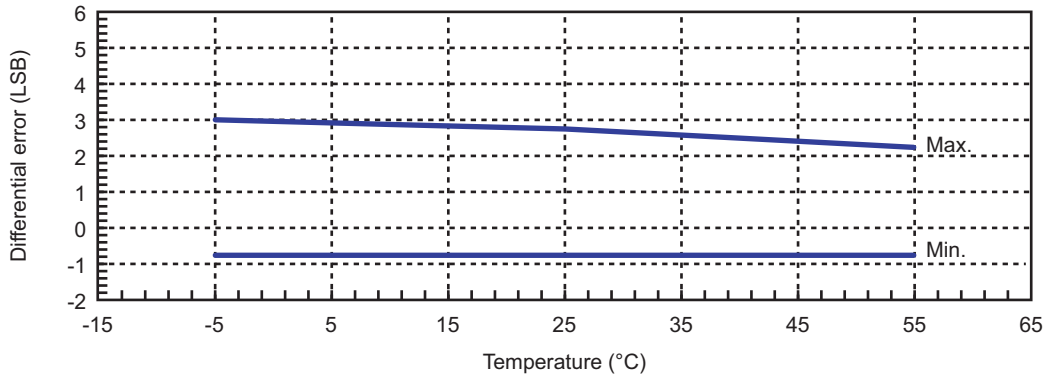


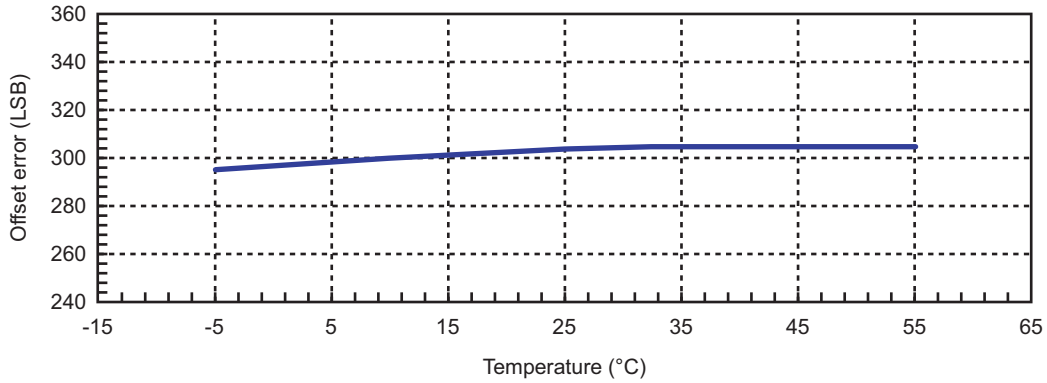


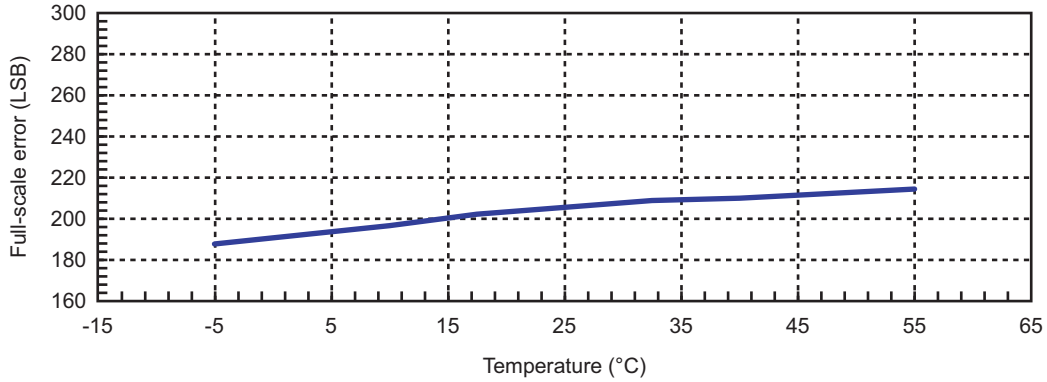


- Temperature dependence 13

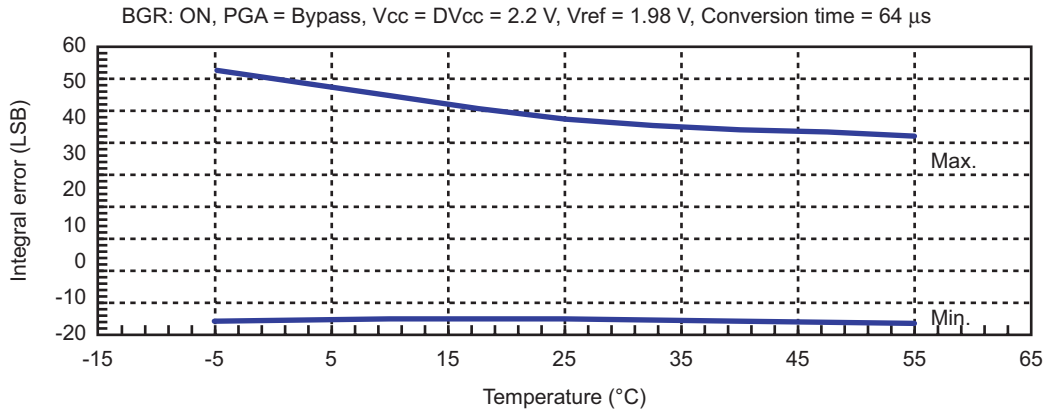


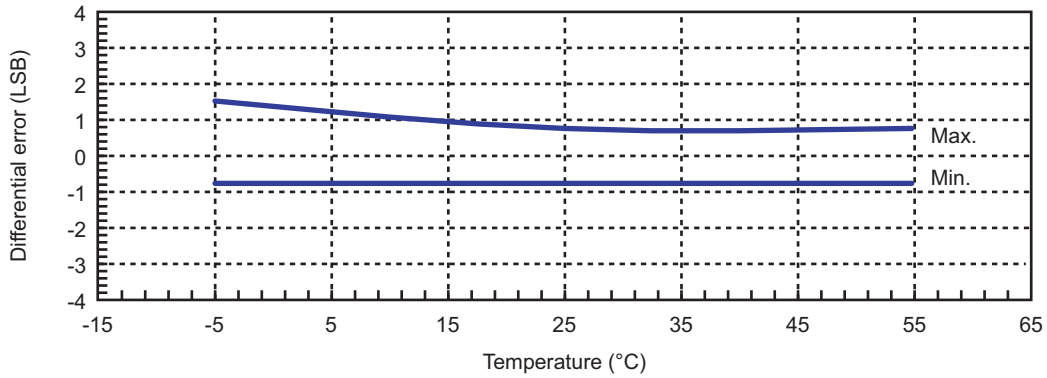


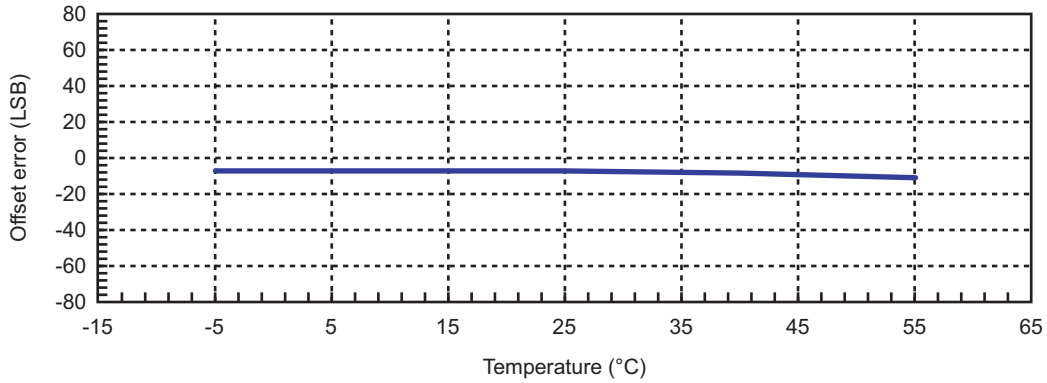


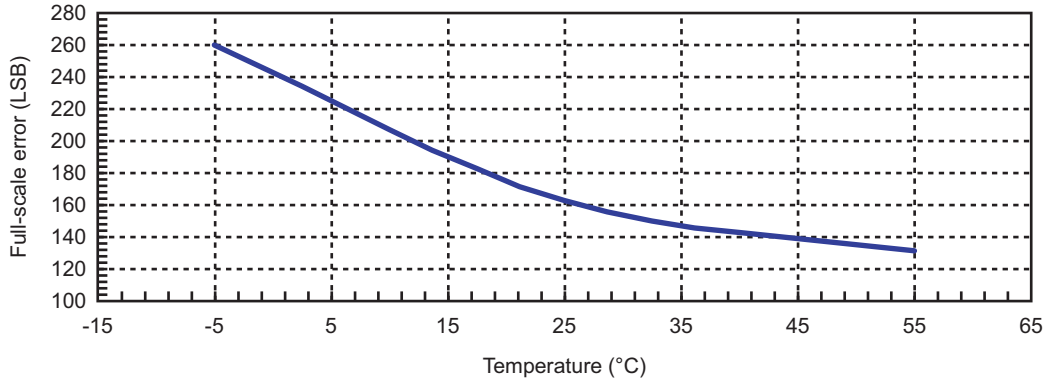


- Temperature dependence 14

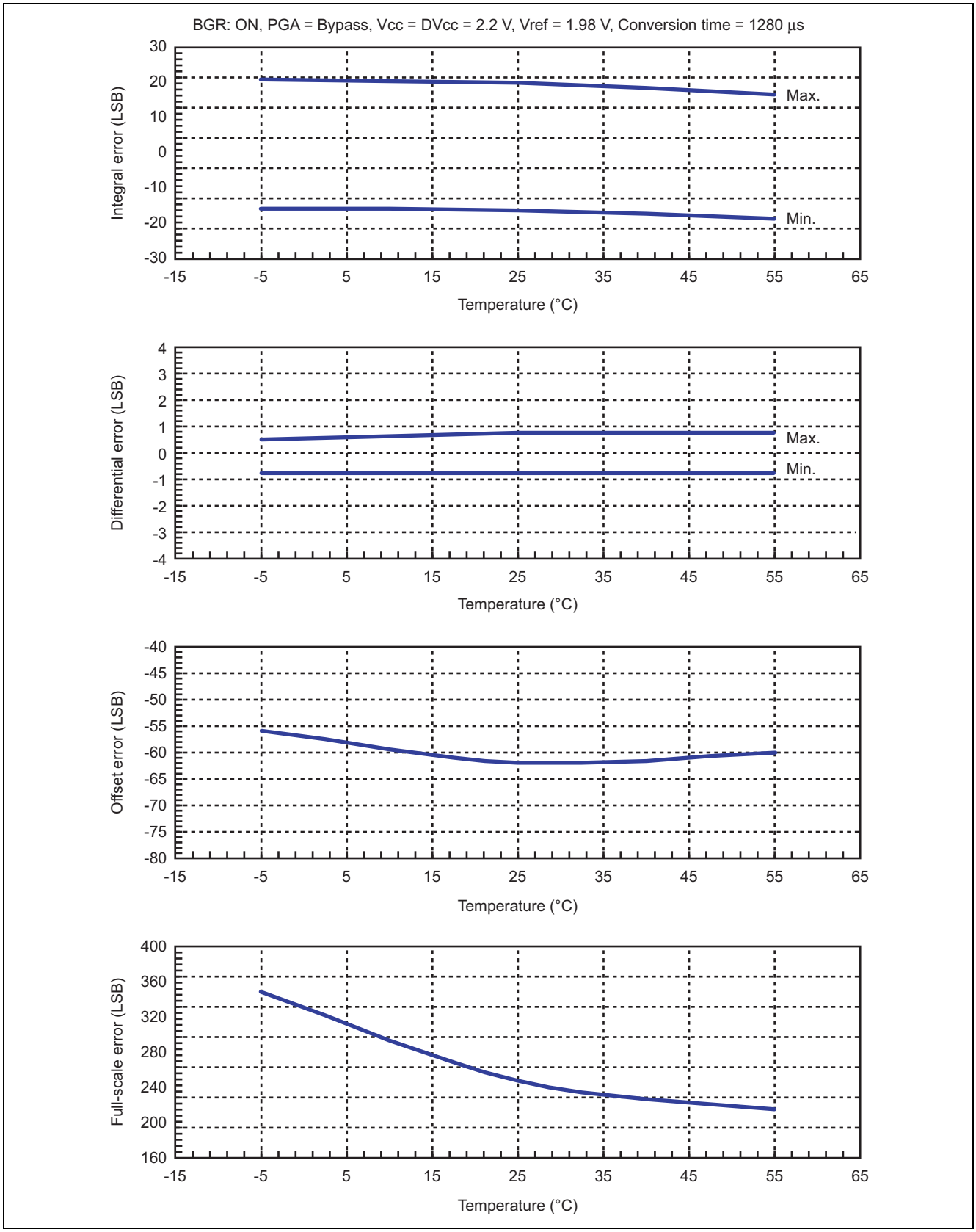




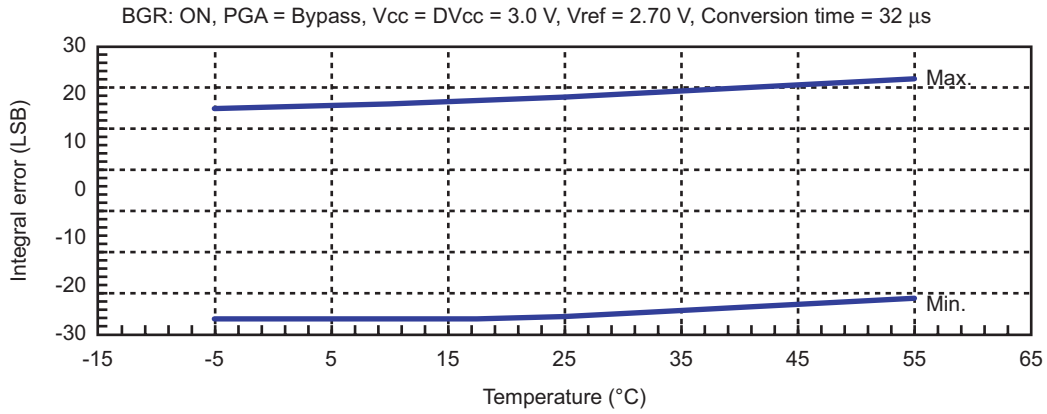


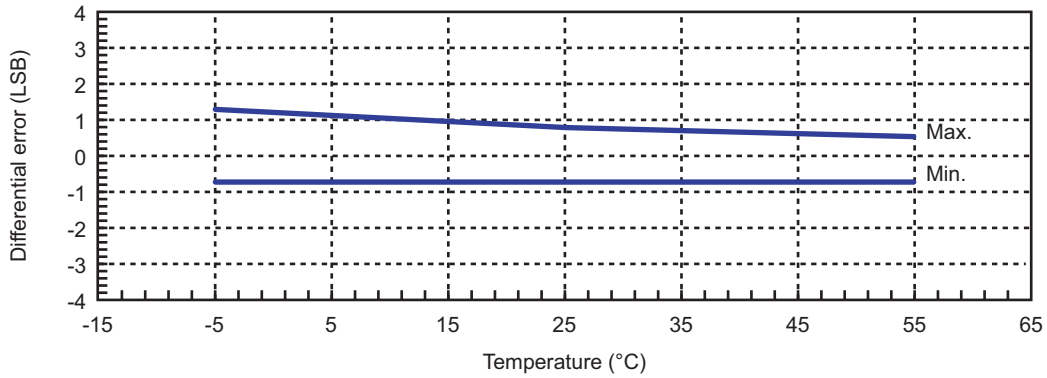


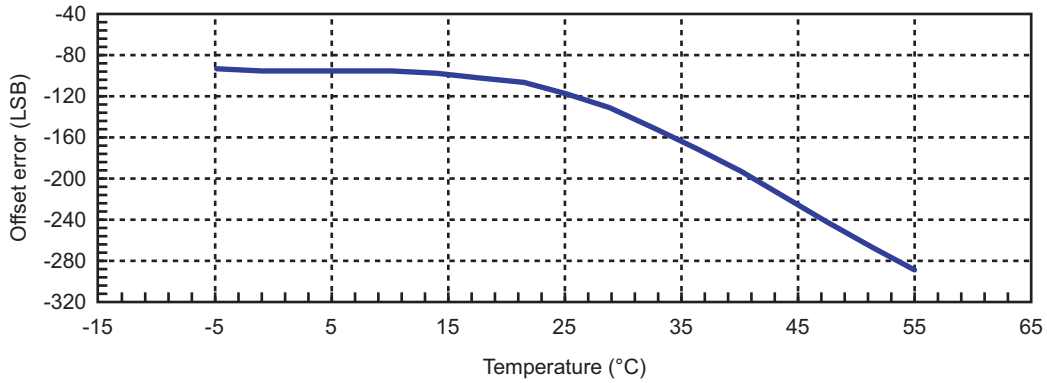
- Temperature dependence 15

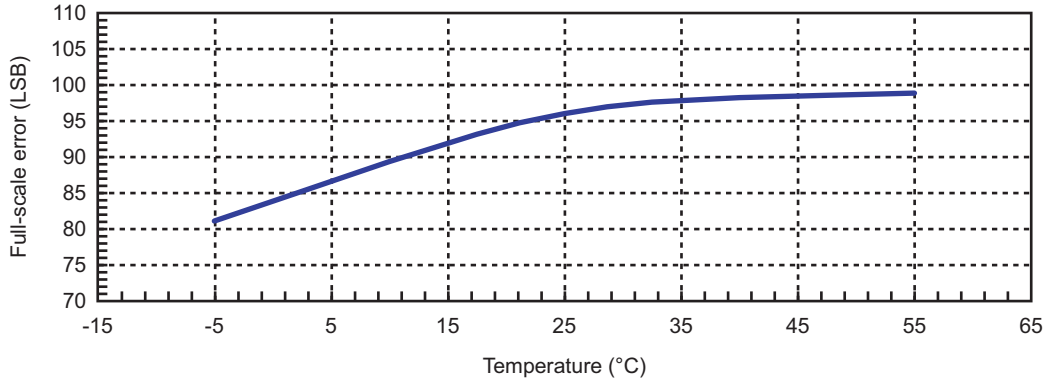


- Temperature dependence 16

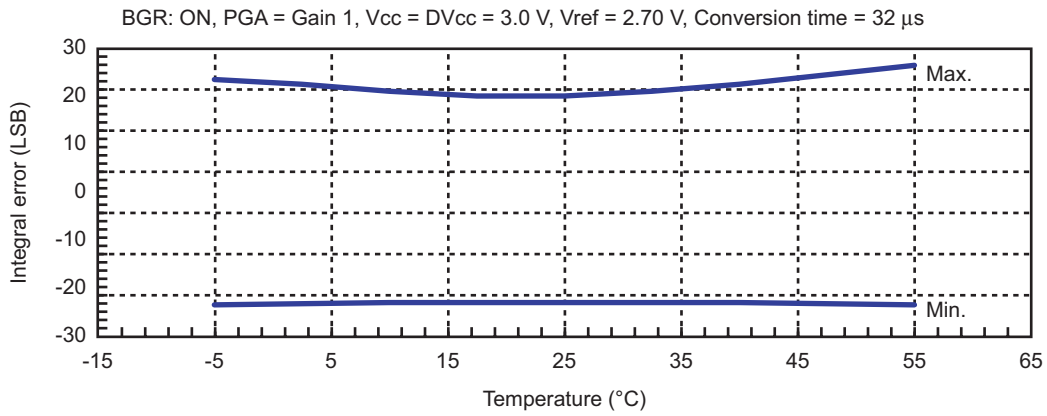


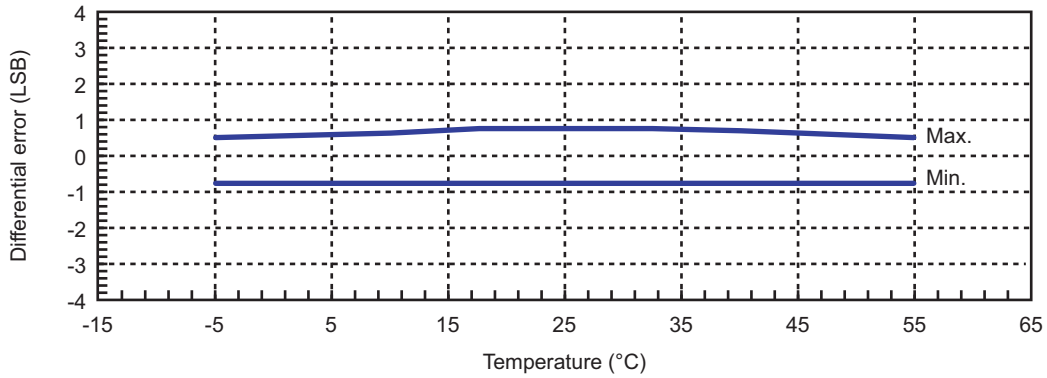


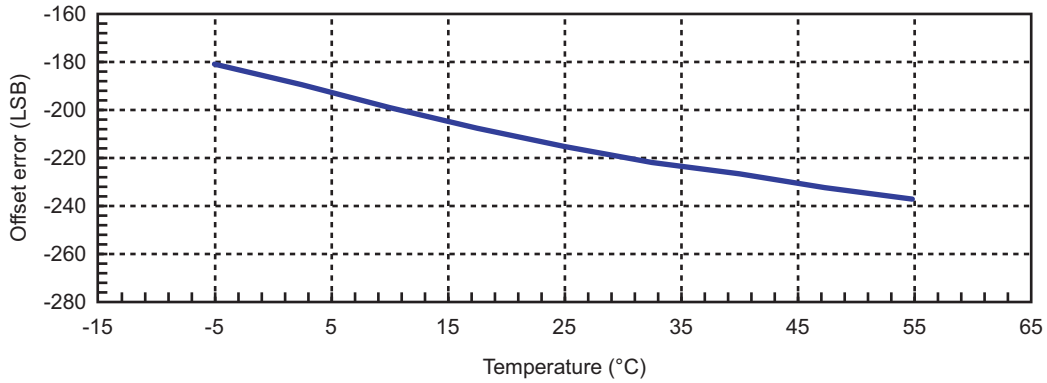


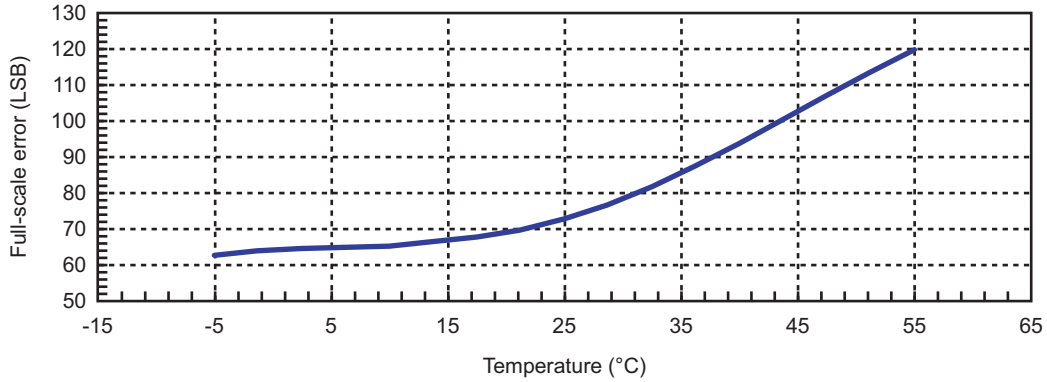


- Temperature dependence 17

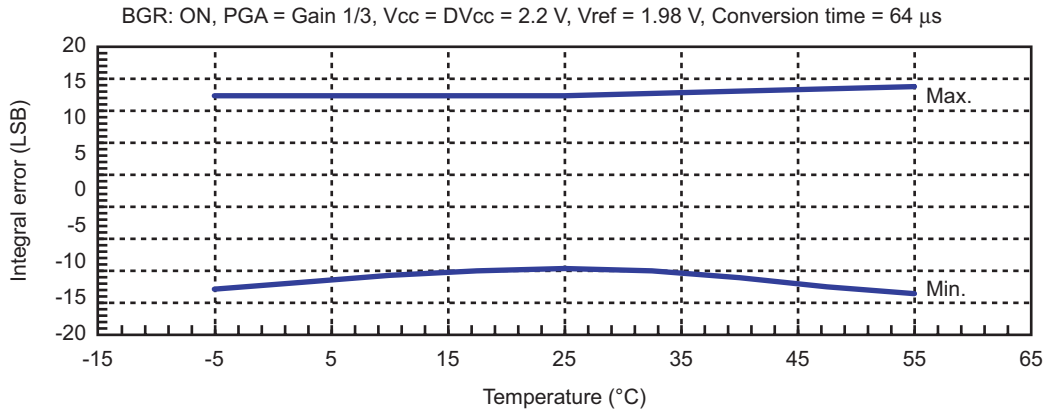


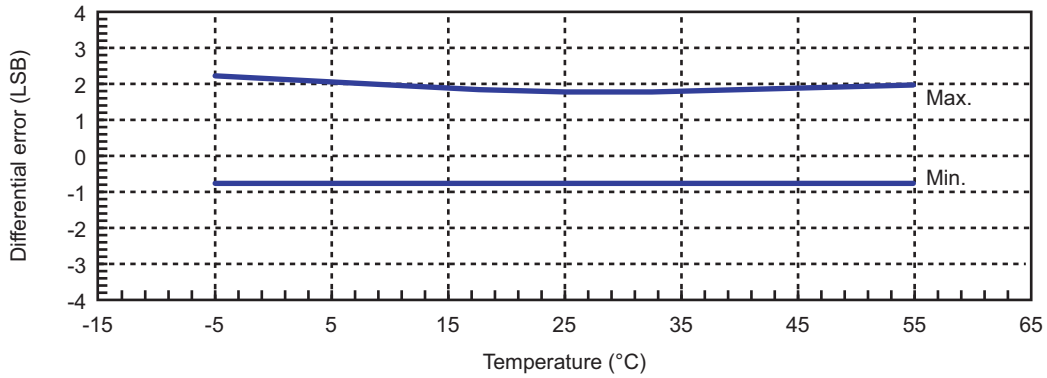


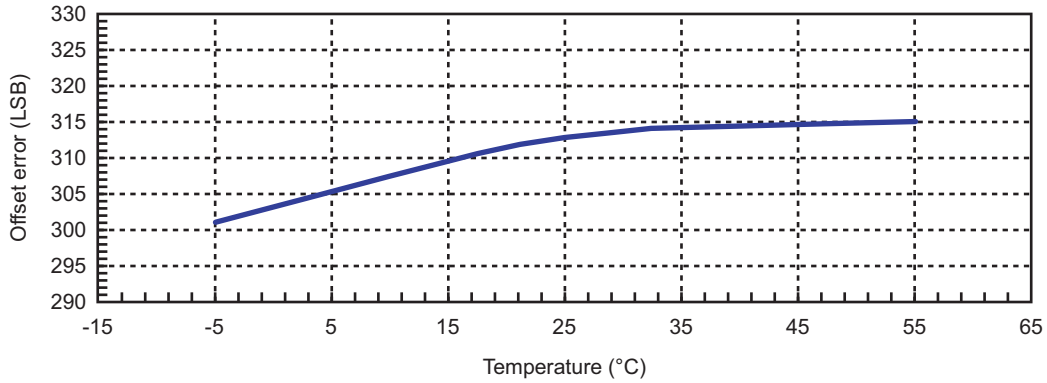


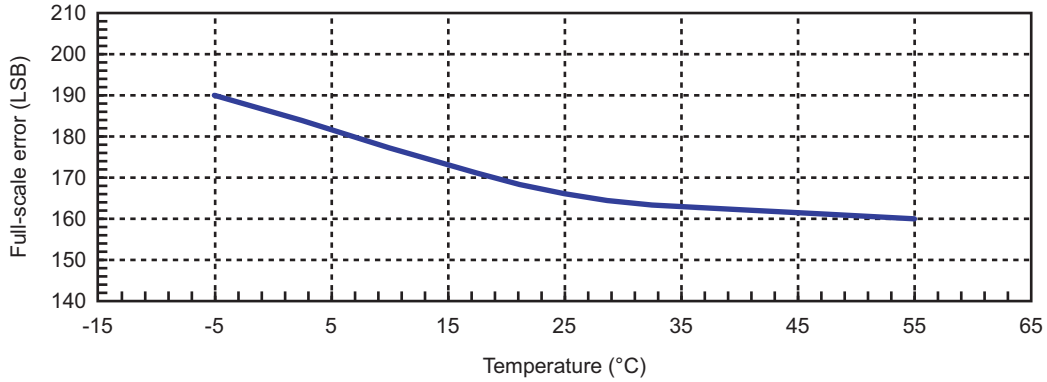


- Temperature dependence 18

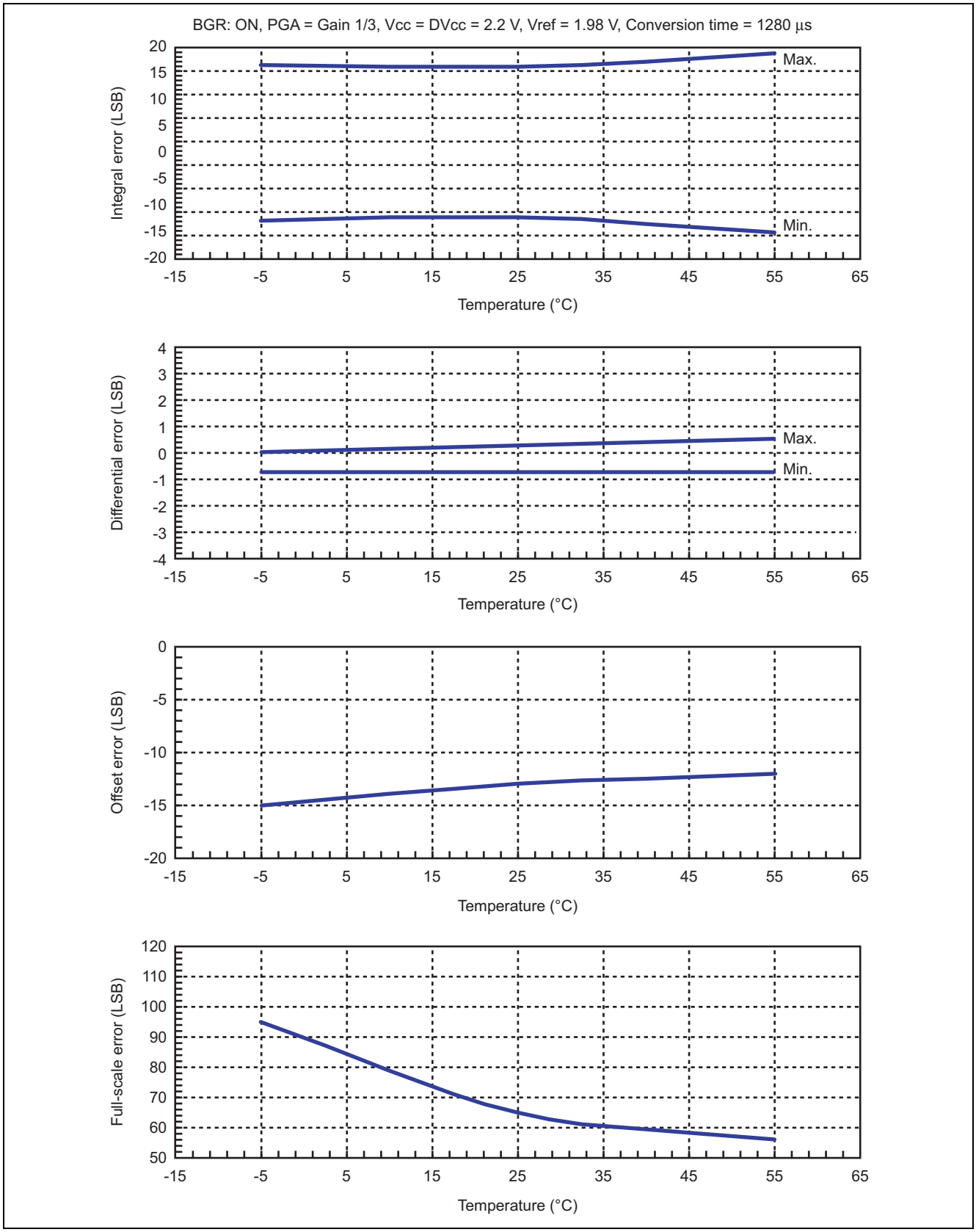




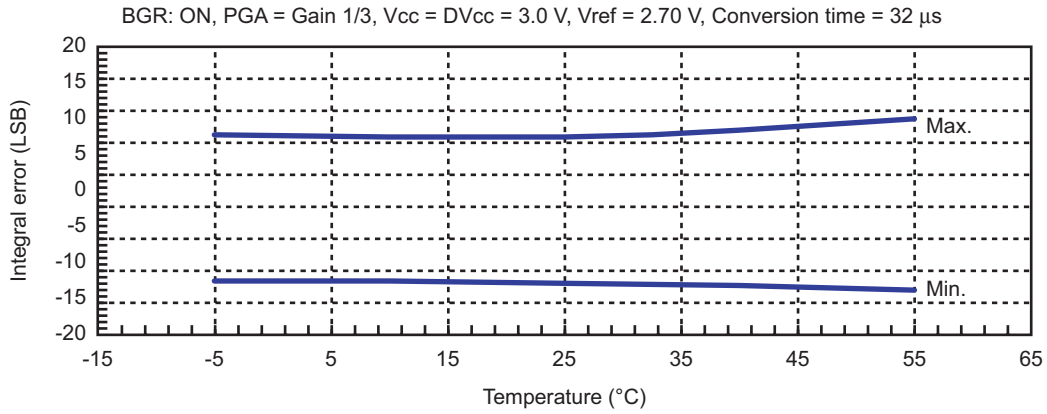


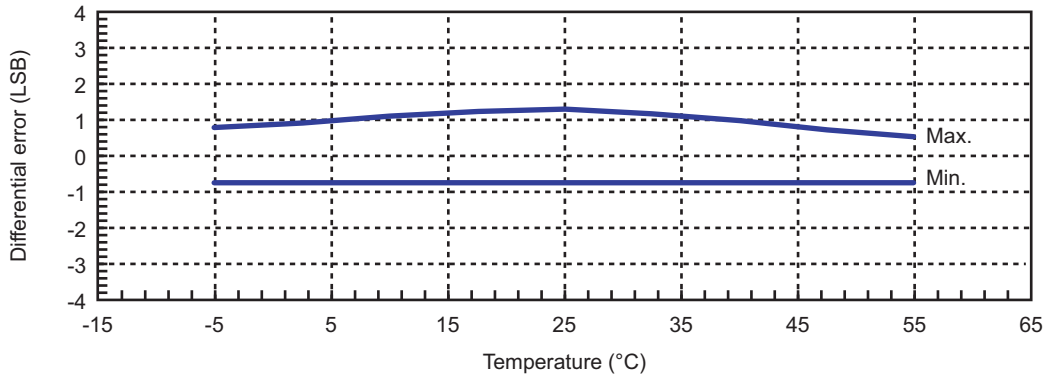


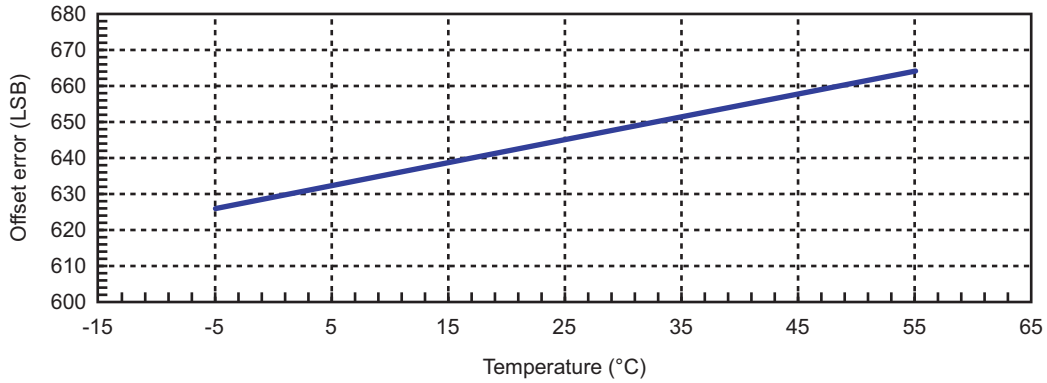
- Temperature dependence 19

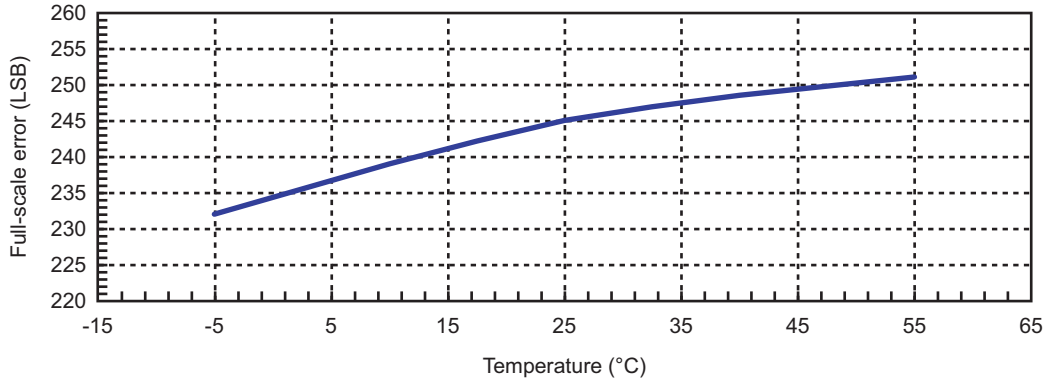


- Temperature dependence 20



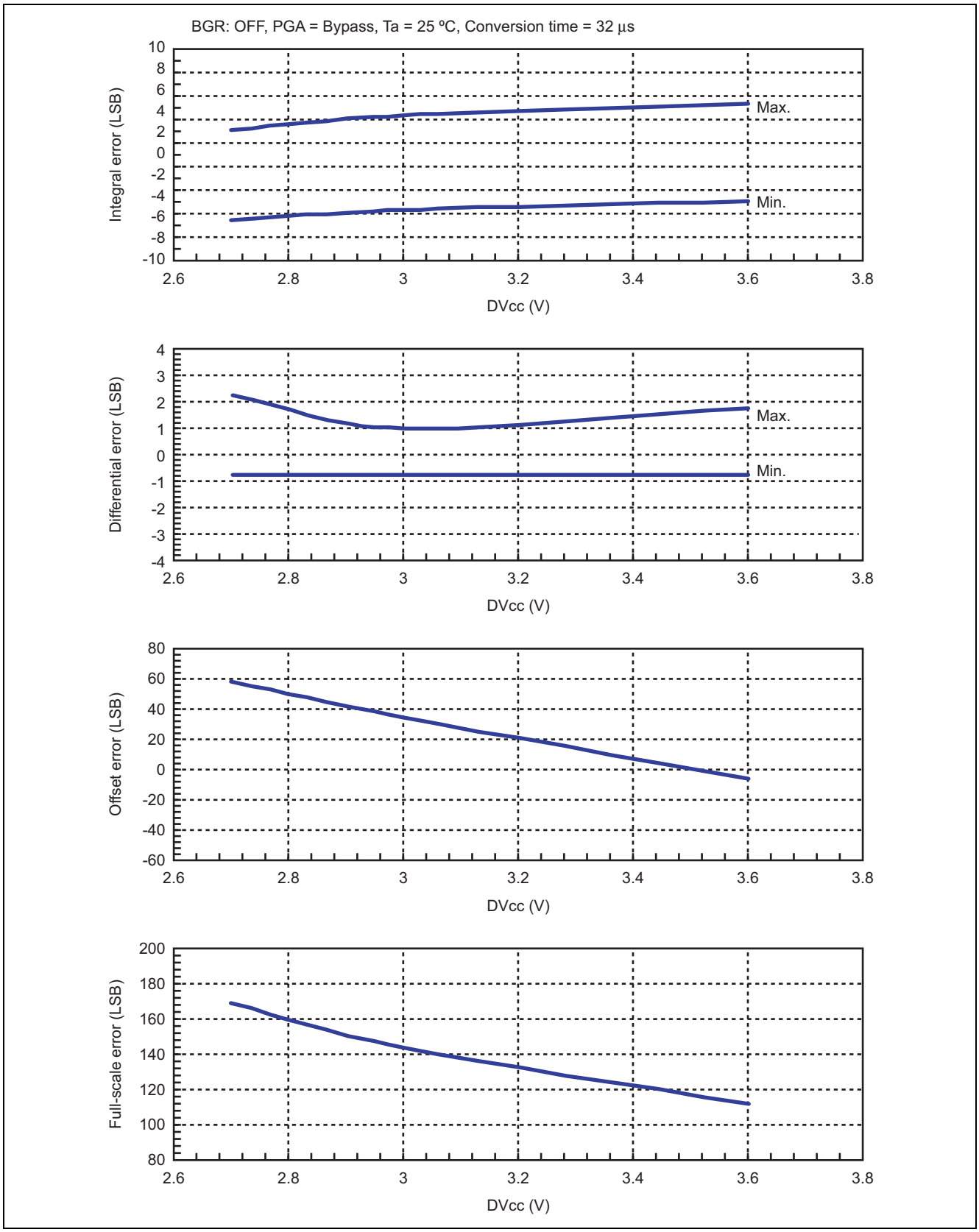




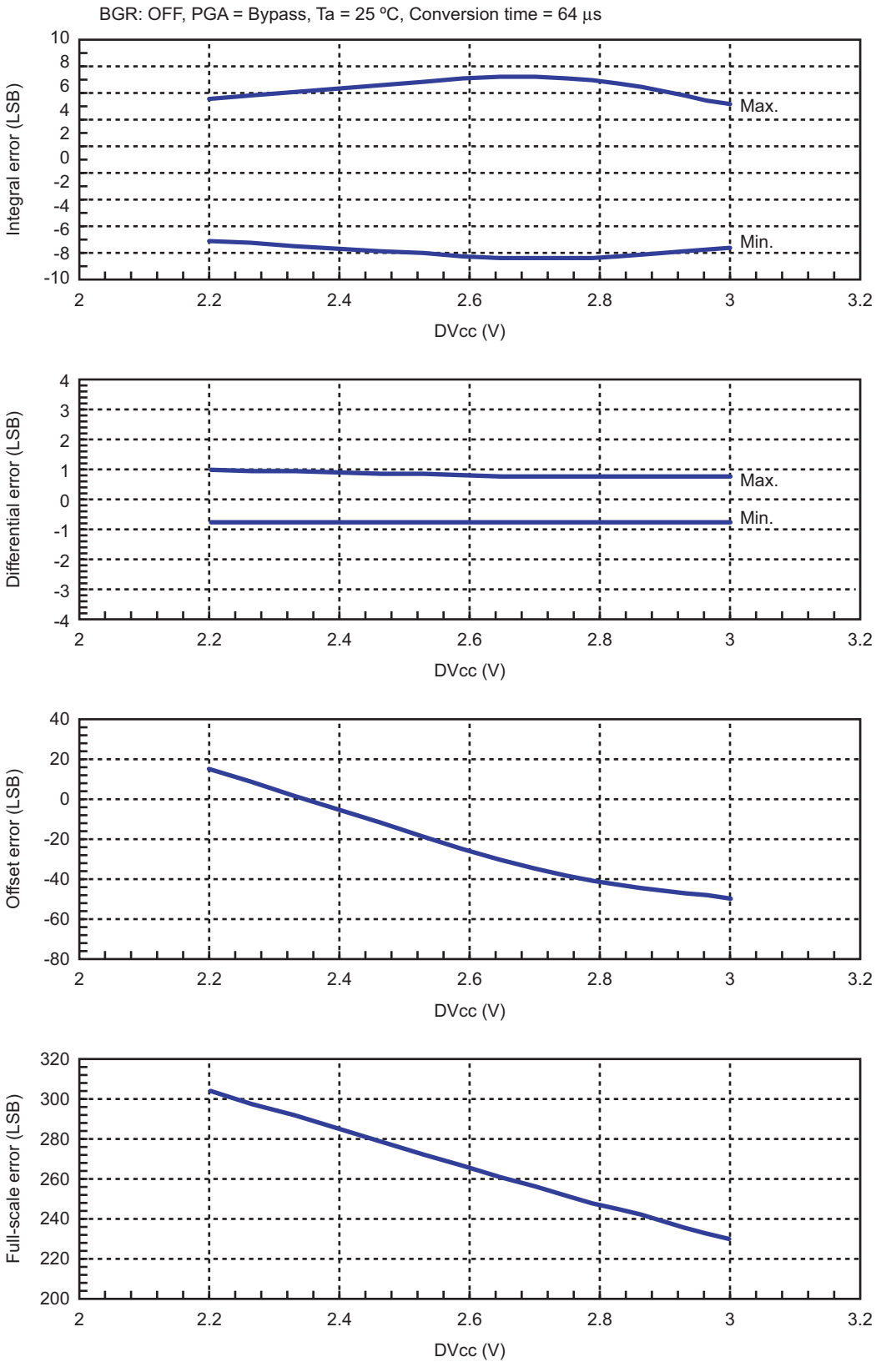


(3) Dependences on DVcc

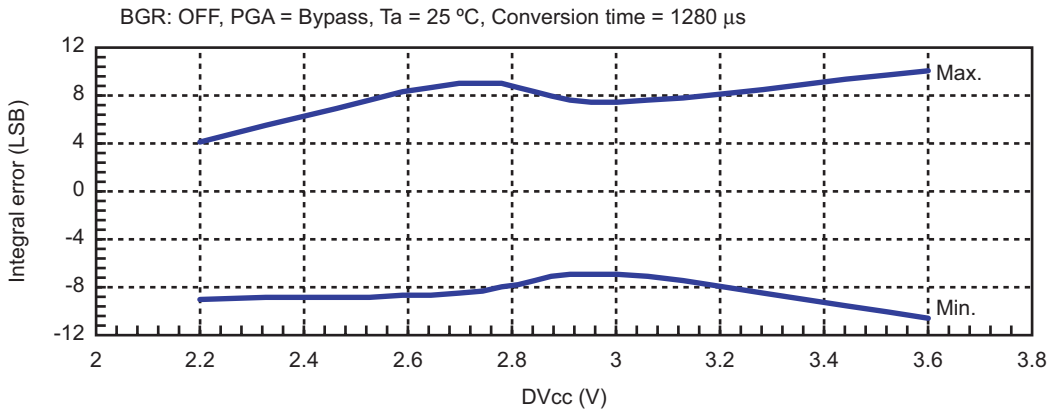
- DVcc dependence 1

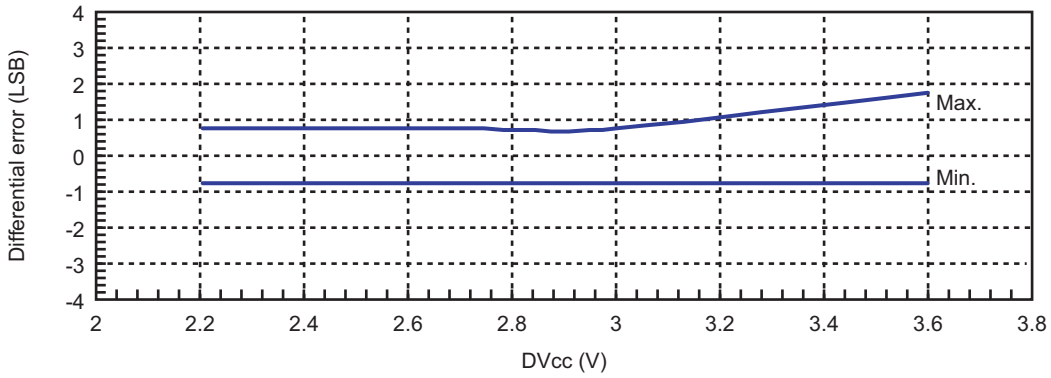


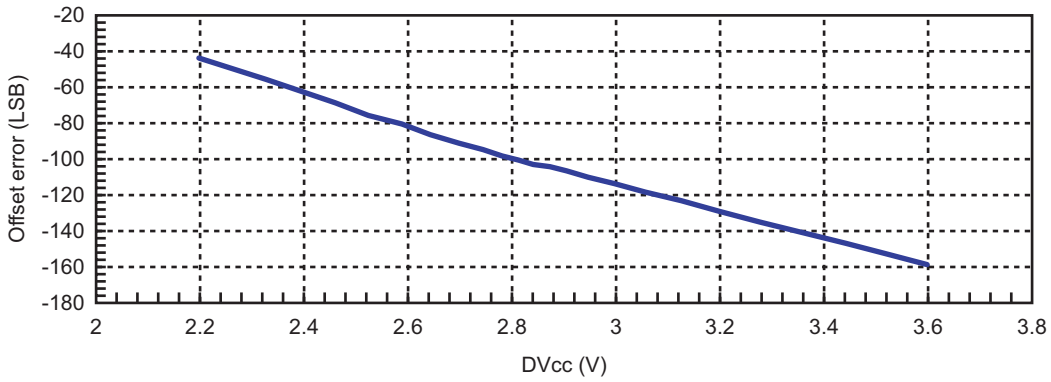
- DVcc dependence 2

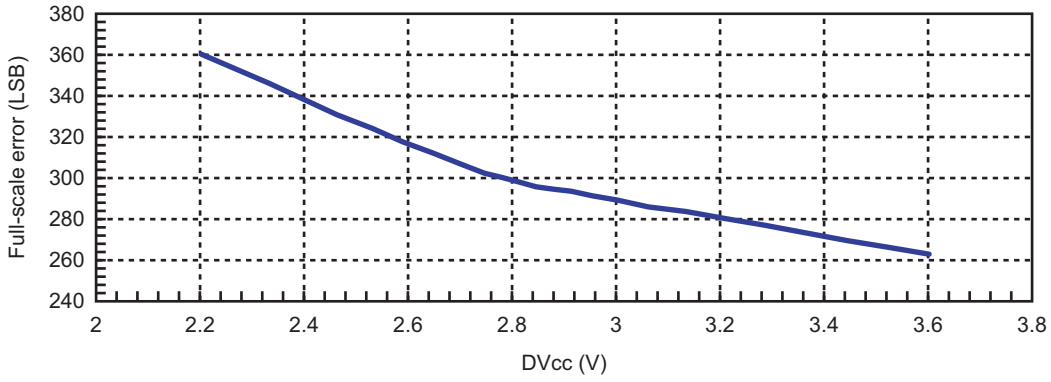


- DVcc dependence 3

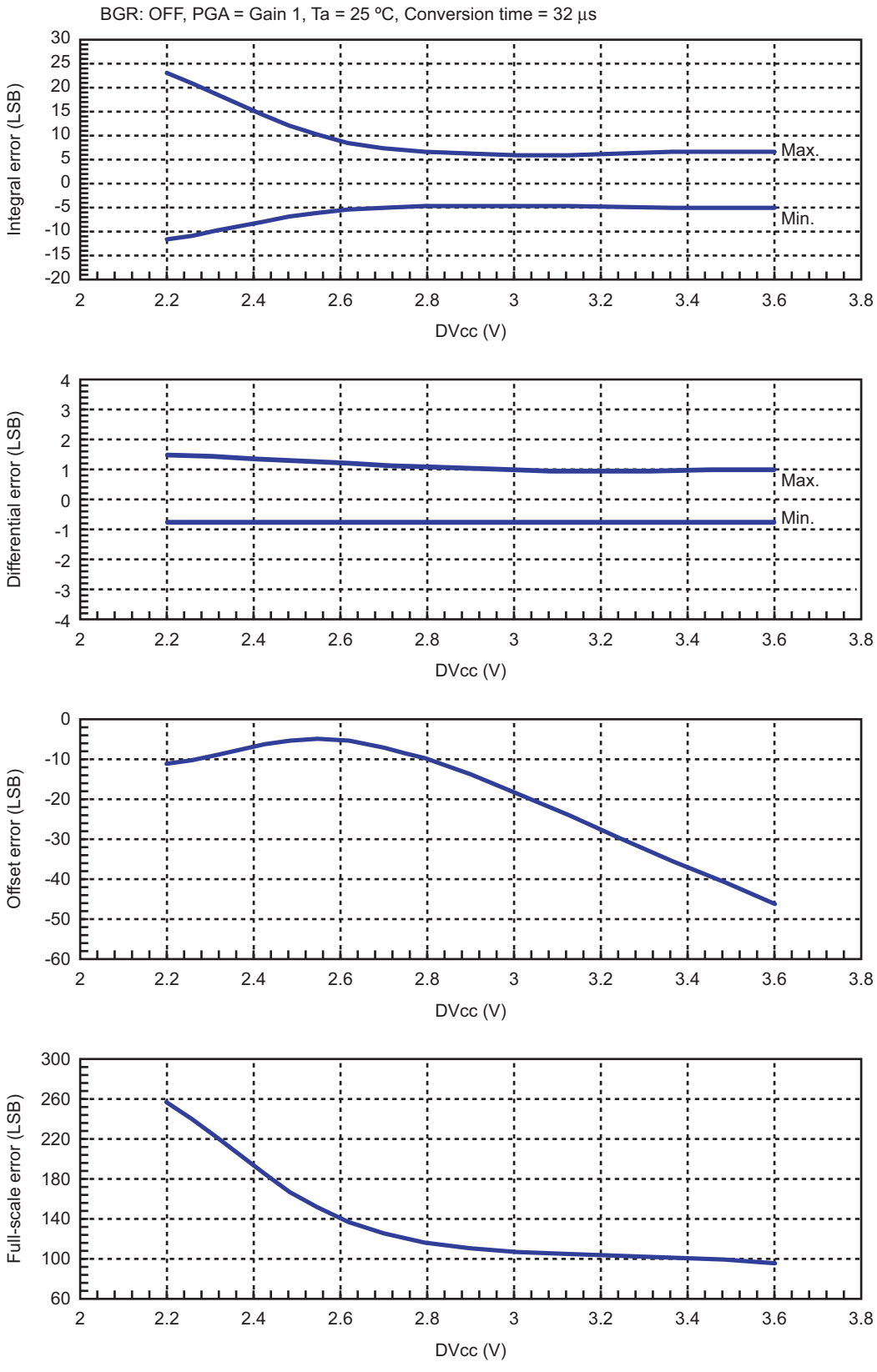




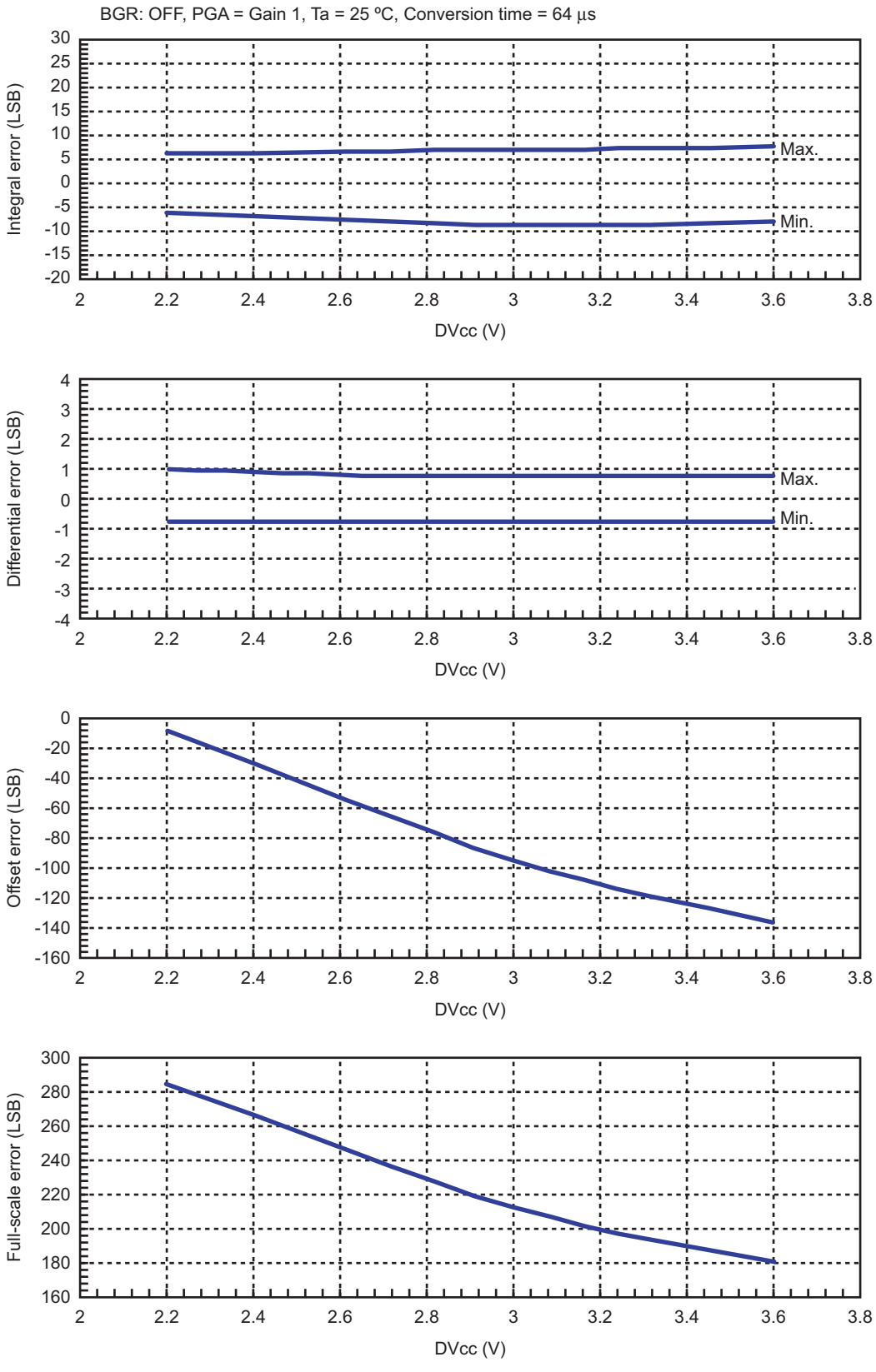




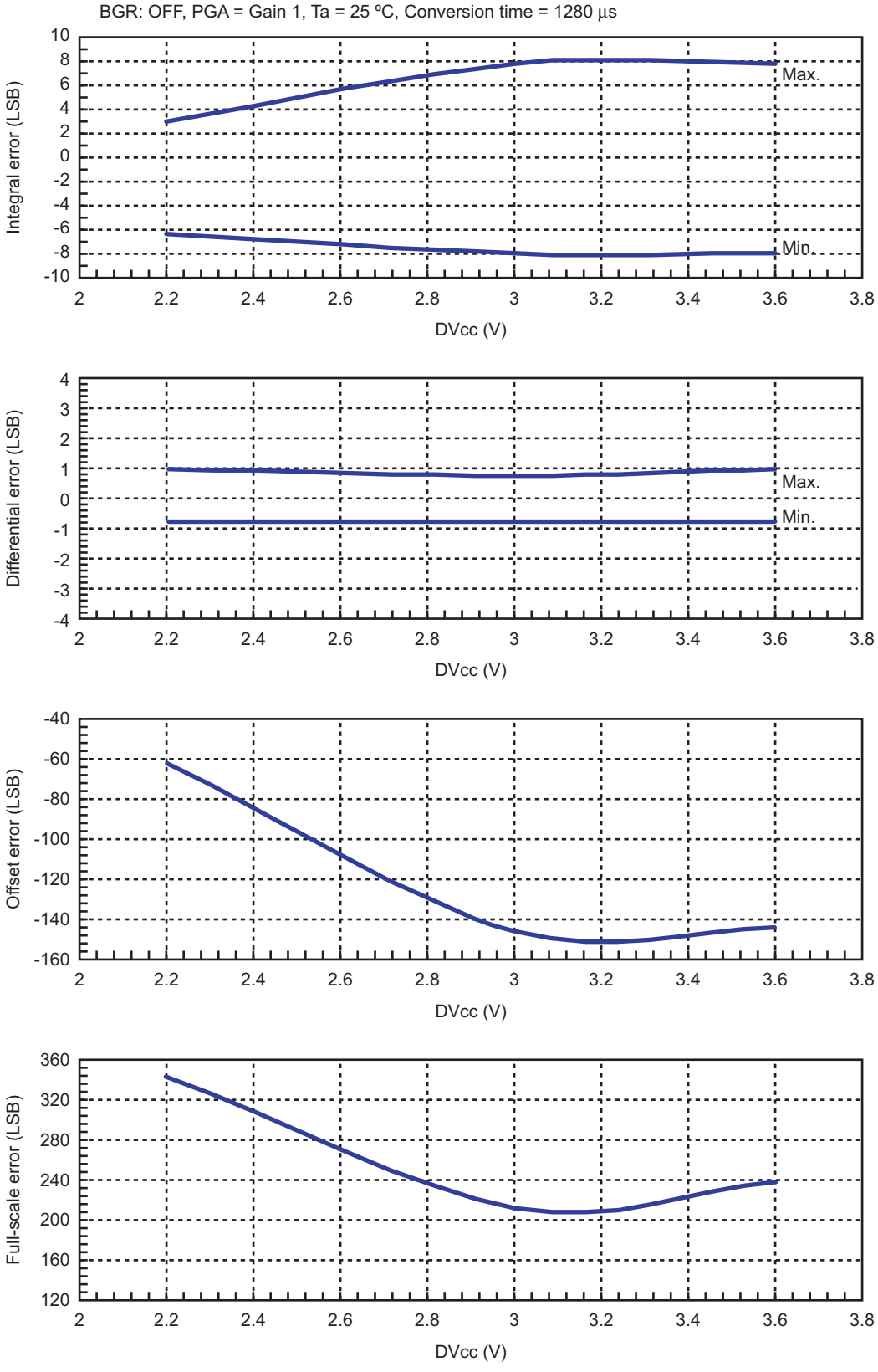
- DVcc dependence 4



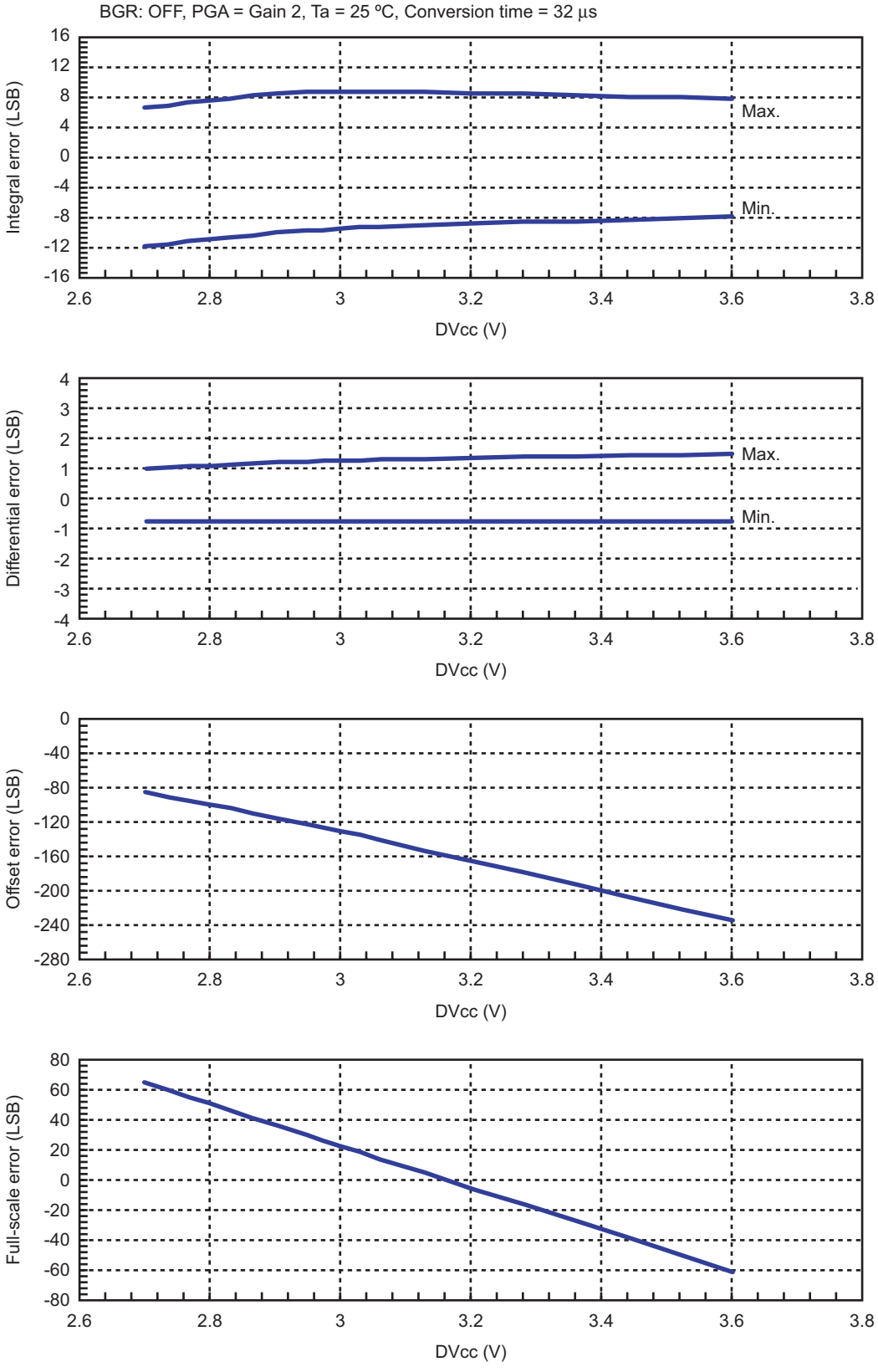
- DVcc dependence 5



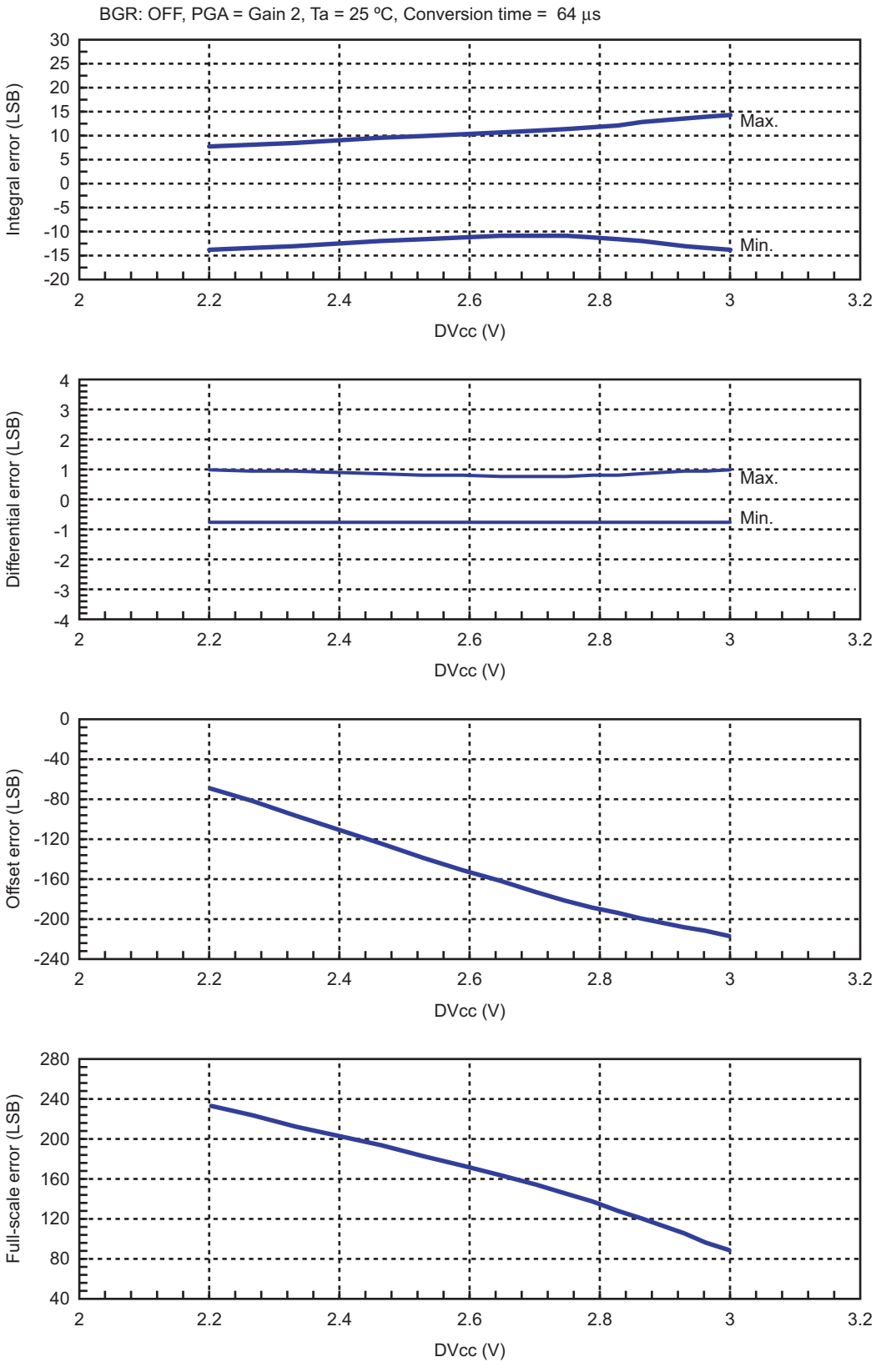
- DVcc dependence 6



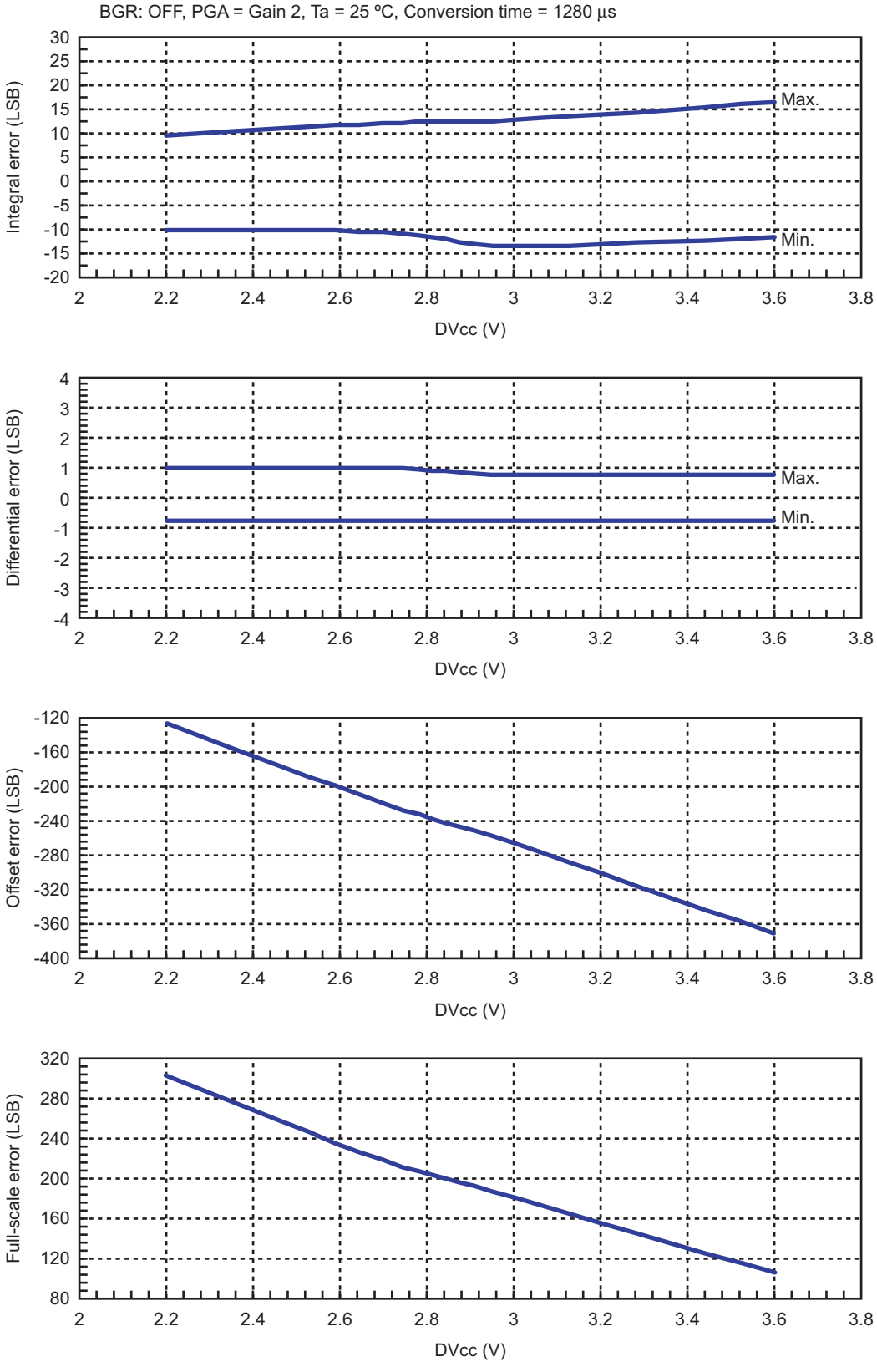
- DVcc dependence 7



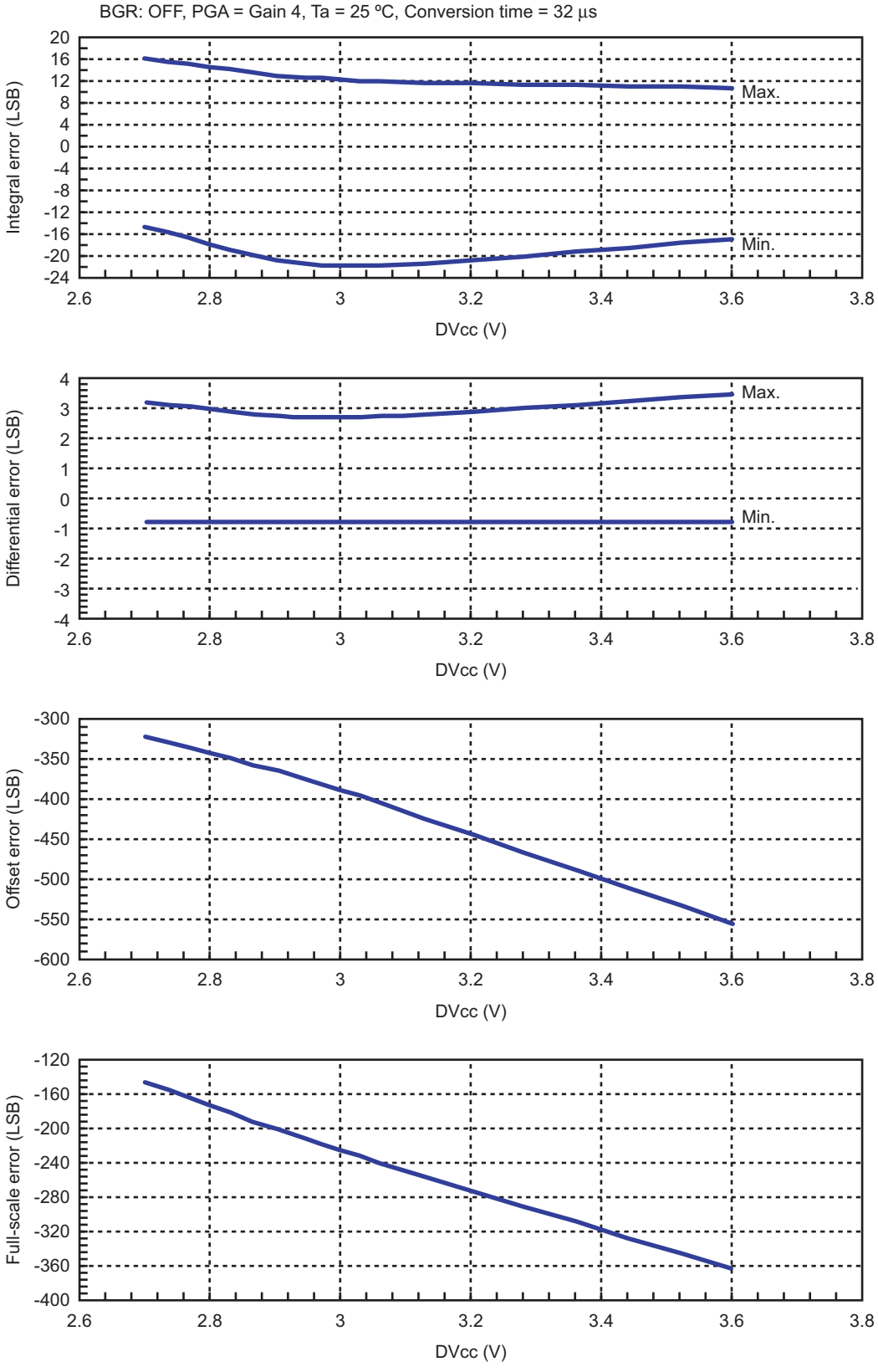
- DVcc dependence 8



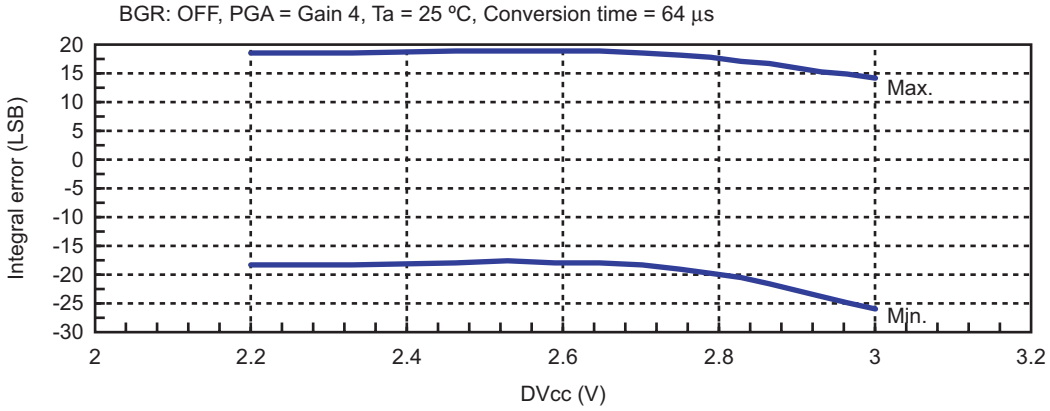
- DVcc dependence 9

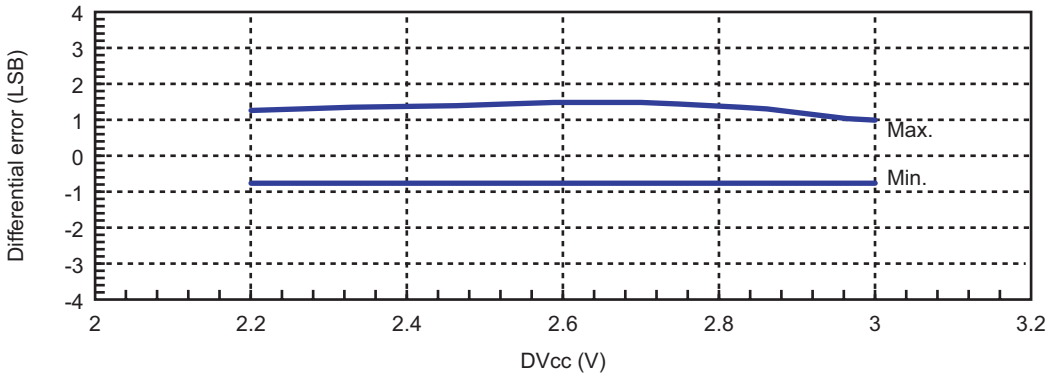


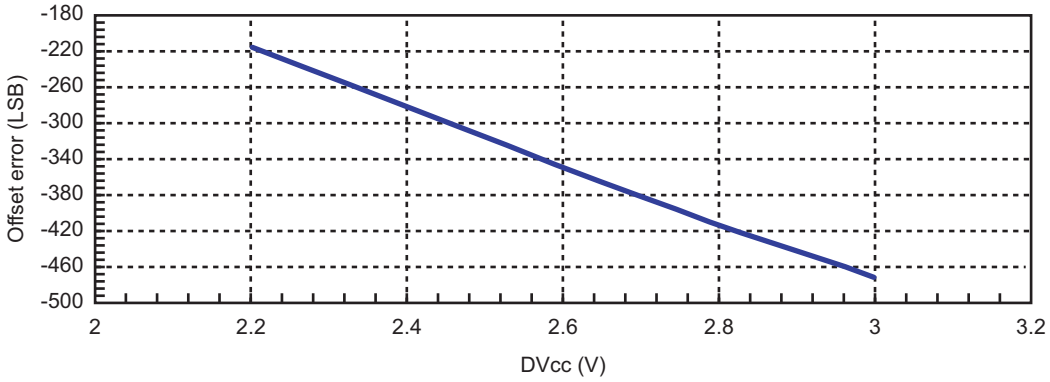
- DVcc dependence 10

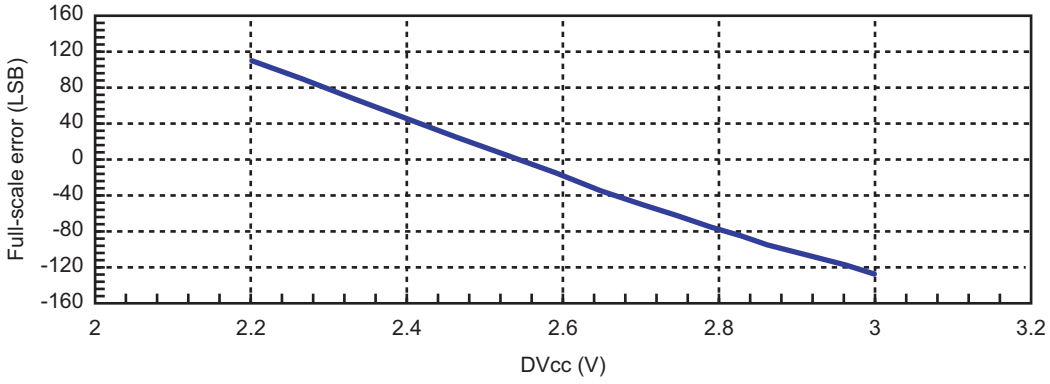


- DVcc dependence 11

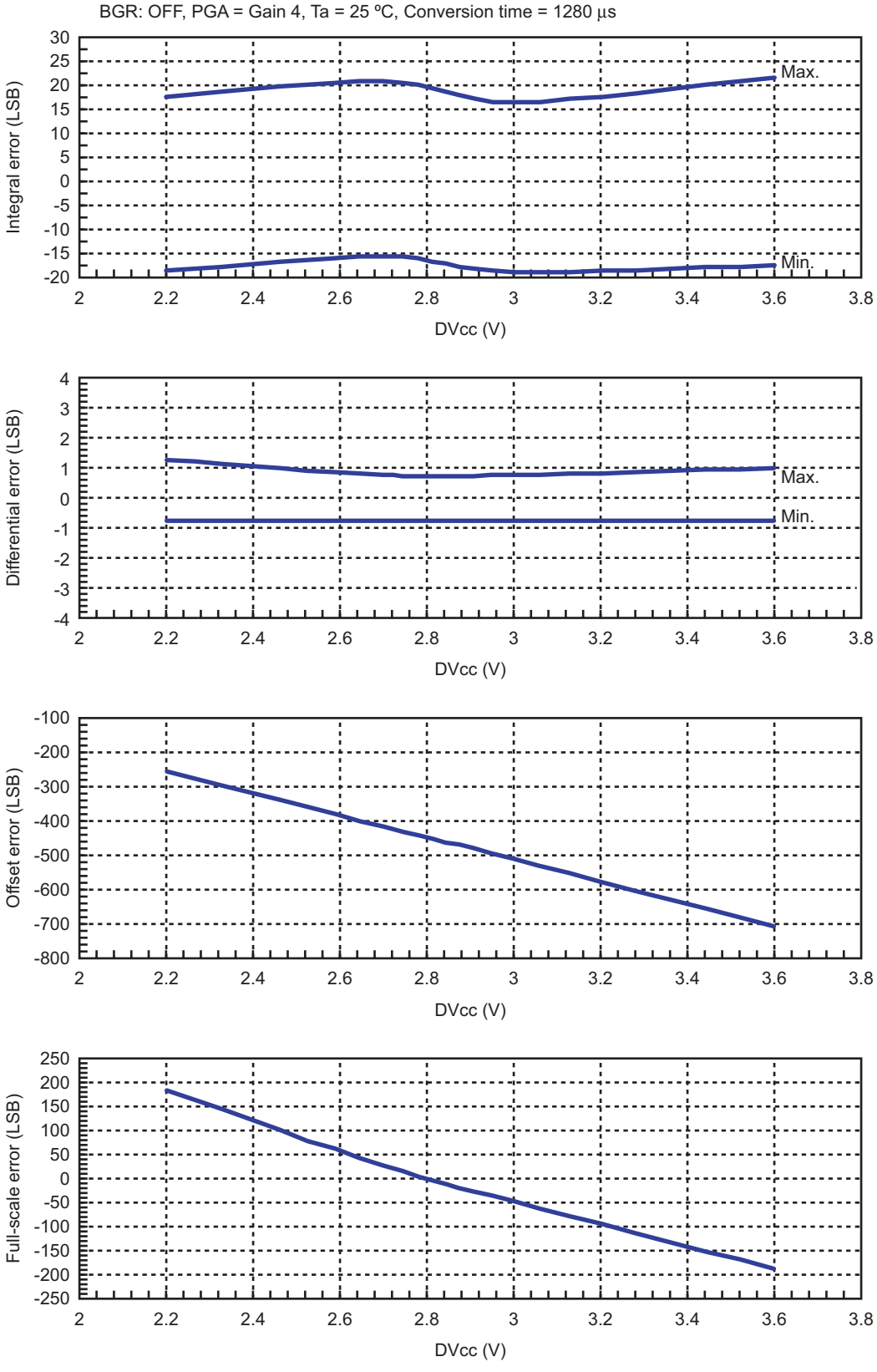




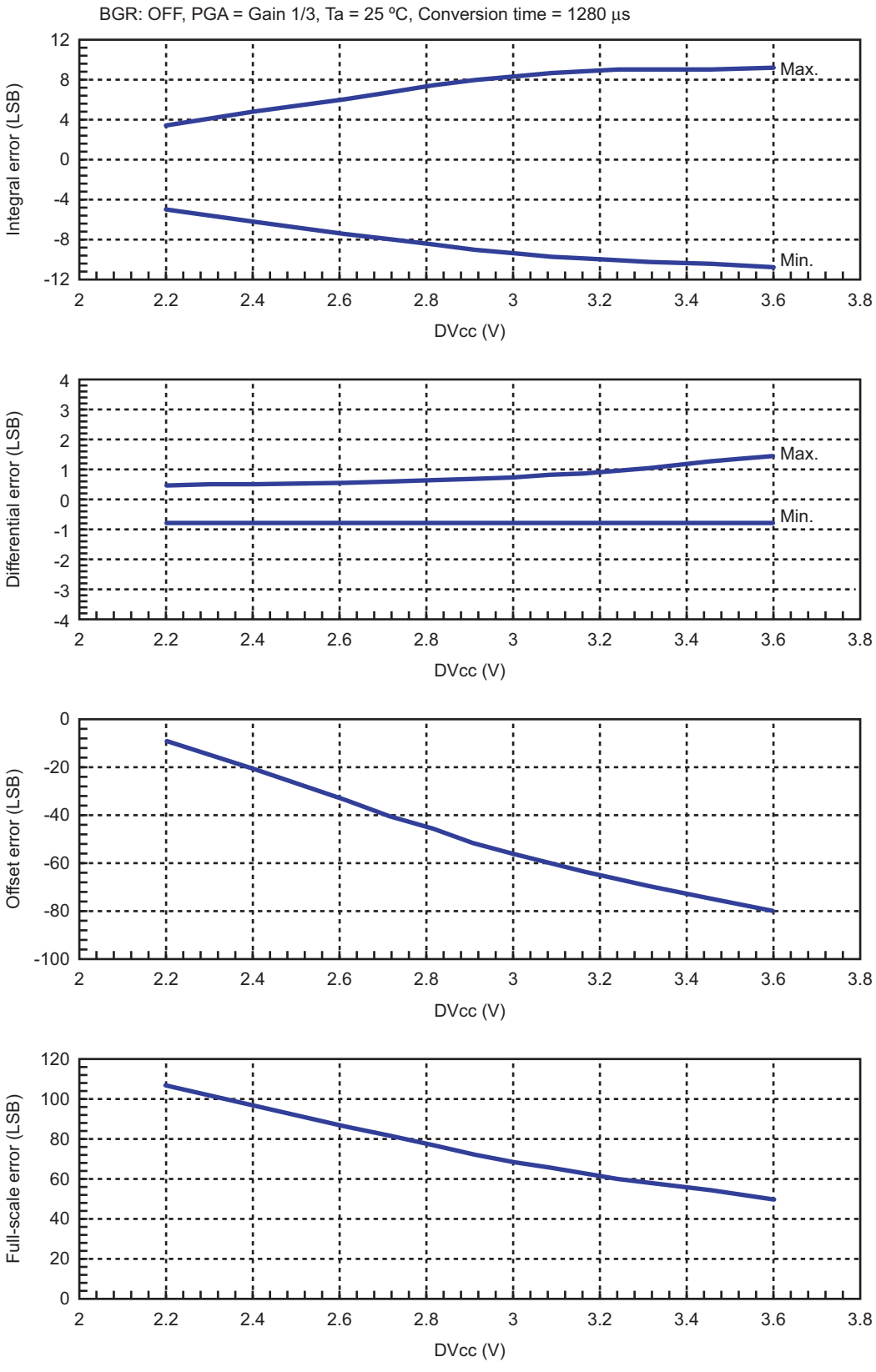




- DVcc dependence 12

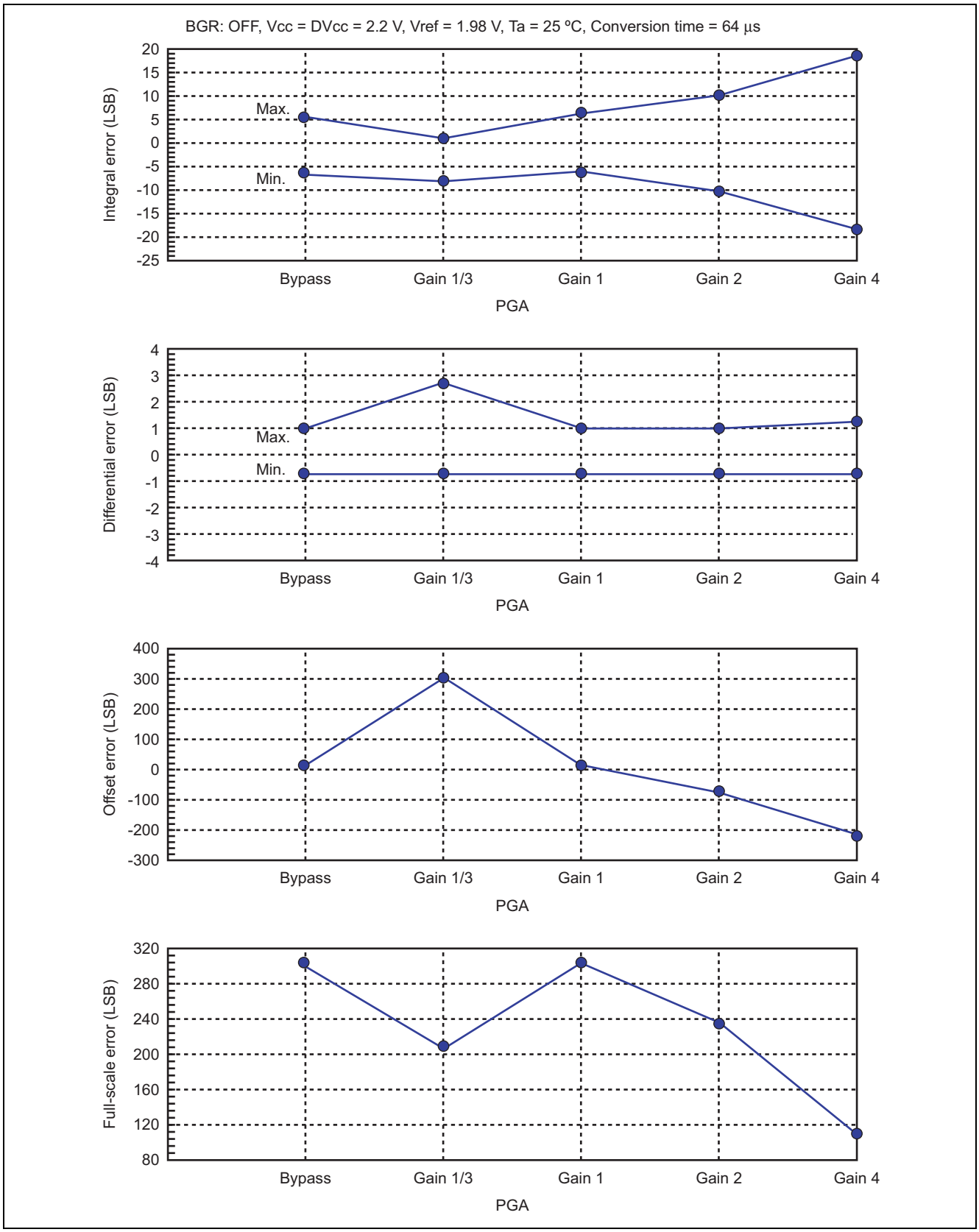


- DVcc dependence 13

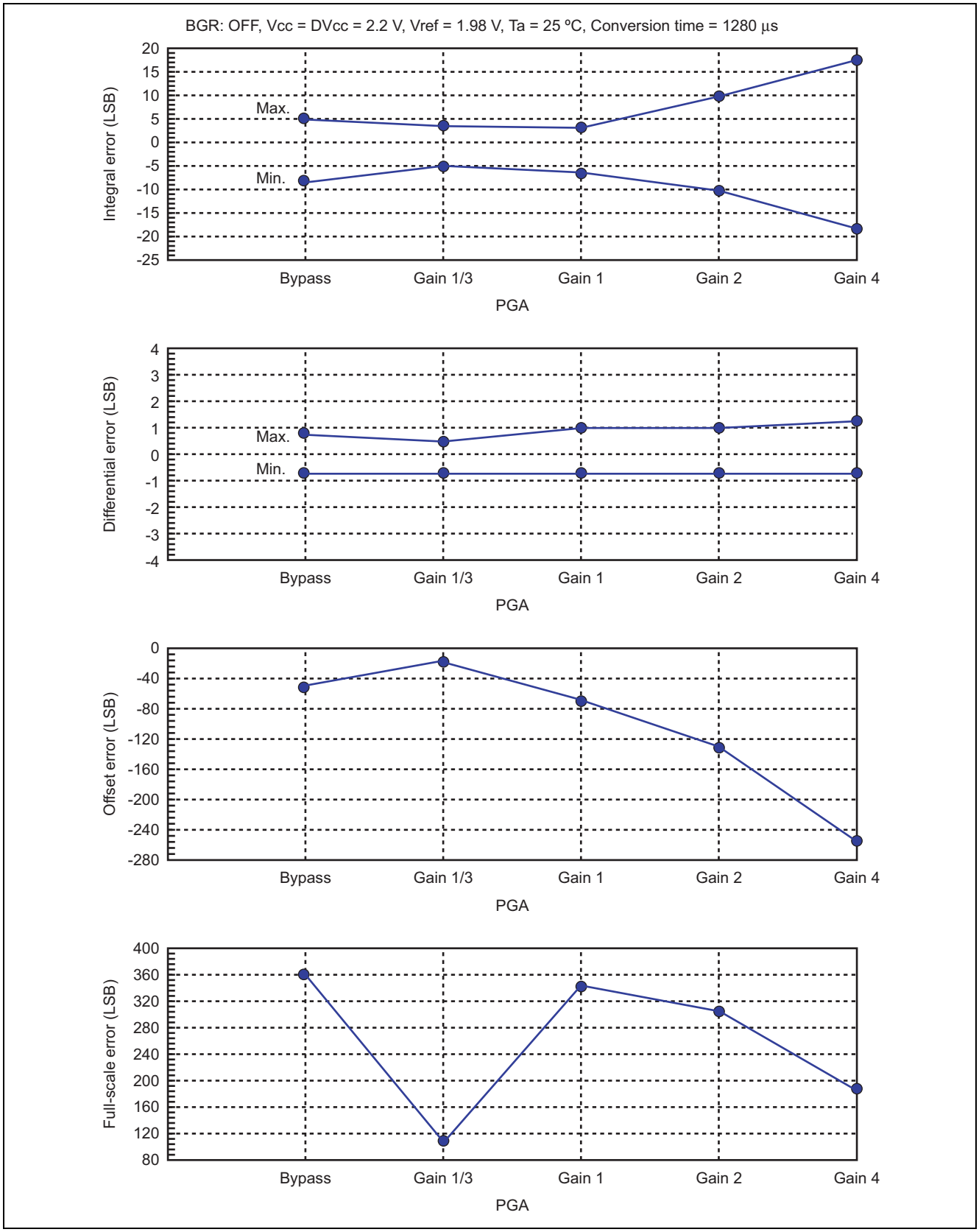


(4) Dependences on PGA Setting

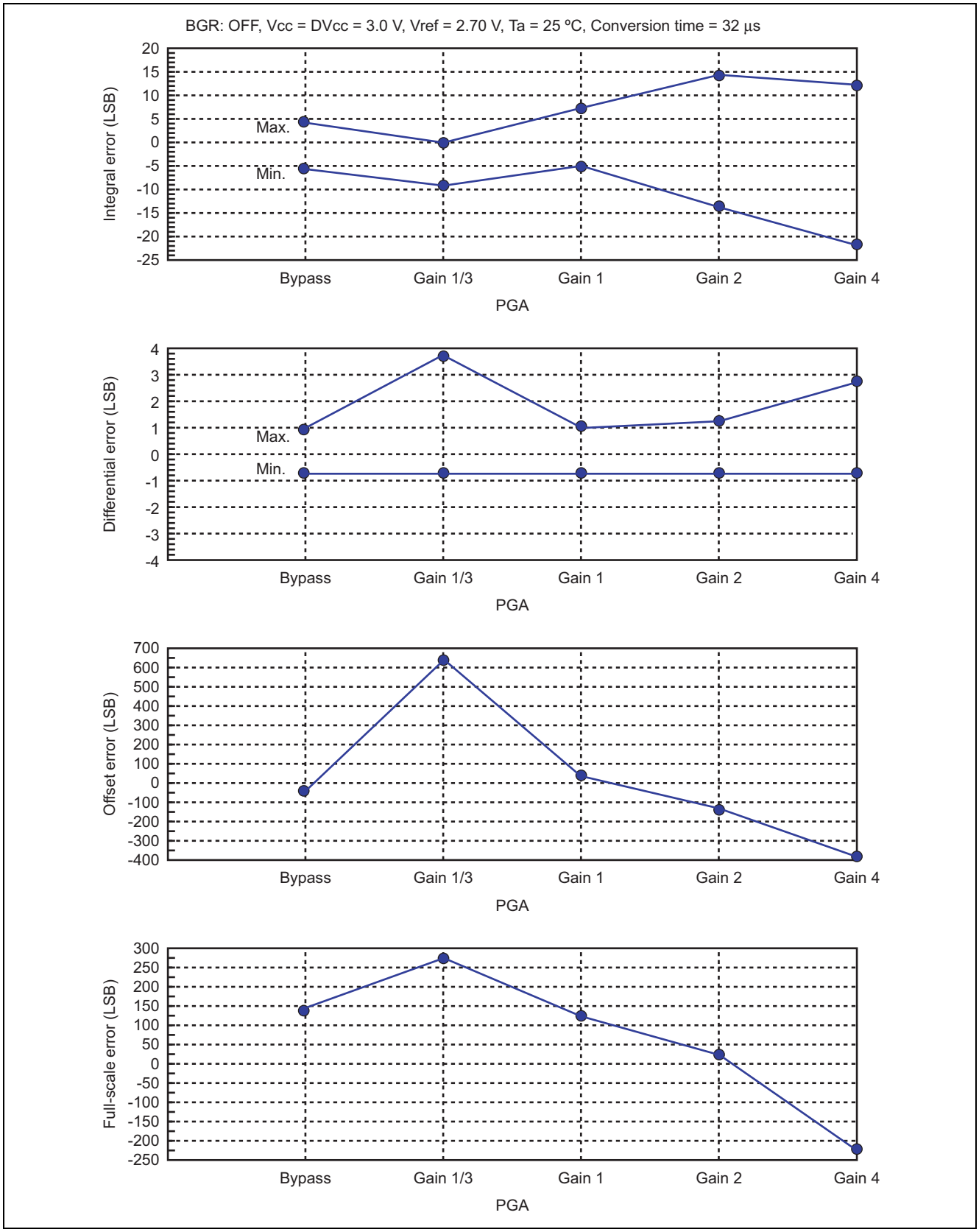
- PGA dependence 1



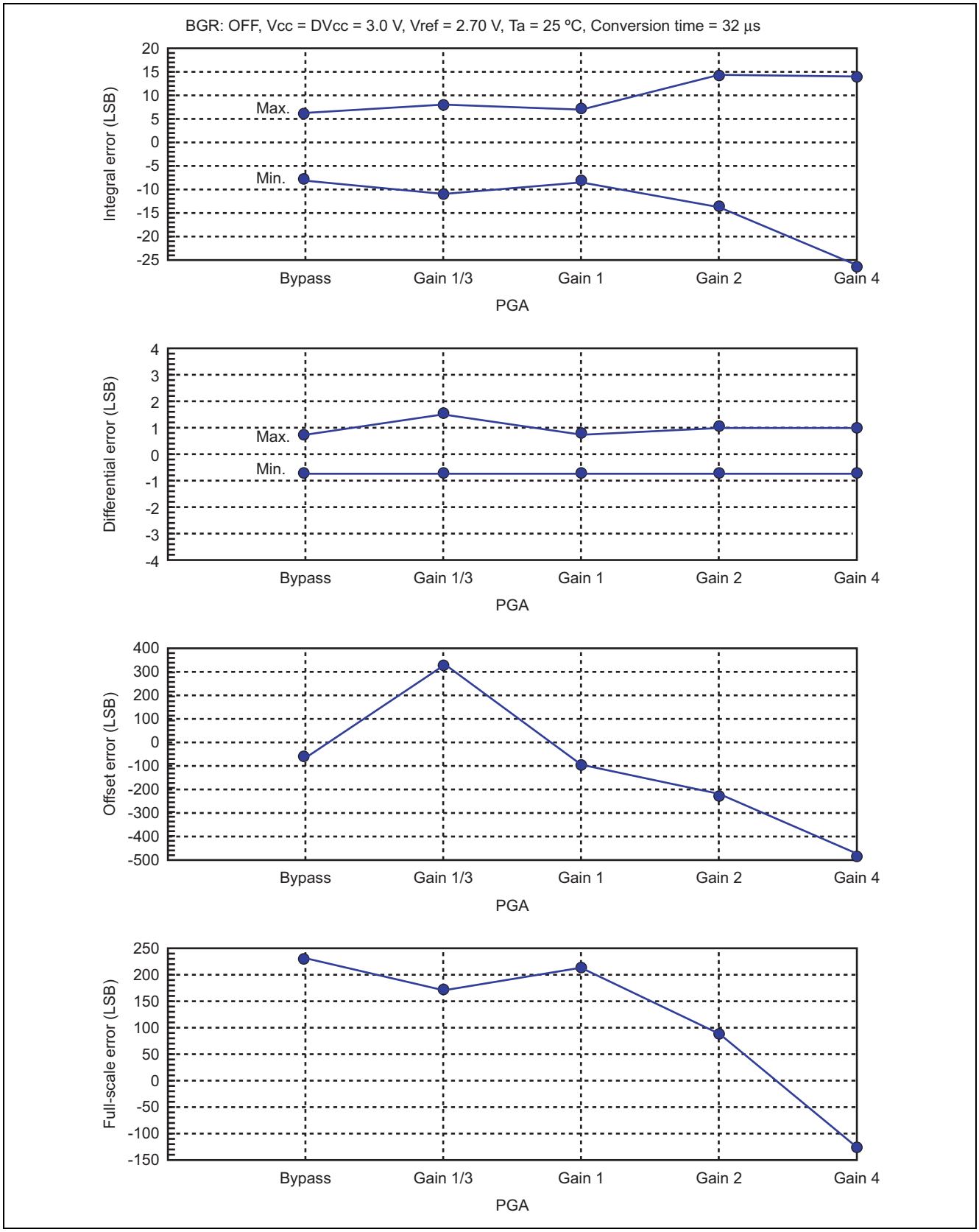
- PGA dependence 2



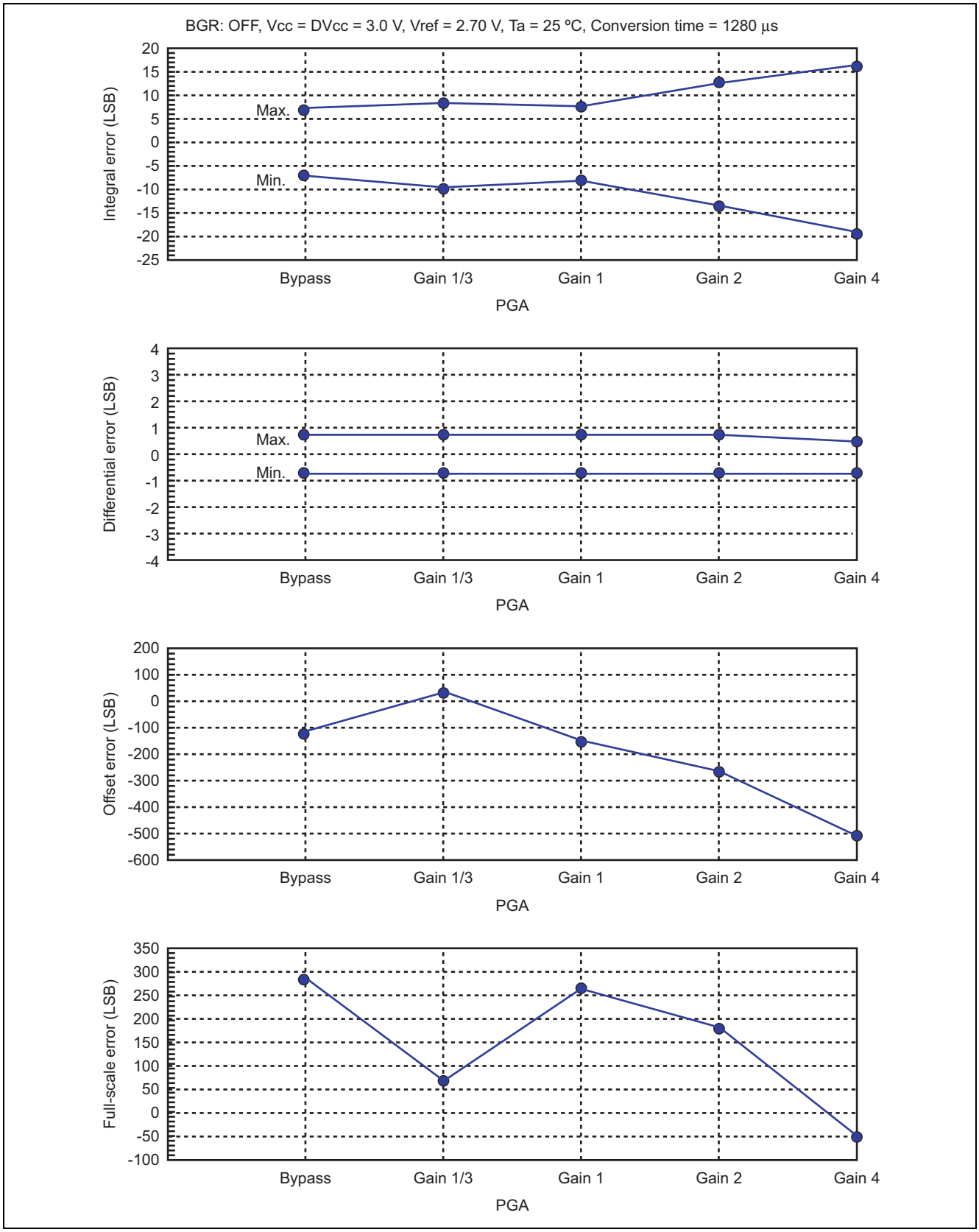
- PGA dependence 3



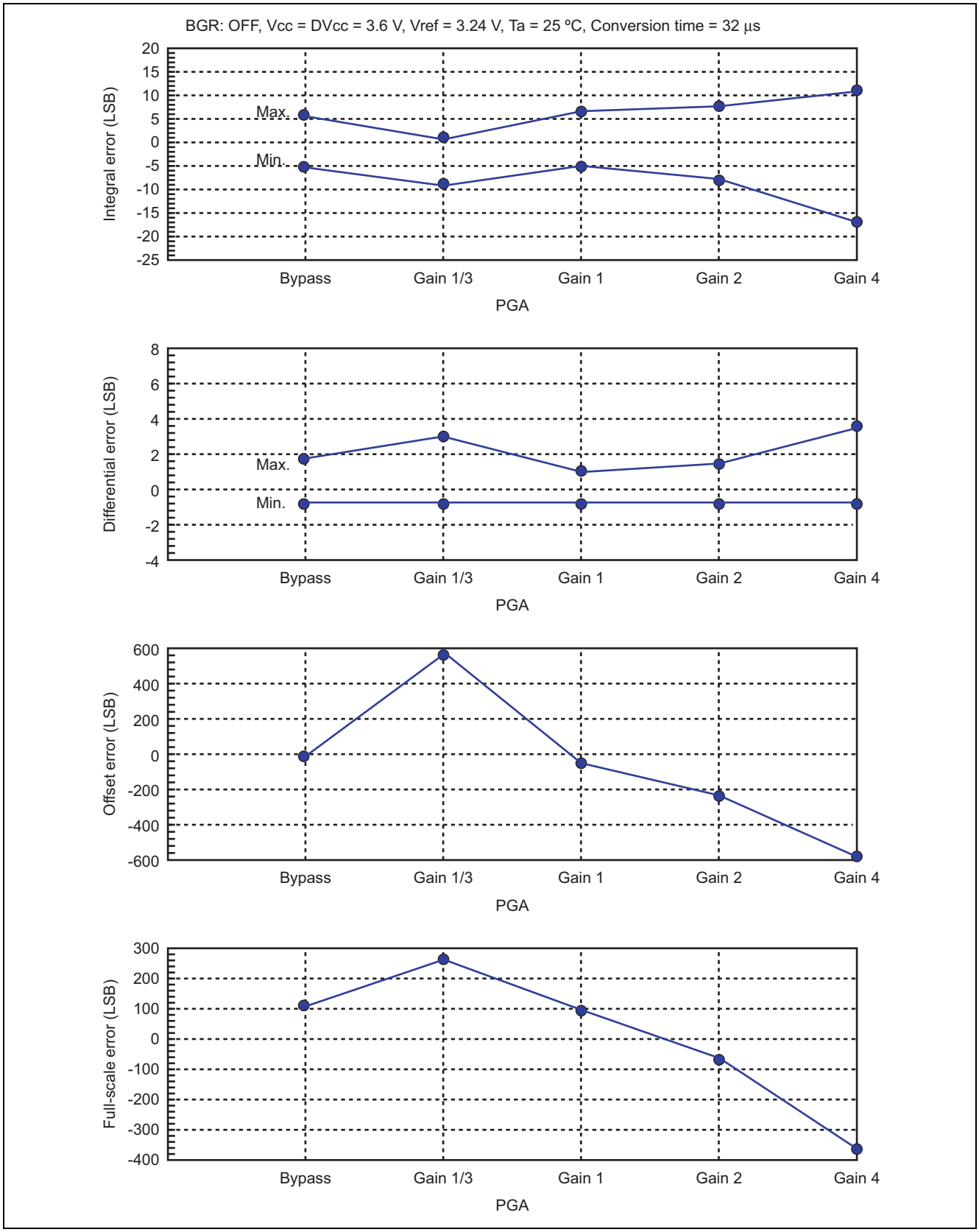
- PGA dependence 4



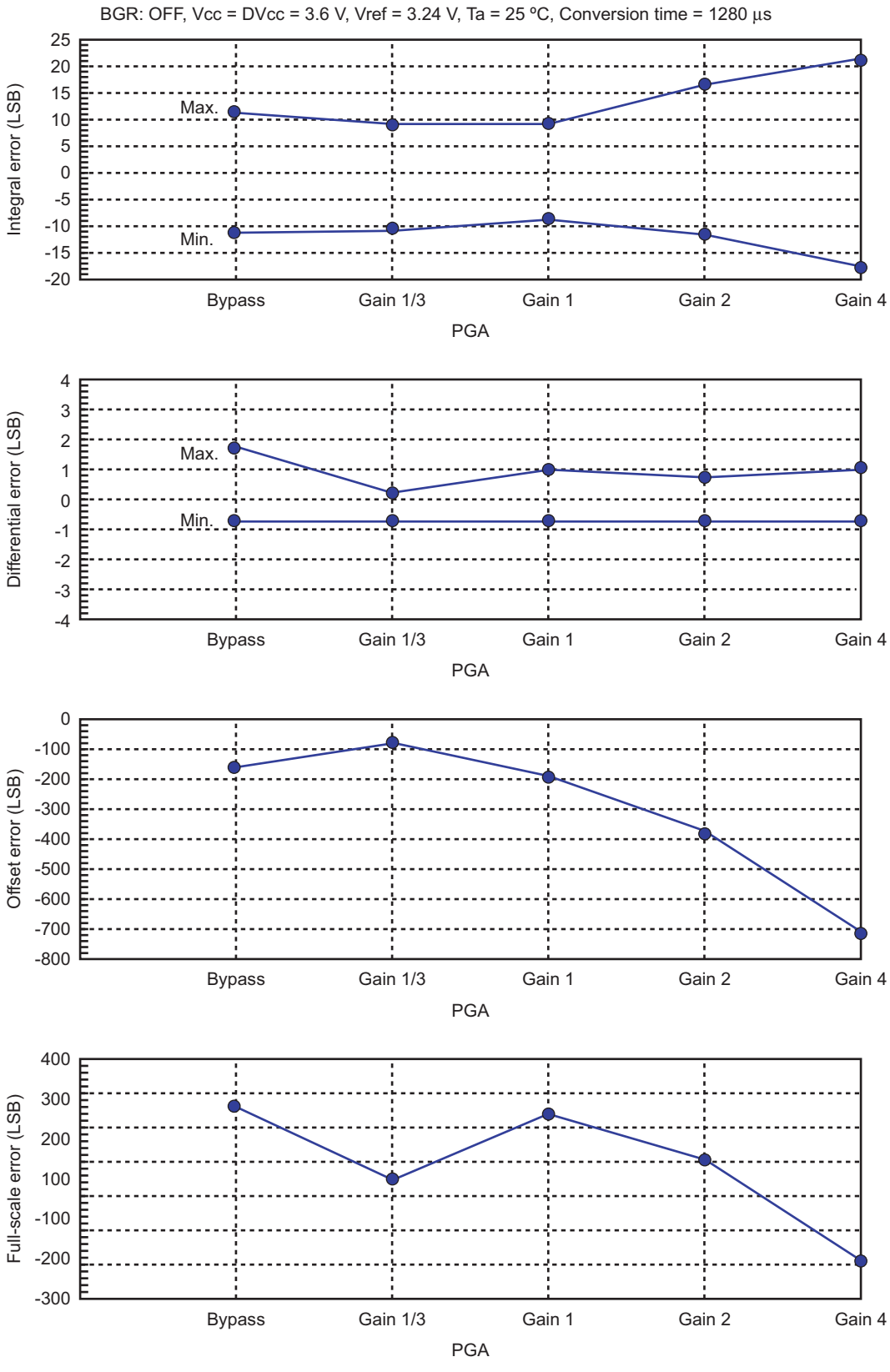
- PGA dependence 5



- PGA dependence 6



- PGA dependence 7



7.1.2 Mask ROM Version

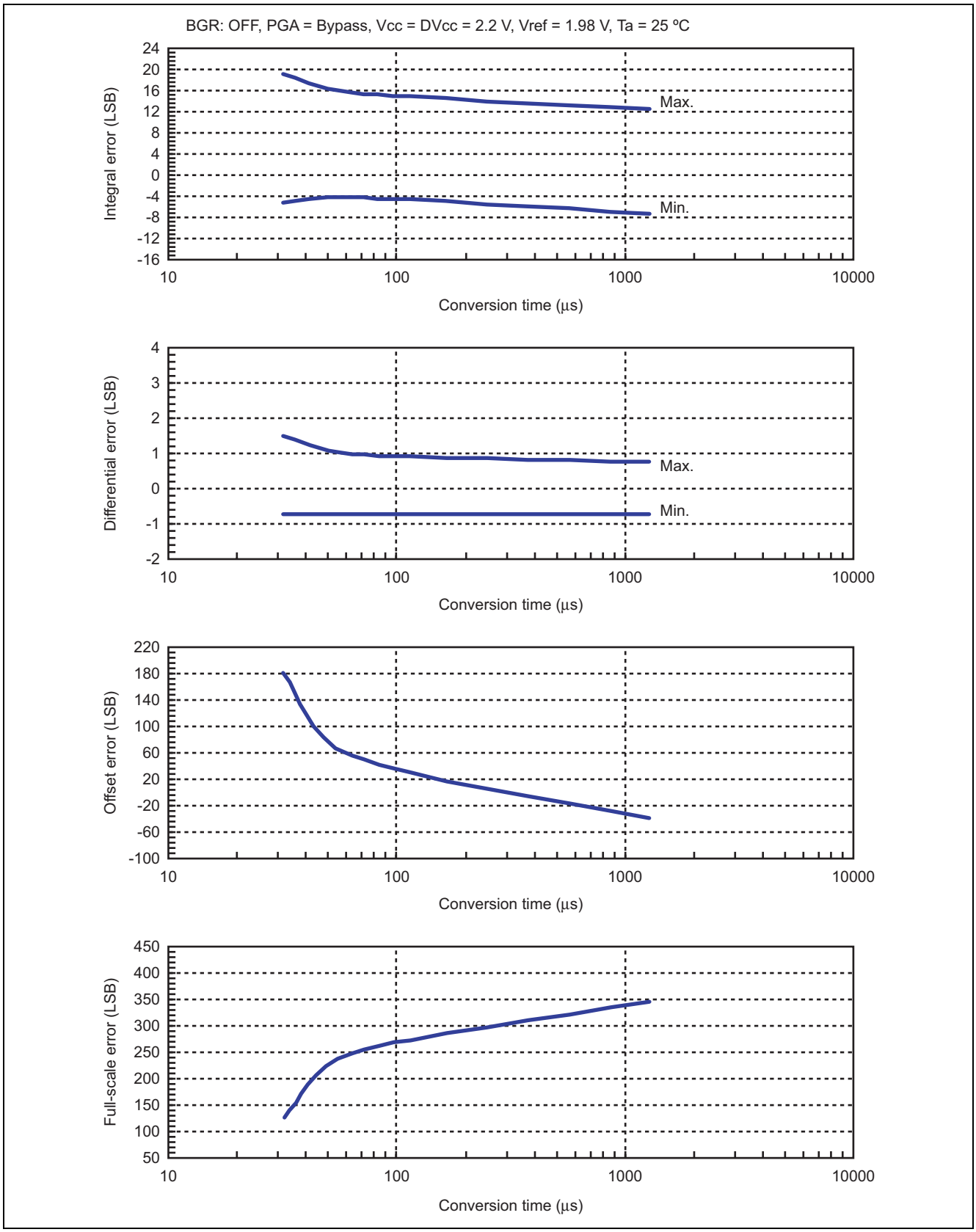
Graphs of the dependences of the integral error, differential error, offset error and full-scale error on the parameters listed in the table below are given after the table.

Table 7.2 Conditions in Parameter-Dependence Measurement (MASK ROM Version)

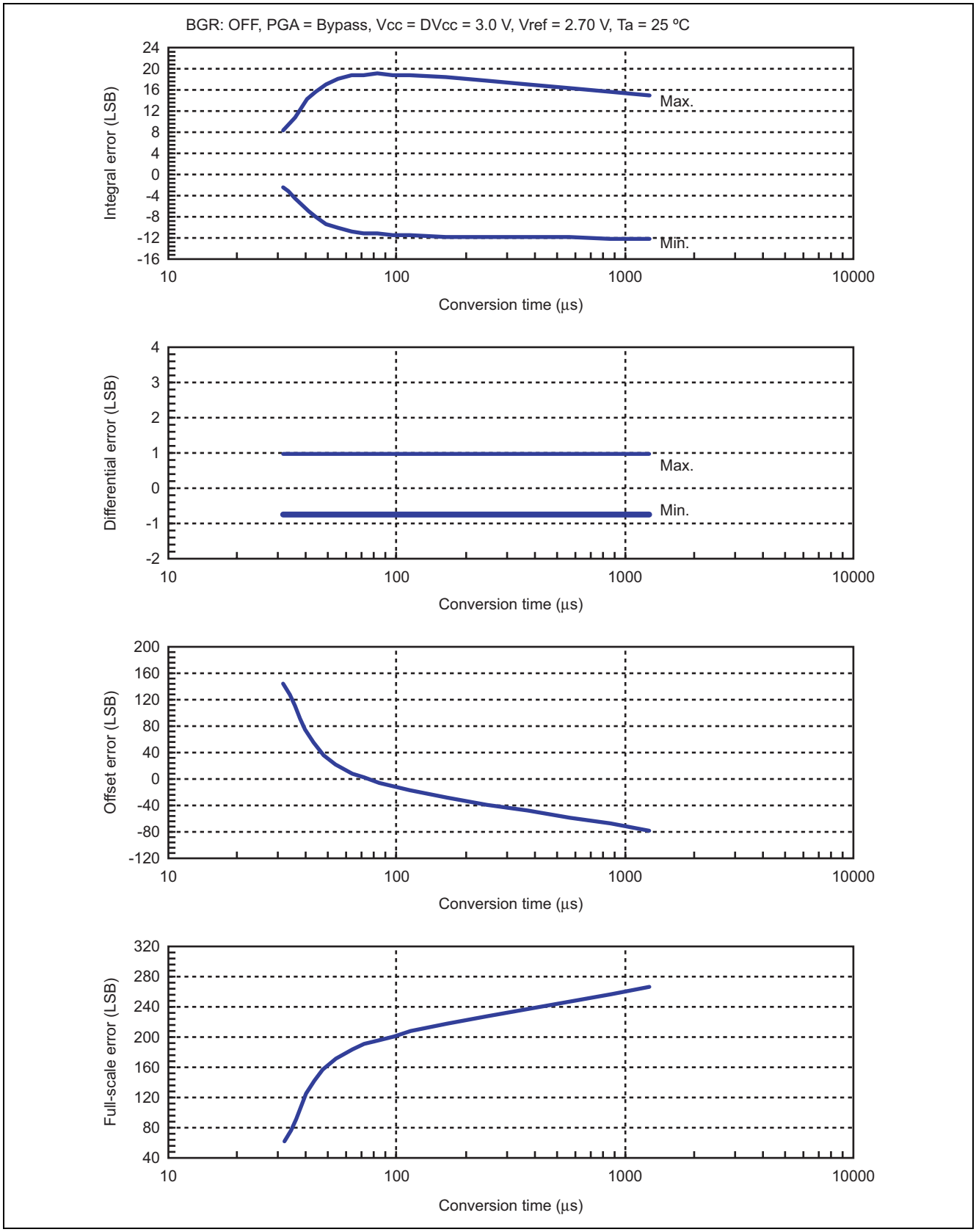
	Measurement Conditions						
Graph Name	**BGR**	**Vcc (V)**	**DVcc (V)**	**Vref (V)**	**Ta (°C)**	**PGA**	**Conversion Time (µs)**
Conversion time dependence 1	OFF	2.2	2.2	1.98	25	Bypassed	—
Conversion time dependence 2	OFF	3.0	3.0	2.70	25	Bypassed	—
Conversion time dependence 3	OFF	2.2	2.2	1.98	25	1	—
Conversion time dependence 4	OFF	3.0	3.0	2.70	25	1	—
Conversion time dependence 5	OFF	3.6	3.6	3.24	25	1	—
Conversion time dependence 6	OFF	2.2	2.2	1.98	25	2	—
Conversion time dependence 7	OFF	3.0	3.0	2.70	25	2	—
Conversion time dependence 8	OFF	2.2	2.2	1.98	25	4	—
Conversion time dependence 9	OFF	3.0	3.0	2.70	25	4	—
Conversion time dependence 10	OFF	2.2	2.2	1.98	25	1/3	—
Conversion time dependence 11	OFF	3.0	3.0	2.70	25	1/3	—
Conversion time dependence 12	ON	2.2	2.2	—	25	Bypassed	—
Conversion time dependence 13	ON	3.0	3.0	—	25	Bypassed	—
Conversion time dependence 14	ON	2.2	2.2	—	25	1	—
Conversion time dependence 15	ON	3.0	3.0	—	25	1	—
Conversion time dependence 16	ON	2.2	2.2	—	25	1/3	—
Conversion time dependence 17	ON	3.0	3.0	—	25	1/3	—
Temperature dependence 1	OFF	2.2	2.2	—	—	Bypassed	64
Temperature dependence 2	OFF	3.0	3.0	—	—	Bypassed	32
Temperature dependence 3	OFF	3.0	3.0	—	—	Bypassed	64
Temperature dependence 4	OFF	2.2	2.2	—	—	1	64
Temperature dependence 5	OFF	3.0	3.0	—	—	1	32
Temperature dependence 6	OFF	3.0	3.0	—	—	1	64
Temperature dependence 7	OFF	3.0	3.0	—	—	2	32
Temperature dependence 8	OFF	3.0	3.0	—	—	2	64
Temperature dependence 9	OFF	3.0	3.0	—	—	4	32
Temperature dependence 10	OFF	3.0	3.0	—	—	4	64
Temperature dependence 11	OFF	3.0	3.0	—	—	1/3	32
Temperature dependence 12	OFF	3.0	3.0	—	—	1/3	64
DVcc dependence 1	OFF	—	—	—	25	Bypassed	64
DVcc dependence 2	OFF	—	—	—	25	1	64
DVcc dependence 3	OFF	—	—	—	25	2	64
DVcc dependence 4	OFF	—	—	—	25	4	64
DVcc dependence 5	OFF	—	—	—	25	1/3	64
DVcc dependence 6	ON	—	—	—	25	Bypassed	64
DVcc dependence 7	ON	—	—	—	25	1	64
DVcc dependence 8	ON	—	—	—	25	1/3	64
PGA dependence 1	OFF	2.2	2.2	1.98	25	—	64
PGA dependence 2	OFF	3.0	3.0	1.98	25	—	32

(1) Conversion Time Dependence

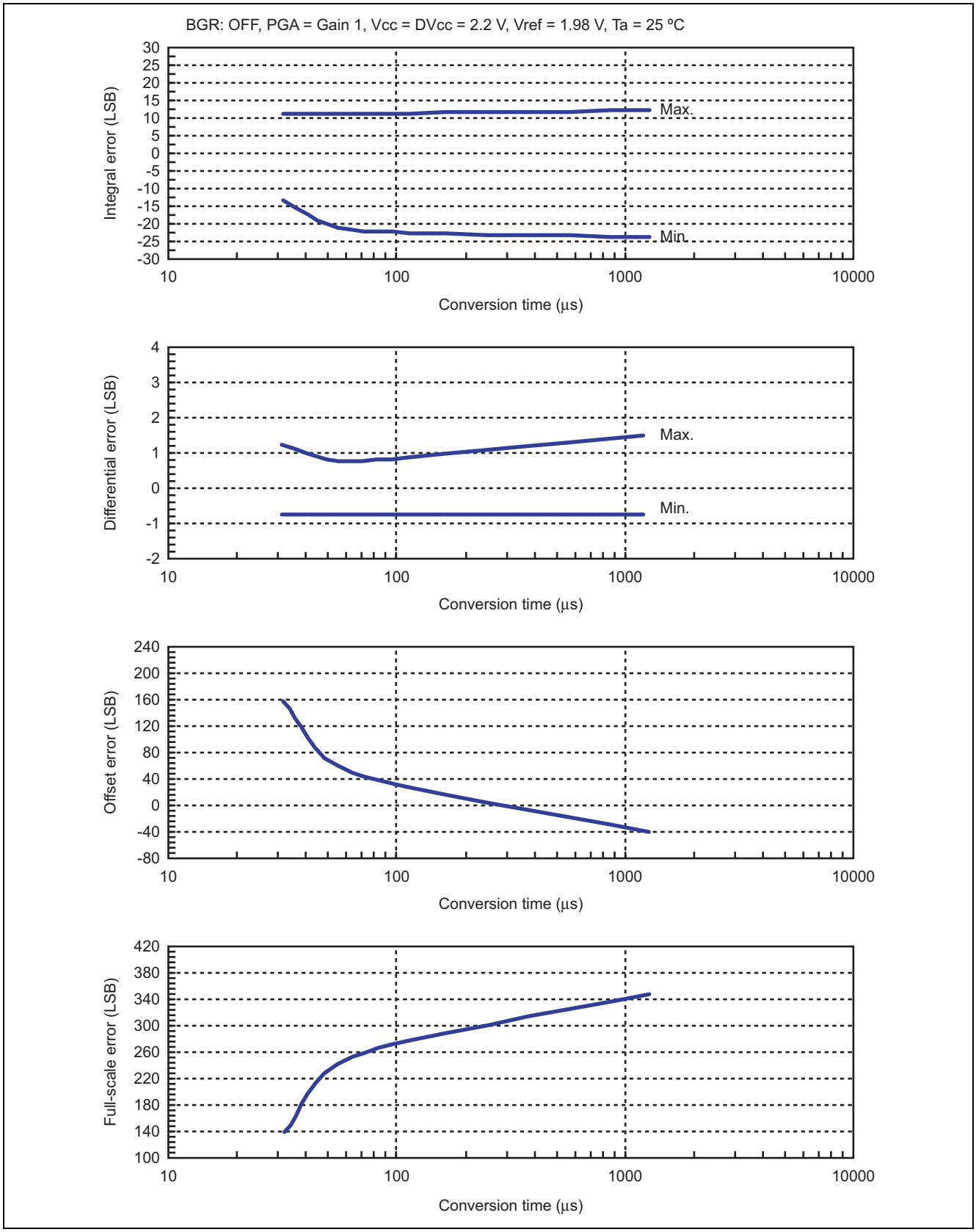
- Conversion time dependence 1



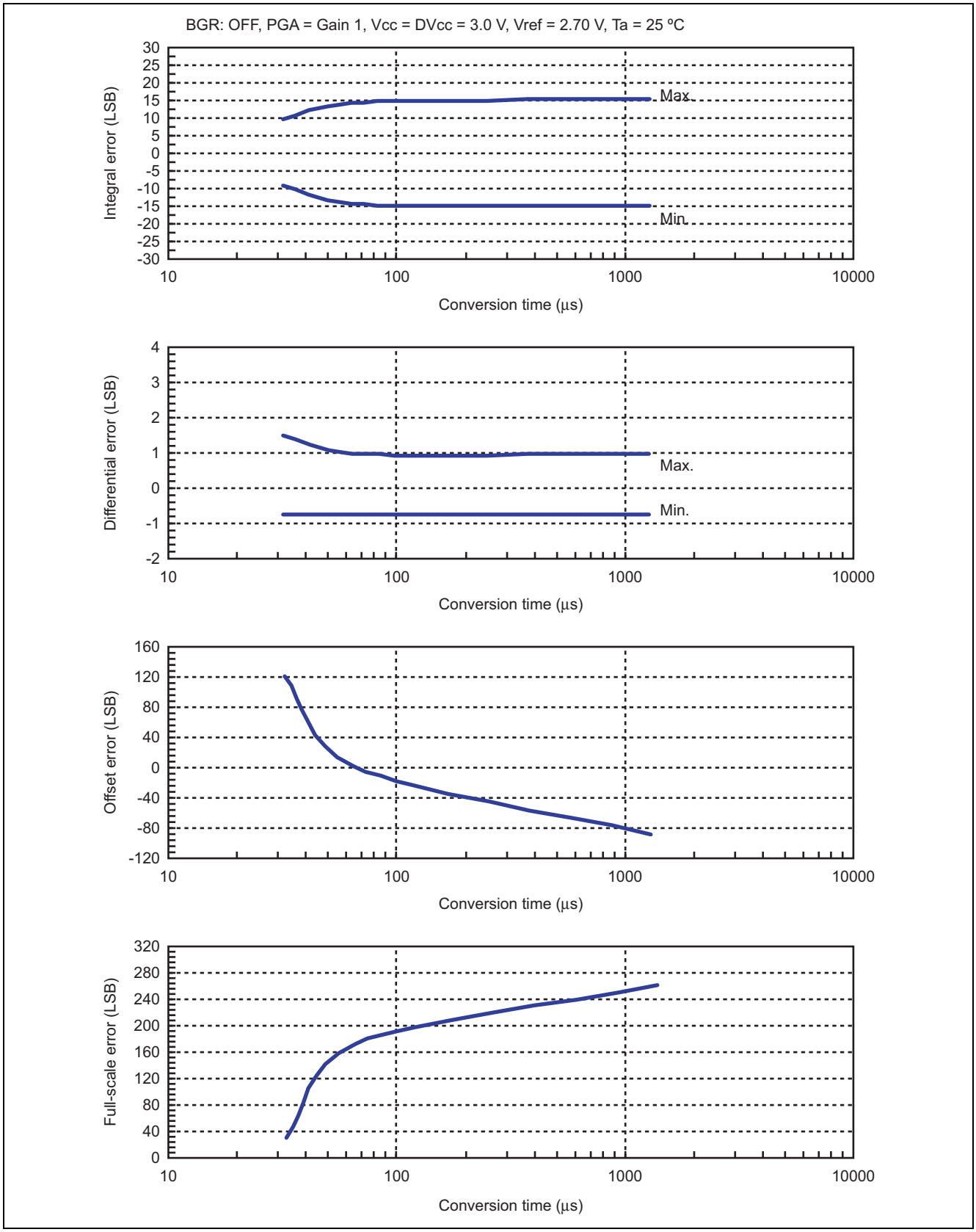
- Conversion time dependence 2



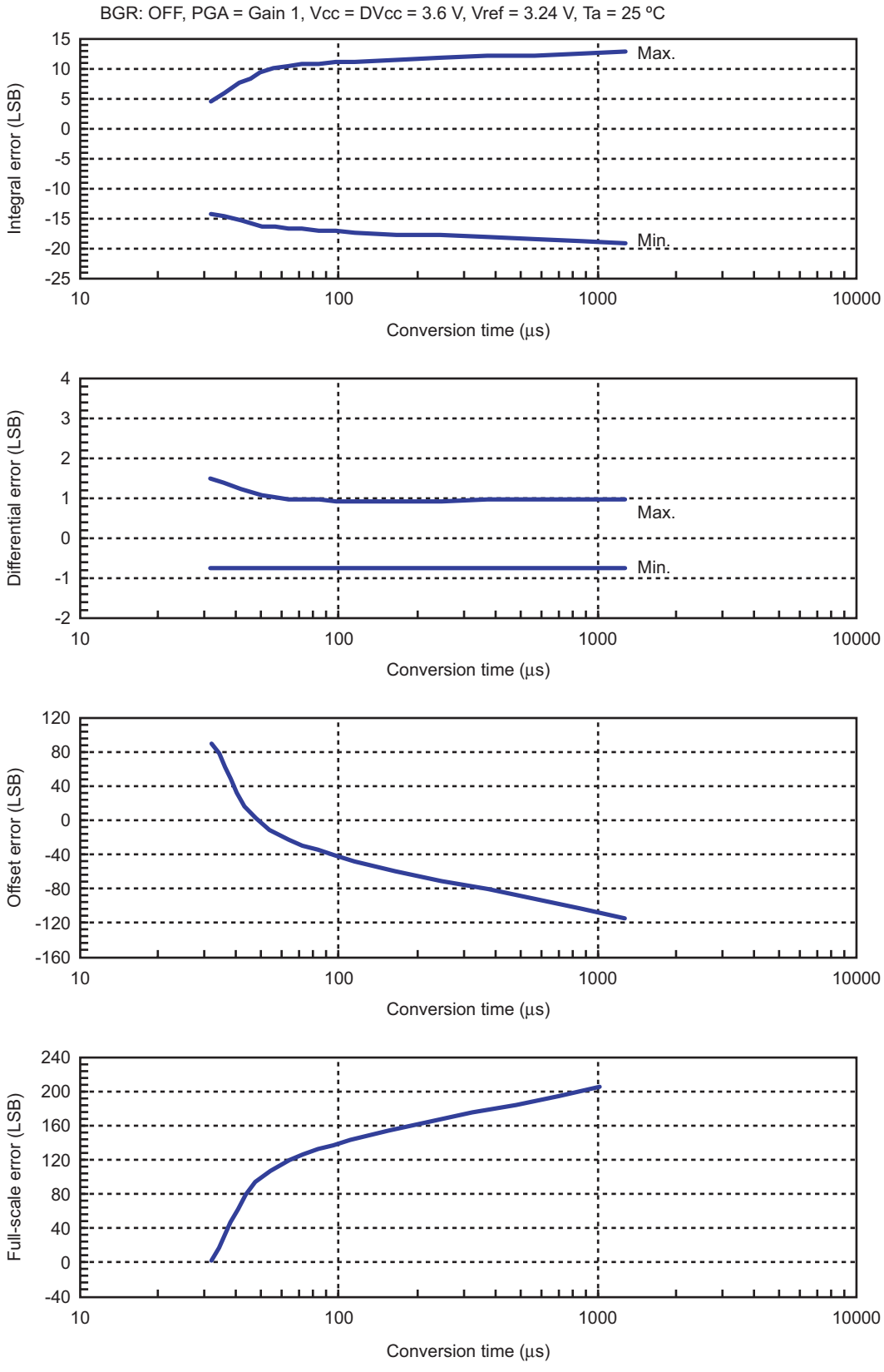
- Conversion time dependence 3



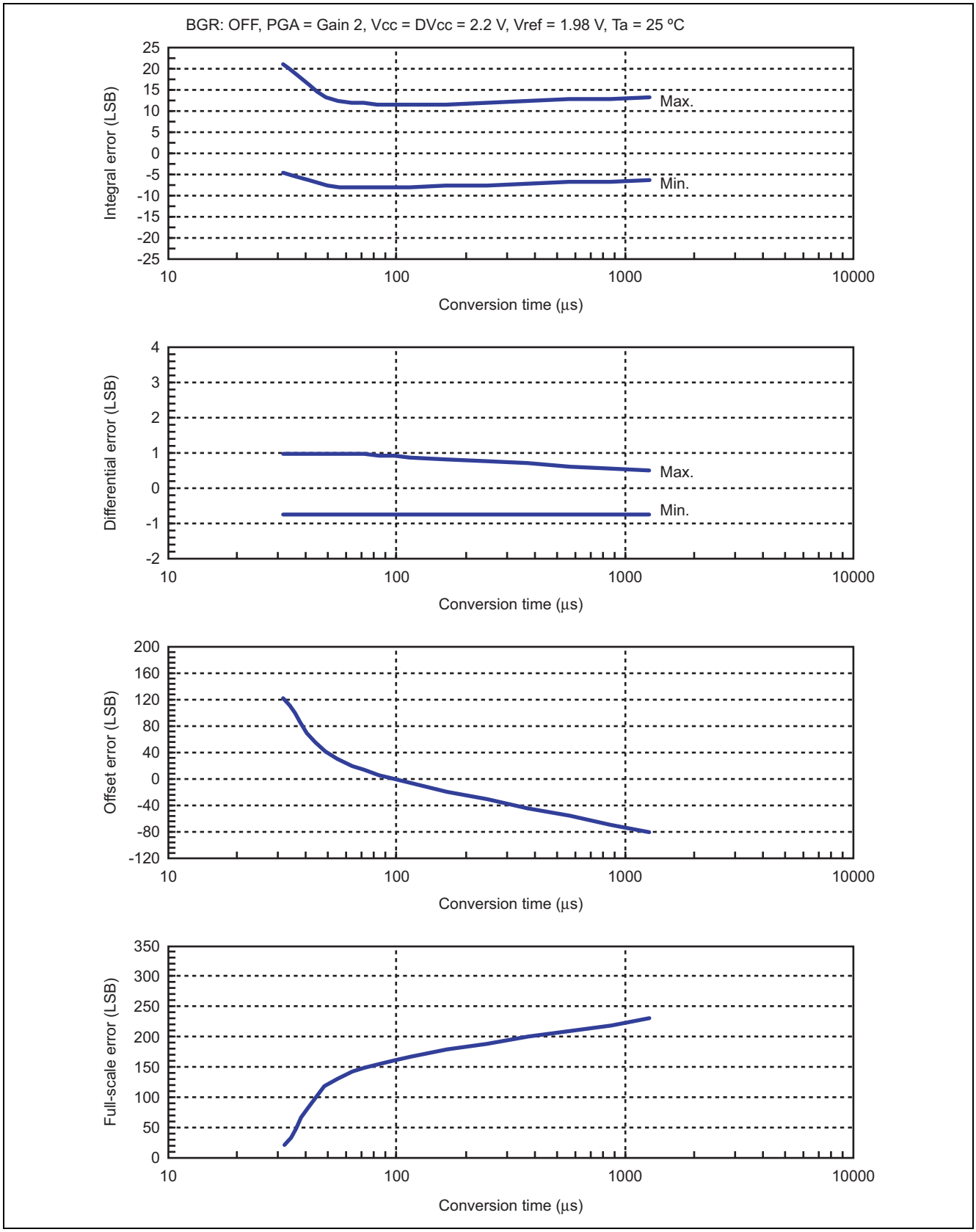
- Conversion time dependence 4



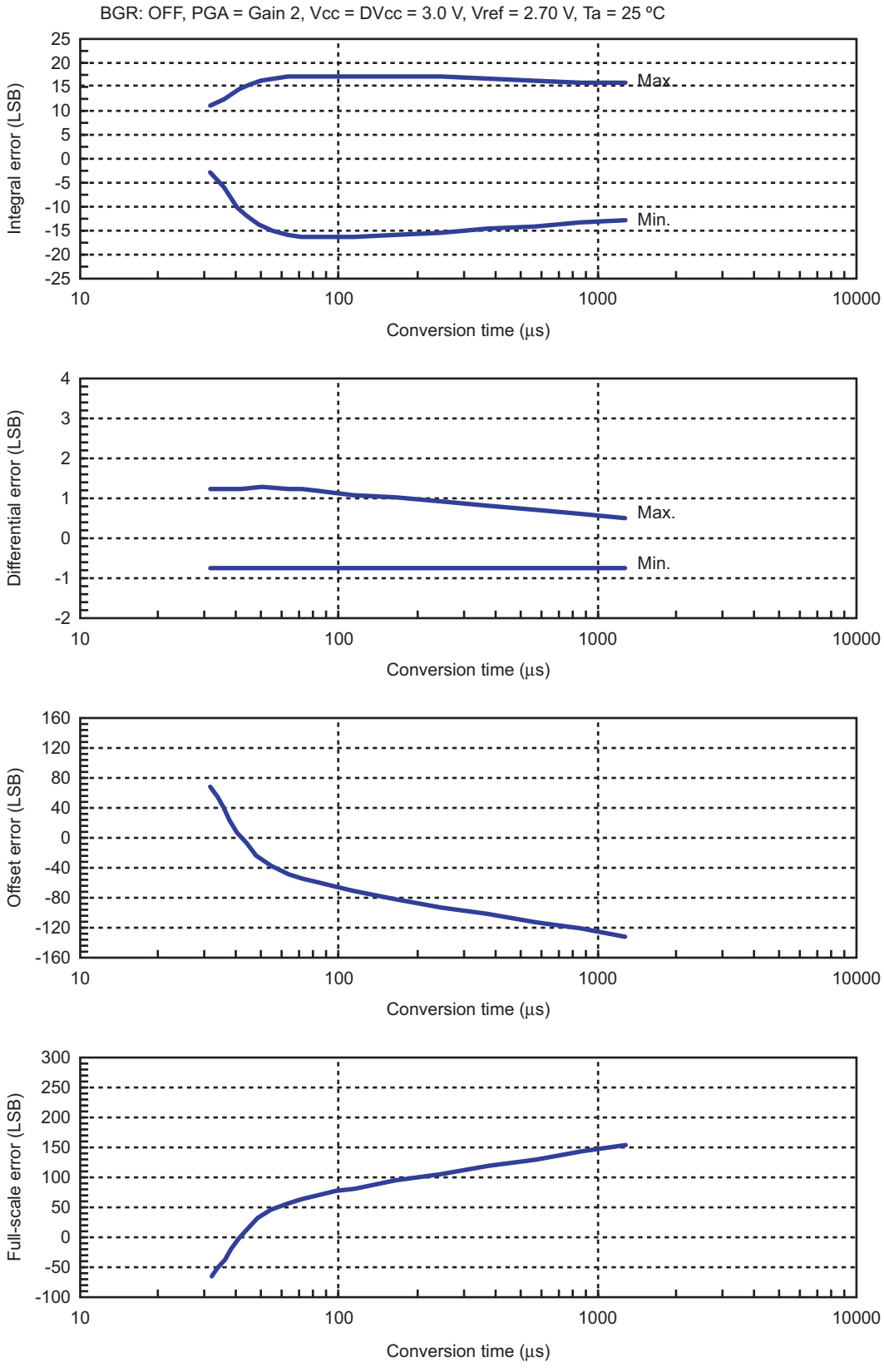
- Conversion time dependence 5



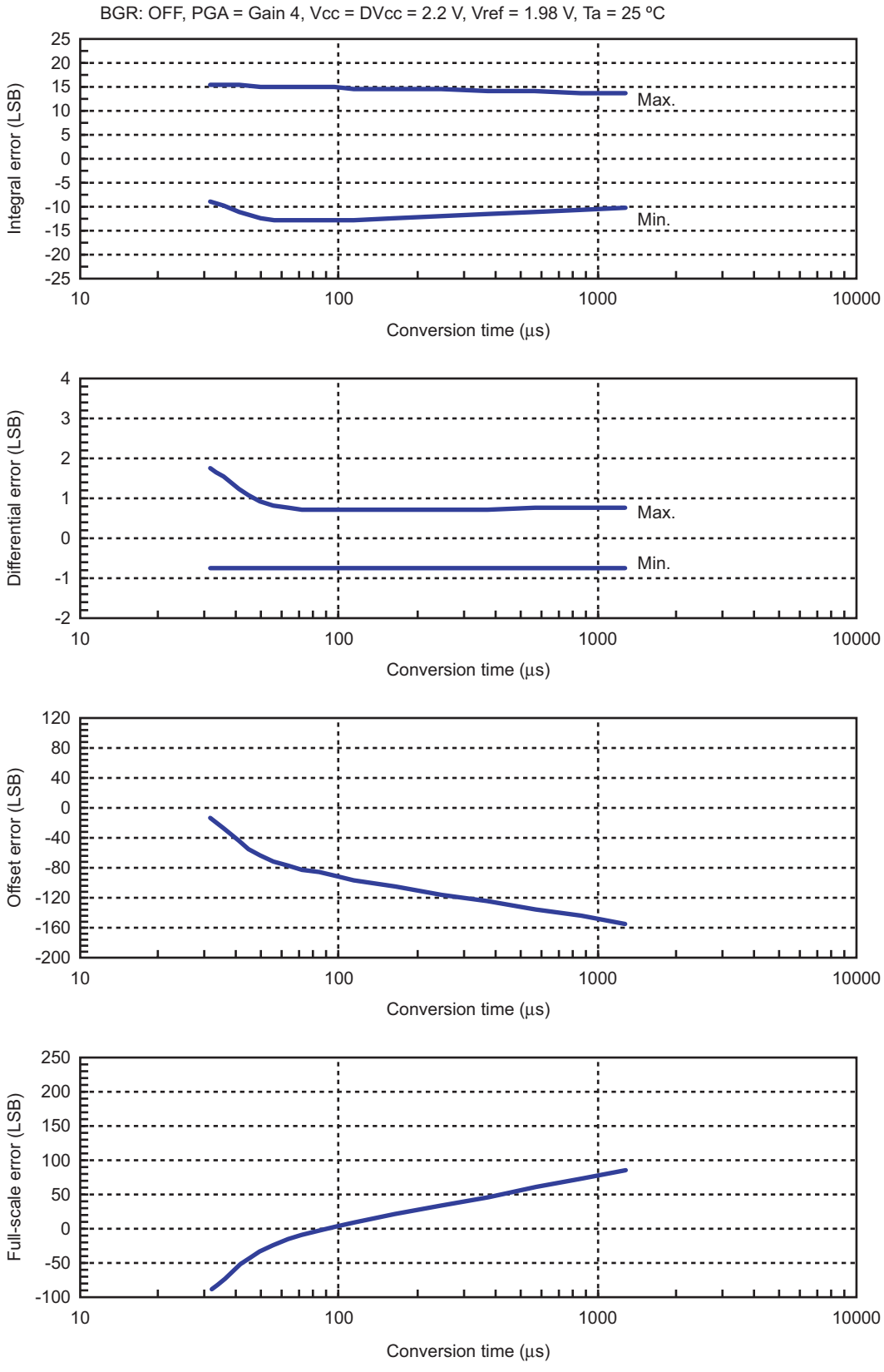
- Conversion time dependence 6



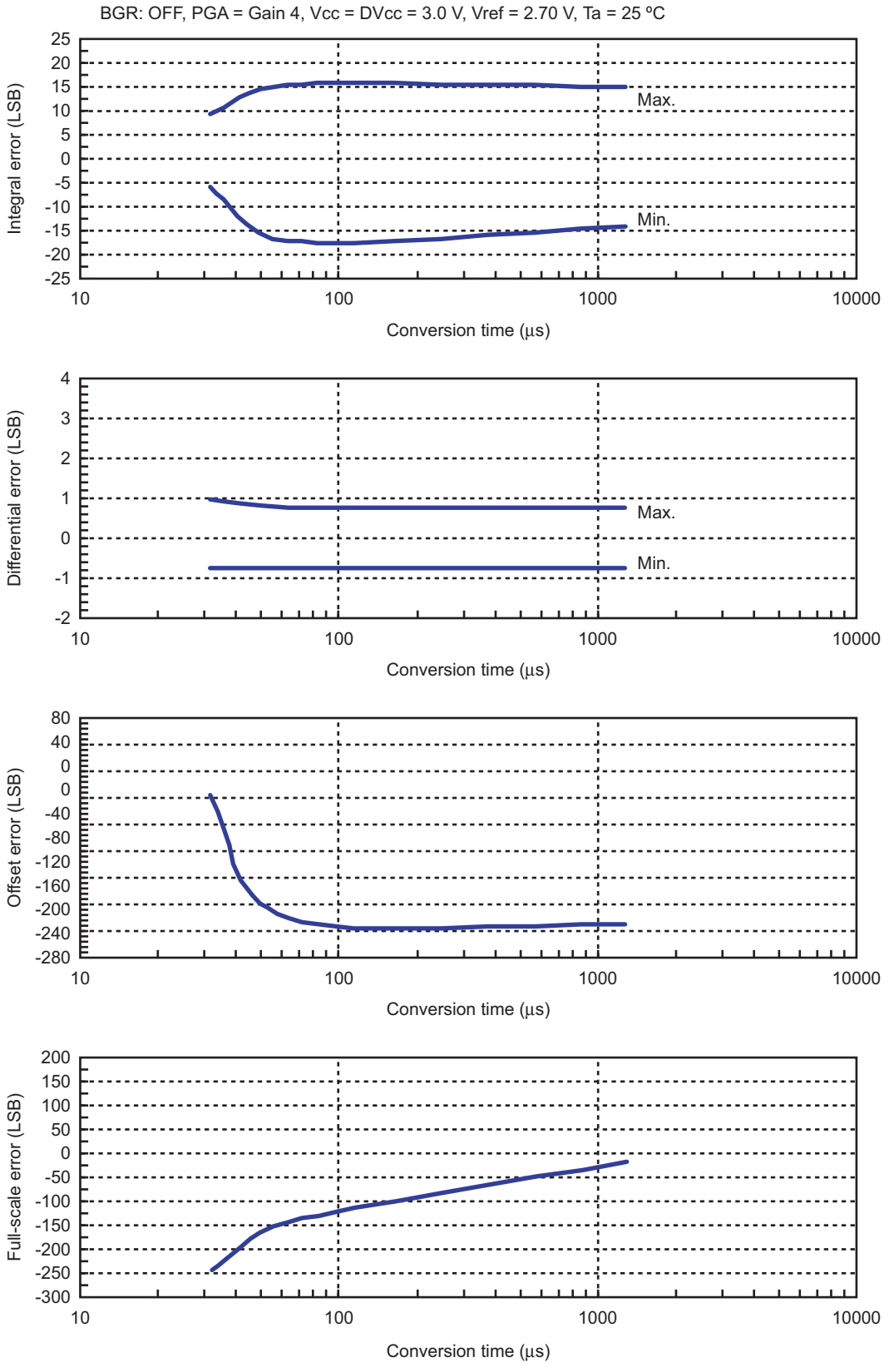
- Conversion time dependence 7



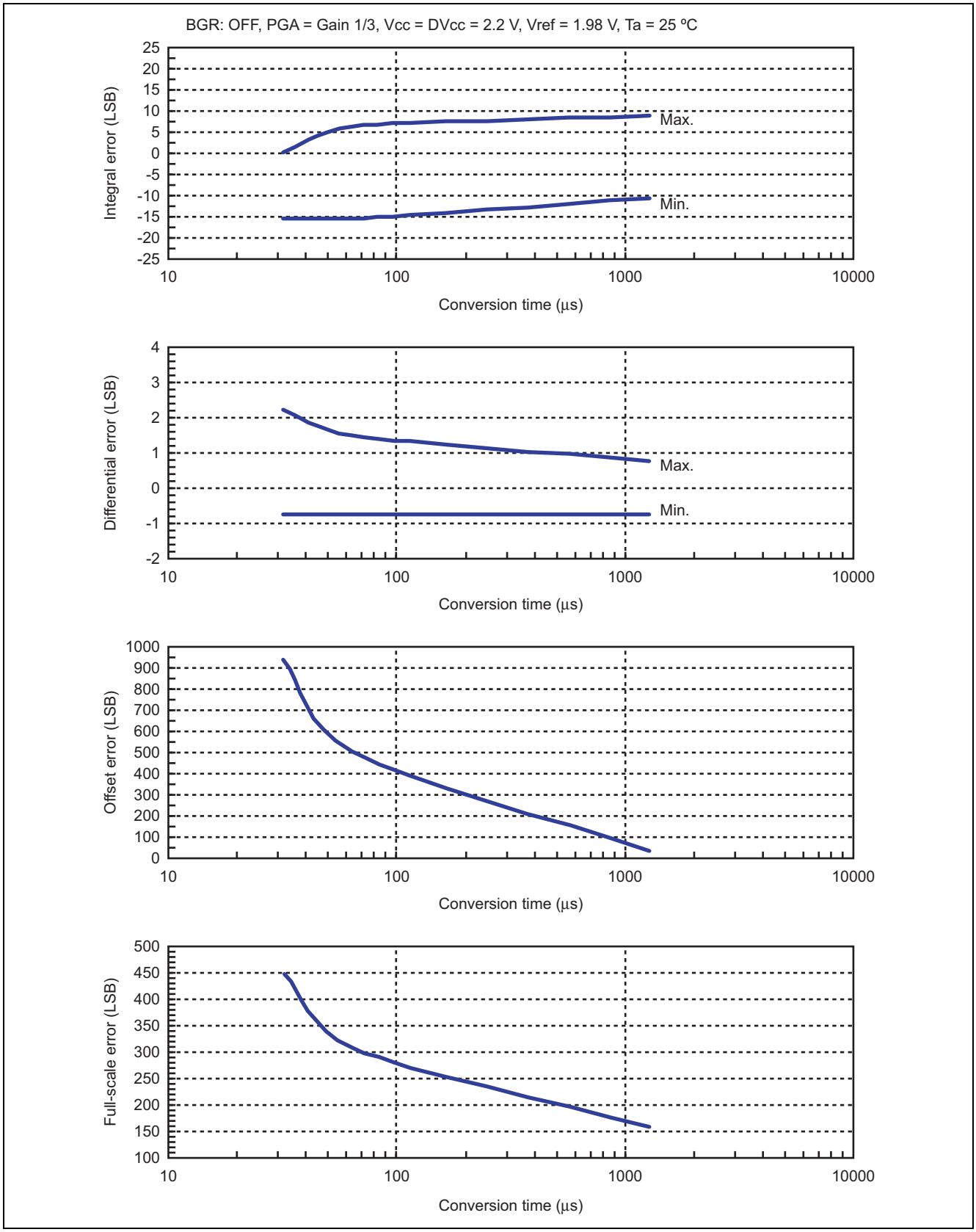
- Conversion time dependence 8



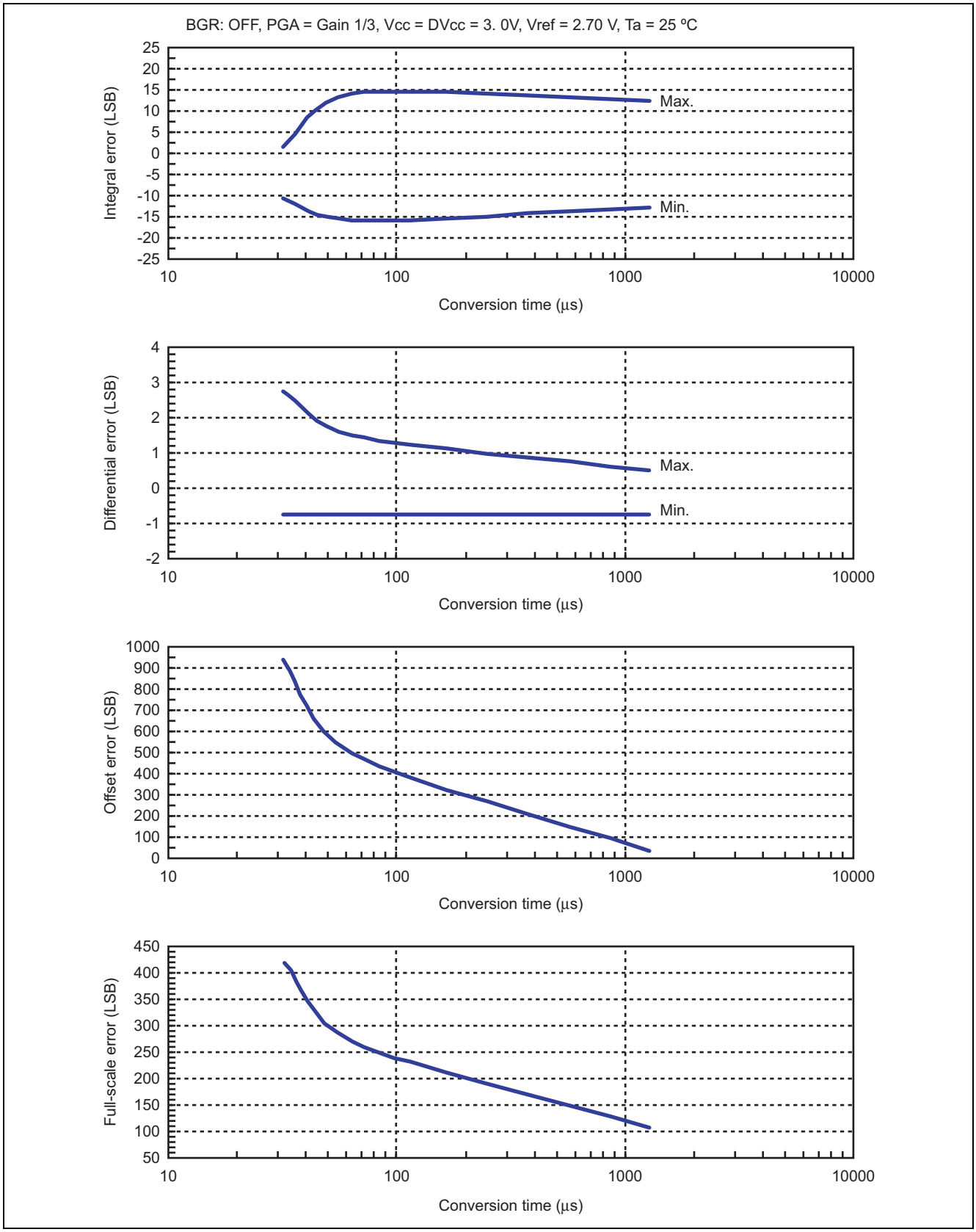
- Conversion time dependence 9



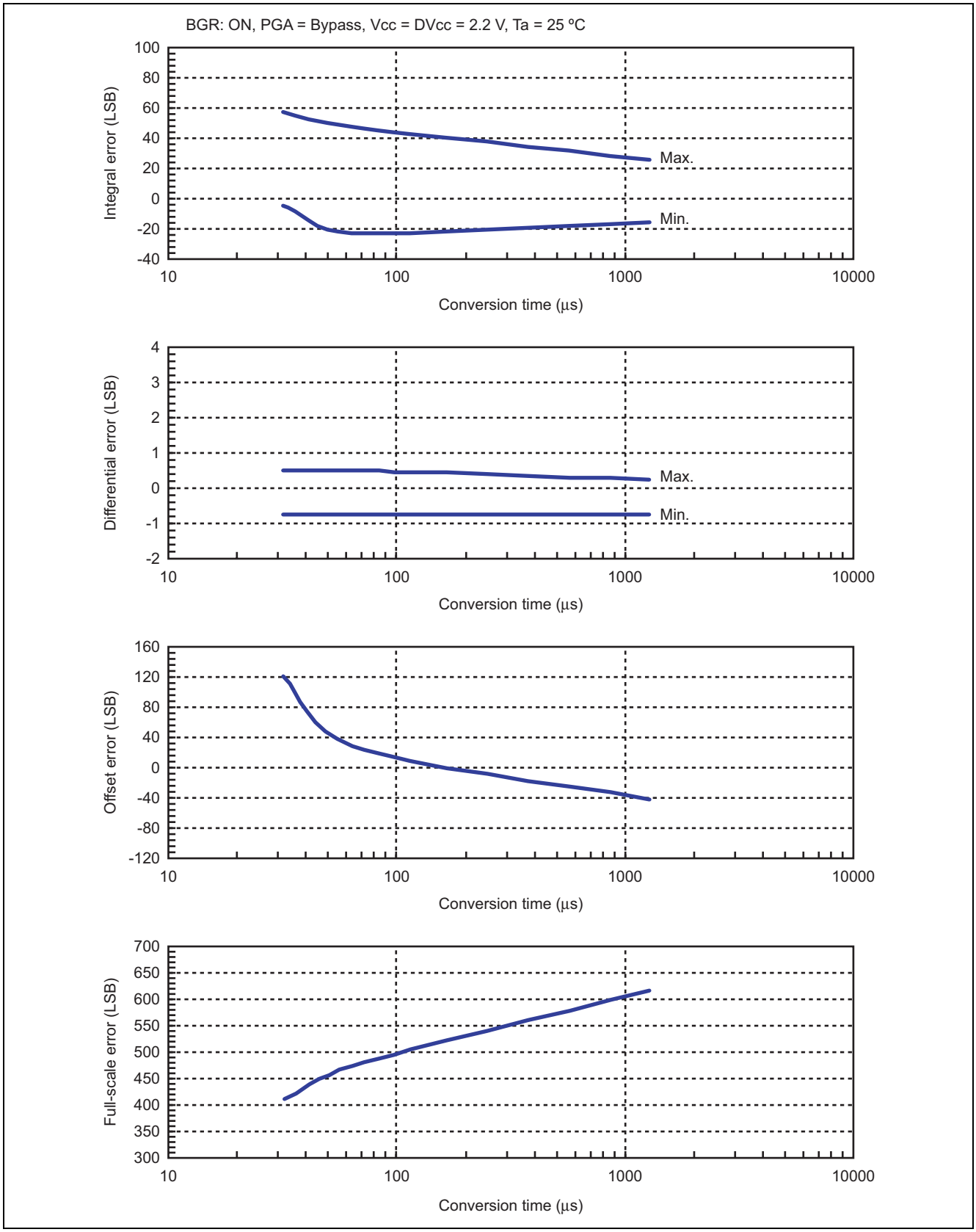
- Conversion time dependence 10



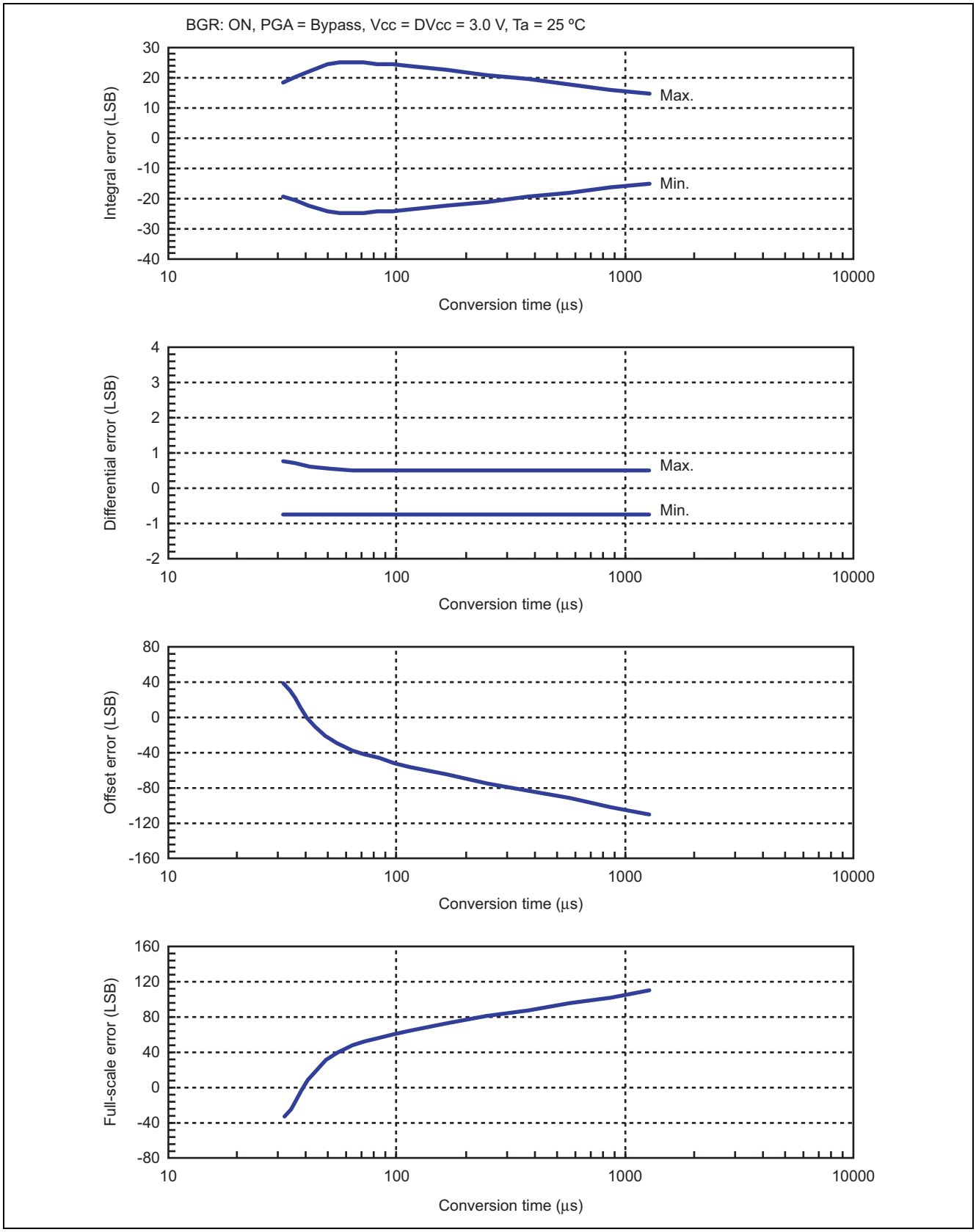
- Conversion time dependence 11



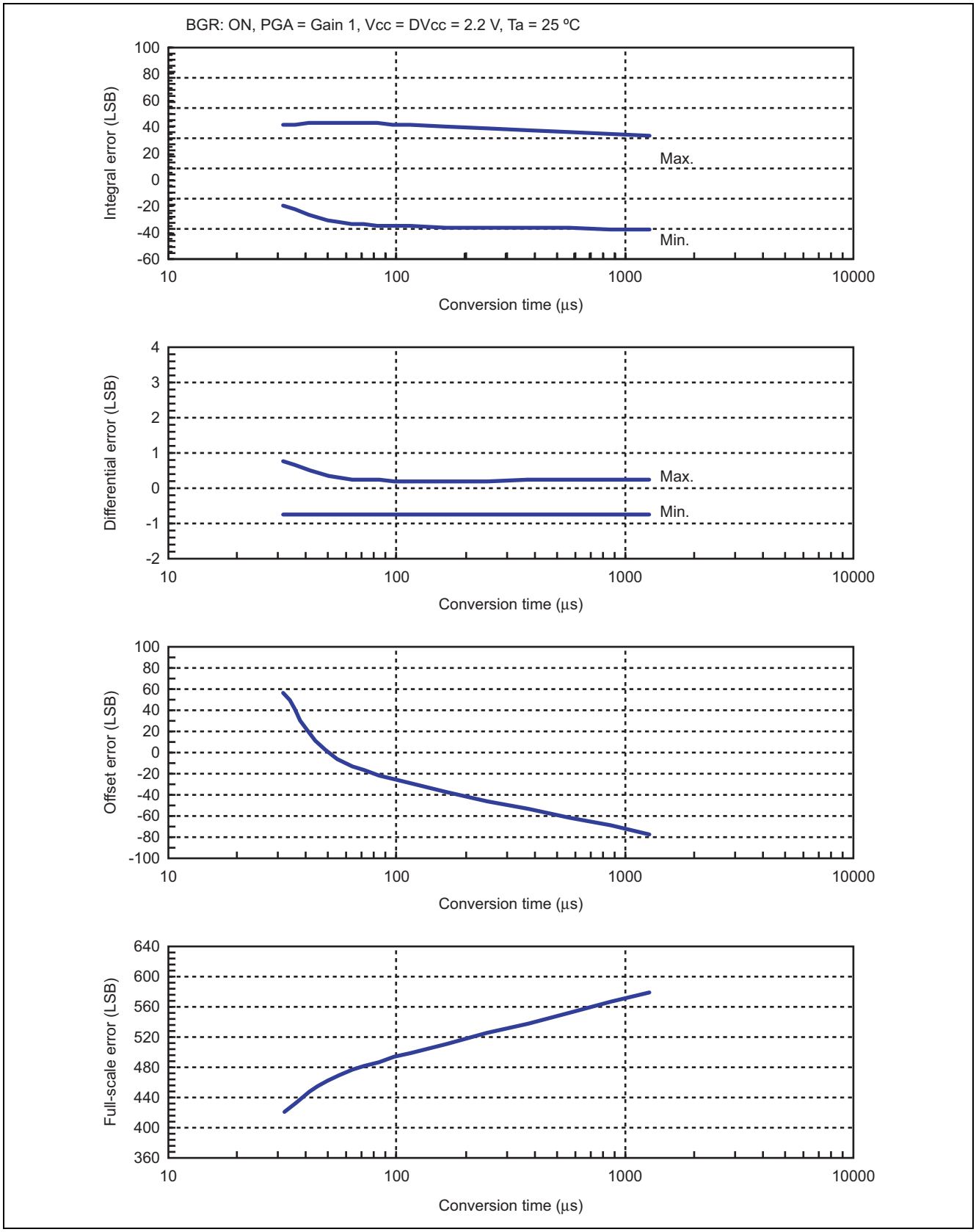
- Conversion time dependence 12



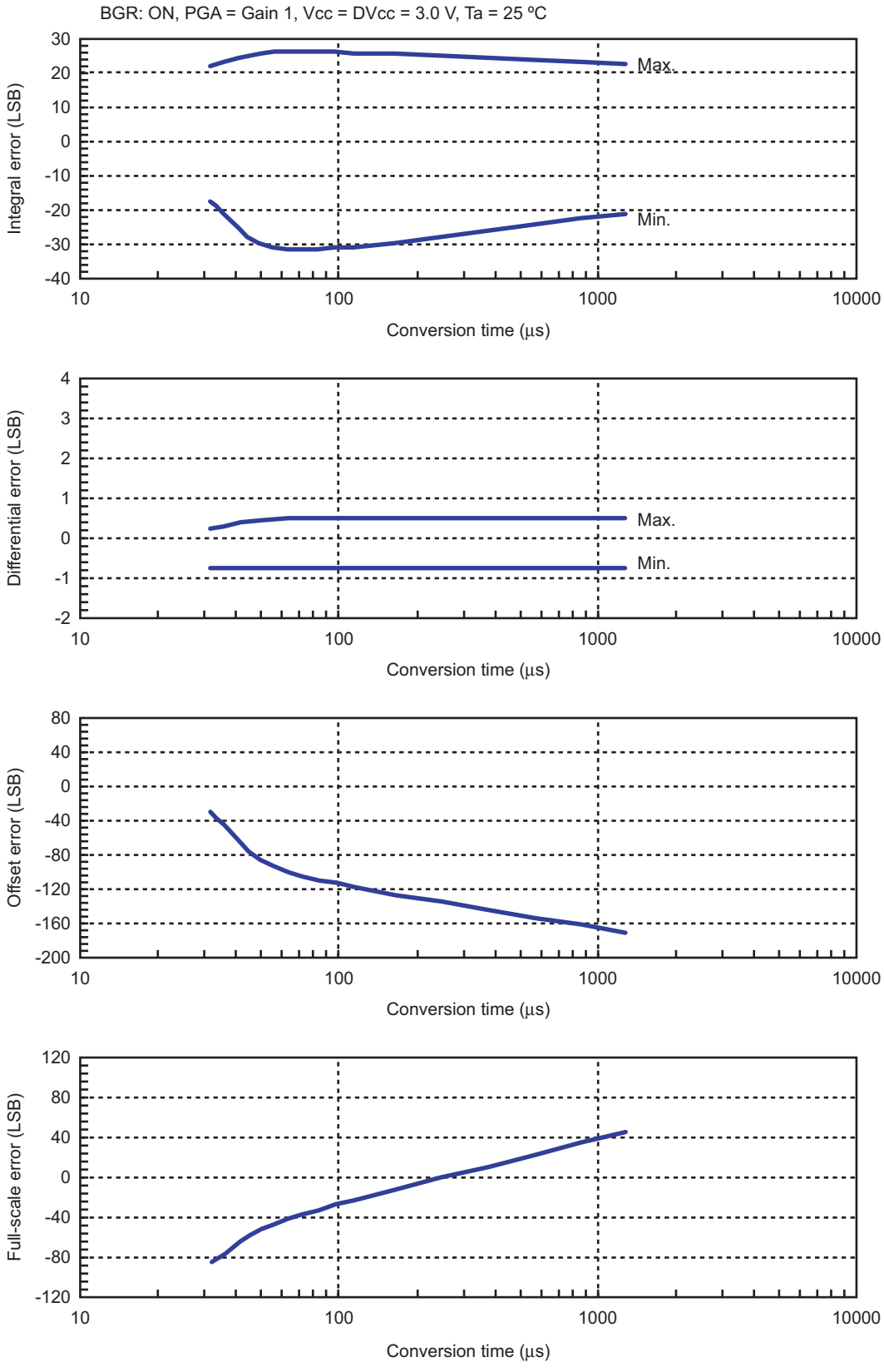
- Conversion time dependence 13



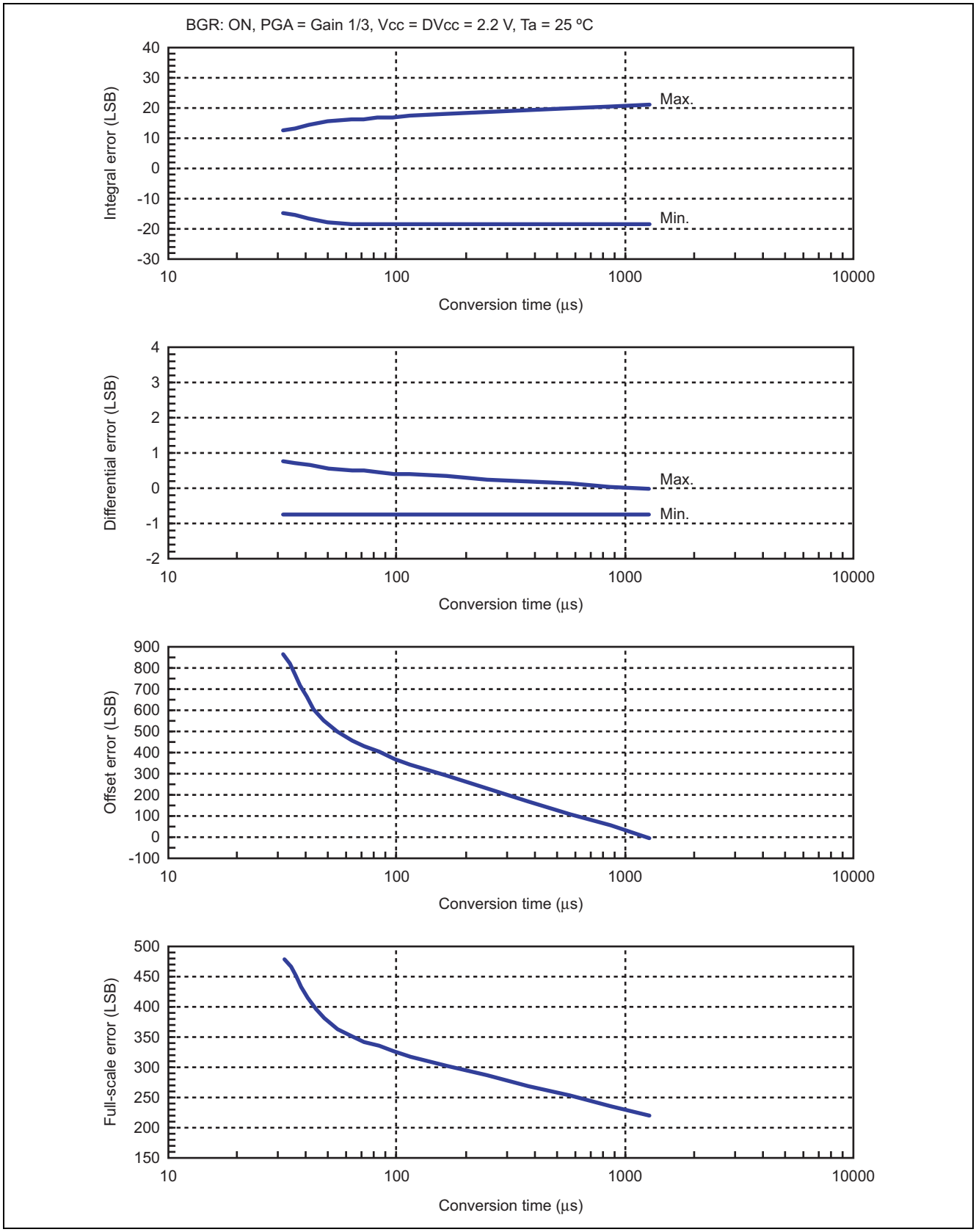
- Conversion time dependence 14



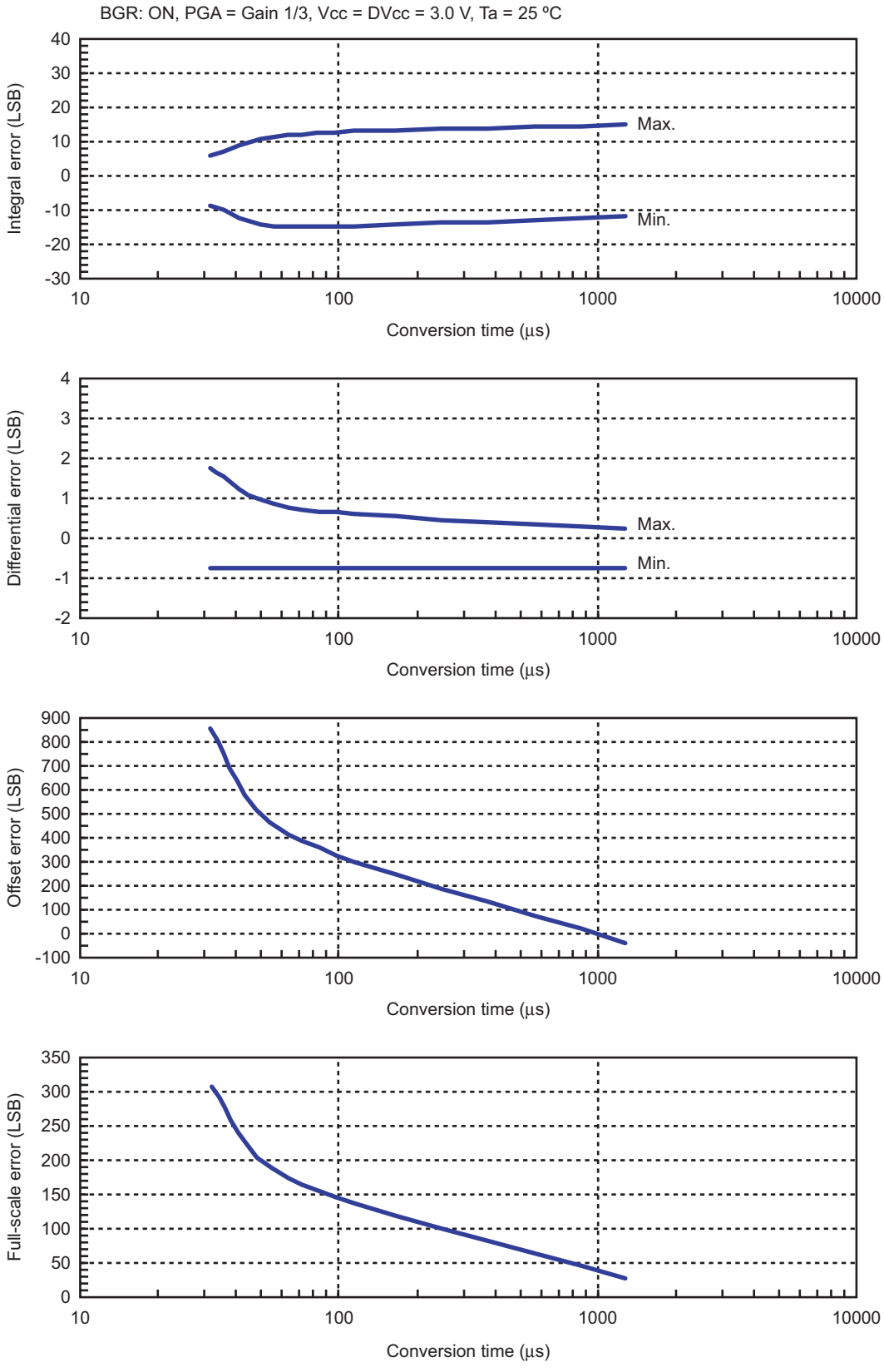
- Conversion time dependence 15



- Conversion time dependence 16

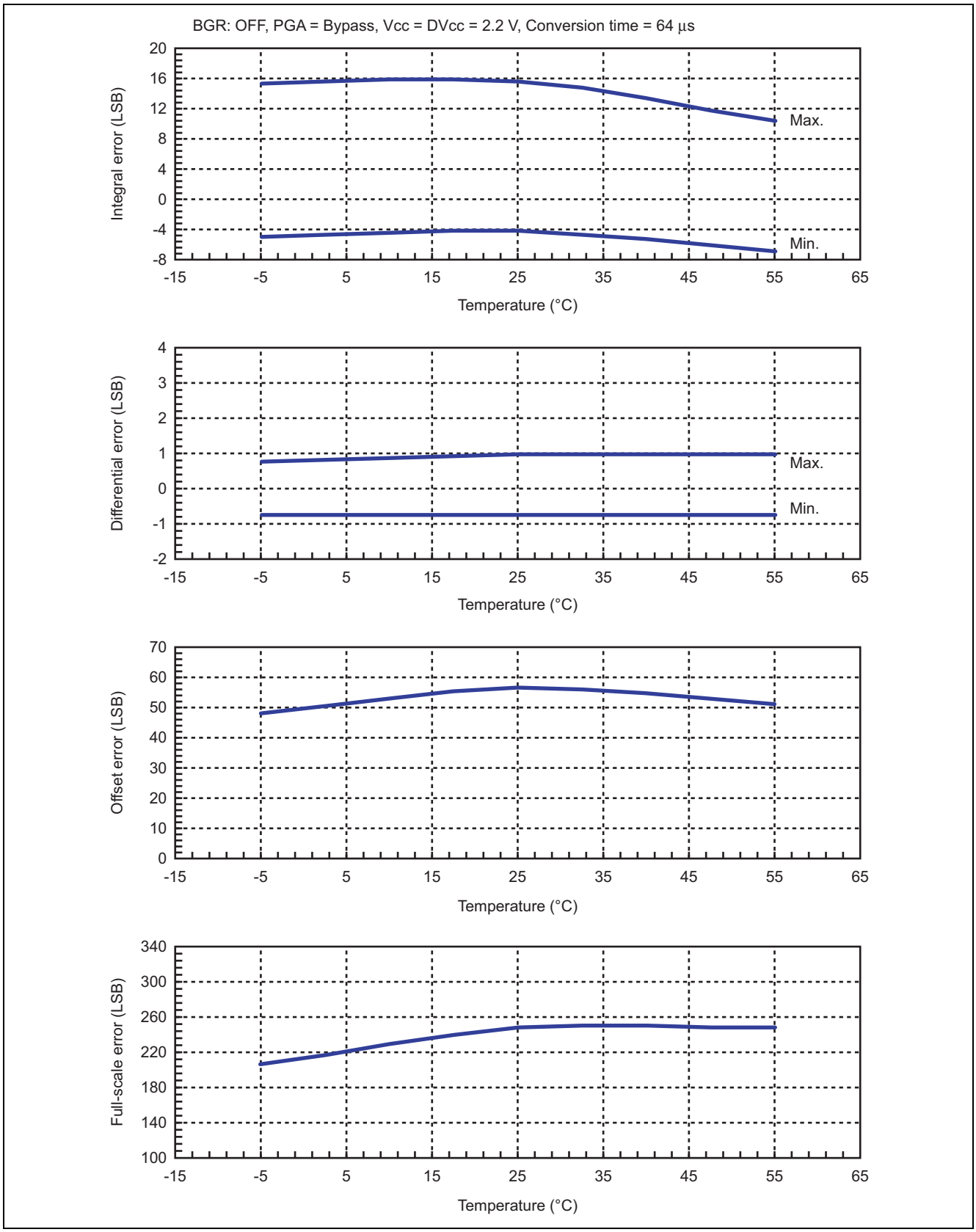


- Conversion time dependence 17

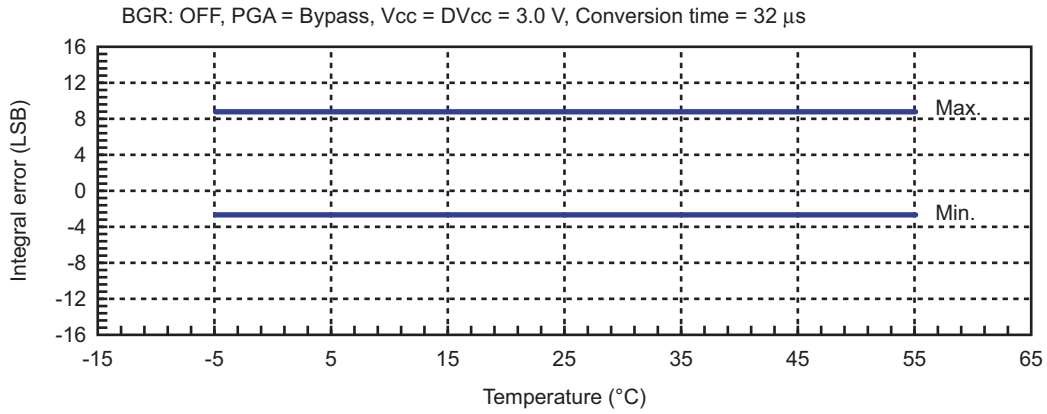


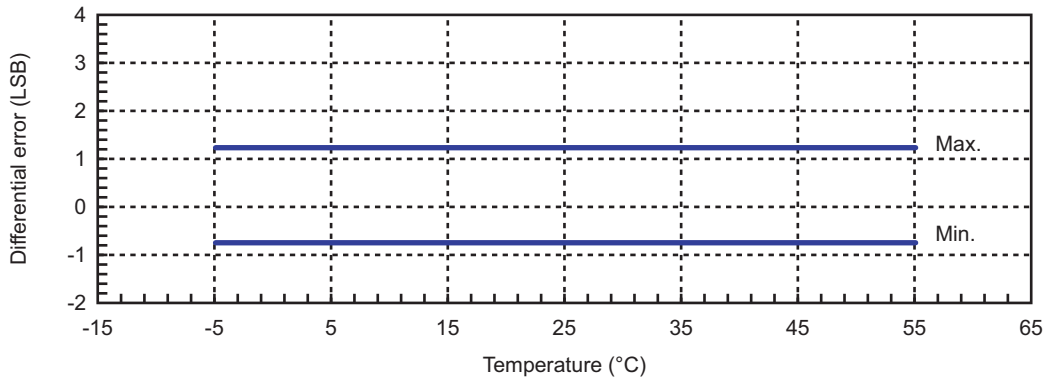
(2) Temperature Dependence

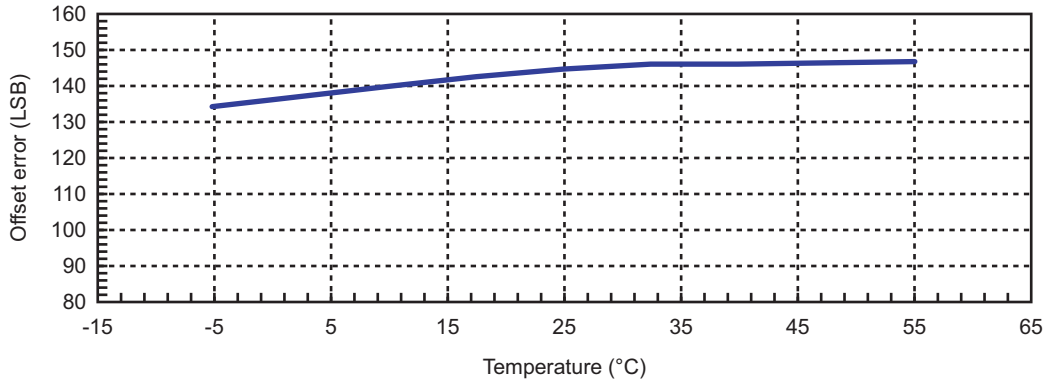
- Temperature dependence 1

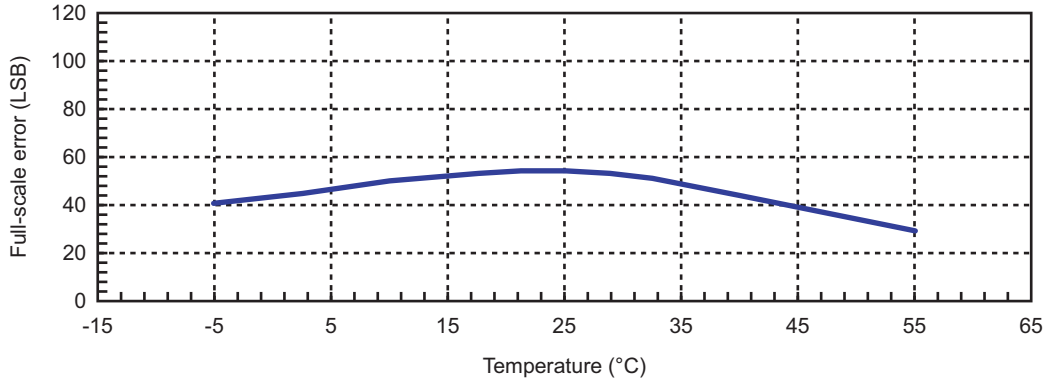


- Temperature dependence 2

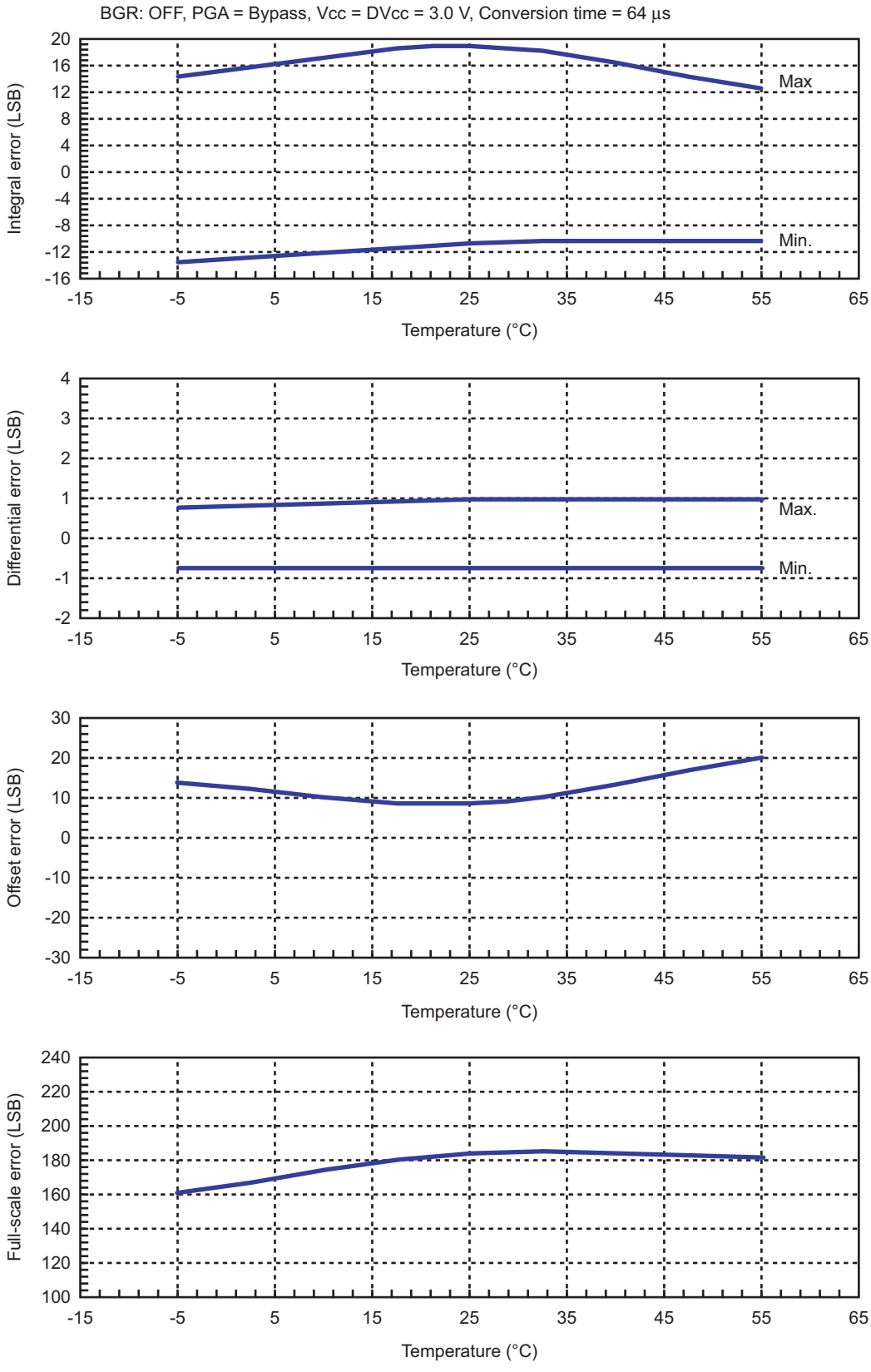




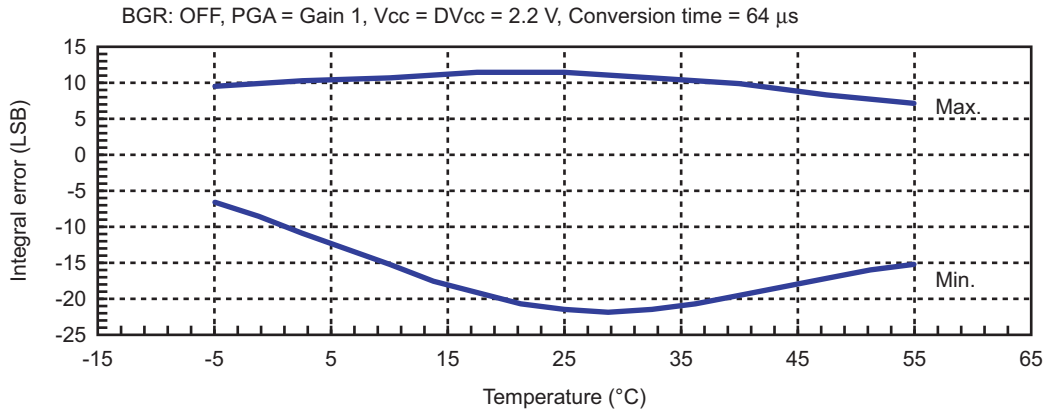


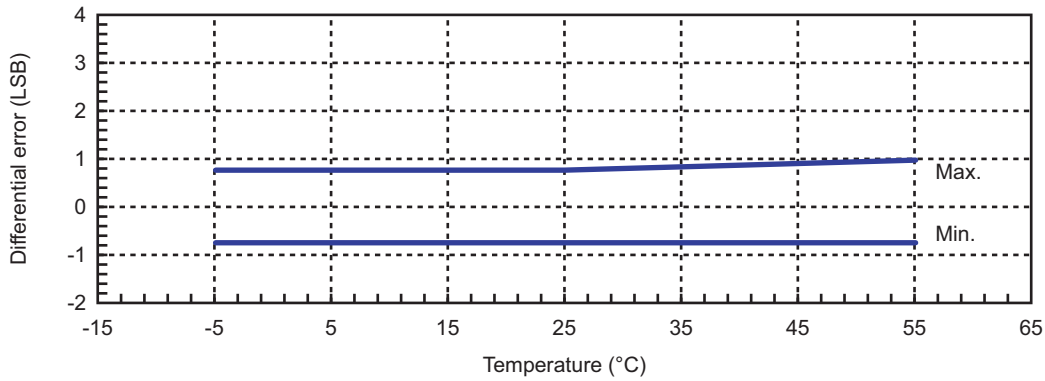


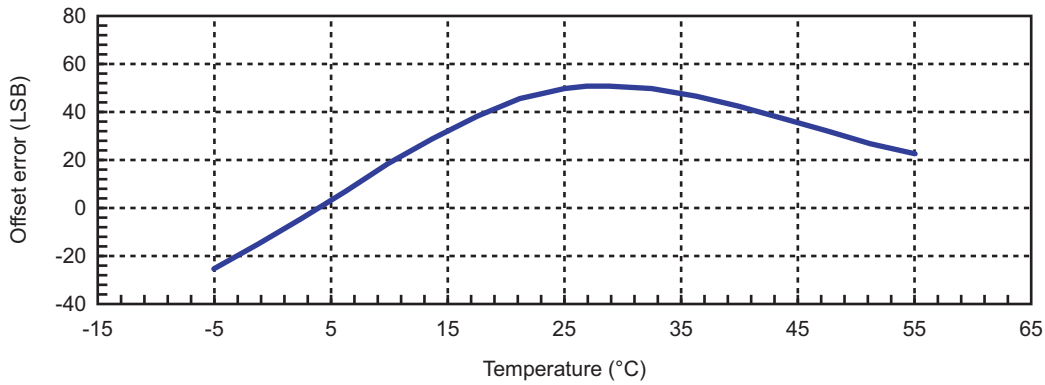
- Temperature dependence 3

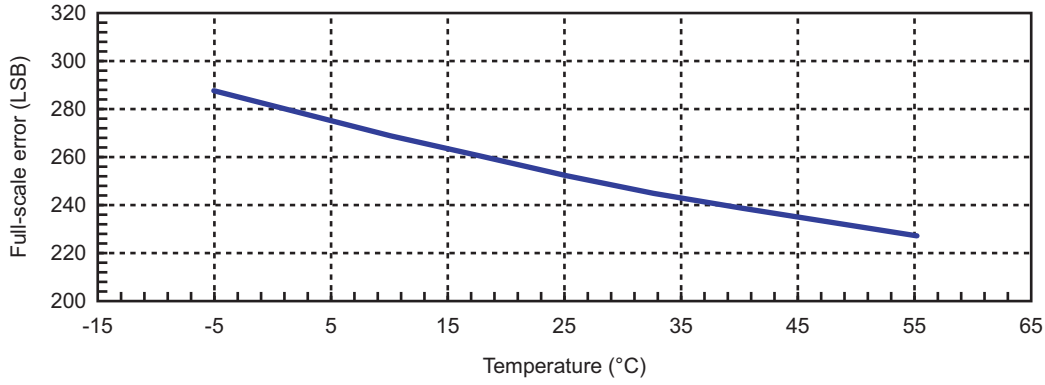


- Temperature dependence 4

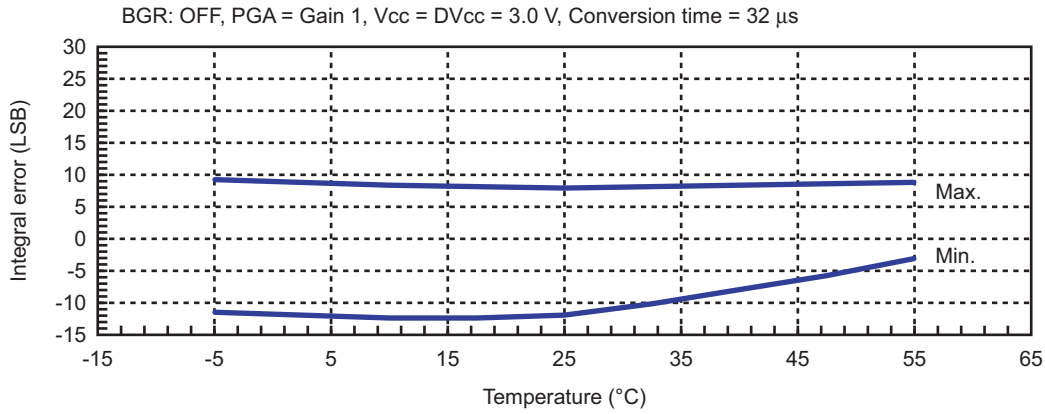


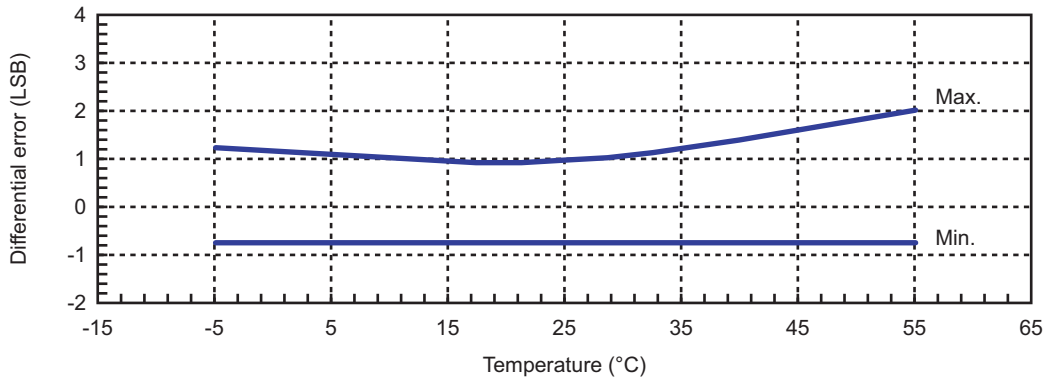


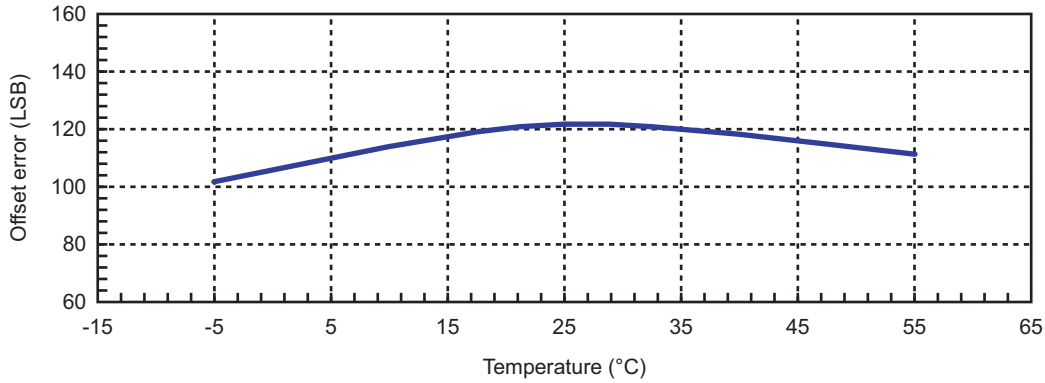


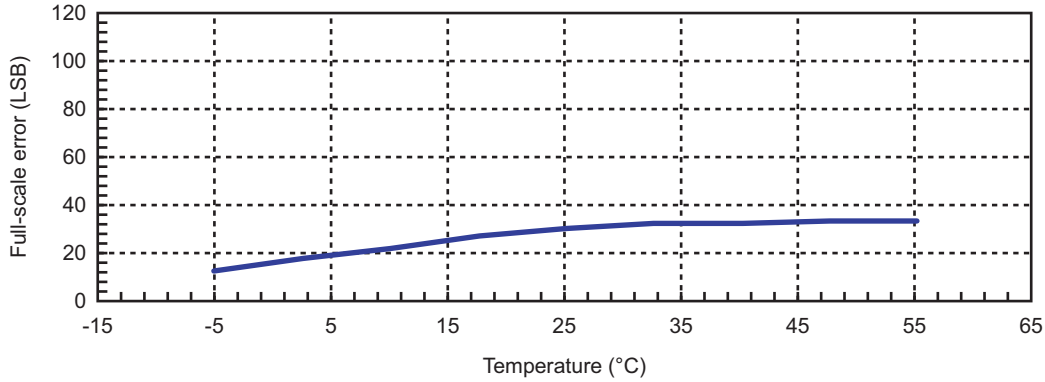


- Temperature dependence 5

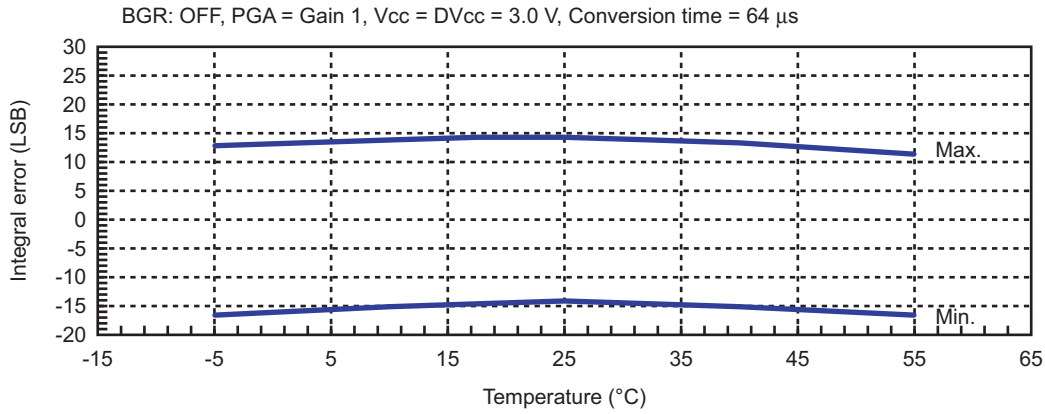


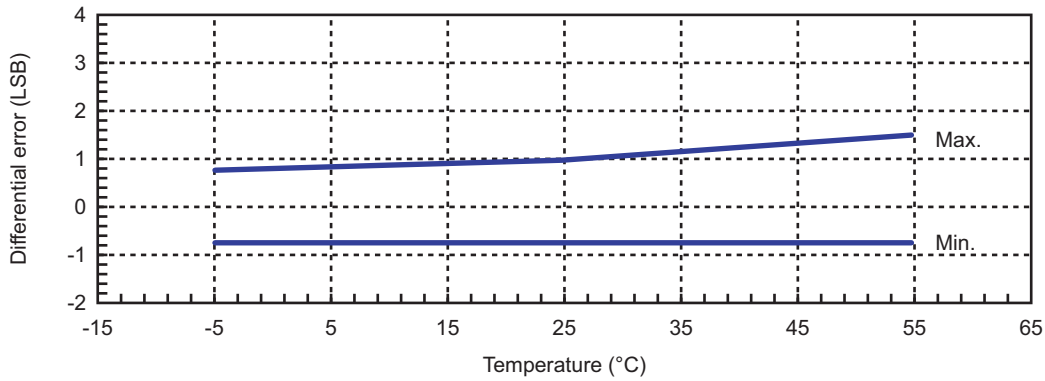


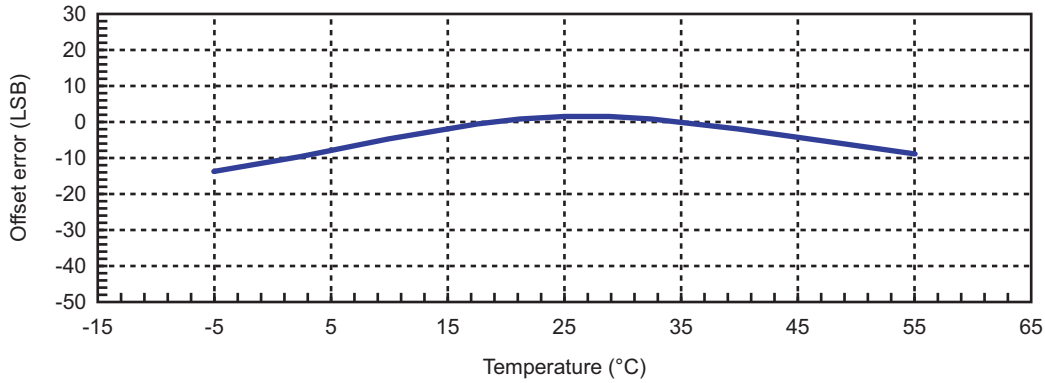


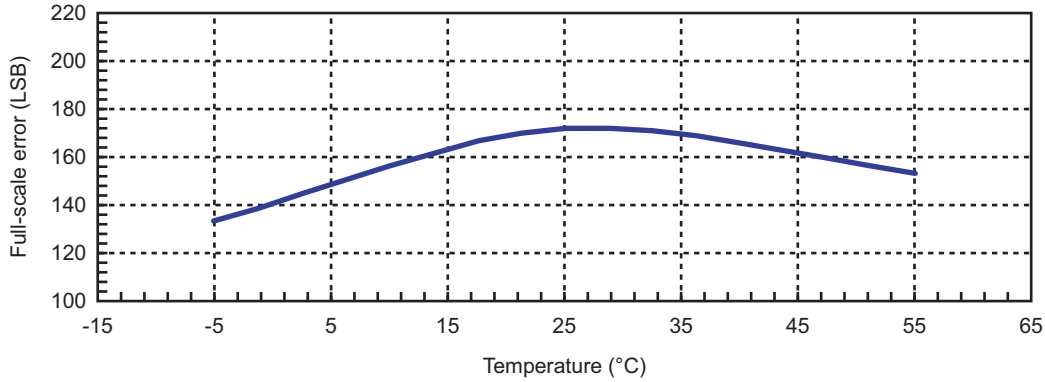


- Temperature dependence 6

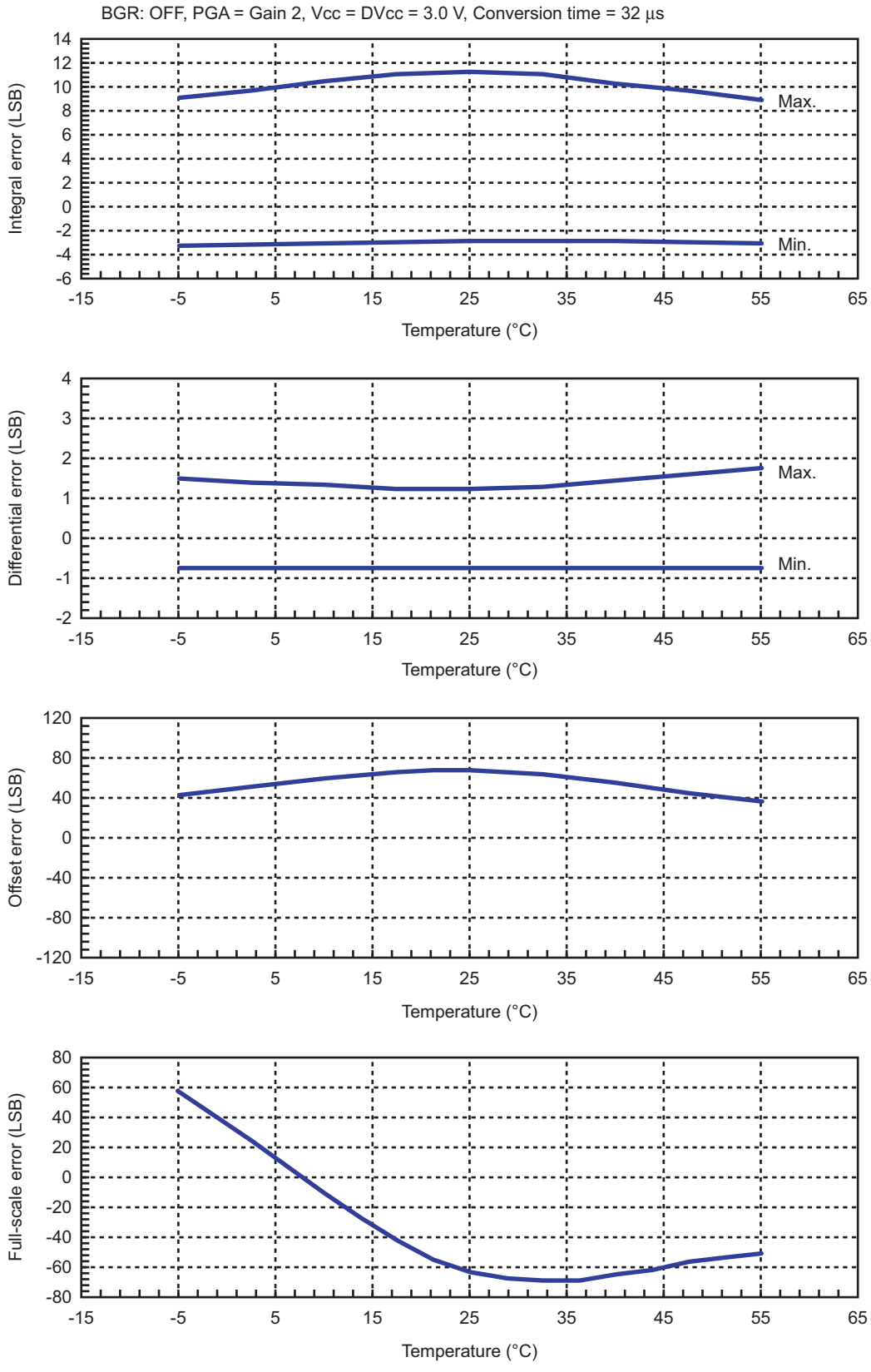




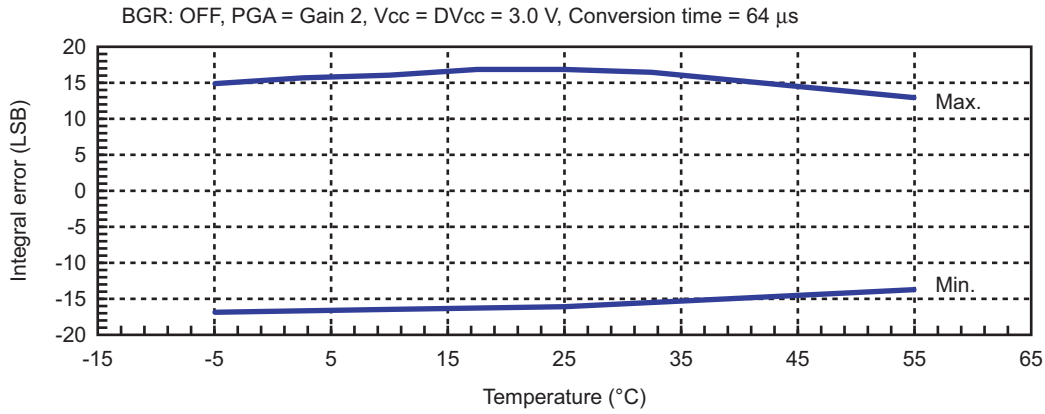


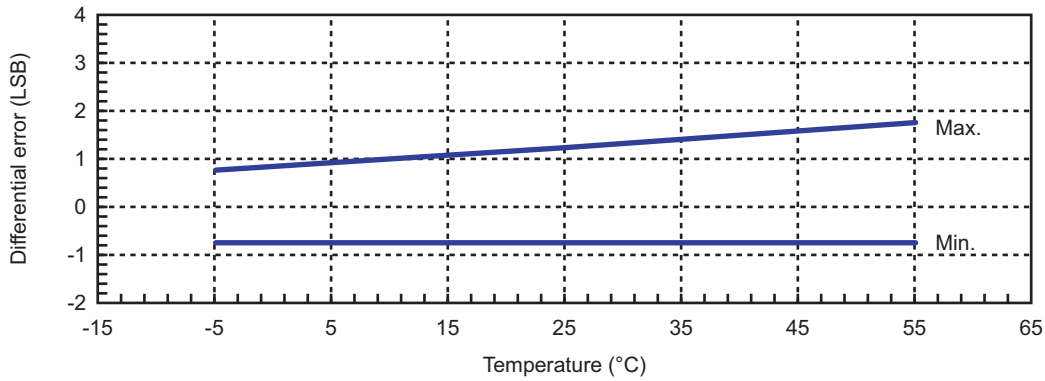


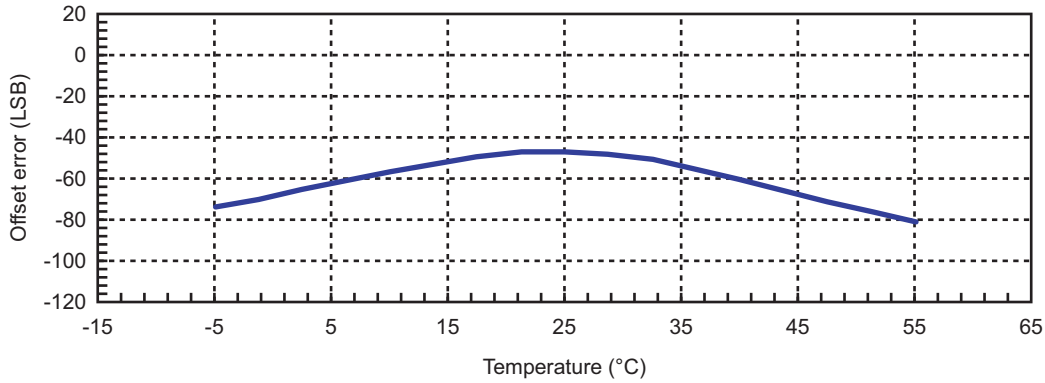
- Temperature dependence 7

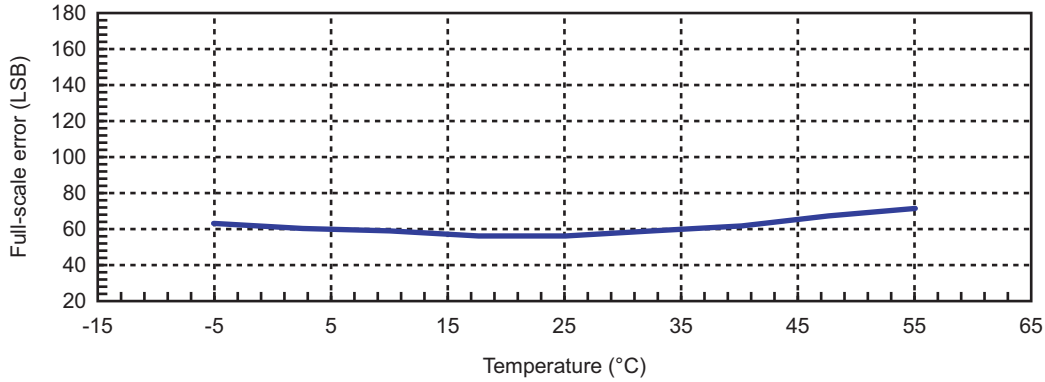


- Temperature dependence 8

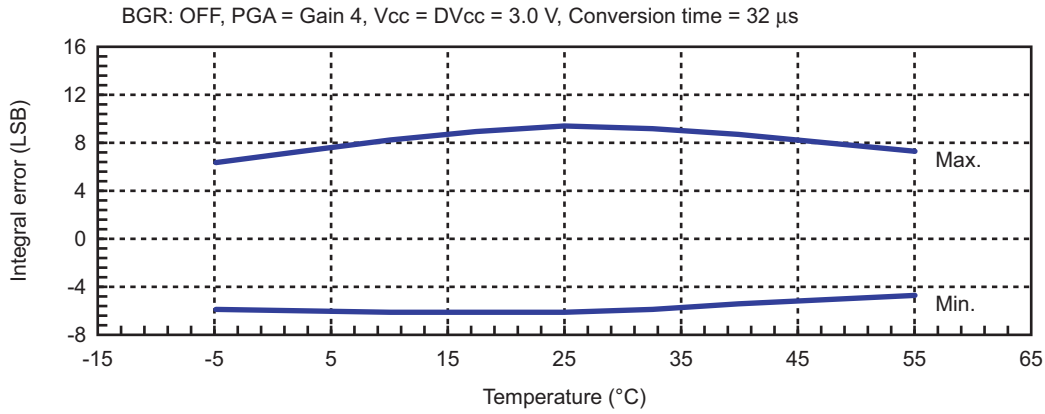


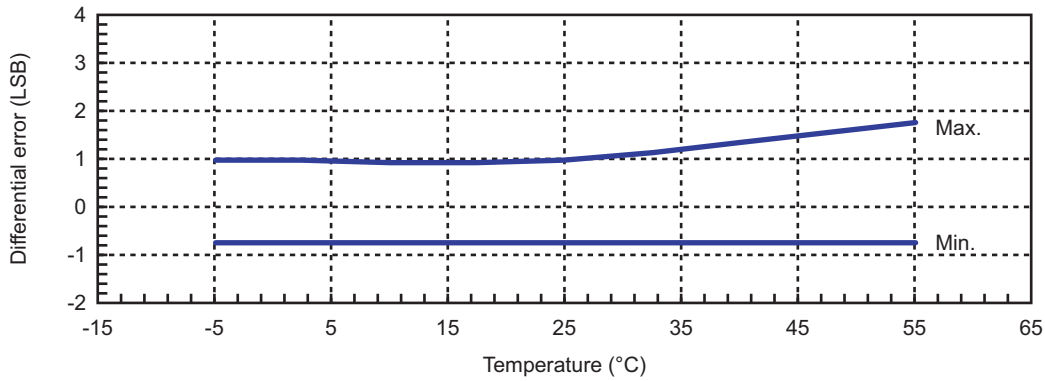


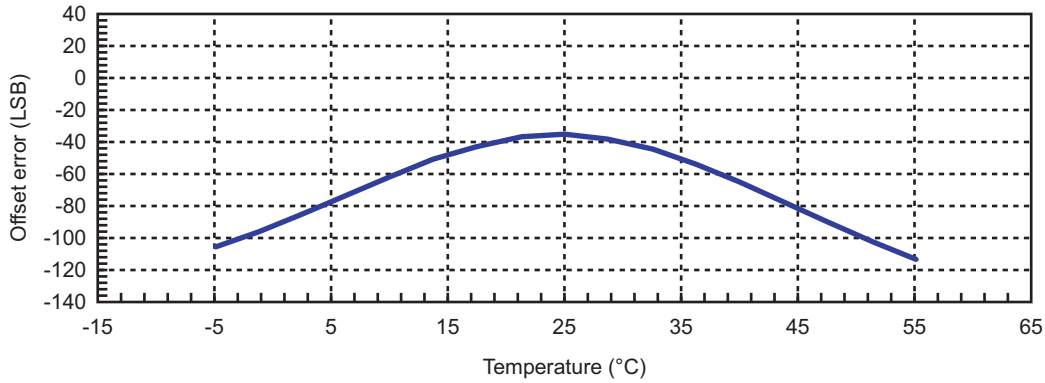


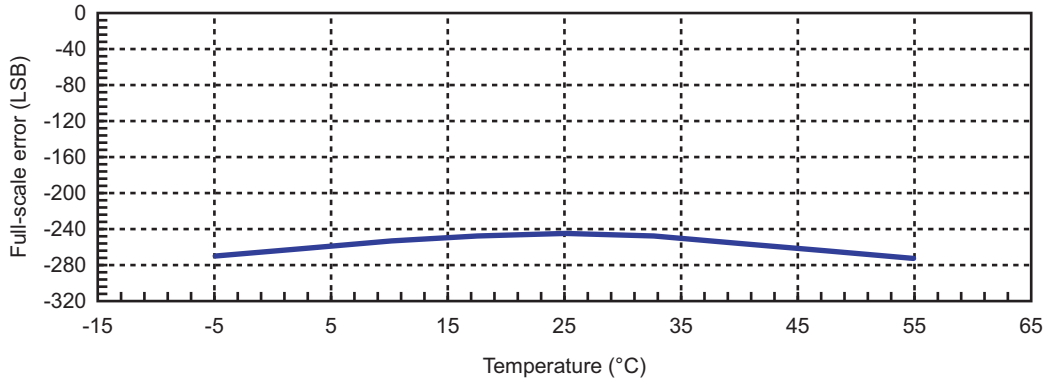


- Temperature dependence 9

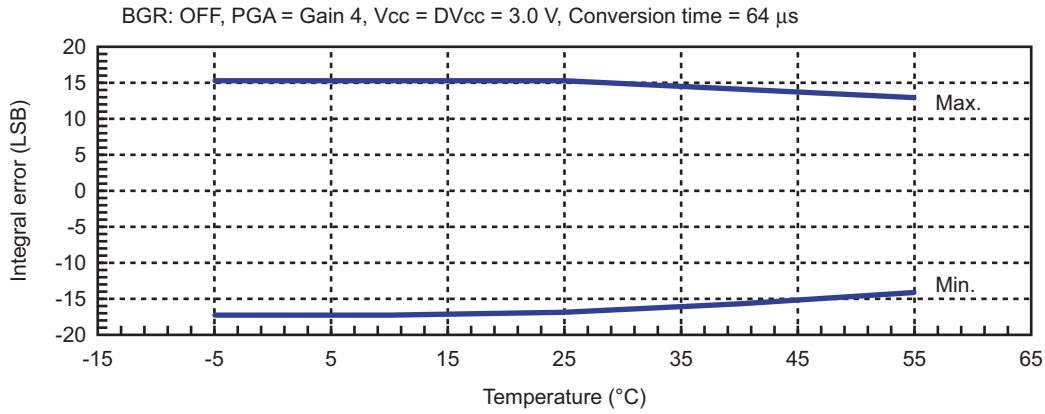


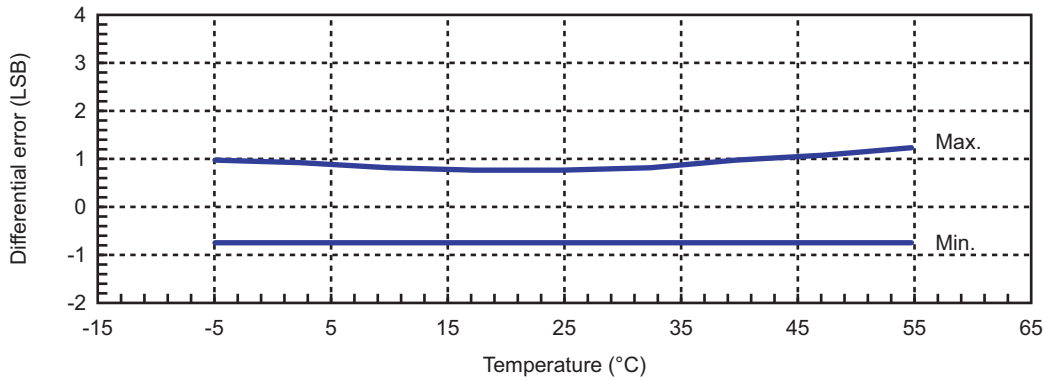


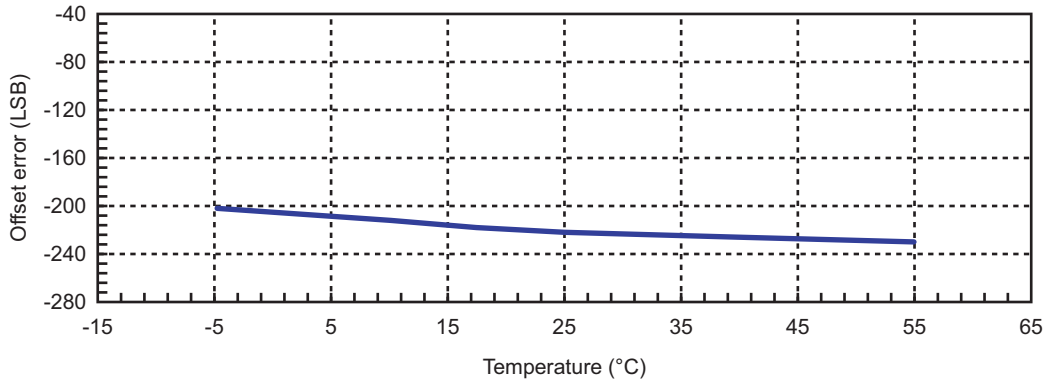


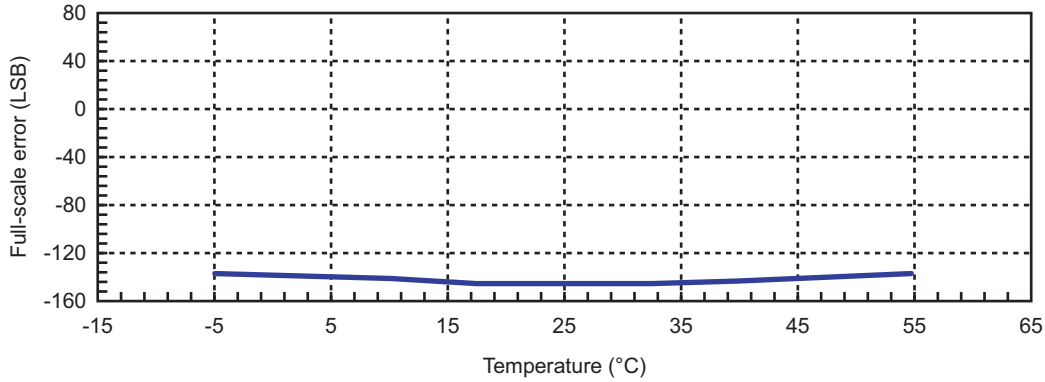


- Temperature dependence 10

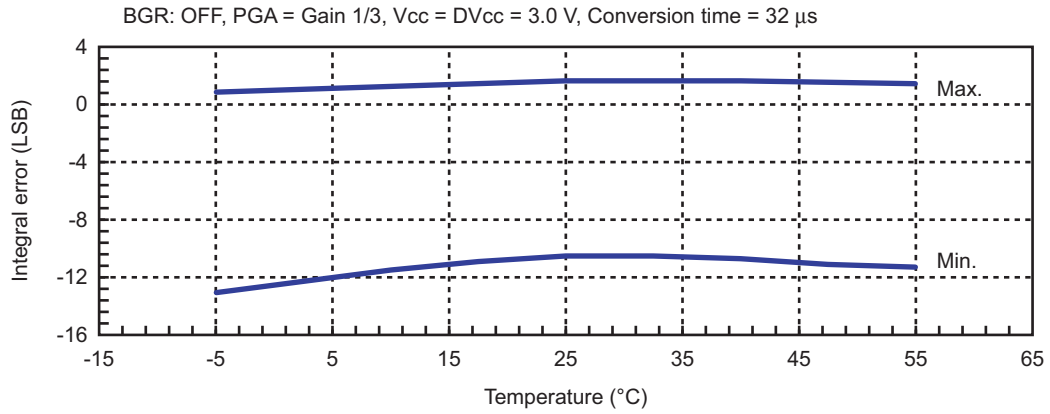


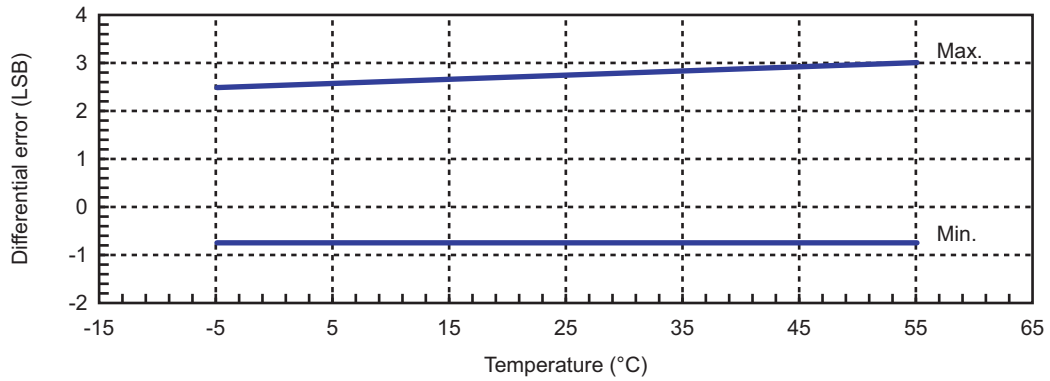


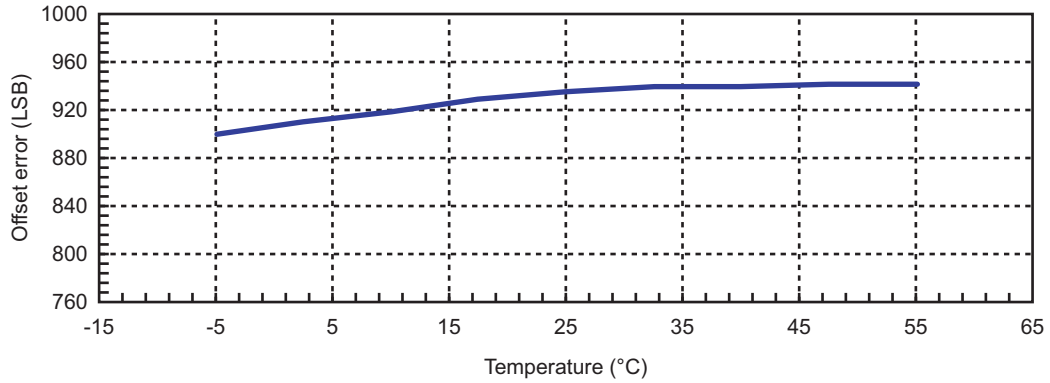


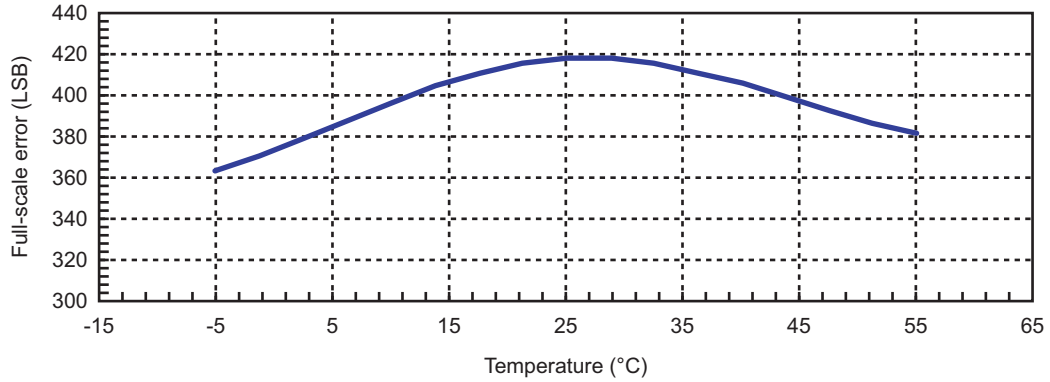


- Temperature dependence 11

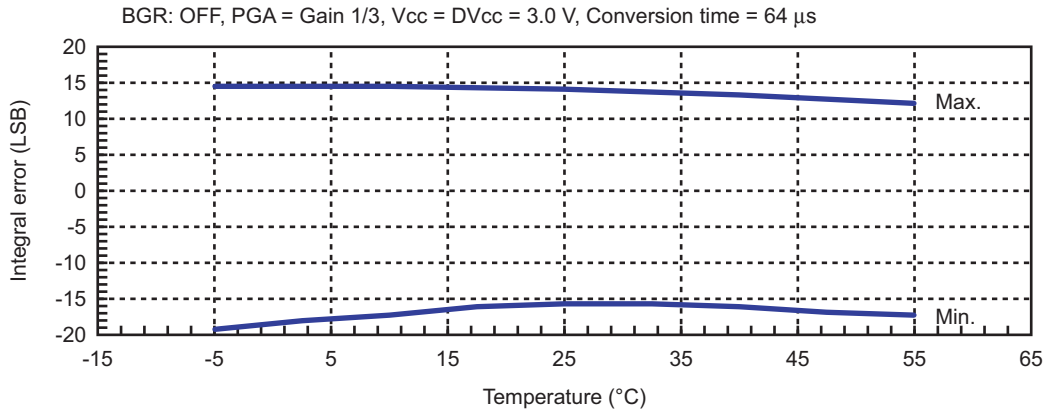


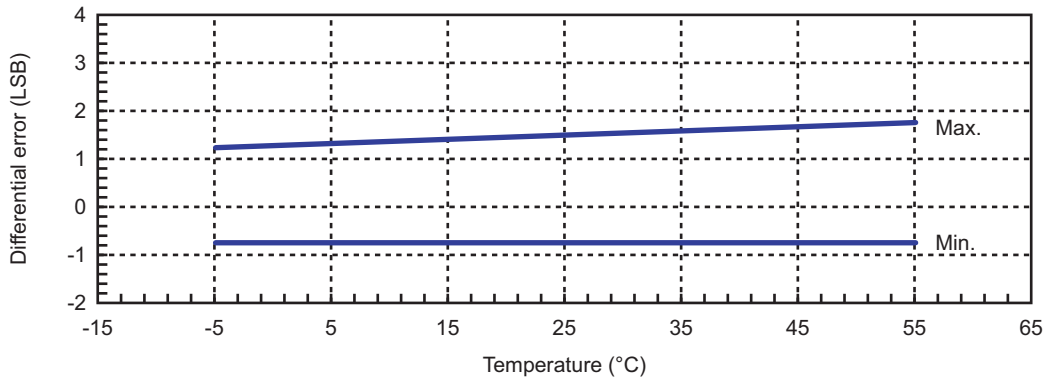


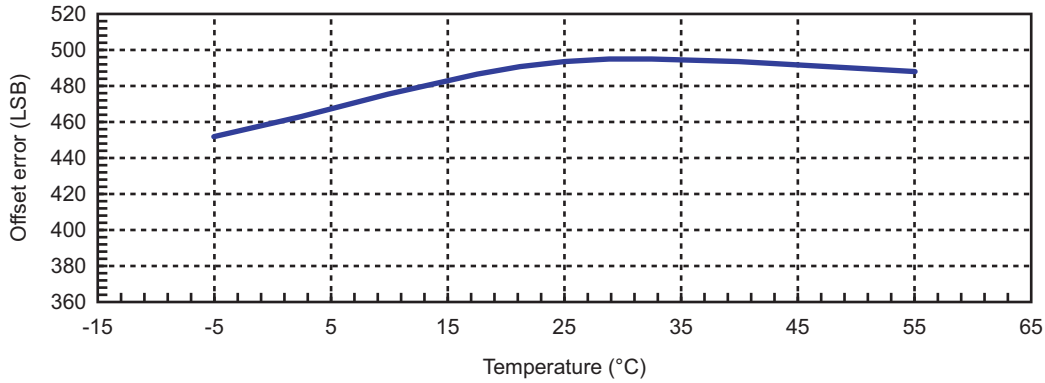


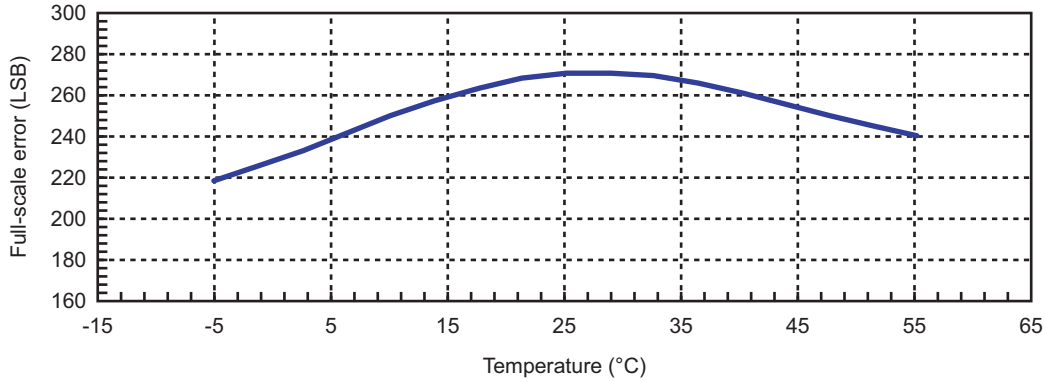


- Temperature dependence 12



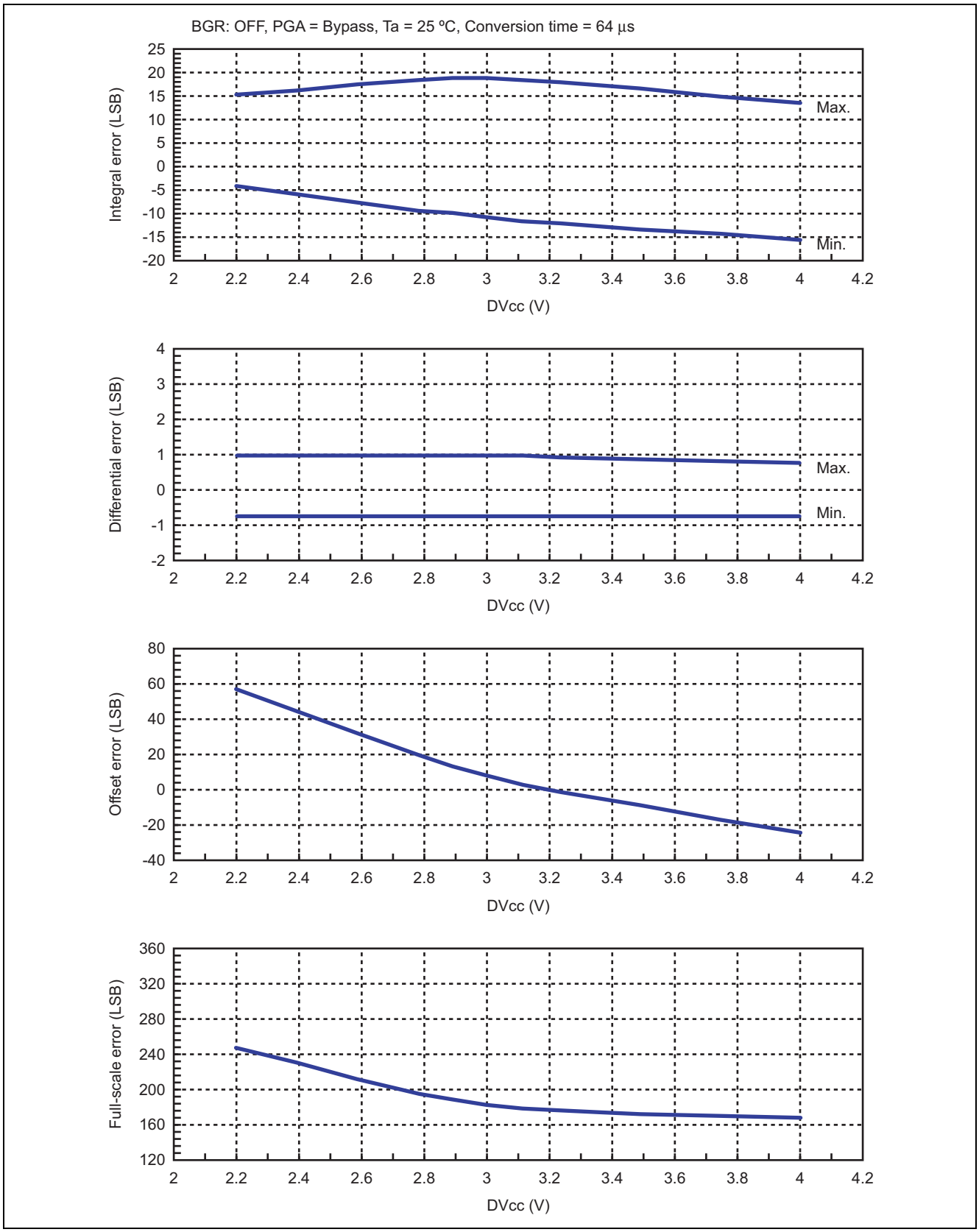




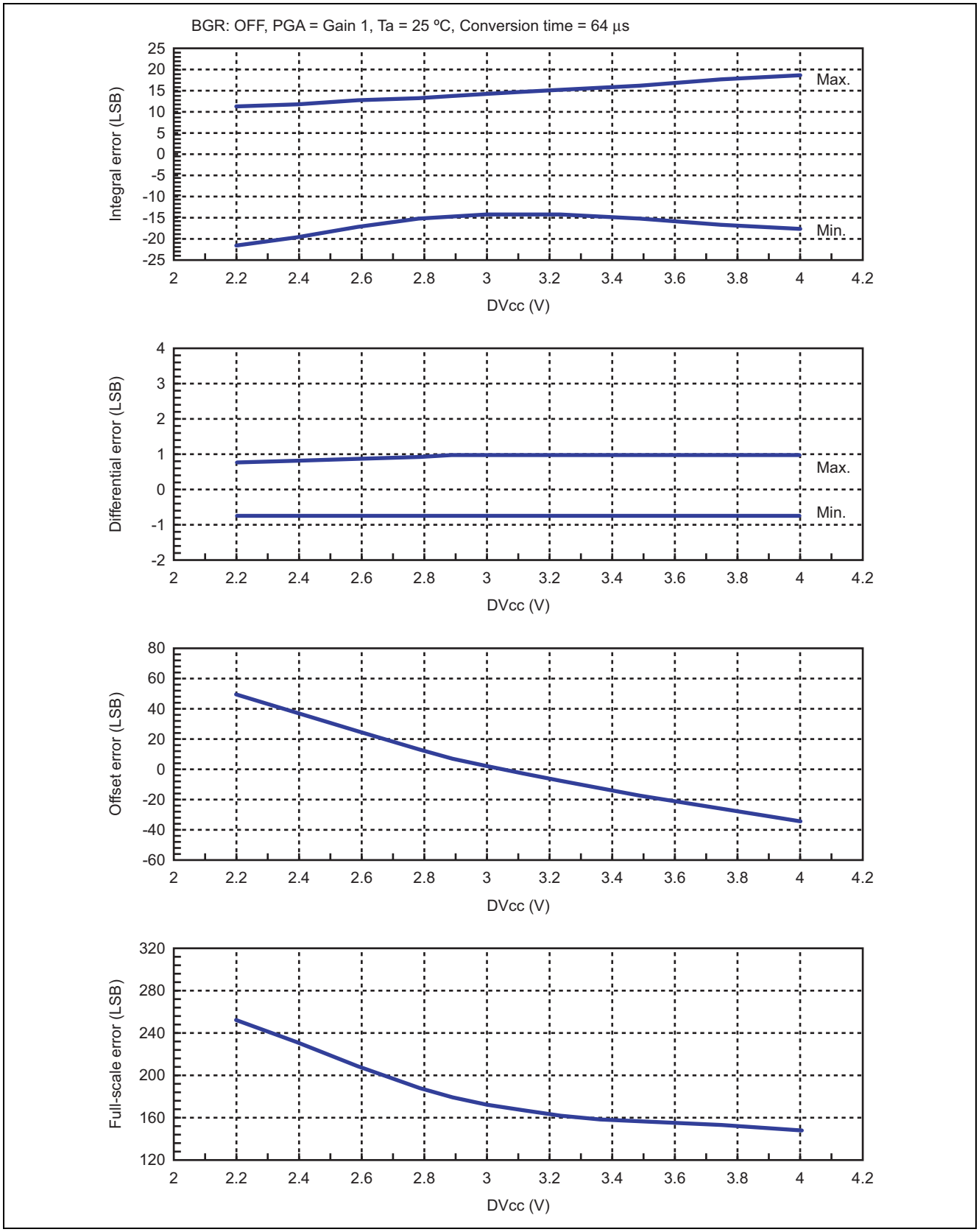


(3) Dependences on DVcc

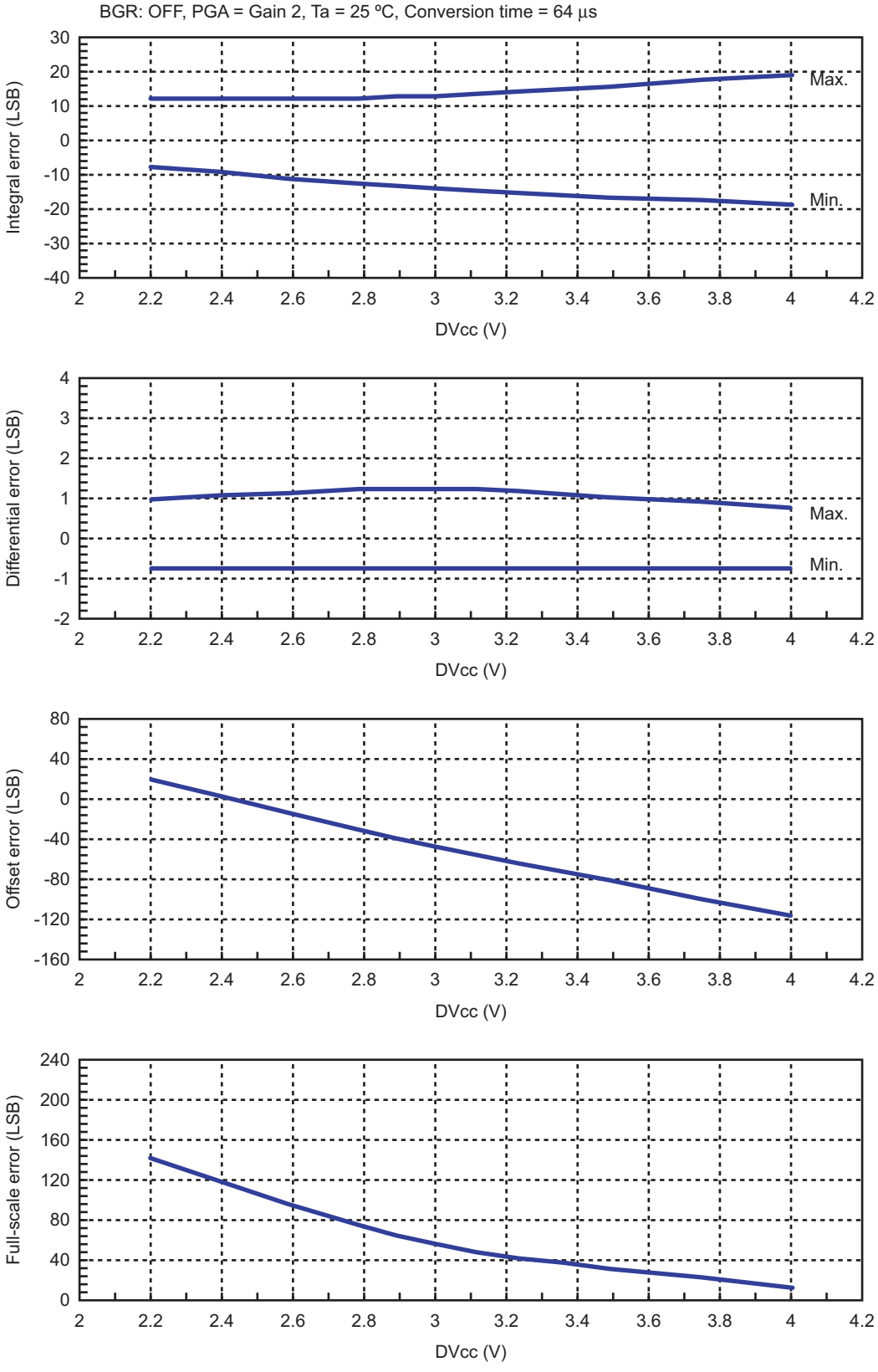
- DVcc dependence 1



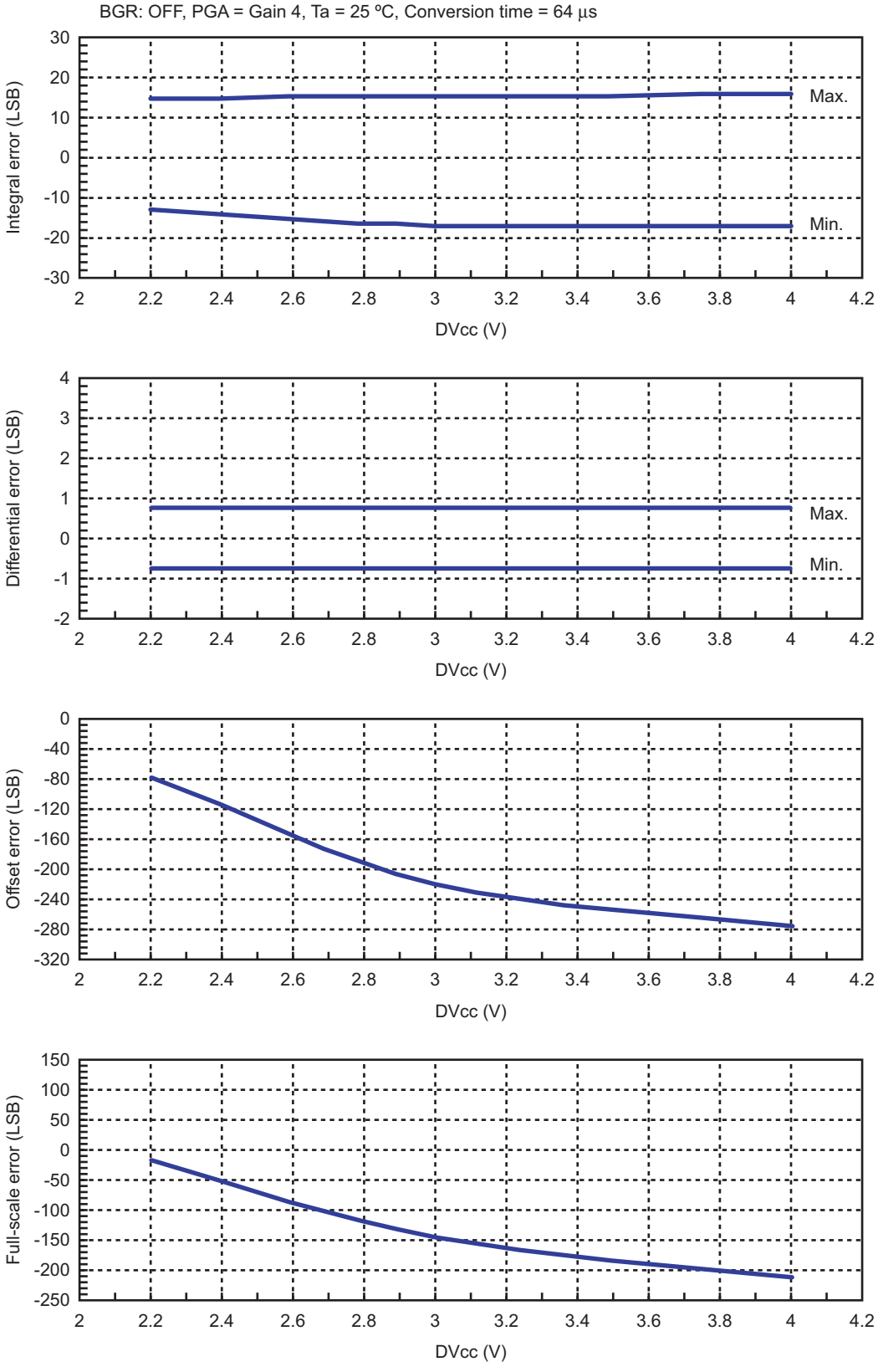
- DVcc dependence 2



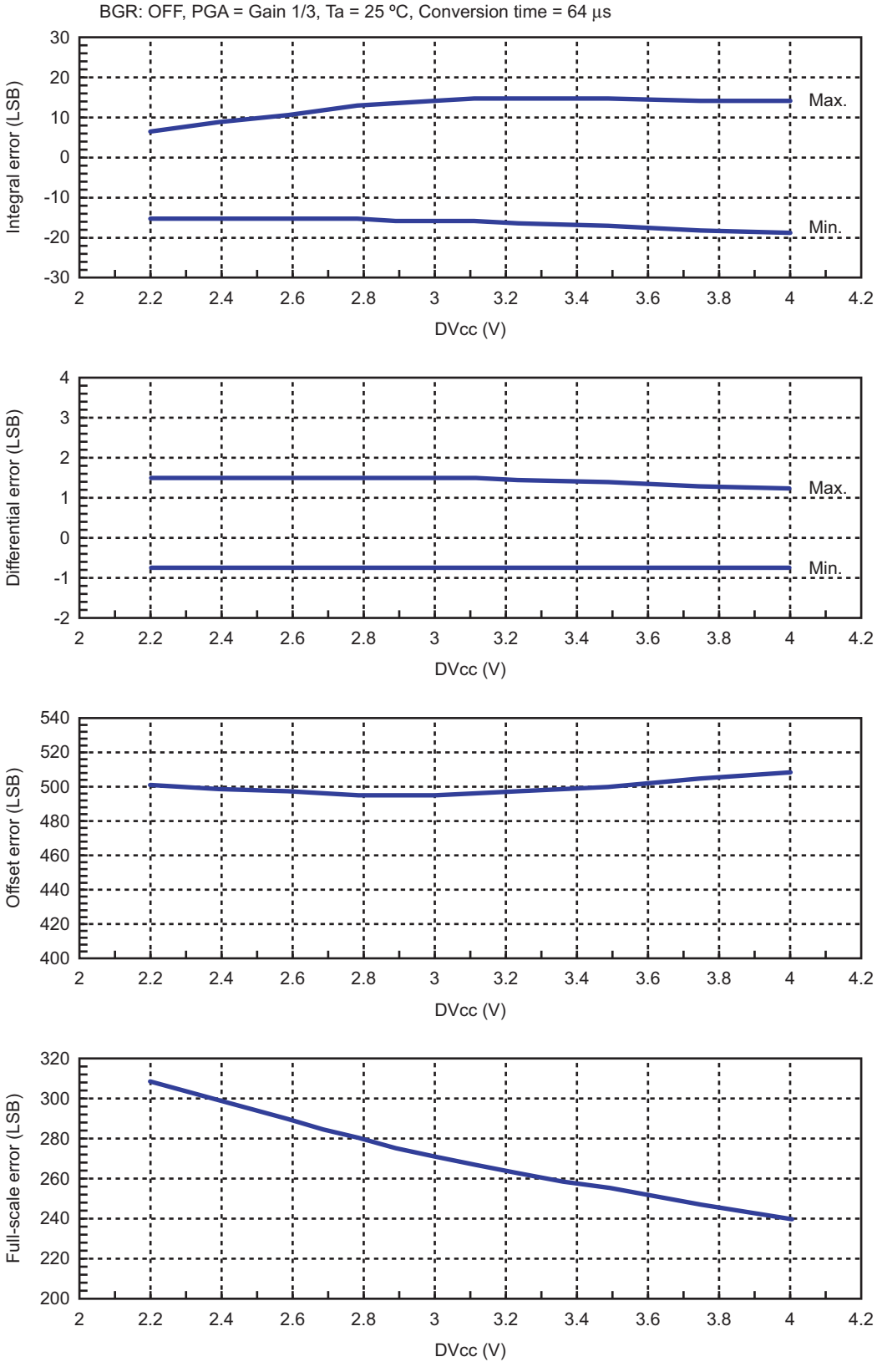
- DVcc dependence 3



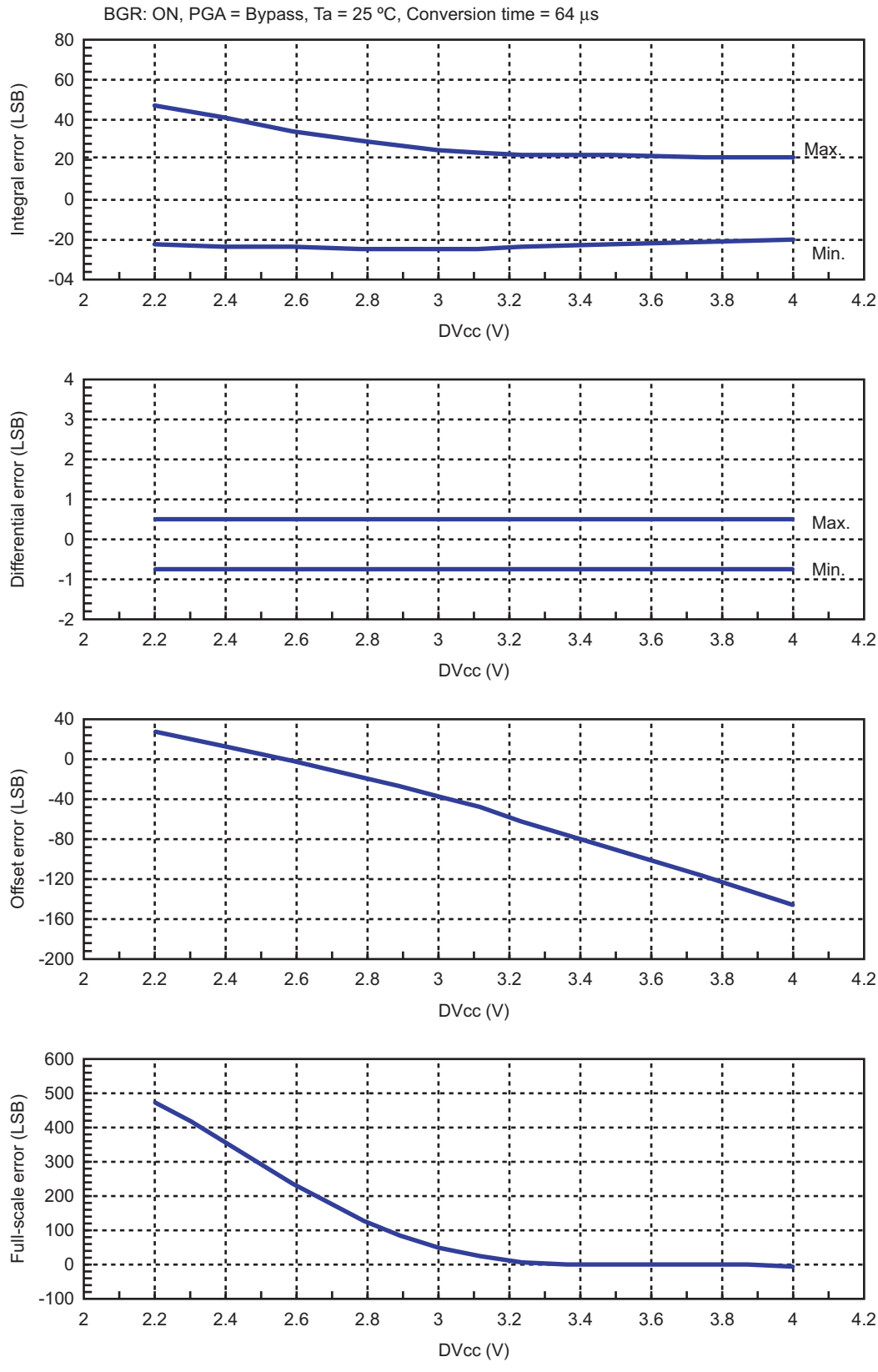
- DVcc dependence 4



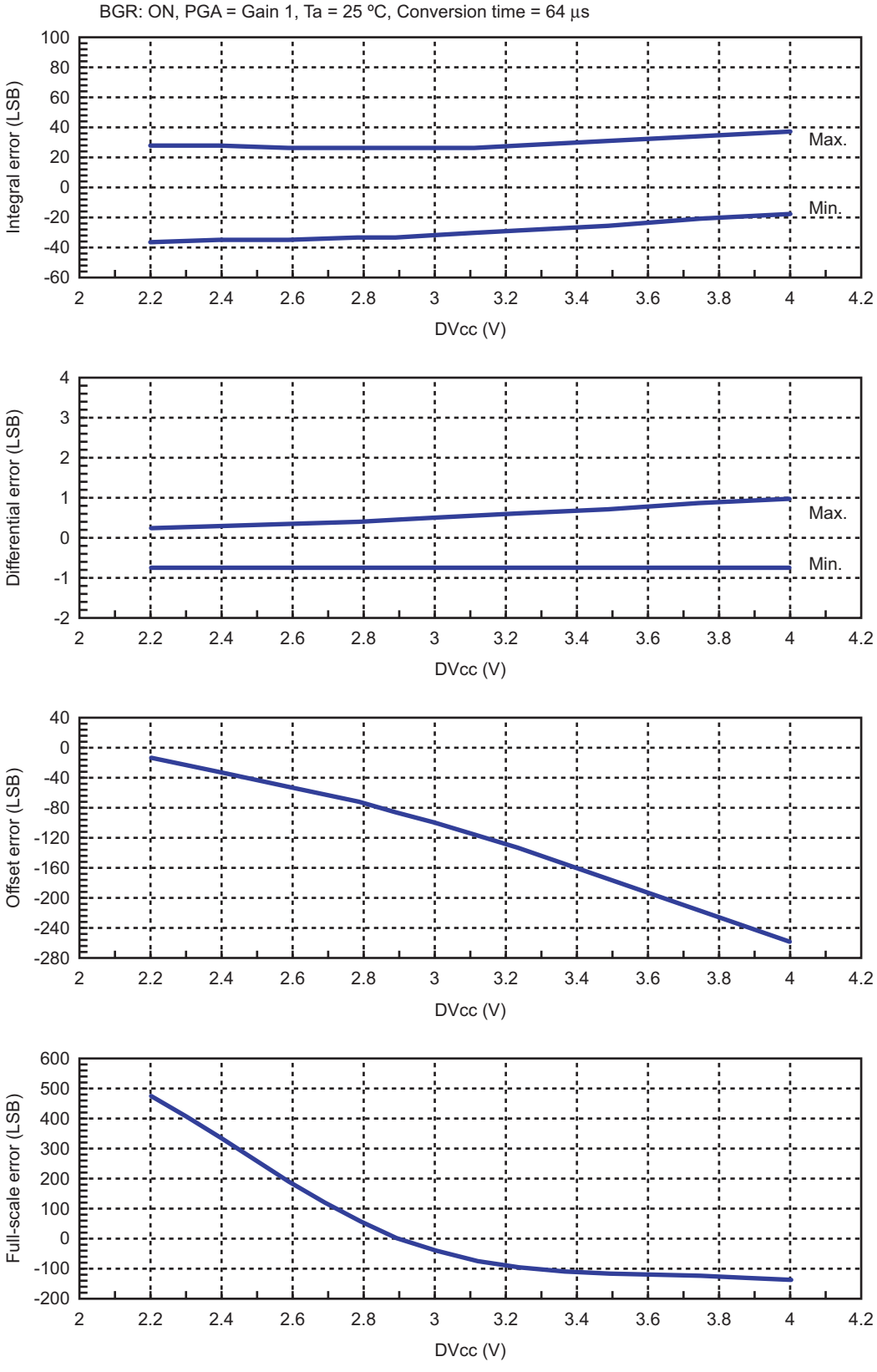
- DVcc dependence 5



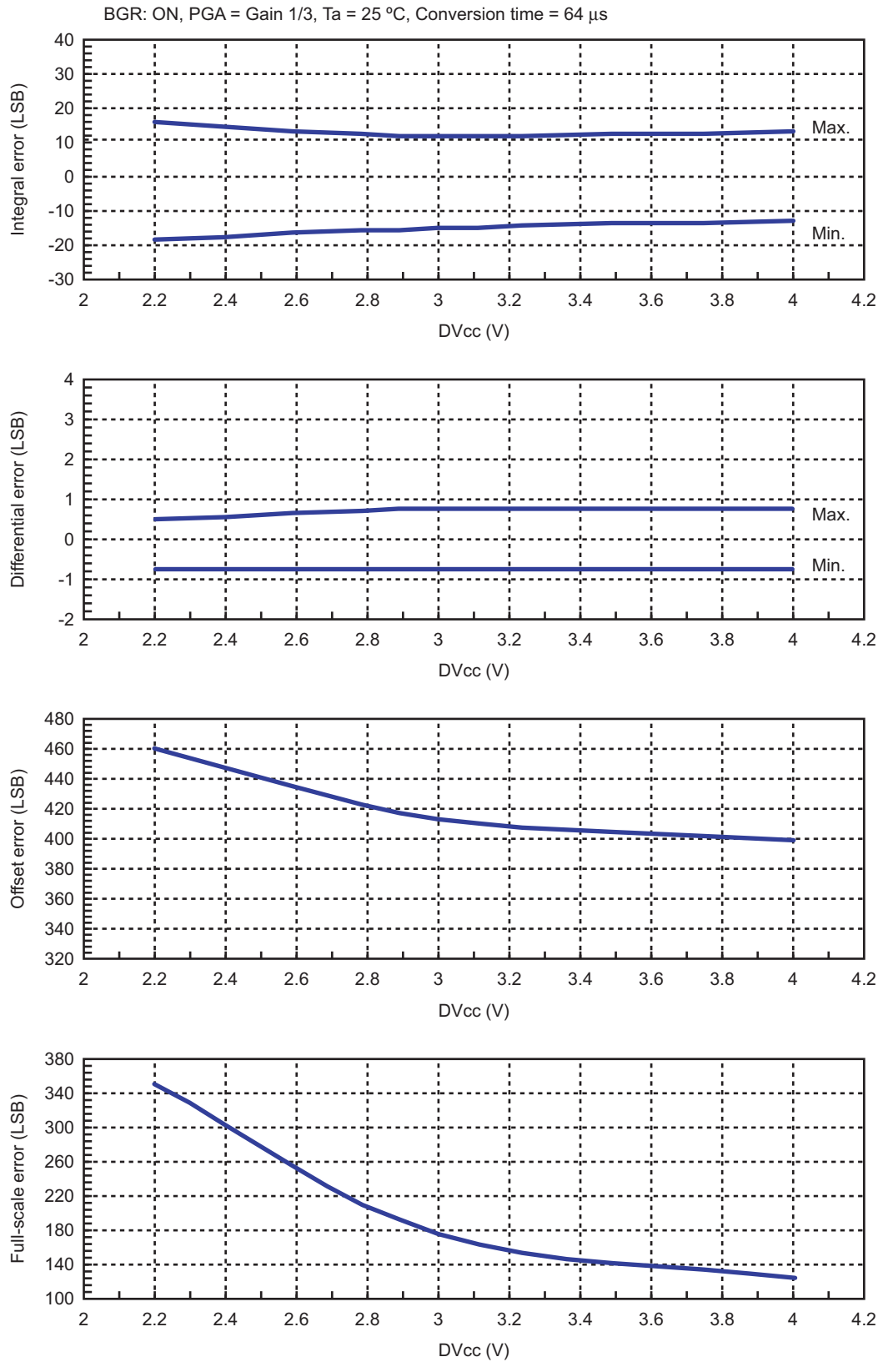
- DVcc dependence 6



- DVcc dependence 7

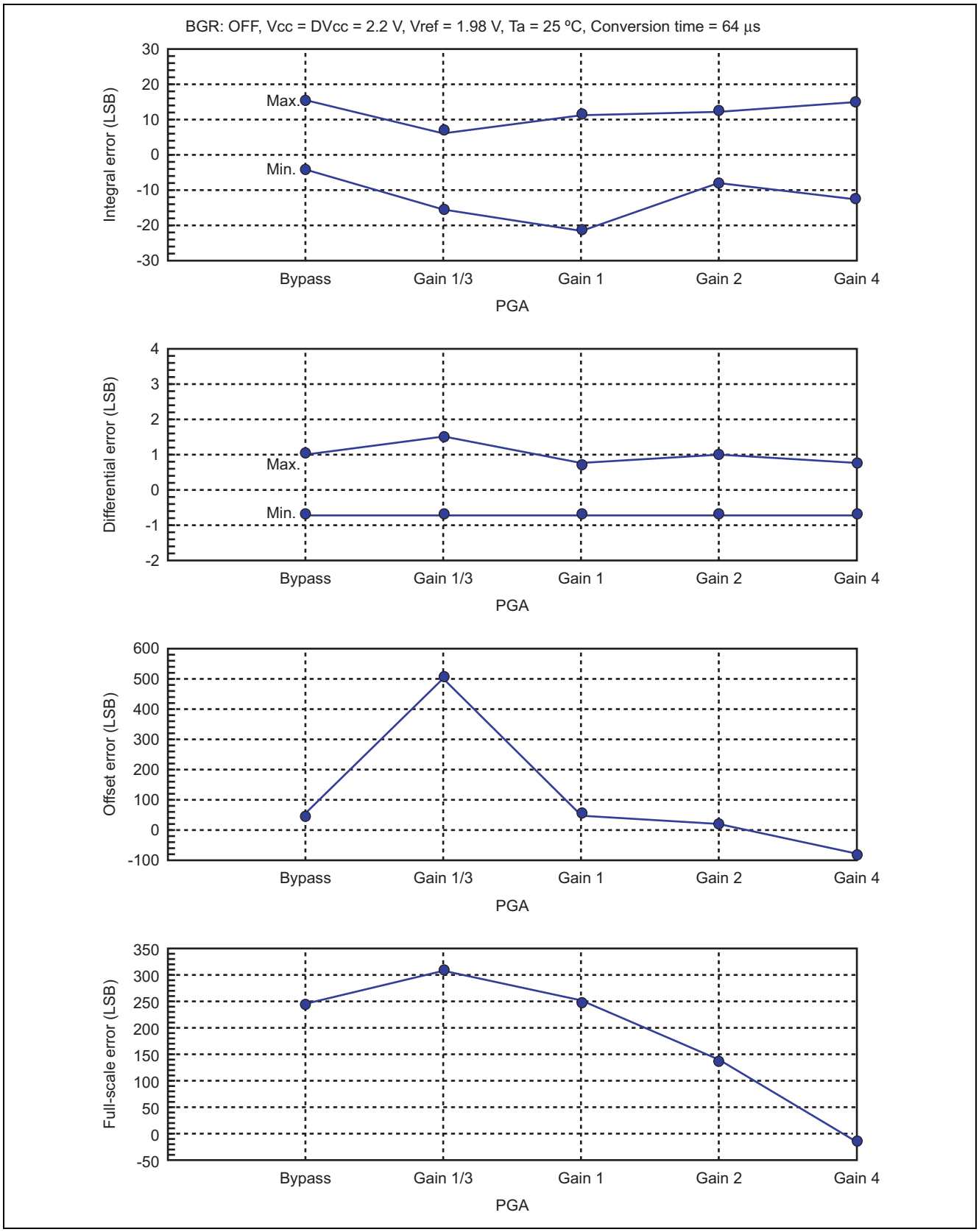


- DVcc dependence 8

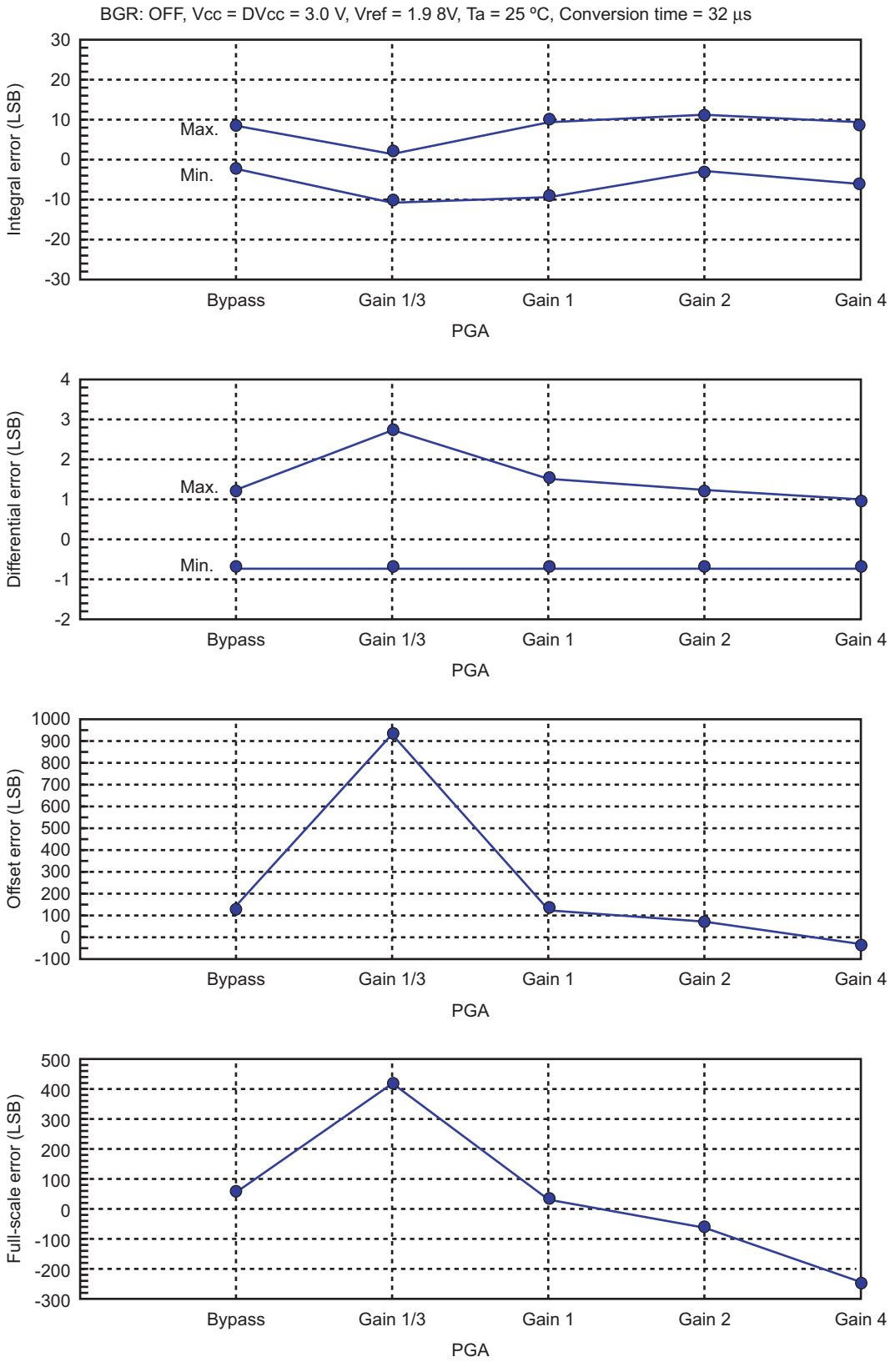


(4) Dependences on PGA Setting

- PGA dependence 1



- PGA dependence 2



7.2 Electric-Current Characteristics

Table 7.2 Current Drawn

Common Conditions

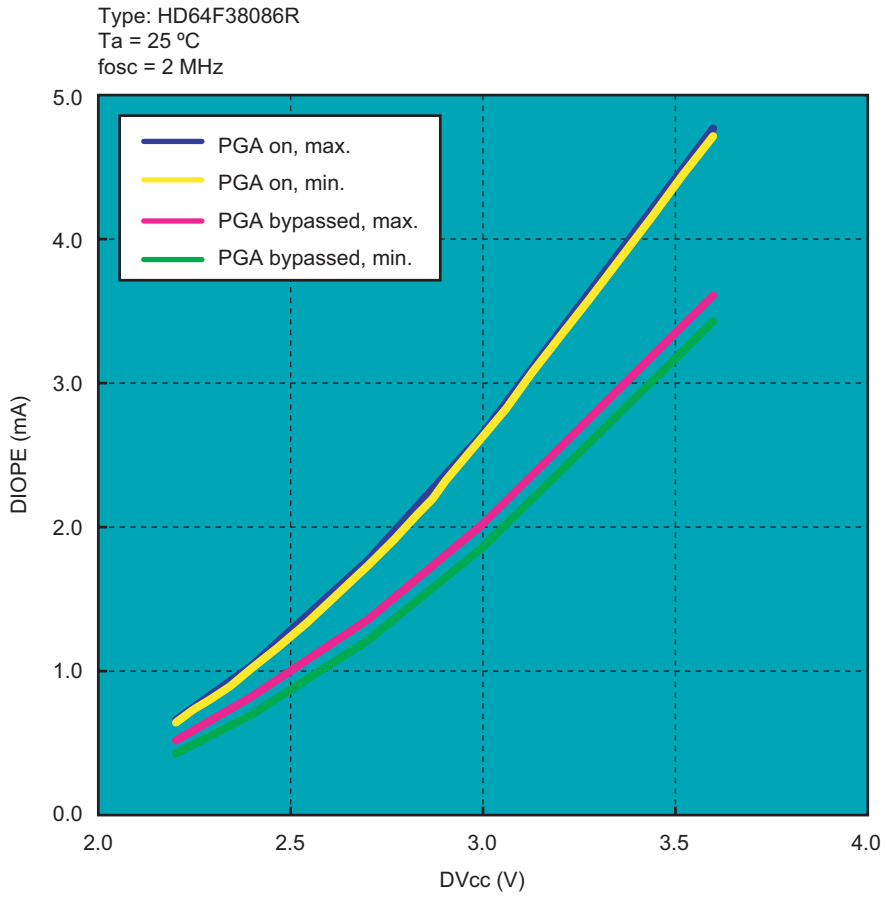
Mode: Active (high-speed) mode
Oversampling frequency (fovs): ϕ

DIOPE: Current drawn from the power supply by the ΔΣ A/D converter
DVcc: Power supply voltage for the ΔΣ A/D converter

No.	Item	Mode	BGR	fovs	fosc (MHz)	Ta (°C)	DVcc (V)
1	DIOPE vs. DVcc (fosc = 2 MHz)	Active (high speed)	Halted	ϕ	2	25	—
2	DIOPE vs. DVcc (fosc = 2 MHz)	Active (high speed)	Running	ϕ	2	25	—
3	DIOPE vs. DVcc (fosc = 10 MHz)	Active (high speed)	Halted	ϕ	10	25	—
4	DIOPE vs. DVcc (fosc = 10 MHz)	Active (high speed)	Running	ϕ	10	25	—
5	DIOPE vs. fosc	Active (high speed)	Halted	ϕ	—	25	3.0
6	DIOPE vs. fosc	Active (high speed)	Running	ϕ	—	25	3.0
7	DIOPE vs. Ta	Active (high speed)	Halted	ϕ	10	—	3.0
8	DIOPE vs. Ta	Active (high speed)	Running	ϕ	10	—	3.0

(1) DIOPE vs. DVcc (fosc = 2 MHz)

Active (high-speed) mode
Continuous mode, BGR halted, fovs = ϕ



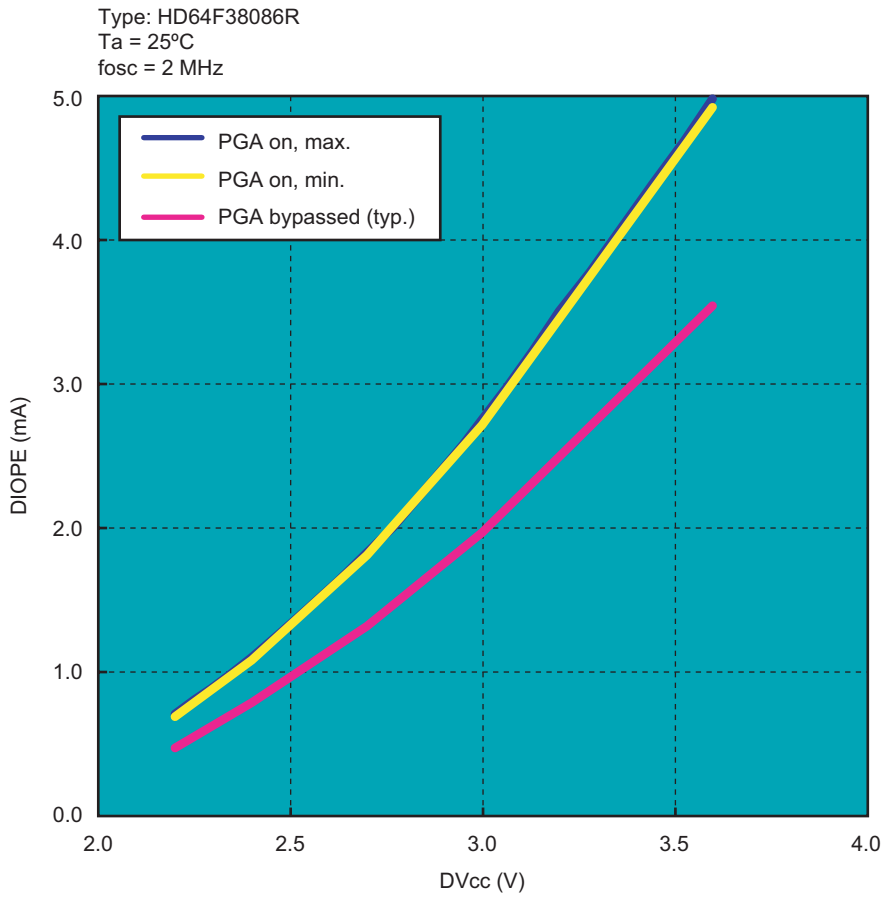
		DVcc (V)				
		2.2	**2.4**	**2.7**	**3.0**	**3.6**
DIOPE (mA)	PGA on, max.	0.66	1.04	1.76	2.64	4.76
	PGA on, min.	0.64	1.02	1.74	2.62	4.72
	PGA bypassed, max.	0.52	0.82	1.36	2.02	3.6
	PGA bypassed, min.	0.42	0.7	1.22	1.86	3.42

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(2) DIOPE vs. DVcc (fosc = 2 MHz)

Active (high-speed) mode

Continuous mode, BGR running, fovs = ϕ



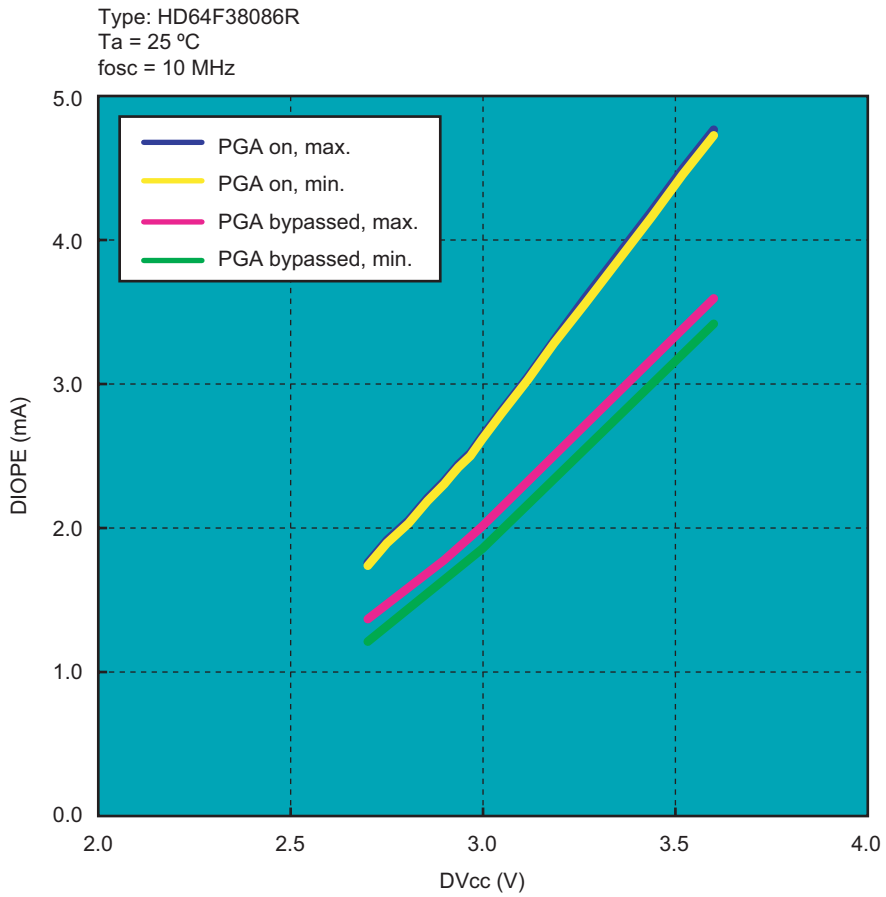
		DVcc (V)				
		2.2	**2.4**	**2.7**	**3.0**	**3.6**
DIOPE (mA)	PGA on, max.	0.7	1.1	1.84	2.76	4.98
	PGA on, min.	0.68	1.08	1.82	2.72	4.92
	PGA bypassed (typ.)	0.48	0.78	1.32	1.96	3.54

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(3) DIPOE vs. DVcc (fosc = 10 MHz)

Active (high-speed) mode

Continuous mode, BGR halted, fovs = ϕ



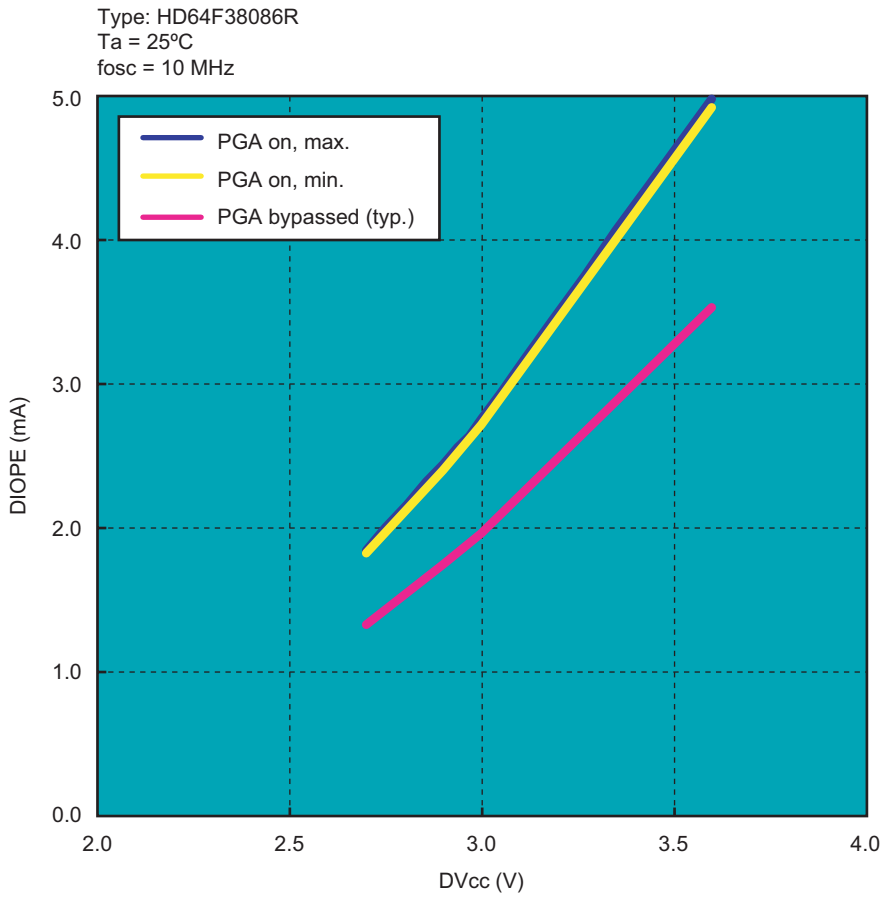
		DVcc (V)			
		2.7	**2.9**	**3.0**	**3.6**
DIOPE (mA)	PGA on, max.	1.76	2.32	2.64	4.76
	PGA on, min.	1.74	2.3	2.62	4.72
	PGA bypassed, max.	1.36	1.78	2.02	3.6
	PGA bypassed, min.	1.22	1.64	1.86	3.42

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(4) DIOPE vs. DVcc (fosc = 10 MHz)

Active (high-speed) mode

Continuous mode, BGR running, fovs = ϕ



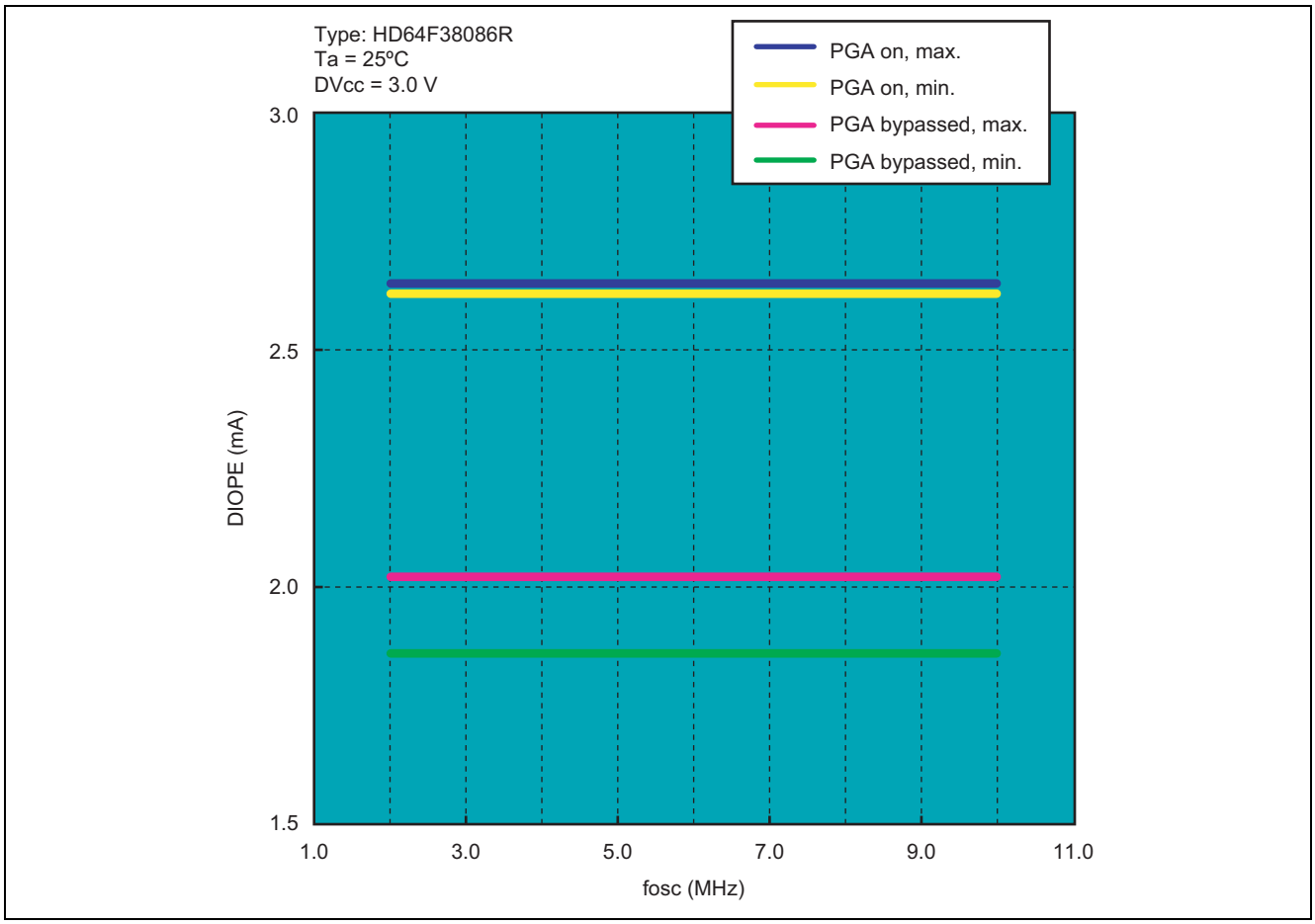
		DVcc (V)			
		2.7	**2.9**	**3.0**	**3.6**
DIOPE (mA)	PGA on, max.	1.84	2.44	2.76	4.98
	PGA on, min.	1.82	2.4	2.72	4.92
	PGA bypassed, typ.	1.32	1.74	1.96	3.54

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(5) DIOPE vs. fosc

Active (high-speed) mode

Continuous mode, BGR halted, fovs = ϕ



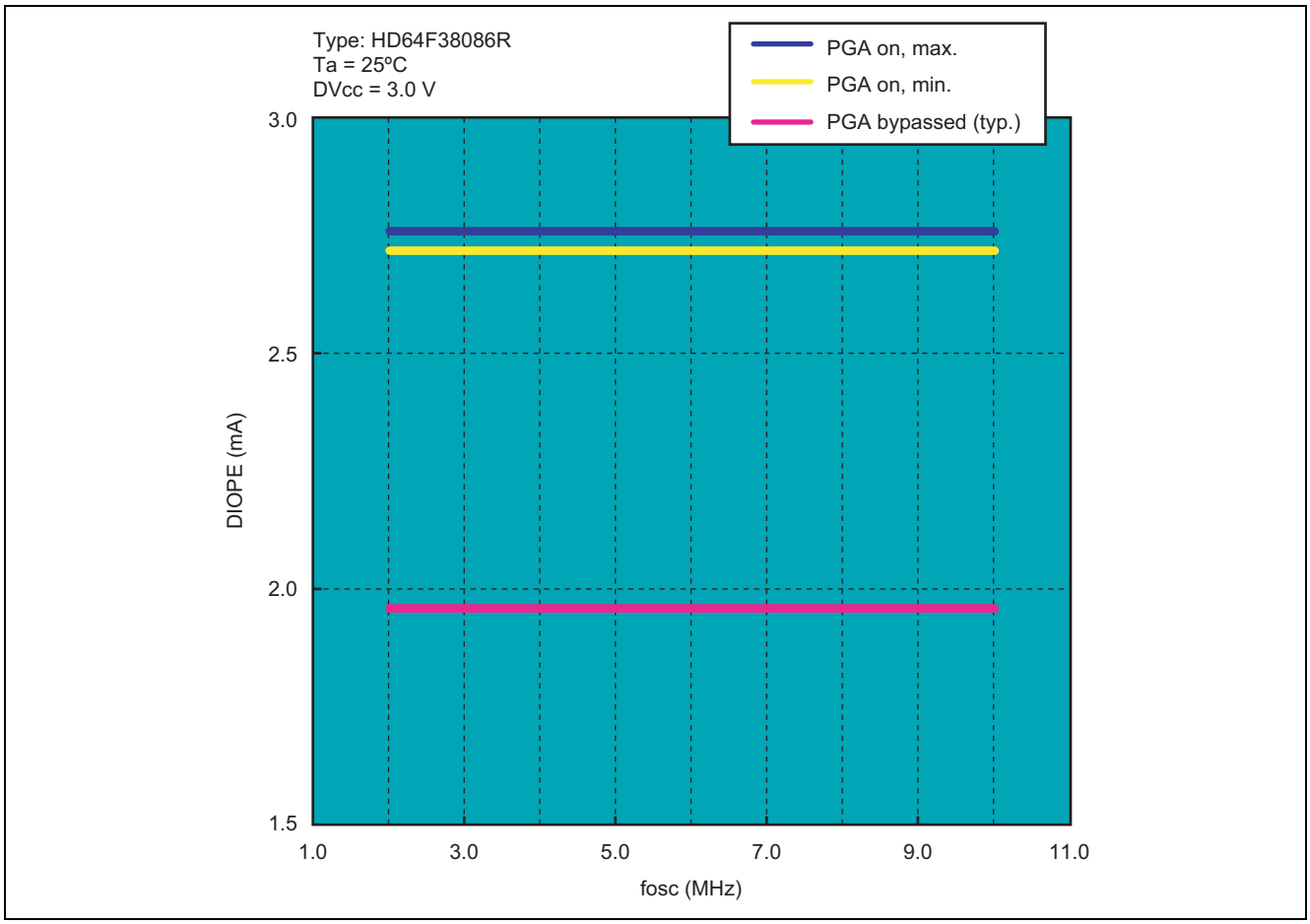
		fosc (MHz)	
		2	**10**
DIOPE (mA)	PGA on, max.	2.64	2.64
	PGA on, min.	2.62	2.62
	PGA bypassed, max.	2.02	2.02
	PGA bypassed, min.	1.86	1.86

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(6) DIOPE vs. fosc

Active (high-speed) mode

Continuous mode, BGR running, fovs = ϕ



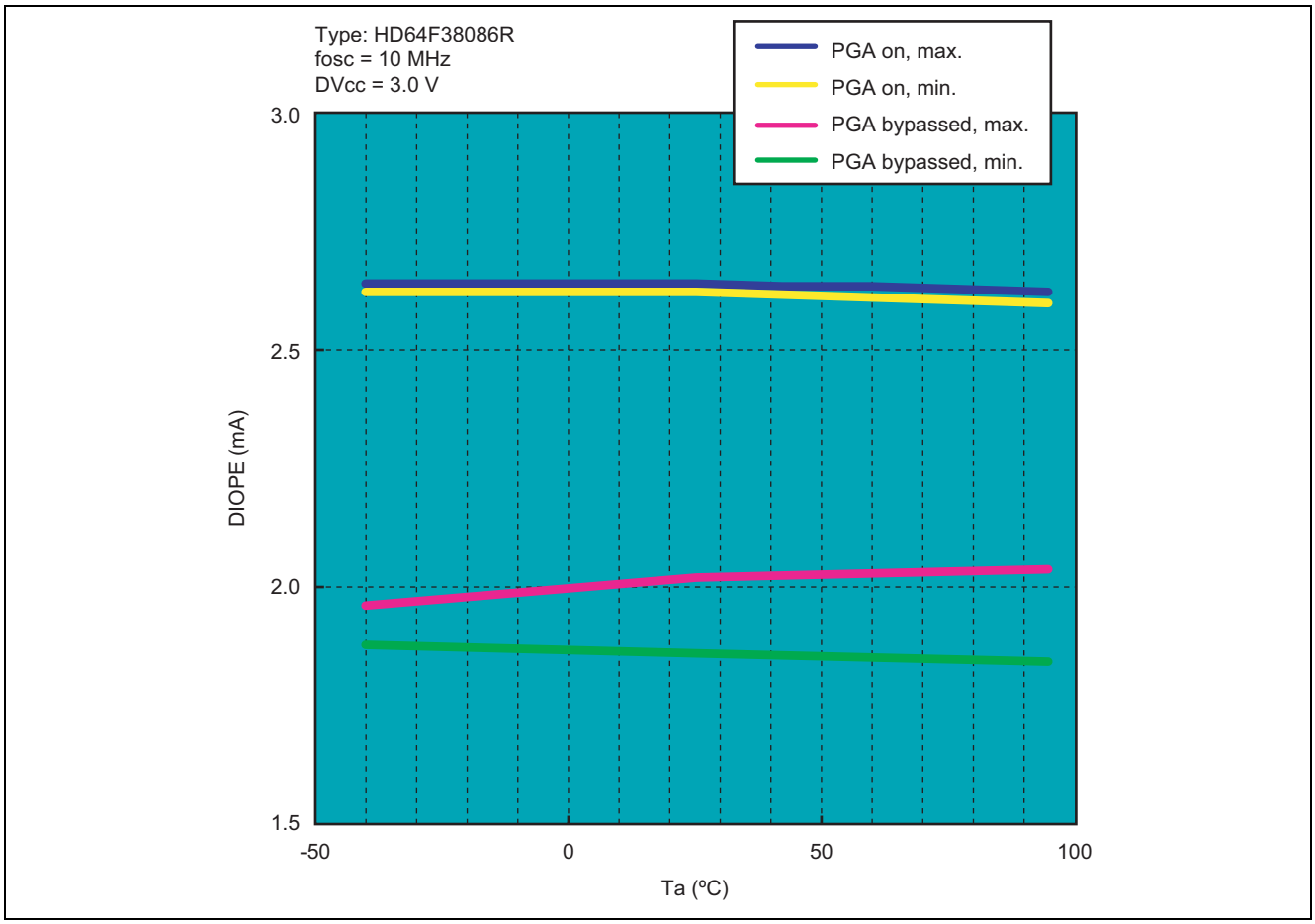
		fosc (MHz)	
		2	**10**
DIOPE (mA)	PGA on, max.	2.76	2.76
	PGA on, min.	2.72	2.72
	PGA bypassed, typ.	1.96	1.96

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(7) DIOPE vs. Ta

Active (high-speed) mode

Continuous mode, BGR halted, fovs = ϕ



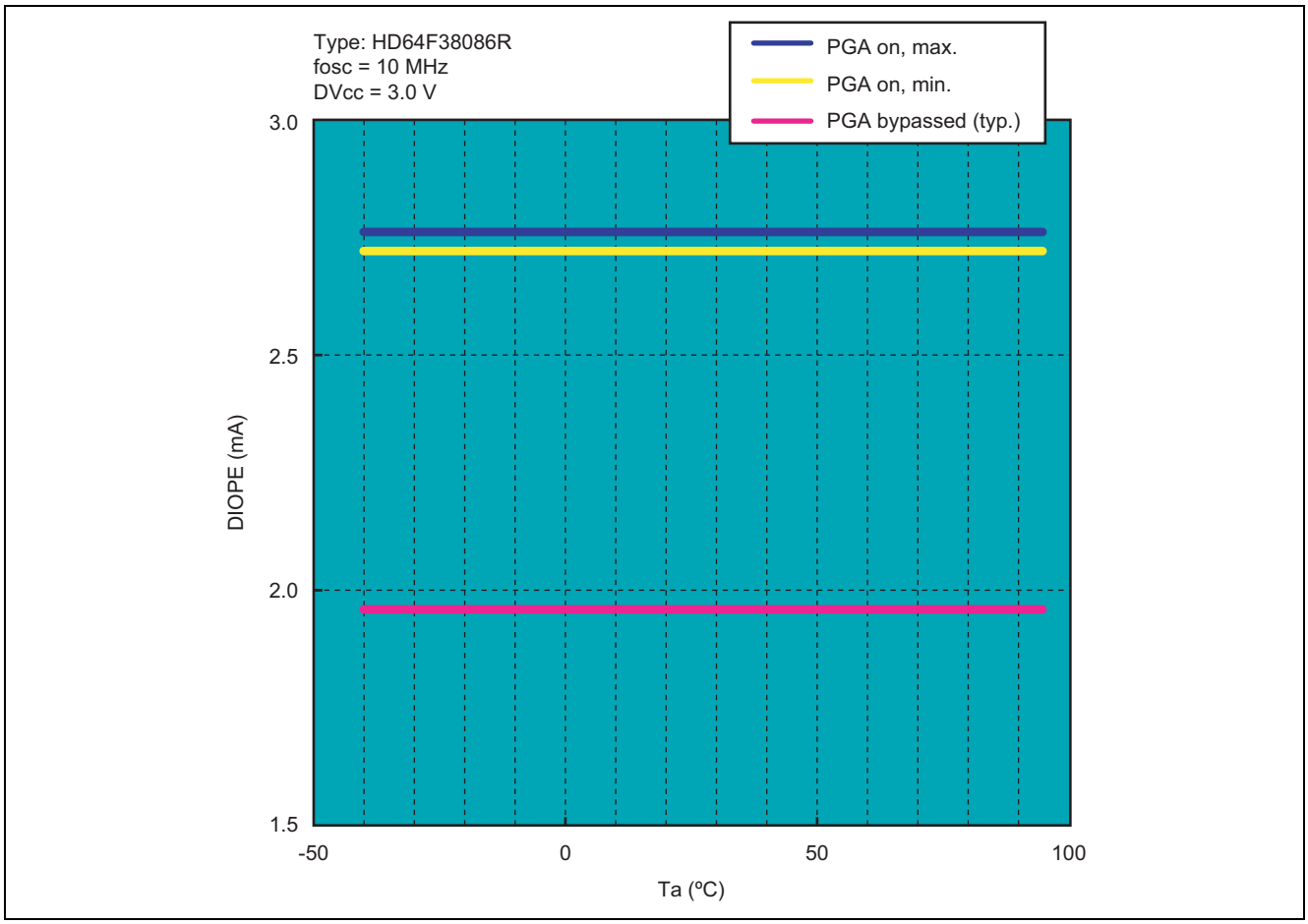
		Ta (°C)		
		-40	**25**	**95**
DIOPE (mA)	PGA on, max.	2.64	2.64	2.62
	PGA on, min.	2.62	2.62	2.6
	PGA bypassed, max.	1.96	2.02	2.04
	PGA bypassed, min.	1.88	1.86	1.84

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

(8) DIOPE vs. Ta

Active (high-speed) mode

Continuous mode, BGR running, fovs = ϕ



		Ta (°C)		
		-40	**25**	**95**
DIOPE (mA)	PGA on, max.	2.76	2.76	2.76
	PGA on, min.	2.72	2.72	2.72
	PGA bypassed (typ.)	1.96	1.96	1.96

Note: All data given above were determined with samples and are for general reference only, i.e. they are not guaranteed values.

7.3 Frequency Characteristics of Digital Filter

Figures 7.2 and 7.3 show the frequency characteristics obtained for the transfer function with an oversampling frequency of 10 MHz.

- Although both figures show the same frequency characteristics, the X-axis is a logarithmic scale in the case of figure 7.3.
- The attenuation is relatively moderate up to a frequency of approximately 70 kHz. Therefore, when aliasing noise is reflected into the region from 70 kHz down, elimination of this noise becomes increasingly difficult at lower frequencies.

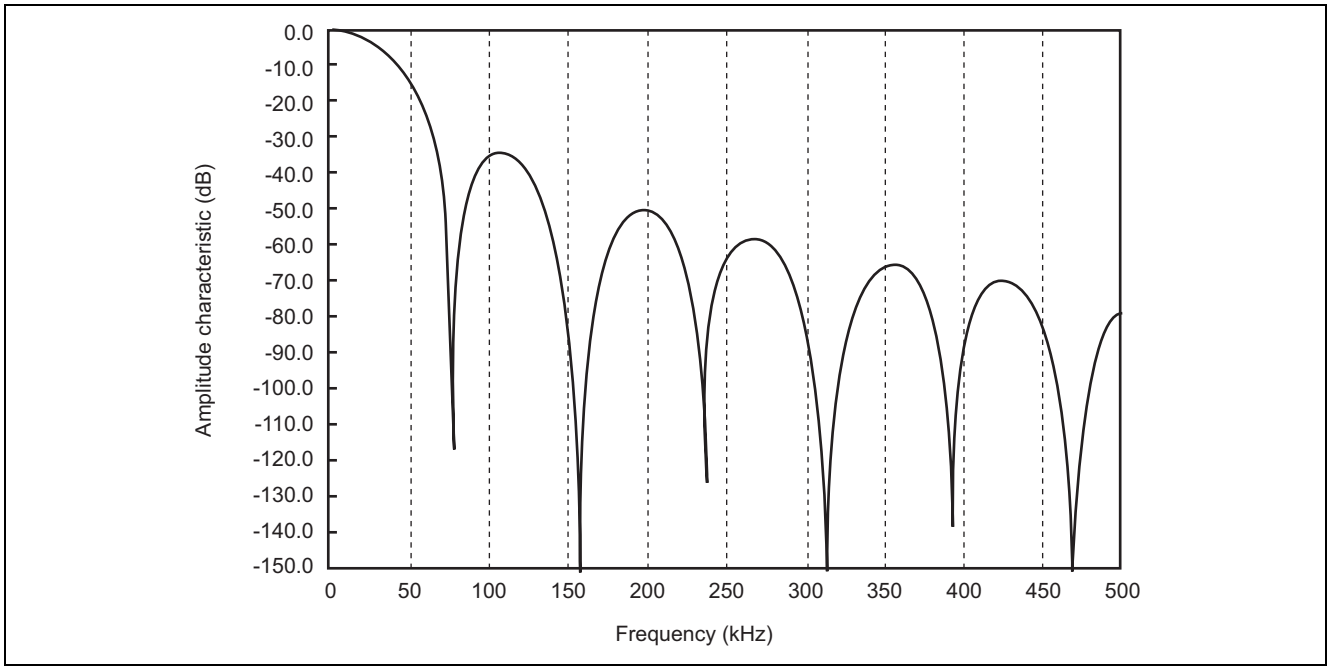


Figure 7.2 Frequency Characteristics of the Digital Filter for the H8/38086R ΔΣ A/D Converter (Oversampling Frequency: 10 MHz) (1)

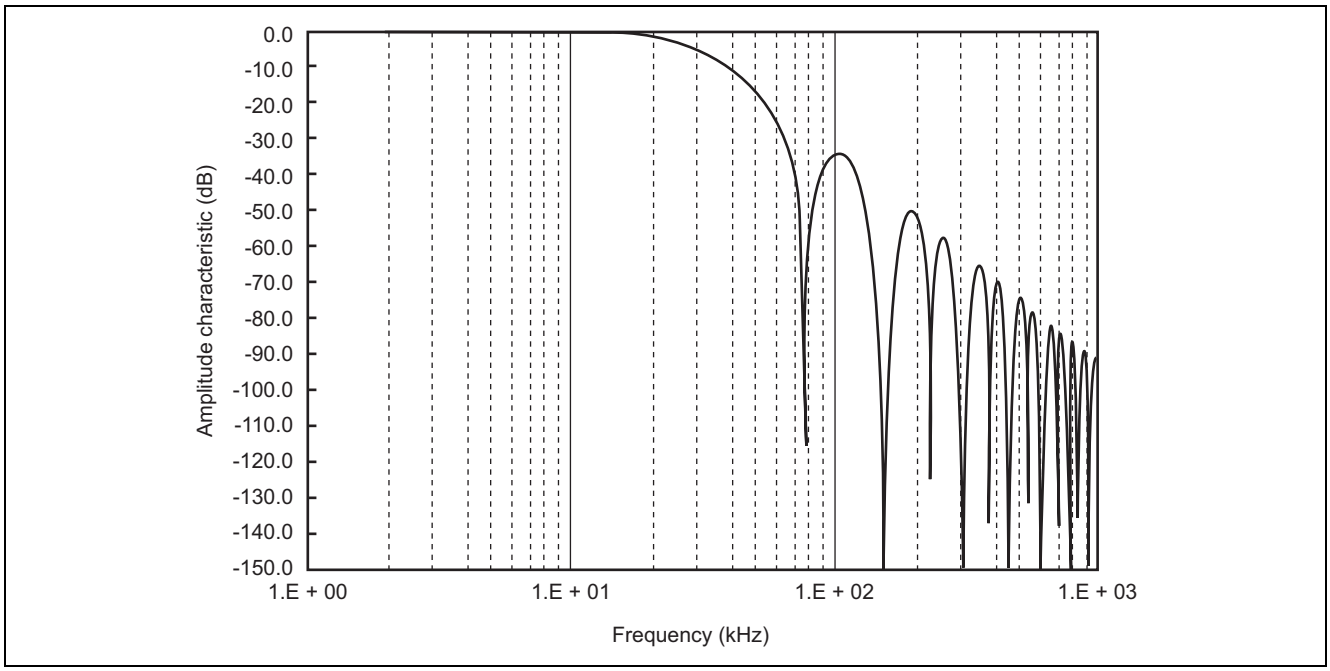


Figure 7.3 Frequency Characteristics of the Digital Filter for the H8/38086R ΔΣ A/D Converter (Oversampling Frequency: 10 MHz) (2)

7.4 REF Output Voltage Characteristics (Rise Time)

(1) Measurement Method

Stabilization time of BGR is the time between setting of BTRSTPN (bit 7) in the BGR control register (BGRMR) and the REF output becoming stable.

To use the H8/38086R's ΔΣ A/D converter, connect a multi-layer ceramic capacitor (0.1 µF) to the internal reference voltage (REF) pin. With this setup, measure the time the output internal reference voltage (BGR output voltage) takes to become stable at 1.2 V.

(2) Measurement Results

The REF output voltage took approximately 70 µs to settle at 1.2 V.

(3) Stabilization Time and Waveform

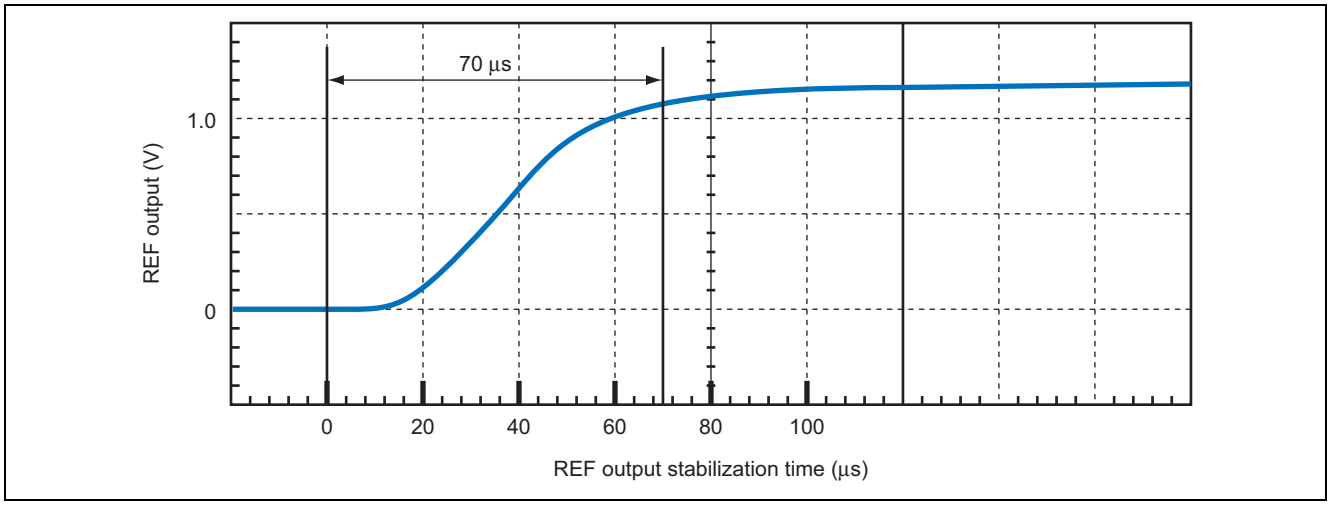


Figure 7.4 Stabilization Time of the REF Output Voltage

(4) Measurement Circuit

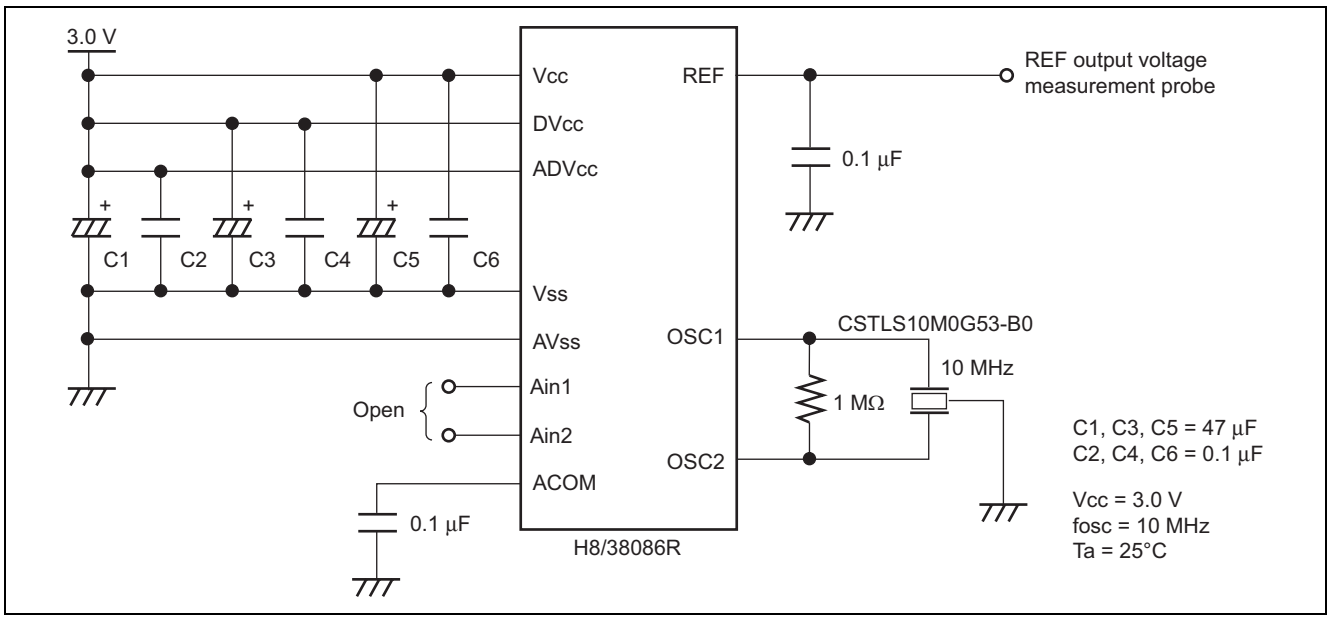


Figure 7.5 REF Voltage Output Characteristic

(5) Usage Note

The REF output pin does not have sufficient driving capability. If the REF voltage is to be used externally, include an element that has a high input impedance to amplify the current.

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Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Dec.19.05	—	First edition
2.00	Sep.21.06	All pages	General Miscellaneous changes for consistency and clarification of descriptions.
		3 to 6	Section 1 Basic Principles of the Delta-Sigma Architecture Updated section name to that given above. Updated figures 1.1 and 1.2. Updated section 1.2.1 for improved readability, including figure 1.4.
		7 to 10	Section 2 ΔΣ A/D Converter Re-worked the entire section as appropriate. Placed description that was formerly section 4, Second-Order ΔΣ A/D Converter in the new section 2.5.
		12, 13	Section 3 Filter Separated out the description of aliasing noise to form the independent section 3.3
		16	Updated section 3.4, including figure 3.8, FIR (Finite Impulse Response) Filter.
		20	Section 4 Errors and Methods of Correction Updated figure 4.5, Relation between the Analog Level (to be Measured) and Digital Value (ADDR Value). Corrected error in equation (3) of section 4.2.1.
		22 to 26	Section 5 Recommended Usage Conditions and Usage Notes Removed the former section 6.1, Ensuring Accurate Conversion. Changed operating conditions of 5.1.1, 5.2.1, and 5.3.1 Re-worked section 5.4, Usage Notes.
		34	Section 6 Application Notes Updated figure 6.5, Relation between the Analog Level (to be Measured) and Digital Value (in ADDR). Corrected the offset error equation in section 6.1.5.
		148	Section 7.2 Electric Current Characteristics Added common conditions to and changed the order of items in table 7.2, Current Drawn.
		157, 158	Section 7.3 Frequency Characteristics of Digital Filter Added figure 7.2, Frequency Characteristics of the Digital Filter for the H8/38086R ΔΣ A/D Converter (Oversampling Frequency: 10 MHz) (1). Corrected the value of resistance (1 MHz) in figure 7.5, REF voltage output characteristic, to 1 MΩ.

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