

Application Note

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

AN-PM-029

Abstract

The Dialog DA9063 Power Management IC (PMIC) provides a complete power solution for DDR3 and DDR3L memory systems. It integrates several synchronous buck converters able to cover the complete power requirements of a DDR3/DDR3L memory system. Any of the internal bucks can be used to supply both core and I/O voltages of the memory.

A dedicated buck (BuckPRO) has been designed to generate a tracking supply voltage for supplying a VTT termination network where it is required. BuckPRO is able to both sink and source current with a fast transient response.

An internal buffered resistive divider generates a high precision reference voltage which tracks the VDDQ supply of the memory and complies with the JEDEC standard (JES79).

The solution covers a wide range of applications including laptops, desktops, tablets and other applications in consumer, industrial and automotive markets.

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

Contents

Abstract	1
Contents	2
Figures	2
Tables	2
1 Terms and Definitions	3
2 Introduction	4
3 DDR3 and DDR3L Power and Termination System Requirements	4
3.1 DDR And Memory Controller Supply:	4
3.2 Memory System Supply	5
3.3 VDDQ, VDD Rails	5
3.4 VTT.....	6
3.5 VREFCA, VREFDQ.....	6
4 Example Application Using DA9063 PMIC	7
5 Buck PRO Transient Performance in VTT Mode	11
6 Summary	12
Revision History	13

Figures

Figure 1: Block Level Diagram of a Generic System with DDR	4
Figure 2: Point to Point Connection.....	7
Figure 3: Typical Supply and DDR3 Termination Using DA9063.....	8
Figure 4: Detailed Schematic Configuration of DA9063 for a DDR3/DDR3L Application	9
Figure 5: Load Transient of BuckPRO in Sink/Source Mode with VTT = 0.75 V	11
Figure 6: Load Transient of Buck PRO in Sink/Source Mode with VTT= 0.675 V	12

Tables

Table 1: DDR3/DDR3L Power Requirements	5
Table 2: DDR3/DDR3L Power Requirements	10
Table 3: Example Component Selection List	10

**Complete DDR3/DDR3L SDRAM Power Solution
Using DA9063**

1 Terms and Definitions

SSN	Simultaneous Switching Noise
SSTL_15	Series Stub Termination Logic
OTP	One Time Programmable Memory

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

2 Introduction

In today's applications the need for large memory and increased data rates, brings challenges to the memory system design. To support these faster data rates requires an increased clock frequency which necessitates fast edges. Additionally, the demand for increased storage capacity leads to denser packaging and more complex interconnects. The result is an increase in signal-integrity concerns such as reflections, distortions, cross-talk, ground bounce, jitter and SSN on the PCB, which cause inter-symbol interference (ISI).

In applications where a large memory is needed the memory supplier will generally recommend implementation of memory termination to mitigate the above concerns. The DA9063 integrates full support for DDR termination. This feature enables a reduction in the overall system cost and in reduced PCB area required to implement the solution.

3 DDR3 and DDR3L Power and Termination System Requirements

Figure 1 shows a typical block diagram of a system with DDR memory where a VRM (Voltage Regulator Module) is used to generate the required power supplies.

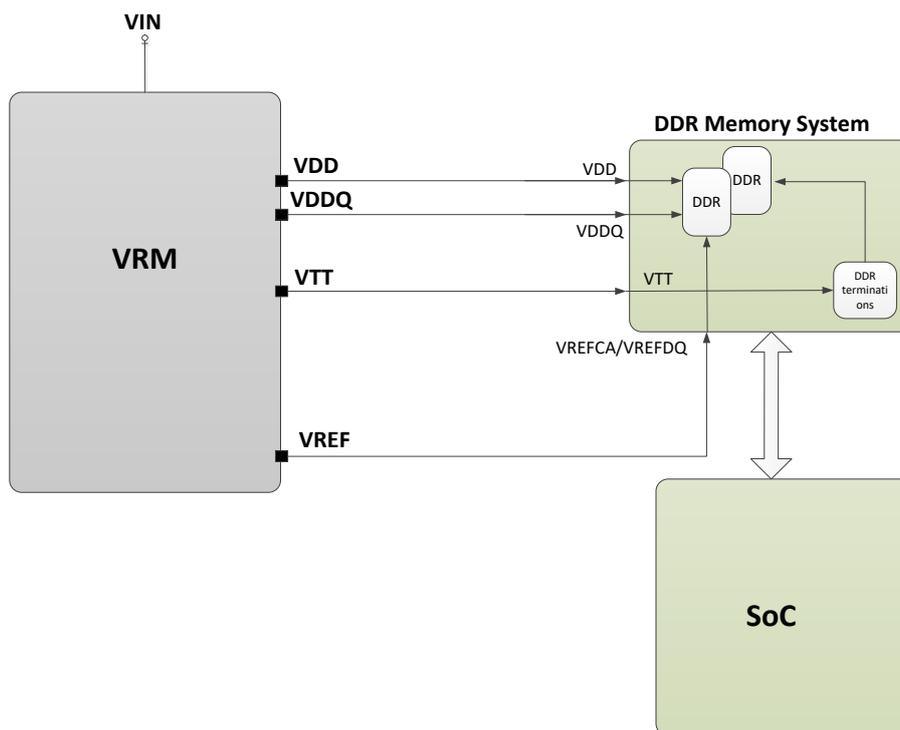


Figure 1: Block Level Diagram of a Generic System with DDR

Specifically, the following supplies are required:

3.1 DDR And Memory Controller Supply:

- VDDQ - I/O supply voltage

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- VDD - Core supply voltage
- VREFCA - Reference voltage for control, command, and address
- VREFDQ - Reference voltage for data

3.2 Memory System Supply

- VTT - Command/address termination voltage

3.3 VDDQ, VDD Rails

These rails can be supplied either independently or from the same regulator.

The current requirement depends upon several factors such as DDR type, density, clock rate, speed grade, bandwidth, number of die in the system and such like. Manufacturers usually provide tools to estimate the power requirement.

Additionally, for correct power up and initialisation of the DDR, the following sequence needs to be applied, as per JEDEC-79 specifications:

Case 1: use of separate VDD and VDDQ rails

1. VDD may be applied without any slope reversal before or at the same time as VDDQ
2. VDDQ may be applied without any slope reversal before or at the same time as VTT, VREFDQ and VREFCA
3. VREFCA, VREFDQ tracks $VDDQ \times 0.5$
4. VTT tracks $VDDQ \times 0.5$

Case 2: use of single power source for both VDD and VDDQ rails

1. Voltage ramp time from 300 mV to VDDmin must be no greater than 200 ms and $VDD > VDDQ$, $VDD - VDDQ < 0.3$ V during the ramp up
2. VREFCA, VREFDQ tracks $VDDQ \times 0.5$
3. VTT tracks $VDDQ \times 0.5$

Typical voltage supply levels for DDR3/DDR3L are summarised in [Table 1](#).

Table 1: DDR3/DDR3L Power Requirements

Nominal Supply (v)	DDR3	DDR3L	Notes
VDDQ	1.5 V \pm 5%	1.35 V (1.283 V – 1.45 V)	
VDD	1.5 V \pm 5%	1.35 V (1.283 V – 1.45 V)	
VREFCA, VREFDQ	0.5 x VDDQ \pm 2%	0.5 x VDDQ \pm 2%	Tracks VDDQ over PVT changes
VTT	0.5 x VDDQ \pm 40 mV	0.5 x VDDQ \pm 40 mV	Tracks VDDQ over PVT changes

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

3.4 VTT

The memory termination voltage VTT requires current at a voltage level as defined in [Table 1](#). It must be generated by a regulator that is able to both sink and source sufficient current.

To comply with JEDEC79 specification, VTT must track variations in VDD/VDDQ over voltage, silicon process, temperature and noise.

The power required for the VTT terminations can be easily calculated once the termination scheme has been determined. An example calculation is given in [Section 4](#).

3.5 VREFCA, VREFDQ

The VREFCA is the reference voltage used to bias the input buffer for address, command and control signals.

The VREFDQ is the reference voltage used to bias the input buffer for data signals.

Both references may be generated from the same power source as long as they are independently routed from the source. The required tolerance must comply with the JEDEC specification.

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

4 Example Application Using DA9063 PMIC

All DDR3 memories present I/O interfaces complying with the SSTL_15 specification. The outputs have a push-pull stage and the inputs a differential stage. This topology was introduced to both reduce the power demand and to facilitate the implementation of a termination network. A memory termination network can mitigate the effects of signal integrity issues reducing the risks of memory instabilities causing a system crash.

Figure 2 shows a typical parallel termination between a DDR controller and a DDR memory in a point to point system configuration.

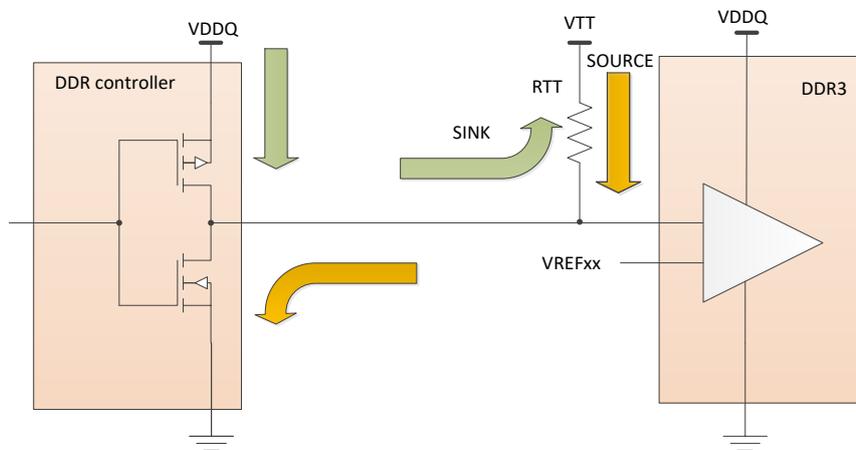


Figure 2: Point to Point Connection

To estimate the VTT current requirement consider a typical memory system using four MT41K128M16JT (2 Gbit = 128Mb x 16), for a total of 1 GByte memory system.

The memory system requires a termination resistor for each of the address, command and control lines:

Address lines [0:13]: 14 lines

Control lines: 3 lines

Command lines: 6 lines

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

The memory system therefore has a total of 23 lines requiring termination. Using the following worst-case operating conditions:

$VDDQ_{max} = 1.575 \text{ V}$ (it is assumed the DDR3L will work in DDR3 compatibility mode)

$VTT_{max} = 0.790 \text{ V}$

$VTT_{min} = 0.710 \text{ V}$

$RDRV = 20 \ \Omega$ (Typical value for max drive strength)

$RTT = 47 \ \Omega$ (Typical values: $25 \ \Omega$ to $50 \ \Omega$)

$VOL \approx 0 \text{ V}$

During the addressing phase, the driver output logic level will be “low” (VTT regulator sourcing) or “high” (VTT regulator sinking):

When VTT is sourcing, the current supplied will be $(VTT_{max} - VOL) / (RTT + RDRV) = 12 \text{ mA}$.

When VTT is sinking, the current supplied will be $(VDDQ_{max} - VTT_{min}) / (RTT + RDRV) = 13 \text{ mA}$

Therefore, the total current demand from the VTT regulator will be:

$13 \text{ mA} \times 23 = 299 \text{ mA}$ when sinking

$12 \text{ mA} \times 23 = 276 \text{ mA}$ when sourcing

The above estimates are likely to be conservative as the bus address will normally present a balanced number of high and low signals.

In general, the transient current demand will depend on various factors such as RTT value, number of DDR devices in the platform and memory configuration.

The DA9063 is well-suited to such applications since it provides a fast transient response buck for the VTT rail and a high precision reference supply for the VREF rail. A typical application using the DA9063 PMIC is shown in [Figure 3](#).

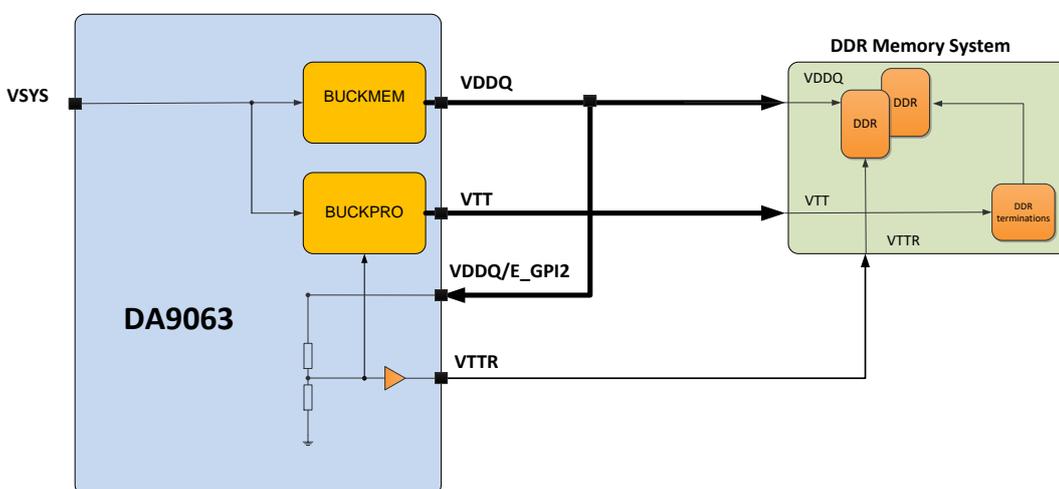


Figure 3: Typical Supply and DDR3 Termination Using DA9063

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The DA9063 memory termination feature is enabled by programming the VTT mode enable bit in the OTP.

As shown in [Figure 3](#), the reference voltage VTTR is generated via an internal divider and then buffered. The internal buffer decouples the divider from the external load, ensuring the precision required by the JEDEC-79 specification.

In the application example of [Figure 4](#), BUCKMEM is configured as the memory core supply rail (VDDQ) and fed back into BUCKPRO via the VDDQ pin. BUCKPRO is then referencing VDDQ for the generation of the two supply rails for the DDR memory, VTT and VTTR.

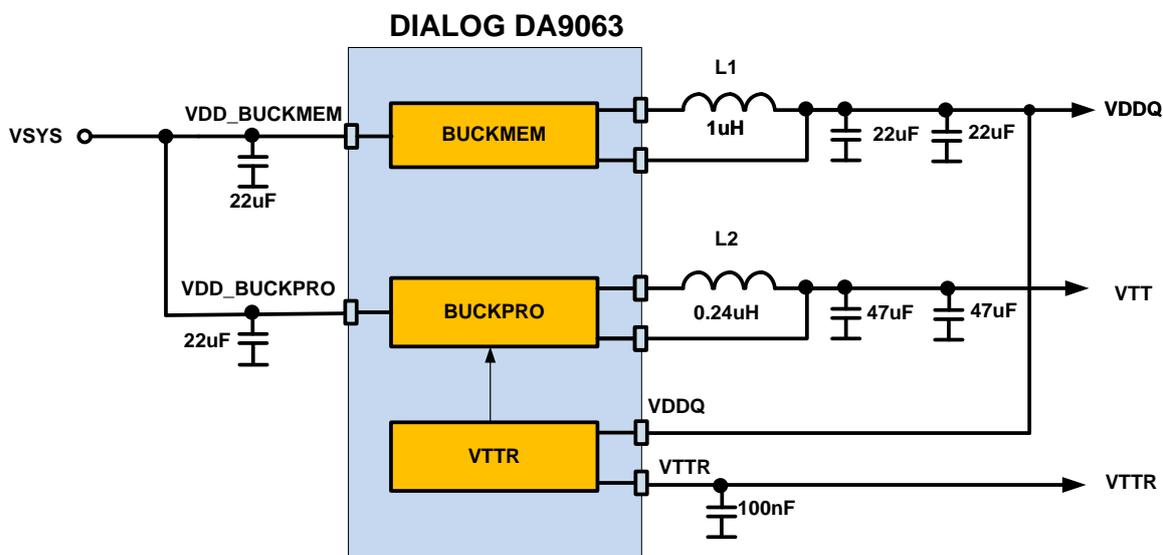


Figure 4: Detailed Schematic Configuration of DA9063 for a DDR3/DDR3L Application

To implement the termination feature supported by DA9063, Dialog recommends that the connections and the external components are selected and connected as shown in [Figure 4](#).

The recommended inductor value when BUCKPRO is used in VTT mode is a 0.24 µH.

For the VDDQ supply, 2 x 47 µF decoupling capacitors are recommended.

A 100 nF decoupling capacitor should be fitted to the VTTR output rail.

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

External components recommendations are provided in [Table 2](#).

Table 2: DDR3/DDR3L Power Requirements

Connection	Component	Description
VTTR	100 nF	Decoupling capacitor
VDDQ - output	1 uH	Inductor with Isat > 2200 mA
	2x 22 uF	Decoupling capacitor
VTT	0.24 uH	Inductor with Isat > 4000 mA
	2x 47 uF	Decoupling capacitor

[Table 3](#) provides example parts currently available from manufacturers.

Table 3: Example Component Selection List

Ref	Description	Manufacturer	Part number	Notes
	BuckPro			
L2	0.24 uH SMD 5 A inductor	Samsung TDK	CIGT201610HMR24M NR VLS201610HBX-R24M	Output inductor
C	47 uF 0805 SMD ceramic capacitor 6.3 V X5R	MuRata	GRM219R60G476M	Output capacitors
	BUCKMEM			
L1	1.0 uH SMD 3.5 A inductor	TDK	TFM252010A-1R0M	Output inductor
C	22 uF 0603 SMD ceramic capacitor 6.3 V X5R	MuRata	GRM188R60J226MEA 0	Output capacitors
	VTTR			
C	100 nF 0402 SMD ceramic capacitor 10 V X5R	MuRata	GRM155R61A104KA0 1D	Output capacitors

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

5 Buck PRO Transient Performance in VTT Mode

Figure 5 illustrates a load transient with a load step of -1250 mA/+1250 mA, under the following test conditions:

$$V_{SYS} = 3.6 \text{ V}$$

$$V_{TT} = 0.75 \text{ V}$$

Similarly, **Figure 6** shows a load transient with a load step of -900 mA/+900 mA, under the following conditions:

$$V_{SYS} = 3.6 \text{ V}$$

$$V_{TT} = 0.675 \text{ V}$$

In the following plots the green trace is the load transient and the blue is the output voltage load transient response of BuckPRO. In both cases V_{TT} is within the specified requirement of $\pm 40 \text{ mV}$ as per JEDEC-79 requirement.

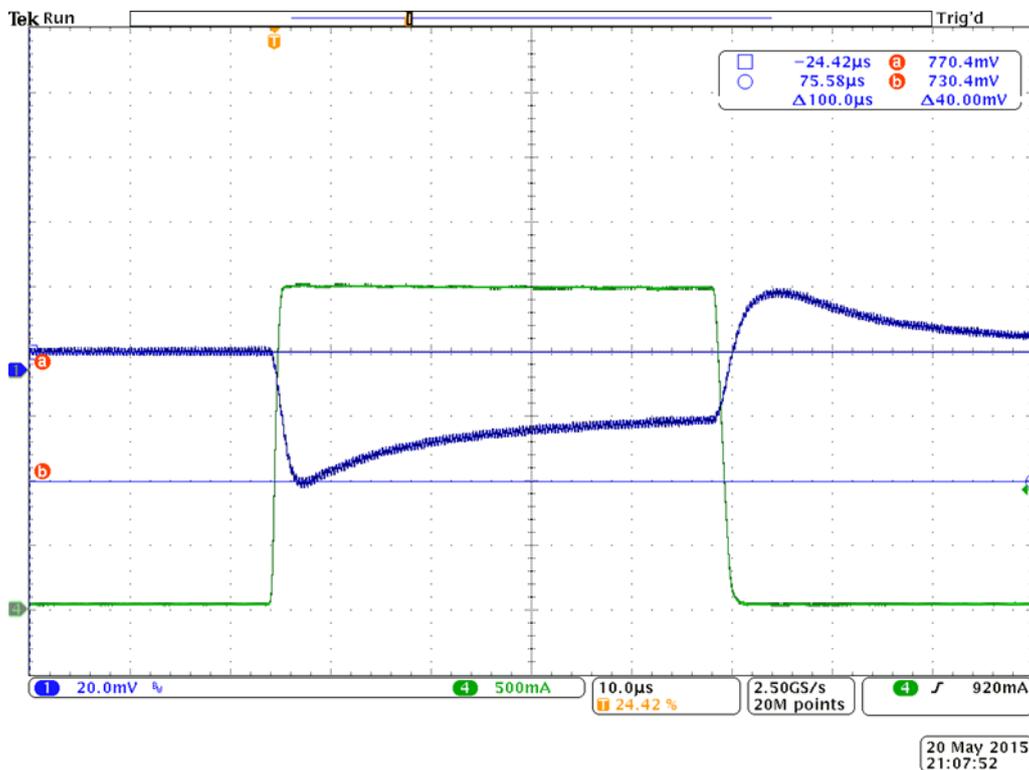


Figure 5: Load Transient of BuckPRO in Sink/Source Mode with $V_{TT} = 0.75 \text{ V}$

Complete DDR3/DDR3L SDRAM Power Solution Using DA9063

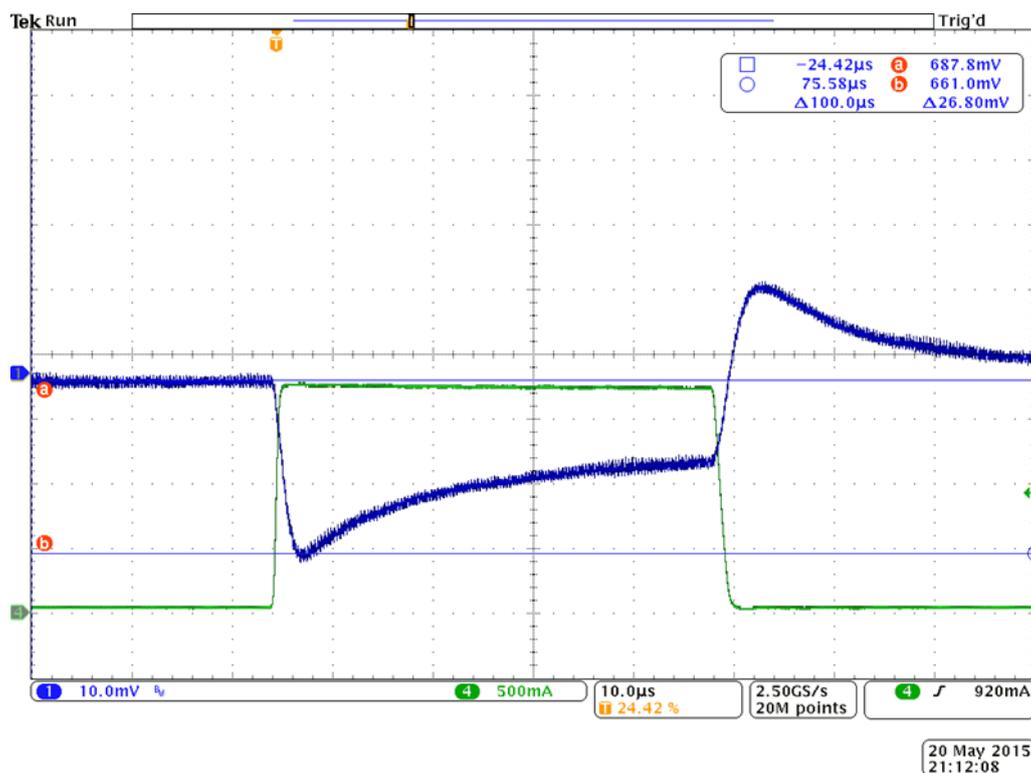


Figure 6: Load Transient of Buck PRO in Sink/Source Mode with $V_{TT} = 0.675\text{ V}$

6 Summary

It has been shown that the integrated V_{TT} Mode of the DA9063 is an optimal solution for management of DDR3/DDR3L memory components. This enables a reduction in the overall system cost and reduced system PCB area.

**Complete DDR3/DDR3L SDRAM Power Solution
Using DA9063****Revision History**

Revision	Date	Description
0.1	26-Feb-2015	Initial version.
1.0	27-May-2015	Added load transient plots
2.0	27-May-2015	Update to new corporate template
3.0	16-Feb-2022	File was rebranded with new logo, copyright and disclaimer

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