Daughter cards for evaluating Renesas's PQFN88 and PQFN56 packaged devices in TO-220 Sockets

1. Overview

This application note describes Renesas's (TPH) TPHDC001 PQFN daughter card and its purpose. The TPHDC001 can be used as a generic carrier to install and evaluate current TPH PQFN 8x8 and PQFN 5x6 GaN devices in existing Si evaluation boards that uses TO-220 Si packages. The main driving point is to quickly observe the performance of the TPH GaN technology in the different Si based topologies or applications.

Renesas's PQFN (Power Quad Flatpack No Lead) package incorporates a DPC (Direct Plated Cu) substrate and a Cu lead frame encapsulated in a green molding compound for bottom electrical connection and thermal contact to the printed circuit board [1].

The most current TPH PQFN devices are listed in the chart below.

TPH Product	TYPICAL Rdson (mOhm)	PACKAGE TYPE
TP65H300G4LSG	300	PQFN88
TP65H150LSG	150	PQFN88
TP65H070LSG	72	PQFN88
TP65H480G4JSG	480	PQFN56

Chart 1. TPH PQFN devices

See the Renesas website https://www.Renesasusa.com/en/products for the detailed list and datasheets of Renesas's PQFN devices.

On behalf of the traditional Si-MOSFET, the metal tab of the PQFN device is Drain, as the bottom of the die is always the Drain terminal. For Renesas's GaN PQFN devices, the metal tab is the Source terminal. GaN FETs have much higher dv/dt switching speed. Refer to figure 1 and figure 2 for package representation.

Figure 1. TPH PQFN 8x8

Figure 2. TPH PQFN 5x6

2. Circuit Parameters and PCB Layout

The TPHDC001 daughter card makes it convenient for Engineers to examine TPH GaN PQFN devices in their existing TO-220 Si application designs.

The output terminals of this daughter-card carrier is configured as GDS so that it can fit the common TO-220 socket design. See figure 3 for the TPHDC001 schematic and figure 4 for the TPHDC001 PCB layout.

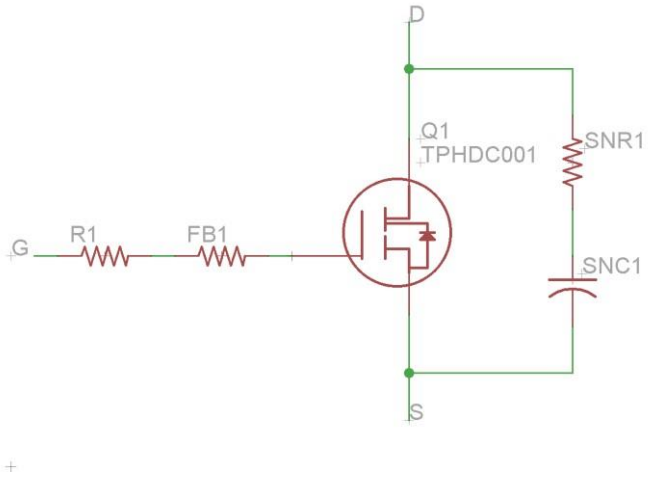
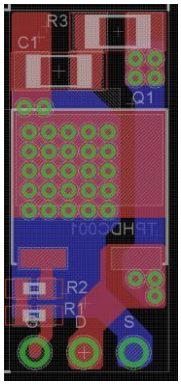


Figure 3. TPHDC001 Schematic



G D S

Figure 4. TPHDC001 PCB Layout (GDS output terminal) The PCB specifications for the daughter card are below:

- Dimension: 0.322in x 0.7389in
- Thickness: 0.062in
- 2 layers - 1 ounce copper each layer
- FR4 material
- Footprints for Rg, FB, and Snubber are included

The exposed copper pads on figure 4 are designed to accommodate the TPH PQFN 8x8 and 5x6 devices. Renesas offers a single landing pattern for both types of PQFN devices offered. See figure 5 for the bottom side view of the TPH PQFN devices.

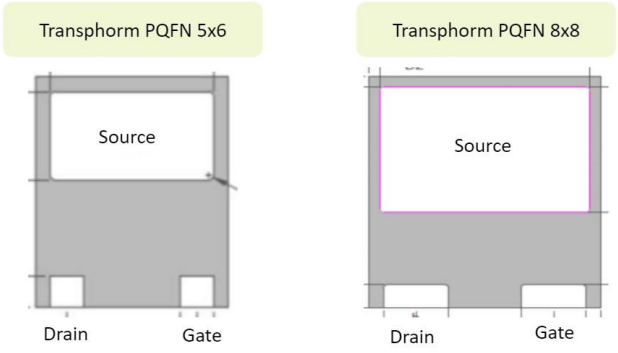


Figure 5. Bottom views of TPH PQFN56 and PQFN88

Based on the LSG (8x8) and JSG (5x6) TPH PQFN solutions, each package has a different assembly location resulting in a 2nd source solution and an increase in capacity. See figure 6 for the bottom view of assembly location of the PQFN devices.

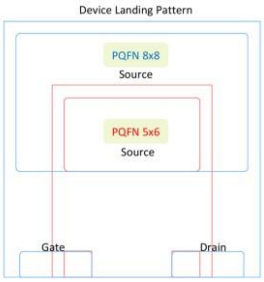


Figure 6. Device Landing Pattern

The PCB design also includes placements for Rg and FB, incase those components are not already positioned on the main driving circuit of the Si development board. These devices may not be required depending on the layout.

The switching node snubber footprints are placed in this daughter card for engineers to populate in order to operate the TPH GaN devices in high current applications.

The TPH product datasheet describes in detail the recommended driving circuit implementation for simplified half bridge and single ended projects. Note that a gate ferrite bead (FB) and the switching node snubber (SNR1 & SNC1)may not be needed for single-end applications (Chart 2), such as ACF, QR Flyback, etc. Those components are recommended for half-bridge circuit applications.

For single ended designs, by recommendation, do not install (DNI) the switching node snubbers for low power operation. See the chart below for the list of standard installed components on TPHDC001. See figure 7 and figure 8 for reference.

TPHDC001				
Qty	**Value**	**Device**	**Parts**	**PN**
1	SNR1	R-US_R1206	SNR1	DNI
1	SNC1	C-USC1206	SNC1	DNI
1	49.9	R-US_R0402	R1	RC0402FR-0749R9L
1	120	R-US_R0402	FB	BLM15AG121SH1D
1	GSD_TO220	GSD_TO220	P1	PRPC003SBAN-M71RC
1	TPH GaN	TPH GaN	Q1	TPH GaN

Chart 2. TPHDC001 BOM.

TPHDC001

G D S

Figure 7. TPHDC001 Top View

S D G

Figure 8. TPHDC001 Bottom View

The exposed copper shown in figure 8 is designed for engineering individuals to install a heatsink for high current testing purposes.

For a visual demonstration of how the TPH daughter card is used, refer to the figure below (figure 9). The TPHDC001 (using TP65H300G4LSG) is mounted on the Silanna ACF 65W adaptor demo board. More information and performance plots of the Silanna ACF demo board can be found on https://www.Transphormusa.com/en/news/65w-usbc-pdgan-adapter-rd/

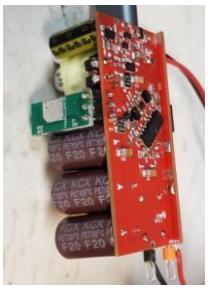


Figure 9. TPHDC001 on Silanna ACF 65W adapter Demo Board

Warning

This TPHDC001 Daughter Card is intended to validate TPH's GaN FET technology and is for demonstration purposes only. No guarantees are made for standards compliance. There are areas of this daughter card that have exposed access to hazardous high voltage levels. Implement caution to avoid contact with those voltages. Also note that the daughter card may retain high voltage temporarily after input power has been removed.

Exercise caution when handling. When testing carriers on an evaluation board, ensure adequate cooling. Apply cooling air with a fan blowing across the evaluation board or across a heat sink attached to the evaluation board. Monitor the evaluation board temperature to ensure it does not exceed the maximum rated per the data sheet.

**Contact your local Sales Representative for more information in obtaining a TPHDC001 for your GaN evaluation.

**TPHDC111 (GSD pinout) is also available

**TPHDC201 (GDS pinout with buffer circuit) is also available

Reference

[1] "AN0007: PQFN88 Lead-free 2nd Level Soldering Recommendations for Vapor Phase Reflow"