Application Note

DA9281-01ATx Variant Overview - RZ/G2L and RZ/V2L MPUs

AN-PM-181

Abstract

This application note describes all the register default settings of the DA9281-01ATx variant (the x denotes the package option).

DA9281-01ATx is highly suited as the power management system solution for RZ/G2L and RZ/V2L MPUs.

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1 Terms and Definitions

CH<x>	Channel <x>, where x = 1 to 8
LDO	Low drop out
OTP	One time programmable
QFN	Quad flat-pack no-lead (package)

2 References

[1] DA9281_Datasheet, Renesas Electronics.

[2] RZ/G2L Group Datasheet, Renesas Electronics.

[3] RZ/V2L Group Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 RZ/G2L and RZ/V2L MPUs Power Requirements

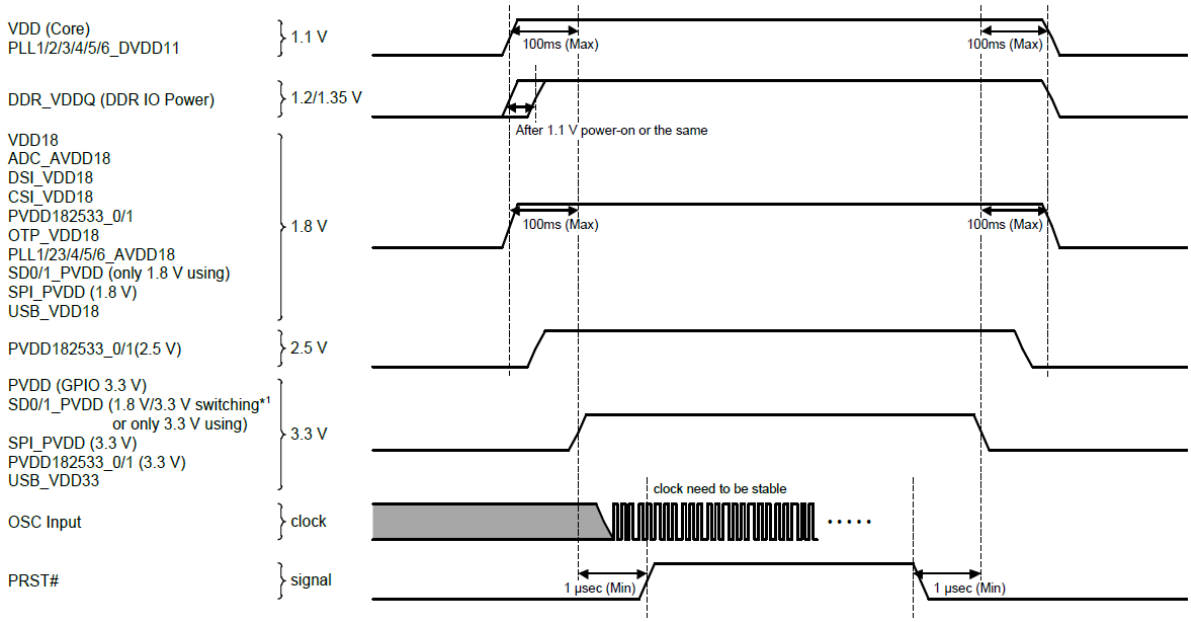

Figure 1: RZ/G2L and RZ/V2L MPU Power On/Off Sequence

- Turn on 3.3 V after 1.1 V/1.8 V.

Note 1 About SD0/1_PVDD, especially in the case of switching between 1.8 V and 3.3 V at same power rail, 1.8-V power-on/off timing can also follow 3.3-V power rail sequence as shown in the Figure 1.

- Turn on the DDR IO power supply at the same time as or after the 1.1-V power supply.
- From first power rising start to last power rising end must be within 100 ms.
- The power-off sequence is the reverse of the power-on sequence (PRST# → Low → 3.3 V = OFF → Other = OFF).
- PRST# should be changed from Low to High after the 3.3-V power supply is turned on, after 1 µs, and after the input clock from the oscillator stabilizes.
- Refer to SD0/1_PVDD when connecting eMMC.

4 DA9281 - RZ/G2L and RZ/V2L Power Supply Tree Diagram (Top Level)

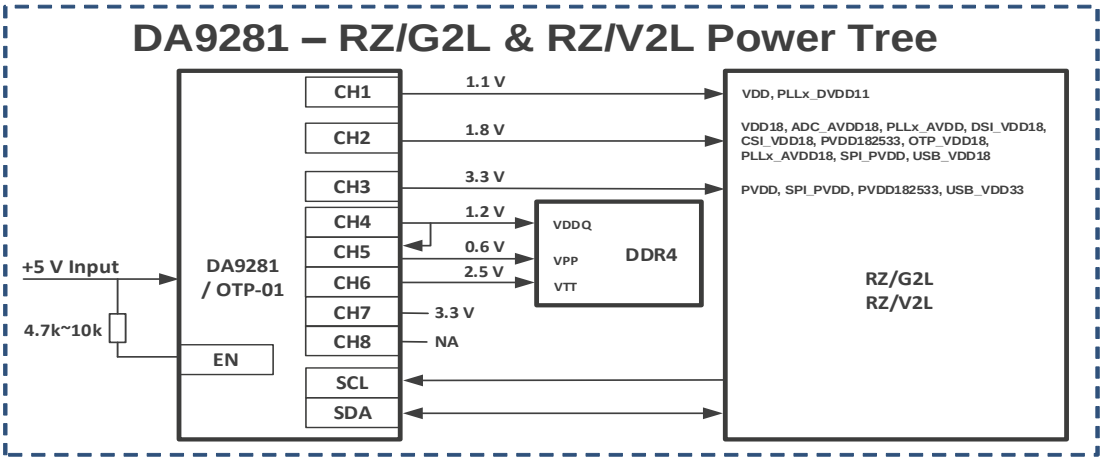

Figure 2: DA9281 - RZ/G2L and RZ/V2L Power Tree

5 DA9281 Power-On/Power-Off Sequences

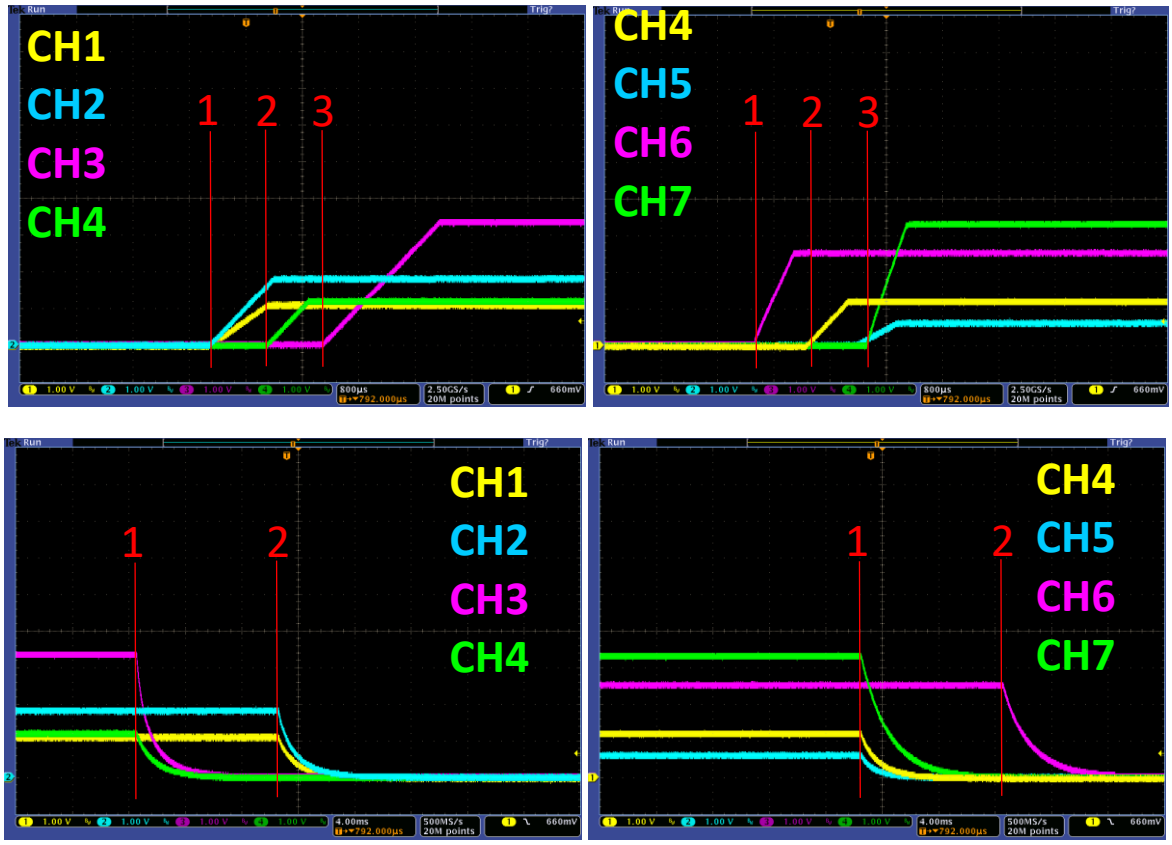

Figure 3: DA9281 Power-On/Power-Off Sequences

Table 1: DA9281 Power-On/Power-Off Timing

Channel	Buck/LDO	Vout	Power-up Slot	Power-down Slot
CH1	Buck	1.1 V	1 (0 ms)	2 (10 ms)
CH2	Buck	1.8 V	1 (0 ms)	2 (10 ms)
CH3	Buck	3.3 V	3 (1.6 ms)	1 (0 ms)
CH4	Buck	1.2 V	2 (0.8 ms)	1 (0 ms)
CH5	VTT	1/2*CH4 = 0.6 V	Same as CH4 (Note 1)	Same as CH4
CH6	LDO	2.5 V	1 (0 ms)	2 (10 ms)
CH7	LDO	3.3 V	3 (1.6 ms)	1 (0 ms)
CH8	LDO	NOT USED	-	-

Note 1 CH5 starts up when CH4 has reached its target voltage.

6 DA9281 Variant Table and Ordering Information

Table 2: Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9281-01AT1	QFN-40	5.0 x 5.0 by 0.4 mm pitch	Waffle Tray	490
DA9281-01AT2			Tape & Reel	5000
DA9281-01ATC				1000

7 DA9281-01ATx Detailed Description - Production Release

Key settings:

- VCH1 = 1.1 V, VCH2 = 1.80 V, VCH3 = 3.3 V, VCH4 = 1.2 V, VCH5 = 1/2*VCH4 (0.6 V), VCH6 = 2.5 V (default), VCH7 = 3.3 V
- Power-on: CH1/CH2/CH6 (0 ms) → CH4(CH5) (0.8 ms) → CH3/CH7 (1.6 ms)
- Power-down: CH3/CH4(CH5)/CH7 (0 ms) → CH1/CH2/CH6 (10 ms)
- CH8 (1.8 V) disabled
- CH<1:4> operate in AUTO mode, 2 MHz
- I^2C standard speed. I^2C slave address = 0xA2h (8-bit)

Table 3: Register Settings DA9281-01ATx Variant

Register Address	Function	Default Value	Description
0x01 *[bit [7:4], [2] & [0] = 0x0 (reserved)]* *[bit [3] = 0x1 (reserved)]*	PMC_VOUT_ADJUST	0x0A	VCH7 = 3.3 V
0x02	PMC_DISCHARGE	0xFF	All CH<1:8> discharge resistors are enabled
0x03	PMC_SOFT_START_1	0x55	CH<1:4> Soft Start is set to 0.6 ms
0x04	PMC_SOFT_START_2	0x55	CH<5:8> Soft Start is set to 0.6 ms
0x05	PMC_ENABLE_DELAY_1	0x09	Enable slot: CH1: SLOT1 (0 ms) CH2: SLOT1 (0 ms) CH3: SLOT3 (1.6 ms) CH4: SLOT2 (0.8 ms)
0x06 *[bit [7:6] = 0x0 (reserved)]*	PMC_ENABLE_DELAY_2	0x08	CH6: SLOT1 (0 ms) CH7: SLOT3 (1.6 ms) CH8: NOT USED
0x07	PMC_DISENDLY	0xC4	Disable slot: CH1: SLOT2 (10 ms) CH2: SLOT2 (10 ms) CH3: SLOT1 (0 ms) CH4: SLOT1 (0 ms) CH6: SLOT2 (10 ms) CH7: SLOT1 (0 ms) CH8: NOTE USED
0x0C	PMC_CONTROL_00	0x00	CH<x> enable: CH<1:7> are disabled
0x0D	PMC_CONTROL_01	0x00	CH<1:4> are set to auto mode
0x0E	PMC_CONTROL_02	0x01	CH<1:7> are enabled by the sequencer CH8 is not enabled by the sequencer
0x0F	PMC_CH1_VOUT_INT	0x6E	VCH1 = 1.1 V
0x10	PMC_CH2_VOUT_INT	0xB4	VCH2 = 1.8 V

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Register Address	Function	Default Value	Description
0x11	PMC_CH3_VOUT_INT	0xA5	VCH3 = 3.3 V
0x12	PMC_CH4_VOUT_INT	0x78	VCH4 = 1.2 V
0x14	PMC_CONFIG_00	0xA2	8-bit slave address is 0xA2h
0x1F *[bit [4] & [2:1] = 0x0 (reserved)]* *[bit [7:5] & [0] = 0x1 (reserved)]*	PMC_CONFIG_0B	0xE9	Sequencer enabled
0x41	OTP_VARIANT_ID	0x02	DA9**2**81
0x42	OTP_CUSTOMER_ID	0x00	OTP file version
0x43	OTP_CONFIG_ID	0x01	OTP variant number: DA9281-**01**ATx
0x4C *[bit [4:0] = 0x0 (reserved)]* *[bit [5] = 0x1 (reserved)]*	BUCK_BUCK_OTP_04 (BUCK1)	0x20	0.8 V ~ 2.2 V range
0x4D *[bit [4] & [2:0] = 0x0 (reserved)]* *[bit [5] & [3] = 0x1 (reserved)]*	BUCK_BUCK_OTP_05 (BUCK2)	0x28	0.8 V ~ 2.2 V range
0x4E *[bit [4] & [2:0] = 0x0 (reserved)]* *[bit [5] & [3] = 0x1 (reserved)]*	BUCK_BUCK_OTP_06 (BUCK3)	0x68	BUCK3_OPT_CTRL6 enabled to allow 1.6 V ~ 3.6 V range
0x4F *[bit [4] & [2:0] = 0x0 (reserved)]* *[bit [5] & [3] = 0x1 (reserved)]*	BUCK_BUCK_OTP_07 (BUCK4)	0x28	0.8 V ~ 2.2 V range

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Table 4: OTP Variant Overview

Reg Add	Function	Standard Variant DA9281-01ATx
0x01	PMC_VOUT_ADJUST	0x0A
0x02	PMC_DISCHARGE	0xFF
0x03	PMC_SOFT_START_1	0x55
0x04	PMC_SOFT_START_2	0x55
0x05	PMC_ENABLE_DELAY_1	0x09
0x06	PMC_ENABLE_DELAY_2	0x08
0x07	PMC_DISENDLY	0xC4
0x0C	PMC_CONTROL_00	0x00
0x0D	PMC_CONTROL_01	0x00
0x0E	PMC_CONTROL_02	0x01
0x0F	PMC_CH1_VOUT_INT	0x6E
0x10	PMC_CH2_VOUT_INT	0xB4
0x11	PMC_CH3_VOUT_INT	0xA5
0x12	PMC_CH4_VOUT_INT	0x78
0x14	PMC_CONFIG_00	0xA2
0x1F	PMC_CONFIG_0B	0xE9
0x41	OTP_VARIANT_ID	0x02
0x42	OTP_CUSTOMER_ID	0x00
0x43	OTP_CONFIG_ID	0x01
0x4C	BUCK_BUCK_OTP_04 (BUCK1)	0x20
0x4D	BUCK_BUCK_OTP_05 (BUCK1)	0x28
0x4E	BUCK_BUCK_OTP_06 (BUCK3)	0x68
0x4F	BUCK_BUCK_OTP_07 (BUCK4)	0x28

Revision History

Revision	Date	Description
1	19-Dec-2023	Initial version.
2	13-Mar-2024	RZ/V2L added.
3	16-Apr-2024	Figure 2 updated; Table 3 & Table 4 updated.
4	31-Mar-2025	Figure 2 updated; Table 3 updated.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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