DA9080 Unused Pin Configuration

This application note describes the recommended configuration for unused pins in applications that use either the DA9080 power management IC.

Contents

Tables

1. Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
LDO	Low drop out (regulator)
OTP	One time programmable
PG	Power good
UQFN	Ultra-thin quad flat-pack no-lead (package)

2. References

[1] DA9080_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

The DA9080 is a high-performance, low cost 5 channel PMIC designed for 32-bit and 64-bit MCU / MPU applications. The internally compensated regulators provide a highly integrated, small footprint power solution for System-On-Module (SOM) applications.

In some applications, certain functions or features may not be required and, to minimize any potential issues with these unused functions, the pins related to them need to be configured correctly. This document provides guidance on how to configure unused connections on the DA9080.

4. DA9080 Functional Blocks

The following tables describe the recommended configurations for unused pins. Mandatory means that the pin is used in all applications.

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AIO	Analog input/output
DIO	Digital input/output	PWR	Power
DIOD	Digital input/output open drain	GND	Ground

Table 2: Pin Description

Pin #	Pin Name	Type (Table 1)	Description	If Unused
1	VDDIO	PWR	Supply for I^2C interface	Connect to GND (no capacitor required) if I2C is not used
2	SDA	DIOD	I^2C interface data, connect SDA to the logic rail via a pull-up resistor	Mandatory - though can be connected to GND if I2C control/monitoring is not required
3	SCL	DI	I^2C interface data, connect SCL to the logic rail via a pull-up resistor	Mandatory - though can be connected to GND if I2C control/monitoring is not required
4	NC	DI	Not used, connect to GND	Mandatory

Pin #	Pin Name	Type (Table 1)	Description	If Unused
5	PG1	DO	Power good output 1, open drain	Leave floating
6	EN	DI	Chip enable (when pulled low, shuts down entire chip after power down sequencing complete)	Mandatory
7	LDOIN	PWR	LDO input, bypass to ground with a ceramic capacitor	Connect to GND (cap not required)
8	LDOOUT	PWR	Output of LDO	Leave floating (cap not required)
9	FB2	AI	CH2 Buck output voltage feedback connection	Connect to GND
10	PGND2	GND	CH2 Buck converter power ground	Mandatory
11	LX2	PWR	CH2 Buck converter switching node	Leave floating (L and Cout not required)
12	PVIN2	PWR	CH2 Buck converter input	Connect to GND (cap not required)
13	PVIN4	PWR	CH4 Buck converter input	Connect to GND (cap not required)
14, 15, 16	LX4	PWR	CH4 Buck converter switching node	Leave floating (L and Cout not required)
17, 18	PGND4	GND	CH4 Buck converter power ground	Mandatory
19	FB4	AI	CH4 Buck output voltage feedback connection	Connect to GND
20	PG2	DO	Power good output 2, open drain	Leave floating
21	AN1	AI	Input to ADC	Tie to non-active state (GND or VSYS) [ADC_EN=0]
22	AN0	AI	Input to ADC	Tie to non-active state (GND or VSYS) [ADC_EN=0]
23	AGND	GND	Quiet ground connection, connect to a quiet ground area	Mandatory
24, 31	VSYS	PWR	Filtered from VIN through an RC to provide a clean 5 V supply	Mandatory
25	FB1	AI	CH1 Buck output voltage feedback connection	Connect to GND
26	PGND1	GND	CH1 Buck converter power ground	Mandatory
27	LX1	PWR	CH1 Buck converter switching node	Leave floating (L and Cout not required)
28	PVIN1	PWR	CH1 Buck converter input – internally connected to PVIN3	- Connect to GND (cap not required) if both PVIN<x> are unused - If one PVIN<x> is used, leave the other PVIN<x> floating (no cap required)
29	PVIN3	PWR	CH3 Buck converter input – internally connected to PVIN1	
30	LX3	PWR	CH3 Buck converter switching node	Leave floating (L and Cout not required)
32	FB3	AI	CH3 Buck output voltage feedback connection	Connect to GND
PAD	GND	GND	Package central pad, connect to PGND	Mandatory

5. Conclusion

Adherence to the recommendations of this document helps minimize spurious application issues such as noise and increased current consumption and may avoid device damage due to incorrectly biased pins. For further information please consult your Renesas Electronics local sales representative.

Revision History

Revision	Date	Description
1.0	Oct 28, 2024	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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