Application Note

DA9063L Schematic Checklist

AN-PM-107

Abstract

Optimizing the schematic for DA9063L ensures correct and efficient operation of the PMIC and the system. This is achieved by selecting appropriate external passive components, and appropriate configuration of the PMIC OTP.

DA9063L Schematic Checklist

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1 Terms and Definitions

PMIC	Power Management Integrated Circuit
DA906x	DA9061, DA9062, DA9063, DA9063L
GUI	Graphical User Interface
OTP	One-Time Programmable (memory)
RTC	Real-Time Clock
SoC	System on (a) Chip
PMIC	Power Management Integrated Circuit
GPIO	General Purpose Input / Output

2 References

[1] DA9063L, Datasheet, Dialog Semiconductor

3 Introduction

DA9063L is a high-current system PMIC suitable for dual- and quad-core processors used in smartphones, tablets, ultra-books, and other handheld and automotive applications that require up to 12 A core processor supply.

This checklist is intended to help a hardware designer identify common errors that can arise in schematics containing the DA9063L. The checklist is only a reference to common errors, and is not a substitute for rigorous system development and an understanding of the PMIC behavior as described in the DA9063L datasheet [1].

4 Schematic Checklist

Table 1: Checklist

General	**Comments**		
Design name			
Schematic version			
Review date			
OTP variant	**Notes**	**Checked (Y/N)**	**Comments**
Which OTP variant is being used?	This can provide useful background for the review.		
OTP version number			
Core Operation			
V_{SYS}	2.8 V to 5.5 V		
V_{DDIO}	1.2 V to 3.6 V		
VSYS capacitor	1 µF		
IREF resistor	200 kΩ. Must be ≤ 1 % tolerance.		
VREF capacitor	220 nF		
VLNREF	220 nF		
VBBAT capacitor	No connect.		
VDDCORE capacitor	2.2 µF		
V_CP	47 nF		
Crystal	The RTC requires an external crystal of 32.768 kHz and load capacitors.		
XTAL_IN and XTAL_OUT	If a crystal or an external 32 kHz source is not required, then both pins should be grounded.		

Core operation	Notes	Checked (Y/N)	Comments
nRESET timing	The nRESET timer control can be set in the GUI. RESET_EVENT sets the timer start reference and RESET_TIMER sets the delay until nRESET is released. Make sure nRESET is active until all important rails have turned on.		
nRESET pin	Register control IRQ_TYPE determines if the pin is push-pull or open-drain. Check that an external pull-up is present if open-drain.		
nONKEY	nONKEY should be either pulled high to V_{SYS} or tied to V_{SYS}, and never left floating.		
nOFF	nOFF should be either pulled high to V_{SYS} or tied to V_{SYS}, and never left floating.		
nSHUTDOWN	nSHUTDOWN should be either pulled high to V_{SYS} or tied to V_{SYS}, and never left floating.		
CHG_WAKE	Wake-up signal from companion charger which triggers a start-up and is a temporary supply voltage for the PMIC (VBUS_PROT in case of an inserted supply until the charger buck provides power to VSYS) Should not be left floating. Pull down to ground, via 10 kΩ.		
TP	TP should not be left floating. Pull down to ground, via 10 kΩ. Ideally, a test-point will be provided for system debug.		
LDOs			
LDO input voltages	2.8 V to 5.5 V If supplied by a buck, the minimum voltage is 1.5 V.		
LDO input capacitor	Note 1		
LDO output capacitor	2.2 µF		
LDO output voltage	LDO3: 0.9 V to 3.44 V LDO7/8/11: 0.9 V to 3.6 V LDO9: 0.95 V to 3.6 V		
LDO output current	LDO3/7/8/9: 200 mA LDO11: 300 mA		
DVC_<x> register control	If VDLO<x>_SEL_A and VDLO<x>_SEL_B have different voltages and only one specific voltage is desired, then the regulator needs to be set correctly.		

DA9063L Schematic Checklist

<table>
<tr><th>Bucks</th><th>Notes</th><th>Checked (Y/N)</th><th>Comments</th></tr>
<tr><td>Buck supply voltage</td><td>2.8 V to 5.5 V</td><td></td><td></td></tr>
<tr><td>Input capacitors</td><td>Note 2, Note 3</td><td></td><td></td></tr>
<tr><td>Buck output current</td><td>BUCKCORE1 and BUCKCORE2:
2500 A
BUCKPRO:
2500 mA
BUCKPERI:
1500 mA
BUCKMEM:
1500 mA
BUCKIO:
1500 mA</td><td></td><td></td></tr>
<tr><td>Buck: current limit register settings I_{LIM}</td><td>Controlled with B<x>_ILIM register.
BUCKCORE1 and BUCKCORE2:
● Full Current Mode:
1000 mA to 4000 mA
● Half Current Mode:
500 mA to 2000 mA
BUCKPRO:
500 mA to 2000 mA
BUCKPERI:
1500 mA to 3000 mA
BUCKMEM:
1500 mA to 3000 mA
BUCKIO:
1500 mA to 3000 mA</td><td></td><td></td></tr>
<tr><td>Minimum ISAT values required at current limits</td><td><table><tr><th>Current limit:</th><th>ISAT:</th></tr><tr><td>3400 mA</td><td>3800 mA</td></tr><tr><td>2800 mA</td><td>3100 mA</td></tr><tr><td>2100 mA</td><td>2400 mA</td></tr><tr><td>1700 mA</td><td>1700 mA</td></tr></table></td><td></td><td></td></tr>
<tr><td>CORE1 / CORE2 dual-phase mode</td><td>5 A output. Enabled by controls BCORE_MERGE. Outputs from both inductors need to be routed together.</td><td></td><td></td></tr>
<tr><td>MEM / IO dual-phase mode</td><td>3 A output. Enabled by controls BUCK_MERGE. Buck outputs should share the same inductor.</td><td></td><td></td></tr>
<tr><td>DVC_<x> register control</td><td>If VBUCK<x>_SEL_A and VBUCL<x>_SEL_B have different voltages and only one specific voltage is desired, then the regulator needs to be set correctly.</td><td></td><td></td></tr>
<tr><td>Output capacitors</td><td>BUCKCORE1 / BUCKCORE2:
Full Current Mode: 2 x 47 µF
Half Current Mode: 2 x 22 µF</td><td></td><td></td></tr>
</table>

DA9063L Schematic Checklist

Bucks	Notes	Checked (Y/N)	Comments
	BUCKPRO: Full Current Mode: 2 x 47 µF Half Current Mode: 2 x 22 µF **BUCKPERI:** 2 x 22 µF **BUCKMEM:** Full Current Mode: 2 x 47 µF Half Current Mode: 2 x 22 µF **BUCKIO:** 2 x 22 µF		
GPIOs			
Unused GPIOs	Check that they are one of the following: ● configured as an input, with internal pull-down enabled via registers CONFIG_L and CONFIG_K, or, ● configured as an output, or, ● tied to GND		
GPIO events	Check unused GPIOs have events masked in register IRQ_MASK_C.		
Are there any GPIOs configured to have special features? (SYS_EN, PWR_EN, Watchdog trigger input)	Check the signal behavior. Ensure the port is correctly configured as active-high or active-low using control GPIO<x>_TYPE.		

Power Sequencer	Notes	Checked (Y/N)	Comments
Start-up sequence	Is it correct for the system requirements?		
WAIT_STEP and dummy slots	Has the WAIT_STEP feature been used correctly, or set to 0x00? If dummy (empty) slots are used, are they correct?		
Minimize in-rush	Turning all regulators on in the same slot will cause a large inrush current and potentially cause a drop-in input voltage and cause the PMIC to power down.		
Are the sequencer pointers placed in a suitable slot?	PART_DOWN ≤ SYSTEM_END SYSTEM_END ≤ POWER_END POWER_END ≤ MAX_COUNT		

Note 1 2 x 1 µF shared by all VDD_LDOx pins if they are all close together, for example, all attached to a power/split plane.

Note 2 22 µF within 1.5 mm of each BUCKCORE1, BUCKCORE2 and BUCKPRO supply pin.

Note 3 10µF within 1.5 mm of each BUCKPERI, BUCKIO and BUCKMEM supply pin or 1 x 22µF if all are attached to a PCB power/split plane

5 Further Assistance

For further assistance on debugging and for a detailed schematic and OTP check, please refer to the DA9063L Datasheet found on the Dialog website (https://www.dialog-semiconductor.com/pmics) or contact your local FAE.

Revision History

Revision	Date	Description
1.0	16-Nov-2017	Initial version.
1.1	24-Feb-2022	File was rebranded with new logo, copyright and disclaimer

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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