

# Application Note

## DA9061/2 and NXP i.MX 7Solo Power Connections

### AN-PM-102

#### **Abstract**

*This document describes the connectivity between the Dialog Semiconductor DA9061/2 Power Management Integrated Circuits (PMICs) and NXP i.MX 7Solo system application processors.*

---

## DA9061/2 and NXP i.MX 7Solo Power Connections

### Contents

<b>Abstract</b> .....	<b>1</b>
<b>Contents</b> .....	<b>2</b>
<b>Figures</b> .....	<b>2</b>
<b>Tables</b> .....	<b>2</b>
<b>1 Terms and Definitions</b> .....	<b>3</b>
<b>2 References</b> .....	<b>3</b>
<b>3 Introduction</b> .....	<b>4</b>
<b>4 i.MX 7S Power Requirements</b> .....	<b>4</b>
4.1 DA9061 and i.MX 7S Power Rails .....	4
4.2 DA9062 and i.MX 7S Power Rails .....	6
4.3 DA9062 and i.MX 7S Power Rails for WaRP7 Demo Board .....	8
4.4 Power-up Sequence.....	10
4.5 Power-down Sequence .....	10
4.6 I <sup>2</sup> C Interface .....	10
4.7 Recommended External Components .....	10
<b>5 Scalable Power Management Solutions</b> .....	<b>11</b>
<b>6 Software Driver</b> .....	<b>11</b>
<b>7 Development Support Tools and PMIC Configuration Files</b> .....	<b>11</b>
<b>8 Device Identification and Ordering</b> .....	<b>12</b>
<b>Revision History</b> .....	<b>12</b>

### Figures

Figure 1: DA9061 Connections to i.MX 7Solo .....	5
Figure 2: DA9062 Connections to i.MX 7S.....	7
Figure 3: DA9062 Connections to WaRP7 Demo Board .....	9
Figure 4: DA9061 Power-up Sequence.....	10
Figure 5: DA9062 Power-up Sequence.....	10

### Tables

Table 1: i.MX 7S to DA9061 Power Rail Mapping .....	4
Table 2: i.MX 7S to DA9062 Power Rail Mapping .....	6
Table 3: i.MX 7S WaRP7 CPU Board to DA9062 Power Rail Mapping.....	8
Table 4: Product Part Numbers .....	12

---

## DA9061/2 and NXP i.MX 7Solo Power Connections

### 1 Terms and Definitions

BOM	Bill of Materials
GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling. Analogous to DVC
POR	Power-On Reset
RTC	Real-Time Clock
SNVS	Secure Non-Volatile Storage

### 2 References

- [1] WaRP7 - Next Generation IoT and Wearable Development Platform, <https://www.nxp.com/support/developer-resources/reference-designs/warp7-next-generation-iot-and-wearable-development-platform:WARP7> [accessed 09/01/2018]
- [2] MCIMX7SABRE: SABRE Board for Smart Devices Based on the i.MX 7Dual Applications Processors, <https://www.nxp.com/support/developer-resources/hardware-development-tools/sabre-development-system/sabre-board-for-smart-devices-based-on-the-i.mx-7dual-applications-processors:MCIMX7SABRE> [accessed 09/01/2018]
- [3] In-Circuit Programming of DA9061/2/3, AN-PM-080, Dialog Semiconductor
- [4] i.MX 7Solo Applications Processor Reference Manual, IMX7SRM, Rev. 0.1, 08/2016, NXP
- [5] i.MX 7Solo Family of Applications Processors Datasheet, IMX7SCEC Rev. 5, 07/2017, NXP.
- [6] DA9061, datasheet, Dialog Semiconductor
- [7] DA9062, datasheet, Dialog Semiconductor
- [8] Reference design files, DA9062\_iMX7\_design\_files.zip, Dialog Semiconductor
- [9] Design files, DA9062 WaRP7 CPU Board, DA9062\_WaRP7\_CPU\_Board\_design\_files.zip, Dialog Semiconductor
- [10] The Linux Kernel Archives, <https://kernel.org/> (DA9061 software driver) [accessed 30/3/2016]

## DA9061/2 and NXP i.MX 7Solo Power Connections

### 3 Introduction

The NXP® i.MX 7Solo™ processor requires dedicated power management for a stable and reliable system. The Dialog DA9061 and DA9062 PMICs provide a convenient and flexible solution that meets the processor power requirements. Although system power consumptions vary due to the differing demands of peripherals, processor, and so on, the DA9061 has sufficient headroom to meet the power requirements of most i.MX 7S systems. The features of DA9061 enable significant power saving, such as dynamic voltage control (DVC) which intelligently manages voltage changes. The DA9061 significantly reduces system cost and size compared to an equivalent discrete solution.

This document provides details of integrating the DA9061 into an i.MX 7Solo system, based on the 'WaRP7 IoT and Wearable Development Platform' [1]. General guidance can be found in the other NXP references listed in Section 2. The focus here is on DA9061 as it creates the lowest cost solution. However, where a system requires further capabilities such as an SNVS coin-cell charger, additional power rails, real-time clock (RTC), or support for powering-down only VDD\_ARM in Low-Power Mode, then the DA9062 provides these capabilities. Systems with higher power demands, such as the NXP SABRE Board [2] and i.MX 7Dual™ processor, are discussed in a separate application note.

### 4 i.MX 7S Power Requirements

All power domains of an i.MX 7 processor require precise power management to ensure reliable system operation. The main domains are:

VDD_SOC and VDD_ARM	supplies the internal peripherals and the internal ARM™ cores
VDD_SNVS_IN	supplies the SNVS regulator for the RTC and SNVS (secure non-volatile storage)

Additional supplies may be required for DDR memory, peripherals, I/O interfaces, USB, and so on. The power management system must also comply with the processor power-up and power-down sequence requirements.

#### 4.1 DA9061 and i.MX 7S Power Rails

The supply rails for an i.MX 7Solo system powered by DA9061 are summarized in Table 1.

**Table 1: i.MX 7S to DA9061 Power Rail Mapping**

i.MX 7S Rail or System Rail	DA9061 Regulator	Voltage (V)	Sequence Slot	Notes
VDD_SNVS_IN	LDO2	3.00	1	Switchable via GPIO3 between 3.0 V and 3.3 V. (GPIO3 = 0 selects 3.3 V)
VDD_ARM_IN VDD_SOC_IN	Buck1	1.15	2	Processor efficiency and lifetime can be optimized by reducing the voltage by I <sup>2</sup> C register writes after system start-up.
NVCC_DRAM (VDDQ_DDR)	Buck3	1.50 / 1.35	3	Switchable via GPIO2 to support DDR3 and DDR3L. (GPIO2 = 0 selects 1.35 V)
NVCC_<x>	Buck2	3.3	4	
Peripherals	LDO1	2.5	5	
Peripherals	LDO3	1.8	6	
Peripherals	LDO4	1.2	7	

This mapping is illustrated in the interconnect block diagram of Figure 1.

VDD\_SNVS\_IN is supplied by LDO2 and must be powered up first in the sequence.

## DA9061/2 and NXP i.MX 7Solo Power Connections

The voltage for VDD\_SOC and VDD\_ARM has been set in OTP as 1.15 V. For PCB layouts that have significant ohmic drops along these supply rails, the losses can be compensated for by slightly increasing the level. This is achieved by an I<sup>2</sup>C software write to DA9061 control VBUCK1\_A immediately after system power-up. Additionally, processor efficiency and lifetime can be optimized by reducing the voltage, for example to the recommended typical of 1.00 V, by I<sup>2</sup>C register writes after system start-up.

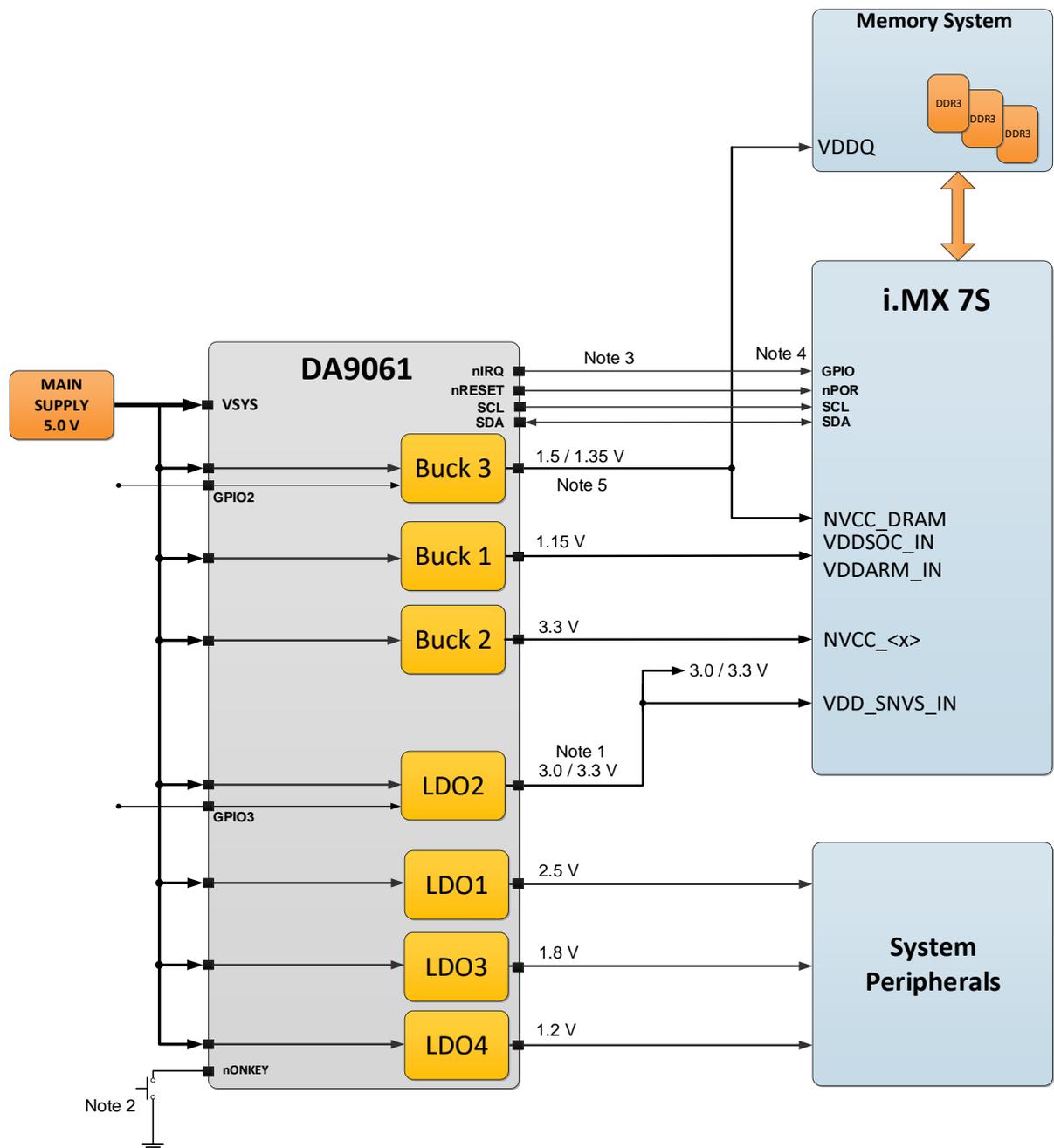


Figure 1: DA9061 Connections to i.MX 7Solo

- Note 1** LDO2 is switchable between 3.0 V and 3.3 V based on GPIO3 level. GPIO3 low gives 3.3 V.
- Note 2** DA9061-71 has the autoboot function enabled in OTP. The DA9061-72 has autoboot disabled and is therefore suited for systems requiring an ONKEY wake-up.
- Note 3** Pull-up resistors for open-drain lines are not shown.
- Note 4** Can connect to an i.MX 7S pin assigned as a GPIO. See [4] Section 8.3.4.

## DA9061/2 and NXP i.MX 7Solo Power Connections

**Note 5** Buck2 is switchable between 1.5 V and 1.35 V based on GPIO2 level. GPIO2 low gives 1.35 V.

### 4.2 DA9062 and i.MX 7S Power Rails

The supply rails for an i.MX 7Solo system powered by DA9062 are summarized in [Table 2](#).

**Table 2: i.MX 7S to DA9062 Power Rail Mapping**

i.MX 7S Rail or System Rail	DA9062 Regulator	Voltage (V)	Sequence Slot	Notes
VDD_SNVS_IN	VBBAT	3.00	0	The VBBAT coin-cell charger is enabled in OTP and is powered before other sequenced supplies.
VDD_ARM_IN VDD_SOC_IN	Buck1	1.15	1	Processor efficiency and lifetime can be optimized by reducing the voltage by I <sup>2</sup> C register writes after system start-up.
NVCC_DRAM (VDDQ_DDR)	Buck2	1.50 / 1.35	2	Switchable via GPIO2 to support DDR3 and DDR3L. (GPIO2 = 0 selects 1.35 V)
NVCC<x>	Buck3	3.3	3	
Peripherals	Buck4	1.8	4	
Peripherals	LDO1	2.5	5	
Peripherals	LDO2	3.0 / 3.3	6	Switchable via GPIO3 between 3.0 V and 3.3 V. (GPIO3 = 0 selects 3.3 V)
Peripherals	LDO3	1.8	7	
Peripherals	LDO4	1.2	8	

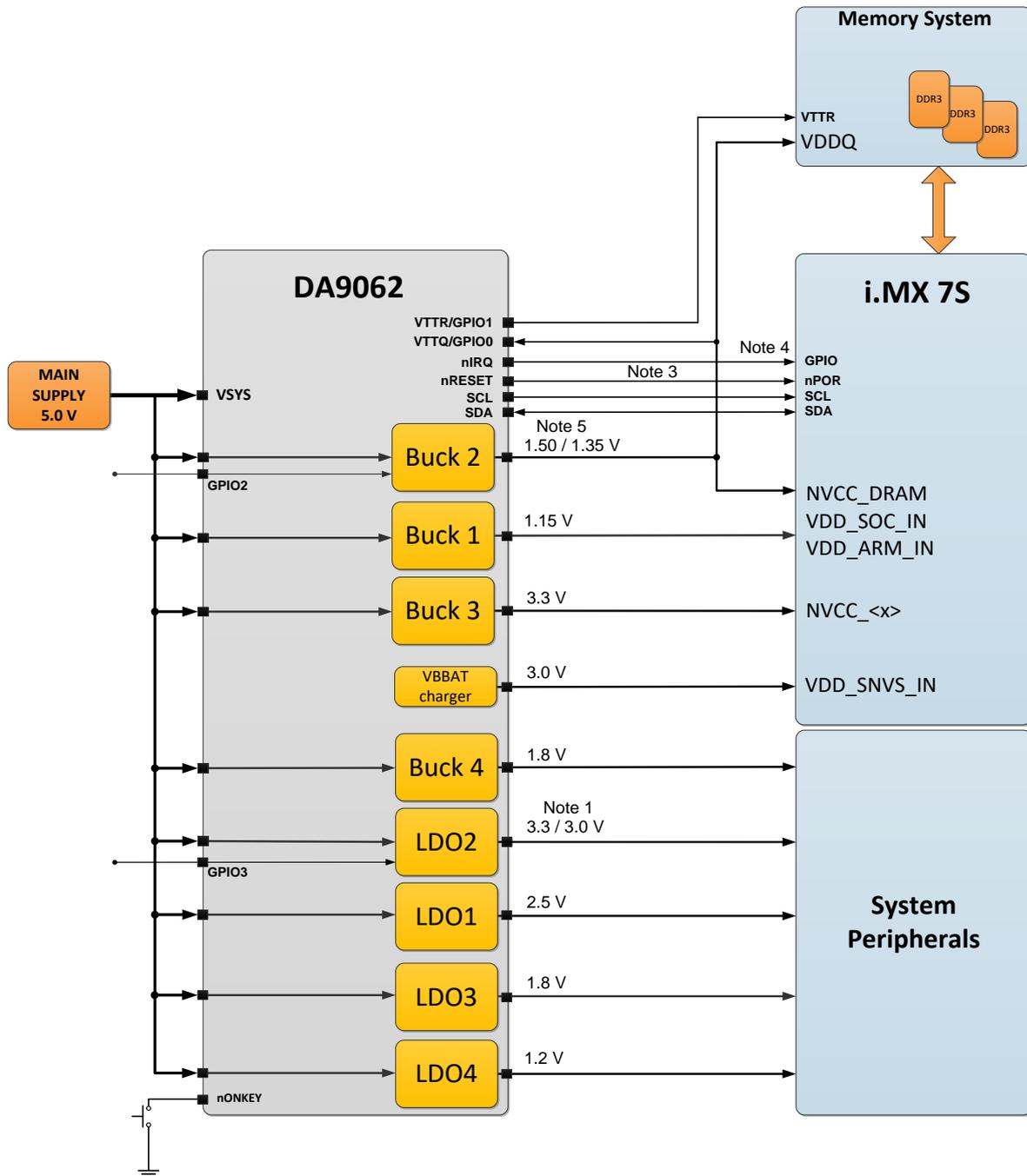
This mapping is illustrated in the interconnect block diagram of [Figure 2](#).

VDD\_SNVS\_IN is supplied by VBBAT and must be powered up first in the sequence. The VBBAT backup charger is on by default, which powers VDD\_SNVS\_IN before other supplies.

The voltage for VDD\_SOC and VDD\_ARM has been set in OTP as 1.15 V. For PCB layouts that have significant ohmic drops along these supply rails, the losses can be compensated for by slightly increasing the level. This is achieved by an I<sup>2</sup>C software write to DA9061 control VBUCK1\_A immediately after system power-up. Additionally, processor efficiency and lifetime can be optimized by reducing the voltage, for example to the recommended typical of 1.00 V, by I<sup>2</sup>C register writes after system start-up.

The i.MX 7Solo 'Low Power Mode' can be supported by a custom OTP variant instead of using the standard variants DA9062-71 and DA9062-72. A custom OTP variant can be supported, for example, by using in-circuit programming of the OTP [\[3\]](#). Buck4 can be reassigned to supply only VDD\_SOC, leaving Buck 1 to supply only VDD\_ARM. Then, setting GPIO4\_PIN = 0 configures GPIO4 as a SYS\_EN port driven by the processor's PMIC\_STBY\_REQ signal. With a modified DA9062 supply sequence, the system can then power off VDD\_ARM when PMIC\_STBY\_REQ becomes active. See [\[2\]](#) Section 4.1.6.5.

## DA9061/2 and NXP i.MX 7Solo Power Connections



**Figure 2: DA9062 Connections to i.MX 7S**

- Note 1** LDO2 is switchable between 3.0 V and 3.3 V based on GPIO3 level. GPIO3 low gives 3.3 V.
- Note 2** DA9062-71 has the autoboot function enabled in OTP. The DA9062-72 has autoboot disabled and is therefore suited for systems requiring an ONKEY wake-up.
- Note 3** Pull-up resistors for open-drain lines are not shown.
- Note 4** Can connect to an i.MX 7S pin assigned as a GPIO. See [4] Section 8.3.4.
- Note 5** Buck2 is switchable between 1.5 V and 1.35 V based on GPIO2 level. GPIO2 low gives 1.35 V.

The OTP standard variants DA9062-71 and DA9062-72 have GPIO0 and GPIO1 configured to sense VTTQ and supply VTTR, respectively. Where the VTTR reference is not required, these can instead be configured as GPIOs by configuring register control BUCK4\_VTTR\_EN = 0.

## DA9061/2 and NXP i.MX 7Solo Power Connections

The variants DA9062-71 and DA9062-72 are used with the schematic and BOM [8] available from the Dialog Support Site.

### 4.3 DA9062 and i.MX 7S Power Rails for WaRP7 Demo Board

Table 3 summarizes the supply rails for a WaRP7 Demo Board powered by DA9062. VDD\_SNVS\_IN must be powered up first in the sequence. It is supplied by the VBBAT backup charger which is on by default. This powers VDD\_SNVS\_IN before other supplies.

**Table 3: i.MX 7S WaRP7 CPU Board to DA9062 Power Rail Mapping**

i.MX 7S Rail or System Rail	DA9062 Regulator	Voltage (V)	Sequence Slot	Notes
VDD_SNVS_IN	VBBAT	3.00	0	The VBBAT coin-cell charger is enabled in OTP and is powered before other sequenced supplies.
VDD_ARM_IN VDD_SOC_IN	Buck1	1.15	1	Processor efficiency and lifetime can be optimized by reducing the voltage by I <sup>2</sup> C register writes after system start-up.
NVCC_1V8	Buck4	1.80	2	
NVCC_DRAM	Buck2	1.2	3	
VLDO1_1V8	LDO1	1.8	2	
VLDO2_1V2	LDO2	1.2	N/A	
VLDO3_1V8	LDO3	1.8	2	
VLDO4_1V8	LDO4	1.8	N/A	
NVCC_SD2	Buck3	3.15	2	
NVCC_3V15	Buck3	3.15	2	

The above mapping is illustrated in the interconnect block diagram of Figure 3.

DA9061/2 and NXP i.MX 7Solo Power Connections

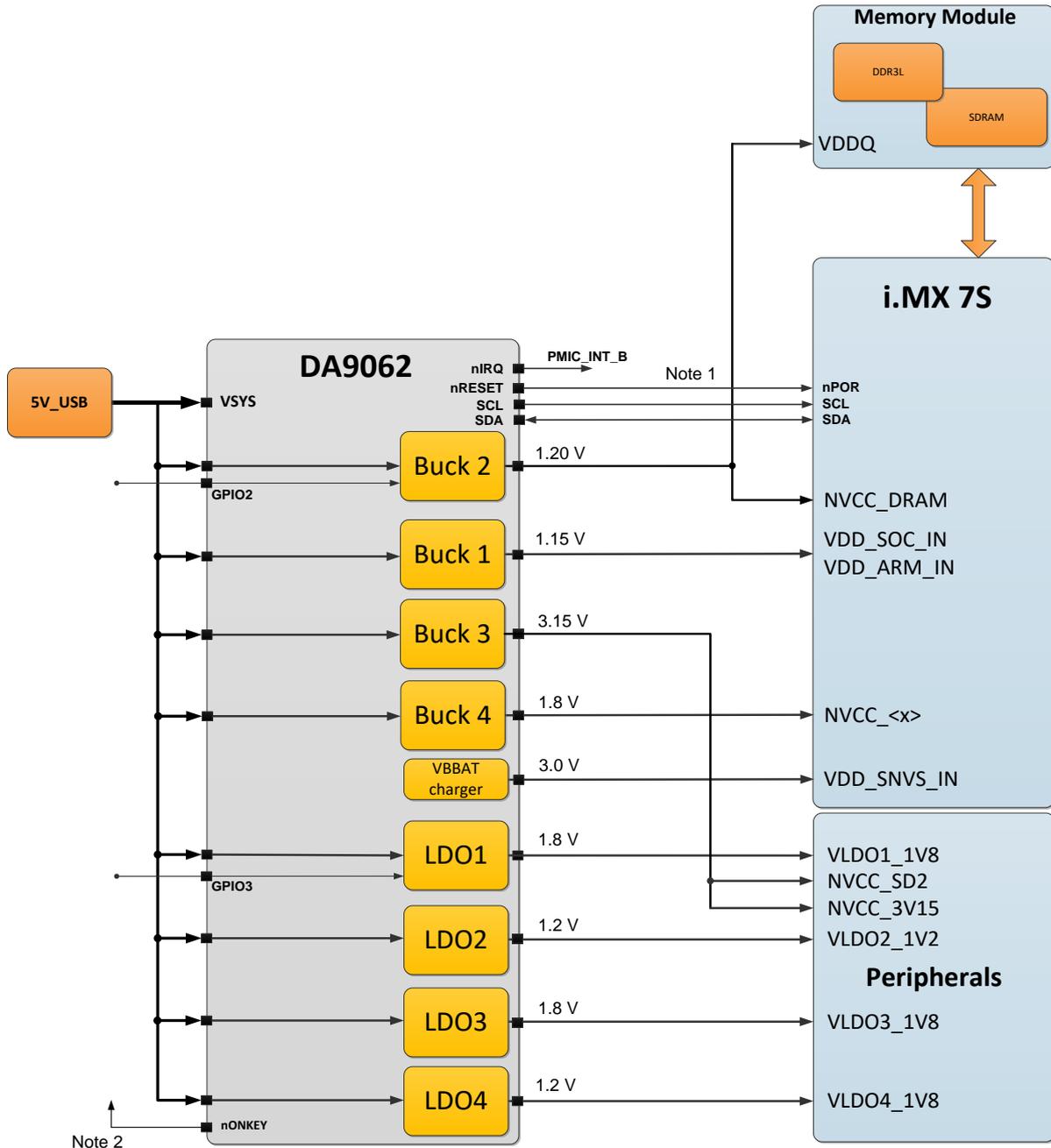


Figure 3: DA9062 Connections to WaRP7 Demo Board

**Note 1** Pull-up resistors for open-drain lines are not shown.

**Note 2** Demo Board on-key is used. DA9062 nONKEY is unused.

The schematic, PCB layout and BOM are available as 'DA9062\_iMX7\_design\_files.zip' [8]. These and the OTP ini files are available from the Dialog Support Site.

## DA9061/2 and NXP i.MX 7Solo Power Connections

### 4.4 Power-up Sequence

The sequence used by the standard variants DA9061-71, DA9061-72, DA9062-71 and DA9062-72 conforms to the requirements described in the i.MX 7Solo datasheet [5] and reference manual [4].

Figure 4 shows the power-up sequence generated by the DA9061-71 and DA9061-72, which meets the i.MX 7S start-up requirements. Figure 5 shows the sequence for DA9062-71 and DA9062-72.

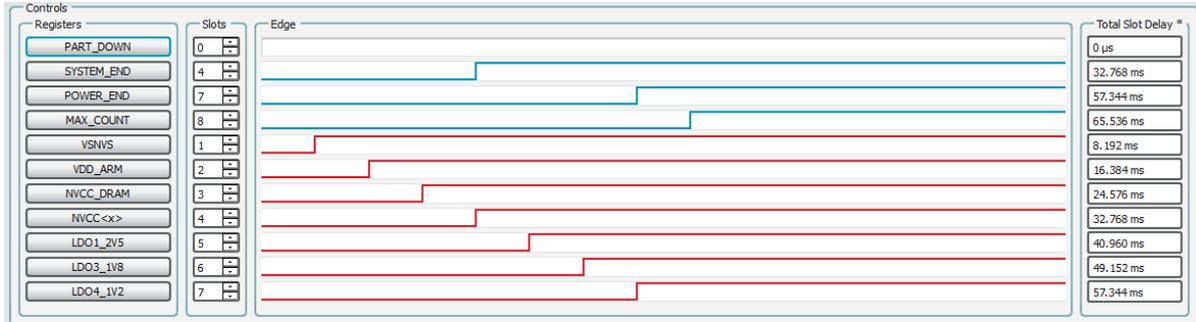


Figure 4: DA9061 Power-up Sequence

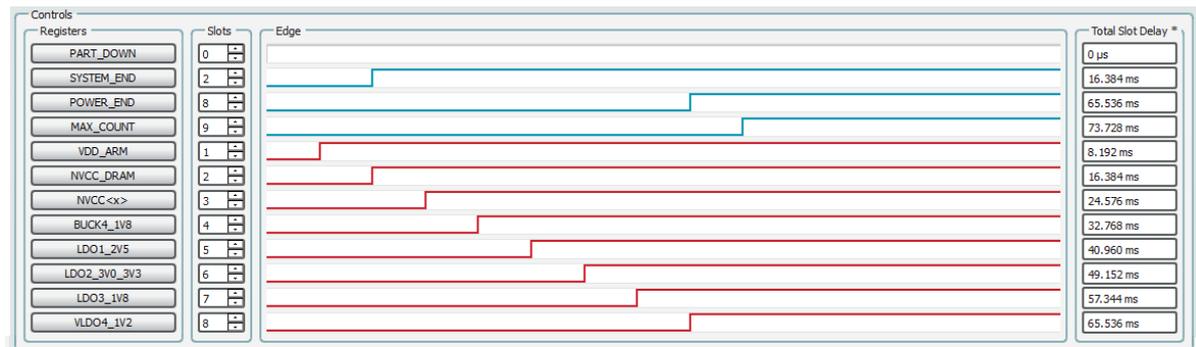


Figure 5: DA9062 Power-up Sequence

### 4.5 Power-down Sequence

The power-down sequence is the reverse of power-up. Therefore, the i.MX 7Solo requirement is met for VDD\_SNVS\_IN to be turned off last after any other power supply. Restrictions for other supplies are discussed in [5].

### 4.6 I<sup>2</sup>C Interface

An I<sup>2</sup>C interface between the i.MX 7S and the DA9061/2 device allows software, including the operating system kernel, to access the internal PMIC registers for control and monitoring. The slave address of the DA9061/2 is 0xB0.

### 4.7 Recommended External Components

For a list of recommended external components, please refer to the schematic [8], and the DA9061/2 datasheets [6], [7]. The recommended values of inductors and capacitors must be used at the output of all bucks and LDOs to guarantee the closed-loop stability and optimum efficiency of the supplies.

## DA9061/2 and NXP i.MX 7Solo Power Connections

### 5 Scalable Power Management Solutions

Some systems require more regulators than available from the DA9061. This is frequently due to the demands of the peripherals. In these circumstances, other Dialog PMICs in the same family (for example, DA9062, DA9063, and DA9063L) are likely to provide suitable solutions. The DA9062 is pin-compatible with the DA9061 and provides additional features often required by i.MX 7 systems such as a real-time clock (RTC), DDR memory termination (DA9062 VTT supply), VTTR memory reference voltage, and a dual-phase (5 A) buck configuration. For battery-powered systems, the DA9021 and DA9022 may also be suitable.

### 6 Software Driver

After the DA9061/2 has started the i.MX 7 system, software can read and write to the PMIC via the I<sup>2</sup>C bus. This can be used for further PMIC configuration, such as the GPIOs, interrupt servicing, DVC, watchdog keep-alive writes, and so on. Dialog drivers for Linux™ are available in the Linux kernel from <https://kernel.org/> [10] or, if interim assistance is required, from a Dialog Sales representative or via the Dialog Discussion Forum.

### 7 Development Support Tools and PMIC Configuration Files

To assist with hardware and software development, Dialog provides the following:

- DA9061 evaluation kit
- DA9062 evaluation kit

These evaluation kits contain motherboard and daughterboard for hardware evaluation and software development. They include the [SmartCanvas™](#) GUI software.

- [SmartCanvas](#) GUI

This PC-driven software provides easy access to a device under test (DUT). The GUI is used to exercise the DUT using the I<sup>2</sup>C interface. Control or measurement of analog and digital pins is supported. [SmartCanvas](#) supports the Dialog PMIC OTP configuration file format – .ini files.

- OTP configuration .ini files

These files define the configuration of the DA9061/2 at boot and define the different variants such as the -71 and -72. The following ini files are available from the Dialog Support Site:

- DA9061-71\_iMX7S\_autoboot\_v2-ED40.ini (autoboot enabled)
- DA9061-72\_iMX7S\_non-autoboot\_v2-A78C.ini (autoboot disabled)
- DA9062-71\_iMX7S\_autoboot\_v1-659C.ini (autoboot enabled)
- DA9062-72\_iMX7S\_non-autoboot\_v1-5B56.ini (autoboot disabled)
- DA9062-70\_WaRP7\_CPU\_Board\_v02-7768.ini (WaRP7 Demo Board, autoboot).

These ini files are opened using the [SmartCanvas](#) GUI.

- Reference design schematic [8] with details of PMIC to processor interconnections
- WaRP7 CPU Board reference design schematic and layout [9]
- Linux software driver, see [Section 6](#)

## DA9061/2 and NXP i.MX 7Solo Power Connections

### 8 Device Identification and Ordering

DA9061-71 / DA9062-71 have the autoboot feature enabled in OTP. The DA9061-72 / DA9062-72 have autoboot disabled and are therefore suited for systems requiring an ONKEY wake-up.

If the above standard variants prove unsuitable for your target i.MX 7 design, please contact a Dialog sales representative to discuss custom variants (minimum order quantities apply for custom variants) or consider OTP in-circuit programming as described in [3].

**Table 4: Product Part Numbers**

Part Number	Description (Note 1)
DA9061-71AMx	Autoboot
DA9061-72AMx	Non-autoboot
DA9062-71AMx	Autoboot
DA9062-72AMx	Non-autoboot

**Note 1** See the DA9061 and DA9062 datasheets [6] and [7] for further information regarding part ordering. All parts are available in tray (x = 1) or Tape and Reel (x = 2).

### Revision History

Revision	Date	Description
1.0	16-Feb-2018	First release.
1.1	18-Dec-2018	<ul style="list-style-type: none"> <li>● Section 4.1: <a href="#">DA9061 and i.MX 7S Power Rails</a> <ul style="list-style-type: none"> <li>○ Added Note 5 to Figure 1.</li> <li>○ Corrected Figure 1 Buck1 voltage from 1.40 V to 1.15 V.</li> <li>○ Added polarity descriptions for GPIO-selectable voltage on GPIO2 and GPIO3 in notes of Figure 1.</li> </ul> </li> <li>● Section 4.2: <a href="#">DA9062 and i.MX 7S Power Rails</a> <ul style="list-style-type: none"> <li>○ Added polarity descriptions for GPIO-selectable voltage on GPIO2 and GPIO3 in notes of Figure 2.</li> </ul> </li> <li>● Section 7: <a href="#">Development Support Tools and PMIC Configuration Files</a> <ul style="list-style-type: none"> <li>○ Corrected OTPs for DA9061. New OTPs created and listed: 'DA9061-71_iMX7S_autoboot_v2-ED40.ini', 'DA9061-72_iMX7S_non-autoboot_v2-A78C.ini'</li> <li>○ Updated OTP for WaRP7 demo board to 'DA9062-70_WaRP7_CPU_Board_v02-7768.ini'.</li> </ul> </li> </ul>
1.2	18-Feb-2022	<ul style="list-style-type: none"> <li>● File was rebranded with new logo, copyright and disclaimer</li> </ul>

## DA9061/2 and NXP i.MX 7Solo Power Connections

### Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

### RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).