DA14533 Hardware Guidelines

This Application Note provides the minimal reference schematic, circuit explanation, and design guidelines for Bluetooth® LE applications based on the DA14533 SoCs.

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1. Terms and Definitions

BOM	Bill of Materials
CS	Chip Select
DCR	DC Resistance
GPIO	General Purpose Input Output (pin)
IC	Integrated Circuit
ILIM	DCDC Inductor peak current limit
JTAG	Joint Test Action Group
OTP	One Time Programmable
PCB	Printed Circuit Board
PCBA	Printed Circuit Board Assembly
PMU	Power Management Unit
Pro-Devkit	DA14531 Pro Development kit
RF	Radio Frequency
RX	Receiver
SDK	Software Development Kit
SoC	System on Chip
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

2. References

[1] DA14533, Datasheet, Renesas Electronics.

[2] UM-B-041, SmartBond Production Line Tool, Manual, Renesas Electronics.

[3] UM-B-144, DA14531 Development Kit Pro Hardware, Manual, Renesas Electronics.

[4] ETSI EN 300 328 and EN 300 440 Class 2 (Europe).

[5] FCC CFR47 Part 15 (US).

[6] ARIB STD-T66 (Japan).

[7] AN-B-099, DA14535 Requirements for Spurious Reduction, Application Note, Renesas Electronics.

[8] AN-B-072, DA14531 Booting Options, Application Note, Renesas Electronics.

[9] AN-B-088, DA145xx Flash Selector Guide, Application Note, Renesas Electronics.

[10] UM-B-119, SW Platform Reference, Manual, Renesas Electronics.

[11] UM-B-083 SmartSnippets Toolbox, Manual, Renesas Electronics.

[12] UM-B-159, DA14535-Module-getting-started-Guide, Renesas Electronics.

3. Introduction

The DA14533 is an ultra-low power SoC integrating a 2.4 GHz transceiver and an Arm® Cortex®-M0+ microcontroller with a RAM of 64 kB and a One-Time Programmable (OTP) memory of 12 kB. It can be used as a standalone application processor or as a data pump in hosted systems.

Key characteristics:

- Compatible with:
  - Bluetooth V5.3
  - ETSI EN 300 328 and EN 300 440 Class 2 (Europe)
  - FCC CFR47 Part 15 (US)
  - ARIB STD-T66 (Japan)
  - AEC Q100 Grade 2 Automotive Qualification
  - Supports up to 3 Bluetooth® LE connections
  - Typical cold boot to radioactive 35 ms.
- Memories:
  - 12 kB One-Time-Programmable (OTP)
  - 64 kB Retainable System RAM
  - 160 kB ROM
  - RAM retainability configured in 2 blocks
  - SysRAM1 (32 kB)
  - SysRAM2 (32 kB).
- Power management
  - Integrated Low I_Q Buck DCDC converter
  - Buck: 1.8 V ≤ V_{BAT_HIGH} ≤ 3.6 V
  - Clock-less hibernation mode: Buck <550 nA
  - Built-in temperature sensor for die temperature monitoring.
- Digital interfaces:
  - 9 x GPIOs
  - 2 x UARTs (one with flow control)
  - SPI Master/Slave up to 32 MHz (Master)
  - I2C bus at 100 kHz and 400 kHz
  - 3-axis capable Quadrature Decoder
  - Keyboard controller.
- Analog interfaces:
  - 3-channel, 10-bit ADC.
- Radio transceiver:
  - Fully integrated 2.4 GHz CMOS transceiver
  - Single wire antenna.
- Package:
  - Wettable Flanks FCQFN 22 pins, 3.5 mm × 3.5 mm x 0.55 mm, 0.5 mm pitch.

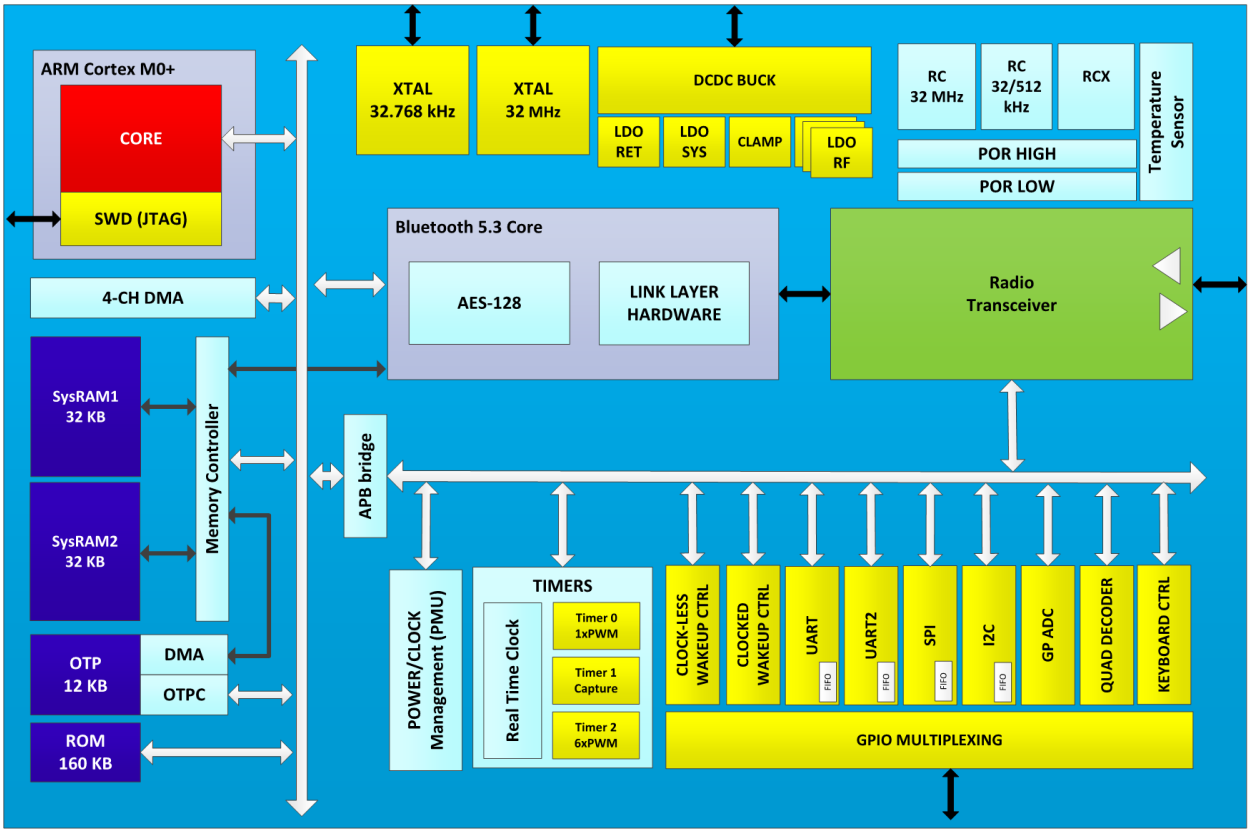

Figure 1. DA14533 block diagram

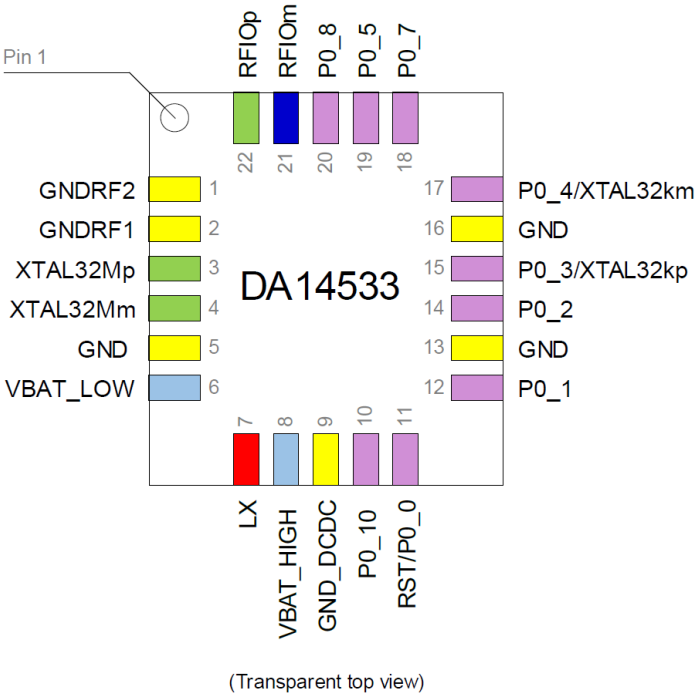

Figure 2. WFFCQFN22 pin assignment (top view)

Table 1. Ordering information

Part number	Package	Pitch (mm)	Size (mm)
DA14533-00000RN2	WFFCQFN22	0.5	3.5 × 3.5 x 0.55

3.1 Device Revision Numbering and Marking

The revision number of the chip can be read from the device by reading the registers mentioned in Table 2 and Table 3. The result should be one of the options in Table 4.

Table 2. CHIP_REVISION_REG (0x50003214)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII 0x41 = 'A', 0x42 = 'B'.	0x41

Table 3. CHIP_TEST1_REG (0x500032F8)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_LAYOUT_REVISION	Chip layout version, corresponds with type number in ASCII	0x42

Table 4. Chip revision numbering

Commercial number	Package	CHIP_REVISION_REG (0x50003214)	CHIP_TEST1_REG (0x500032F8)
DA14533-00A02RN2	WFFCQFN22	0x41 (A)	0x42 (B)

3.2 The DA14533 System

Only a few external components are required to have DA14533 operational:

- Inductor, 2.2 µH for internal DCDC buck converter. In bypass configuration, the inductor can be removed.
- Capacitors on VBAT_HIGH and VBAT_LOW for internal DCDC converter. Their value depends on the type of power source.
- XTAL 32 MHz, provides the main system and Bluetooth LE clock.
- XTAL 32 kHz, as the low-power clock in Sleep mode. When RCX (less accurate) is used, XTAL 32 kHz can be omitted.
- For some applications an RF low-pass filter is required to suppress spurious emissions.
- Antenna is either printed or ceramic.

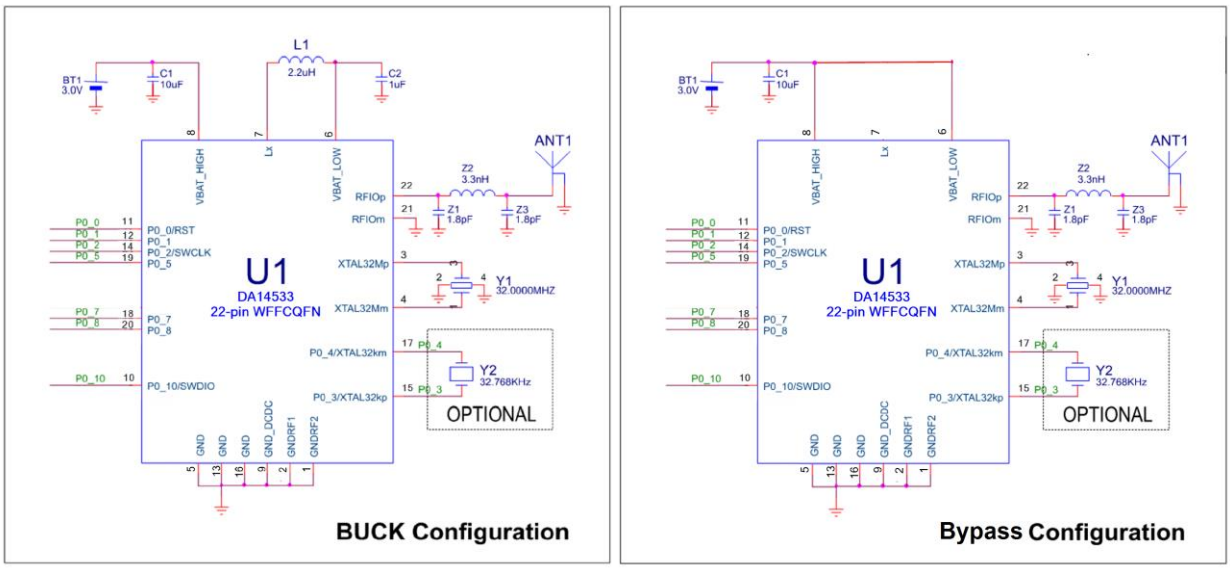

Figure 3. DA14533 system configurations

3.2.1 The Power Section of DA14533

The DA14533 has a flexible power setup and can operate in two different power configurations: Buck and Bypass. Depending on the needed power efficiency, Buck mode is providing a better efficiency than Bypass

mode. In Bypass mode, the DCDC converter is not used and because of that there is no need for an external inductor. This results in a cheaper BOM, but also in lower power efficiency.

The integrated power management logic allows you to effortlessly select their preferred mode with minimal hardware adjustments.

3.2.1.1 The PMU of DA14533

The DA14533 has an integrated Power Management Unit (PMU), which consists of a VDD Clamp, Power on Reset (POR) circuitry, a DCDC converter and various LDOs.

The PMU integrates two main power rails VBAT_HIGH, VBAT_LOW and the internal VDD power rail.

- VBAT_HIGH voltage is in the range of 1.8 V – 3.6 V. This power rail is used for the blocks that require a higher supply voltage. The OTP and the GPIOs are connected to this power rail. The lowest voltage for OTP reading is 1.66 V whereas to write OTP this is 2.25 V.
  VBAT_HIGH is protected by the power-on-reset circuit POR_HIGH, which generates a Power On Reset when the voltage drops below 1.66 V (V_{TH_L}) for more than 50 µs and releases the reset at typically 1.75 V.
- VBAT_LOW is the main system supply, with the lowest voltage equal to 1.2 V. The functional range is between 1.2 V - 3.3 V.
  As most internal blocks are powered from this power rail through LDOs (Figure 4), the most efficient voltage to apply is 1.2 V.
  VBAT_LOW is protected by the power-on-reset circuit POR_LOW, which generates a hardware reset when the voltage drops below 1.1 V (V_{TH_L}) for more than 50 µs and release the reset at typically 1.15 V. See Power On Reset section in datasheet of DA14533.

The internal VDD power rail supplies the digital power domains including RAM blocks. It is generated internally, and the voltage is between 0.75 V and 0.9 V, depending on the Power mode of the system (active, sleep, and so on).

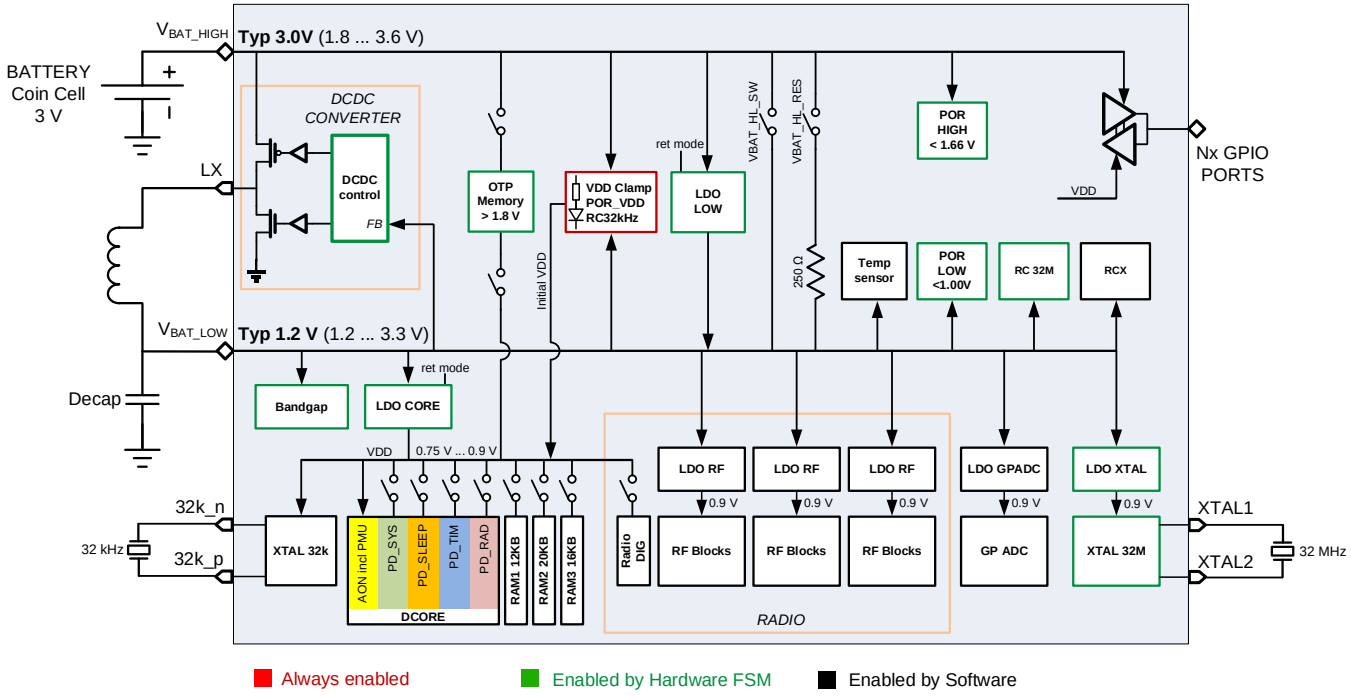

Figure 4. DA14533 SoC power management unit (PMU)

There are 2 setups for the DCDC converter of the PMU: Buck and Bypass mode. The difference of these setups is given by the connection of the supply voltage (Figure 5).

In Bypass mode, VBAT_HIGH and VBAT_LOW rails are tied together and the DCDC converter is not used.

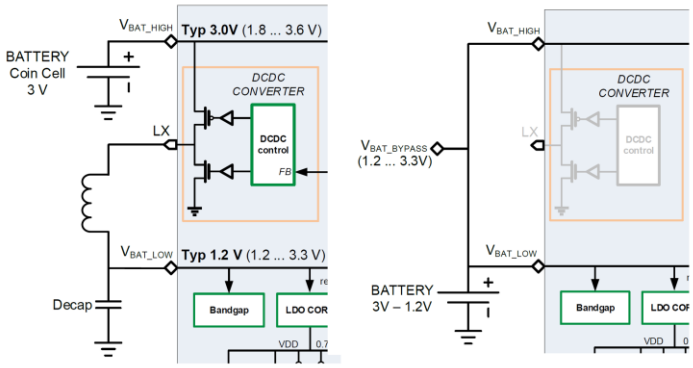

Figure 5. Battery connection for buck (left) or bypass (right) configuration

Table 5. Typical rail voltages and their sources in the various PMU modes

Configuration	Mode	VBAT_HIGH		VBAT_LOW	
		Voltage rang	Supplied to/generated from	Voltage range	Supplied to/generated from
BUCK *Supply on VBAT_HIGH*	Active	1.8 V to 3.6 V	VBAT	1.2 V	DCDC out
	Deep or Extended Sleep	1.8 V to 3.6 V	VBAT	1.2 V	LDO_LOW
	Hibernation	1.8 V to 3.6 V	VBAT	0 V	
Bypass *Supply on VBAT_HIGH, VBAT_LOW*	Active	1.8 V to 3.3 V	VBAT	1.8 V to 3.3 V	VBAT
	Deep or Extended Sleep	1.8 V to 3.3 V	VBAT	1.8 V to 3.3 V	VBAT
	Hibernation	1.8 V to 3.3 V	VBAT	1.8 V to 3.3 V	VBAT

3.2.1.2 Important Notices for PMU

Bypass mode: VBAT_HIGH and VBAT_LOW are shorted on the PCB. This mode is detected by the chip as boost mode. The software should set the CFG_POWER_MODE_BYPASS flag. Otherwise, the software would stop after booting, when the supply is below 3 V.

As the DCDC converter cannot boost VBAT_HIGH to 1.8 V (default), the initial voltage on VBAT_HIGH must be above 1.75 V to release the POR_HIGH and allow booting.

If the voltage in the system drops below 1.66 V after booting, POR_HIGH must be masked or disabled to prevent a reset.

3.2.1.3 Supplying External Loads

The internal DCDC converter of the DA14533 can be used to supply external loads. Use the application software to select and trim the output voltage.

In Table 6, the external load driving capability of the DCDC converter is summarized.

Table 6. DA14533 DCDC external load supply capability

Configuration	VBAT_HIGH	VBAT_LOW	Maximum load current
BUCK	3.0 V (in)	1.1 V (out)	20 mA

3.2.1.4 The Passive Components

The DCDC converter is internal to the SoC circuit and requires only three external components: two capacitors and one inductor. As the DCDC converter must meet the input and output voltage and load current specifications, proper selection of the external components is very important.

Capacitors

Two capacitors are required, C1 attached to the VBAT_HIGH rail pin, and C2 attached to the VBAT_LOW rail.

The capacitors are of the type Multi-Layer Ceramic Capacitor (MLCC). Note that in MLCC capacitors, the effective capacitance value depends on the DC voltage applied to the capacitor.

For example, GRM155R61E225ME15D is a 2.2 µF capacitor with a rated voltage of 25 V. With 3 VDC applied on its pins, the effective capacitance drops to 1.39 µF.

This effect must be considered, because a low capacitor value can degrade system performance.

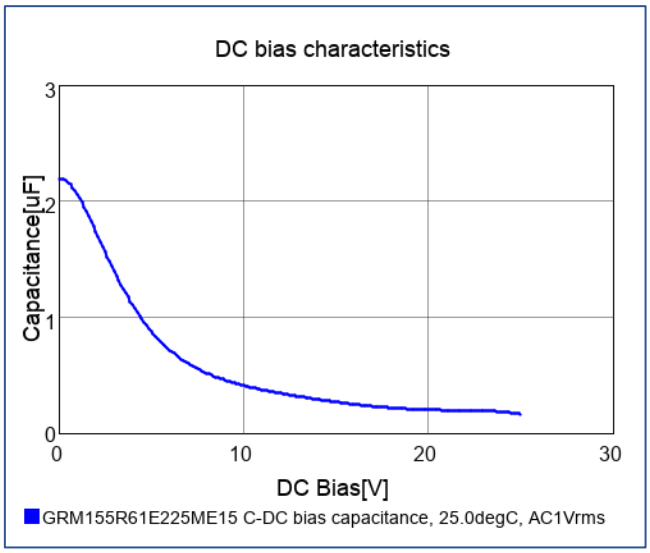

Figure 6. Effective capacitance of a 2.2 µF ceramic capacitor

Buck mode:

- C1: 10 µF effective (input capacitor)
- C2: 1 µF effective (output filter capacitor).

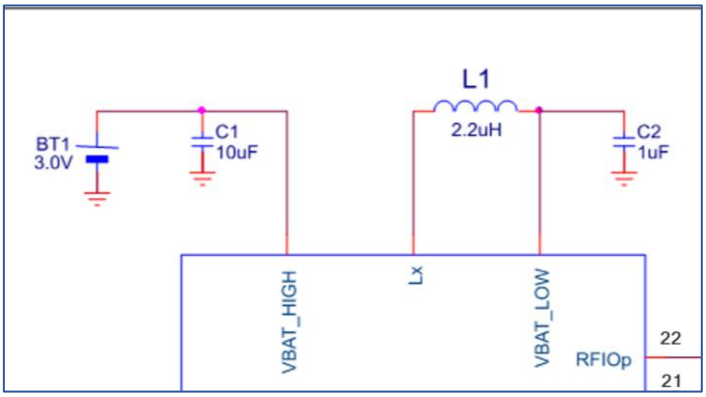

Figure 7. Buck configuration

Bypass mode

In Bypass mode, the DCDC converter is not used and C1, C2 are used for decoupling. As the two power pins (VBAT_HIGH and VBAT_LOW) are located very close, a capacitor of 1 µF is enough. See Figure 8.

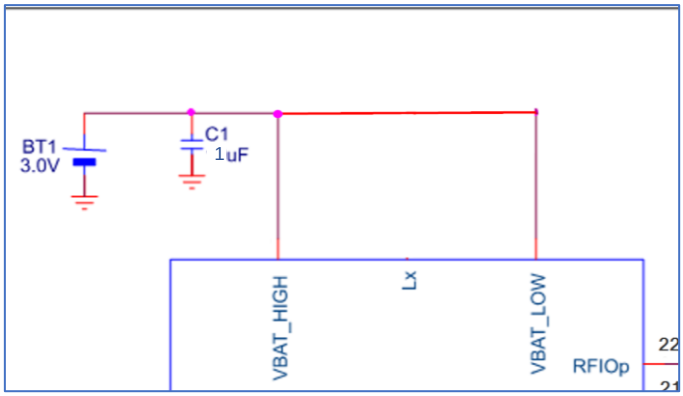

Figure 8. Bypass configuration

Inductor

The DA14533 DCDC converter requires an external 2.2 µH inductor. The choice of inductor impacts the DCDC converter efficiency. Generally, larger inductors with alloy/metal composite cores, low DC resistance and high resonance frequency give better efficiency.

For optimal operation of the DCDC converter, use the general criteria below to select a suitable part:

- 40 MHz Self resonance or higher
- 500 mΩ ESR or lower (the lower the better)
- 2.2 µH with 20% or lower tolerance
- Shielded inductors preferred over unshielded types.

The inductor used on DA14533 Pro-development kit is the DFE201610E-2R2M of Murata.

Table 7. DFE201610E-2R2M characteristics

DCR	0.14 Ω
Imax	1.7 A
Package	0806
Shielded	yes

In cases where the aim is to reduce the size of the system, and the external load currents are negligible, it is possible to reduce the physical size of the DCDC inductor. However, this reduction typically comes at the expense of some conversion efficiency. Therefore, you must seek the optimal balance between power efficiency, size, and cost, aligning with the specific requirements of their intended application.

Figure 9 shows the performance (efficiency) of the DCDC converter for buck mode (3 V, 2.5 V and 1.8 V) configuration. The efficiency is measured for the load as described in Table 6.

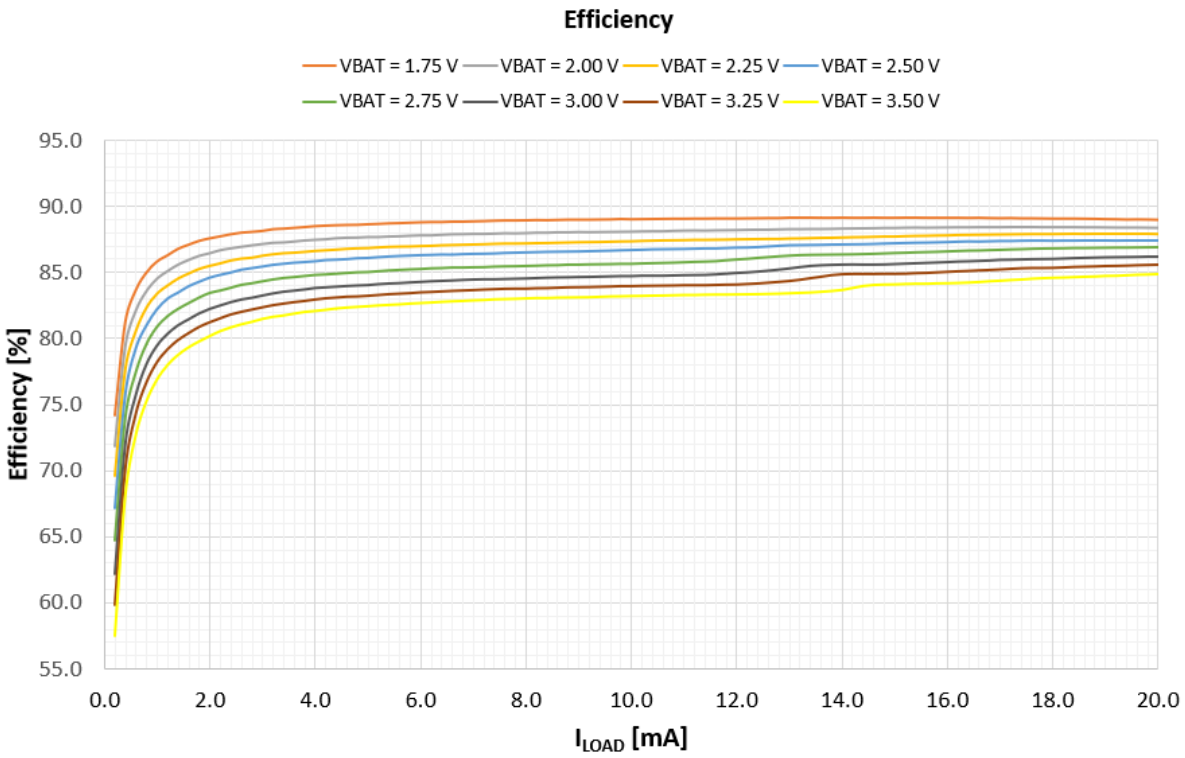

Figure 9. DCDC efficiency in buck configuration

ILIM defines the peak current of the Inductor of the DCDC converter (L1). The peak current varies between DCDC_ILIM_MAX (iLimH) and DCDC_ILIM_MIN (IiLimL). DCCD_ILIM_MAX is the maximum peak current that can pass through the Inductor. For a peak current higher than this limit, the internal switch of the DCDC converter opens.

DCDC_ILIM_MIN and DCDC_ILIM_MAX can be set between 6 mA and 96 mA, with a 6 mA step.

Table 8. Inductor peak current limit

Inductor peak current	DCDC_CTRL_REG (0x50000080) bits	Default	Current
DCDC_ILIM_MAX	15:12	0x8	54 mA
DCDC_ILIM_MIN	11:8	0x4	30 mA

The current limit values in Table 8 are set in the SDK and fits in most use cases. In general, the recommendation is to leave the current limit values as is, since the system performance is verified with these settings. In special cases, you can adjust the settings to fit the needs of the application. However, changes in these settings may affect system performance.

3.2.2 XTAL, 32 MHz (Y1)

The system clock of DA14533 is 16 MHz, which is generated from a 32 MHz crystal oscillator. The crystal oscillator consists of an external 32 MHz XTAL and the internal clock oscillator. The recommended operating conditions are given in Table 9.

Table 9. XTAL32 MHz oscillator - recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL_32M	Crystal oscillator frequency			32		MHz
ΔfXTAL	Crystal frequency tolerance	After optional trimming; including aging and temperature drift. Note 1	-20		20	ppm
ΔfXTAL_UNT	Crystal frequency tolerance	Untrimmed; including aging	-40		40	ppm

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		and temperature drift. Note 2				
$ESR_{\_1pF}$	Equivalent series resistance	C_0<1pF			200	Ω
$ESR_{\_3pF}$	Equivalent series resistance	C_0<3pF			80	Ω
$ESR_{\_5pF}$	Equivalent series resistance	C_0<5pF			50	Ω
C_L	Load capacitance	No external capacitors are required	4	6	8	pF

Note 1 Using the internal varicaps a wide range of crystals can be trimmed to the required tolerance.

Note 2 Maximum allowed frequency tolerance for compensation by the internal varicap trimming mechanism.

The selected crystal for the DA14533 Pro-Devkit is the XRCGB32M000F1SBAR0 of Murata. The XTAL specification is shown in Table 10.

Table 10. Selected main XTAL specification

Parameter	Description	Min	Typ	Max	Unit
Frequency	Fo		32		MHz
Operating Temperature Range	Top	-40		105	°C
Load Capacitance	CL		6		pF
Drive Level	DL			300	µW
Equivalent Series Resistance	ESR			50	Ω
Frequency Tolerance	dF/Fo	-10		10	ppm
Frequency shift by Temperature	dF/F25	-20		20	ppm
Aging	dF/F25	-2		2	ppm
Package	2.0x1.6 mm				mm × mm

3.2.2.1 32 MHz XTAL Trimming

The 32 MHz (XTAL32M) crystal oscillator has trimming capability. The frequency is trimmed by two on-chip variable capacitor banks, see Figure 10. Both capacitor banks are controlled by the same 8-bit register, CLK_FREQ_TRIM_REG.

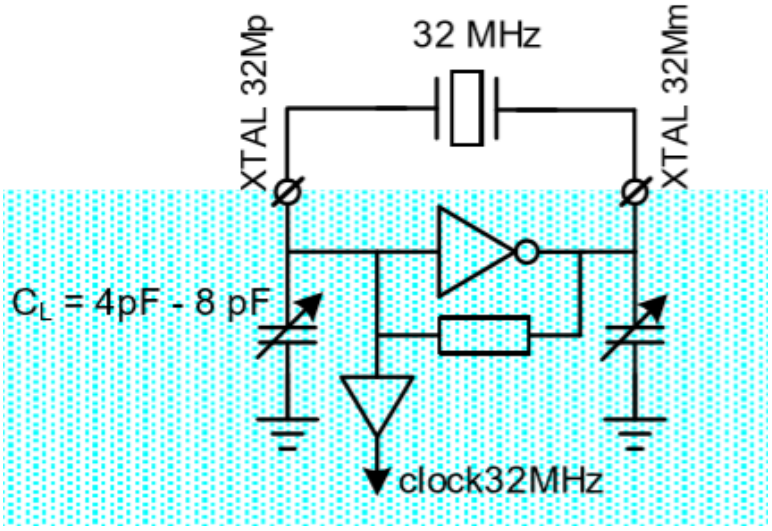

Figure 10. The circuit of 32 MHz crystal oscillator

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0x00, the minimum capacitance and thus the maximum frequency is selected.

With CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0xFF, the maximum capacitance and thus the minimum frequency is selected, see Figure 11.

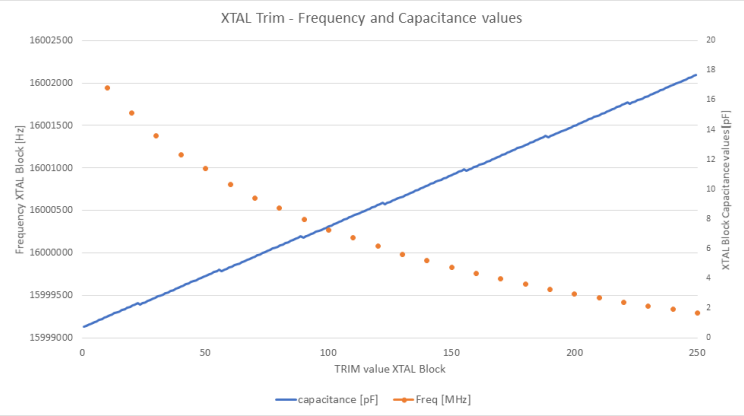

Figure 11. 32 MHz XTAL oscillator capacitance value versus frequency

It is strongly advised to trim the crystal (XTAL) to achieve optimal RF performance and power consumption.

Not trimming the crystal might lead to out of spec RF, especially when taking frequency drift due to temperature changes and aging into account.

Crystal trimming is fully supported by the PLT, see Ref. [2], without the need for external equipment or can be performed manually.

Manual crystal trimming is an iterative algorithm:

1. Set the TRIM-value.
2. Measure the resulting frequency.
3. Adapt the TRIM value until frequency error < 5 ppm.

3.2.3 XTAL, 32.768 kHz (Y2)

You can put an external crystal of 32.768 kHz on pins P0_3 and P0_4 of DA14533 (an external digital clock can also be applied on pin P0_3).

This XTAL oscillator does not have varicap tuning, so the frequency accuracy of this clock depends on the selected component. Select a crystal that matches the specification given in Table 12. The recommended operating conditions for the 32.768 kHz crystal oscillator are in Table 11.

Table 11. XTAL oscillator 32 kHz - recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fXTAL_32M	Crystal oscillator frequency		30	32.768	35	kHz
ESR	Equivalent series resistance				100	kΩ
CL	Load capacitance	No external capacitors are required for a 6pF or 7pF crystal	6	7	9	pF
C0	Shunt capacitance			1	2	pF
PDRV_MAX	Maximum drive power		0.1			µW
ΔfXTAL	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is dominated	-250		250	ppm

A crystal that can be used is the SC20S-7PF20PPM of SEIKO Instruments. The specification is in Table 12.

Table 12. Selected main XTAL specification

Parameter	Description	Min	Typ	Max	Unit
Frequency	Fo		32.768		kHz
Operating Temperature Range	Top	-40		+85	°C
Load Capacitance	CL		7		pF
Equivalent Series Resistance	ESR			90	kΩ
Shunt Capacitance	Co		1.3		pF
Frequency Tolerance	dF/Fo	-20		+20	ppm
Aging, per year	dF/F25		±3		ppm
Drive Level	DL		0.1	1	µW
Package	2.05 x 1.2 x 0.6				mm

Note 1 There is no 32.768 kHz crystal used on the DA14533 PRO-development kit. An internal RCX oscillator is used instead.

In most applications the DA14533 can run with good accuracy with its internal RC oscillator (RCX) and therefore the XTAL32k is not needed. For applications with more demanding accuracy/drift characteristics, such as timekeeping, consider using the XTAL32k.

3.2.4 Reset

During power on and before booting, the reset pin is active high and is assigned on P0_0. This is the hardware reset. After booting, reset pin assignment and operation is handled by software.

During boot, P0_0 is also assigned as output to UART and SPI for the time required from each booting step. At the end of each boot step, P0_0 is assigned again to Reset.

Table 13. P0_0 assignment during boot

Pin	Booting sequence	State	Comments
P0_0	Before boot	RST	Input with pull down
	During boot	MISO, (Boot Step 1) UTX, (Boot Step 4) MOSI. (Boot Step 5) RST	P0_0 is handled from Booting sequence. At the end of each step, and before next booting step, P0_0 is assigned to Reset
	After boot	RST/GPIO	Handled by the software.

The RST functionality on P0_0 can be disabled by setting the HWR_CTRL_REG[DISABLE_HWR] bit.

Special consideration regarding Reset functionality and P0_0 multiplexing, see Appendix A.

3.2.5 JTAG

JTAG consists of SWDIO and SWCLK. SWCLK is assigned to P0_2 and SWDIO is assigned to P0_10. But by changing SYS_CTRL_REG (0x50000012), SWDIO can also be assigned to P0_1, P0_5 or P0_10.

During the booting sequence, JTAG is not enabled. If no bootable device is found on any of the serial interfaces, the booter can do two things depending on what was stored in the Configuration Script (CS). If the ‘Debugger disable’ (0x70000000) command is stored in the CS, the booter starts rescanning the peripherals. Otherwise, it enters an endless loop with the debugger (JTAG) being enabled.

To use the JTAG GPIOs as general-purpose pins, the JTAG function must be disabled by clearing the debugger enable bits. See Figure 12. The same bits can be used to remap the JTAG pins.

SYS_CTRL_REG (0x50000012)

Bit	Mode	Symbol	Description
8:7	R/W	DEBUGGER_ENABLE	Enable the debugger. This bit is set by the booter according to the OTP header. If not set, the SWDIO and SW_CLK can be used as gpio ports. 0x0: no debugger enabled. 0x1: SW_CLK = P0[2], SW_DIO=P0[5] 0x2: SW_CLK = P0[2], SW_DIO=P0[1] 0x3: SW_CLK = P0[2], SW_DIO=P0[10]

Figure 12. Debugger enabling

3.3 UART

There are three different UART configurations possible: single-wire UART (if single-wire is preferable due to low pin number), two-wire UART, and four-wire UART.

UART, single-wire: UTX and URX are multiplexed together on a single pin of DA14533. On board level, a 1 kΩ resistor separates the two signals. See Figure 13.

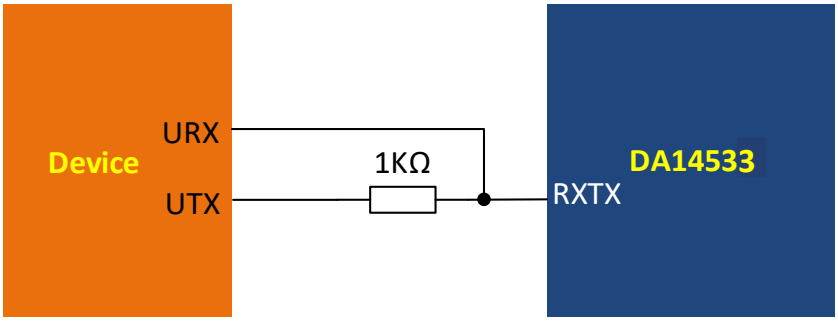

Figure 13. Single UART hardware configuration

In a regular UART bus, UTX and URX lines can be active simultaneously. In most use cases of the DA14533 (boot, HCI commands and so on), the traffic on the UART is half duplex and a single wire can be used for all UART transactions. On the DA14533 side, the SDK UART driver takes care of switching the pin direction.

On the host side, all data sent is echoed back since TX and RX are shorted. For successful communication, the software should be able to discard the echo. Smart Snippets Toolbox, see Ref. [11], implements such a feature and can be used with a single-wire UART.

Single-wire UART is used on the booter. The DA14533 has two options to boot from single-wire UART: from P0_5 in boot step #2 and from P0_3 in boot step #3. After the boot sequence, the application software can redefine any GPIO as single-wire UART.

UART, two-wires: UTX and URX.

Two-wire UART is used in boot step #4. P0_0 and P0_1 are used for UTX (output) and URX (input) respectively.

After booting, the software can reassign the UTX and URX to other pins by setting the Pxx_MODE_REG.

UART, four-wire: This is the full UART with flow control. Set the Pxx_MODE_REG to assign GPIOs. Hardware flow control is mainly needed for external host applications.

3.3.1 SPI Data Flash

There are two available SPI modes on DA14533, Ext-SPI master and Ext-SPI slave. In the Ext-SPI master mode, an external processor (master) can download code to the DA14533. In the Ext-SPI slave, the DA14533 can download code from a slave device such as an external SPI data Flash.

In this case, the bootloader downloads the binary file to RAM and executes it. The default GPIOs during boot are given in Table 14.

Table 14. DA14533 pins assignment for SPI data slave on booting

DA14533 signals	SPI data flash
P0_0	MOSI
P0_1	CS
P0_3	MISO
P0_4	SCK

Booting GPIOs can be changed by either a secondary bootloader, or by declaring them in the OTP header boot-specific mapping.

Data flashes tested successfully are listed in Ref. [9].

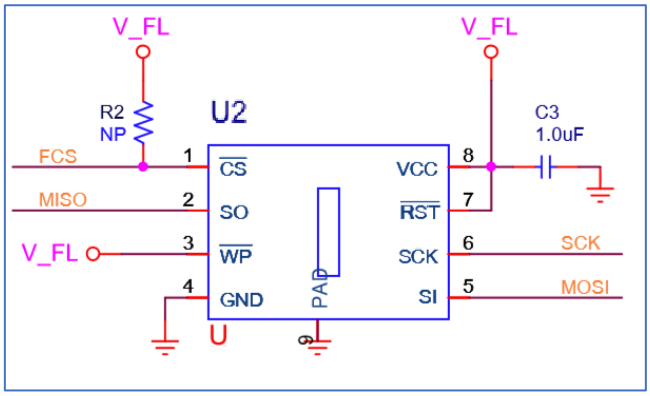

Figure 14. SPI data flash hardware setup

The SPI clock (SCK) frequency is configurable up to 32 MHz. The frequency depends on the physical connections between the DA14533 SoC and the SPI Data flash. On DA14533 Pro Devkit, there is significant capacitive load on the SPI pins, due to signal multiplexing and long traces. On the software development kit (SDK), the frequency used is 2 MHz to boot and 4 MHz for SUOTA.

PCB Layout Notice

The SPI data flash Read/Write frequency depends on the PCB layout. The suggestion is to put the data flash as close as possible to DA14533. In case this is not feasible, consider adding termination resistors in the order of 30 Ω next to source pins. Add GND between routed traces to eliminate crosstalk.

3.4 RF Section

DA14533 provides a 50 Ω single RFIO port for TX and RX without requiring external balun or RF switch. The internal RF power amplifier provides TX RF power from -18 dBm to +4 dBm.

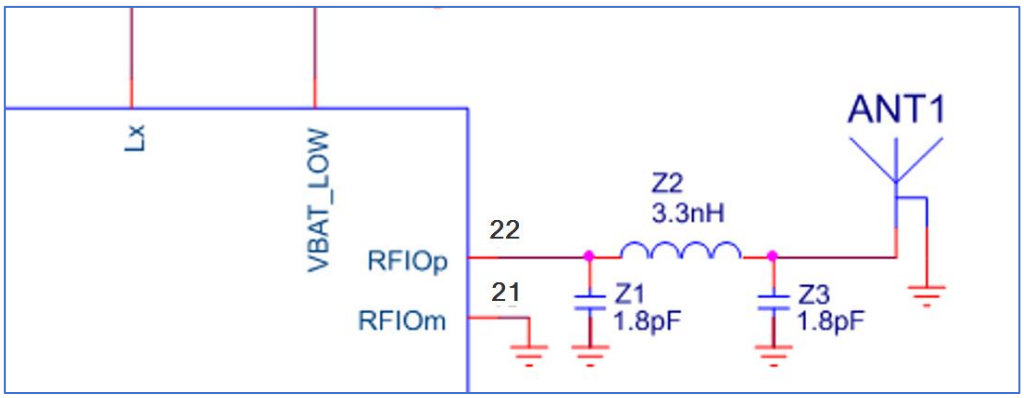

Figure 15. DA14533 RF section

The Pi-filter for Renesas Electronics DA14533 System-on-Ship (SoC) in 2.4 GHz Bluetooth LE applications specifically addresses the conducted and radiated performance.

The objective of the Pi-filter is to suppress the local oscillator leakage, which violates the conducted performance requirements of ETSI, ARIB (Japanese standard) and KC (Korean certification) standards.

There is no violation of FCC regulations. Consequently, you can omit the Pi-filter if only the FCC regulations must be adhered to.

The Pi-filter configuration is chosen, because it gives the best suppression with minimal power loss at fundamental frequencies. The filter is a third order Chebyshev Lowpass Filter with a cut-off frequency at 2600 MHz, and passband ripple of 0.4 dB, see Ref. [7].

3.4.1 Pi Filter

Figure 16 shows the filter topology.

Figure 16. Pi filter topology

Components used:

- Capacitors: 1.8 pF, 0201, Murata, PN: GRM0335C1H1R8CA01
- Inductor: 3.3 nH, 0201, Murata, PN: LQP03TN3N3B02.

Measured S21 parameters give a minimum -15 dBm attenuation at 4.8 GHz. The filter gives a 0.7 dBm to 1.2 dBm loss in sensitivity and 0.2 to 0.7 dBm in TX power.

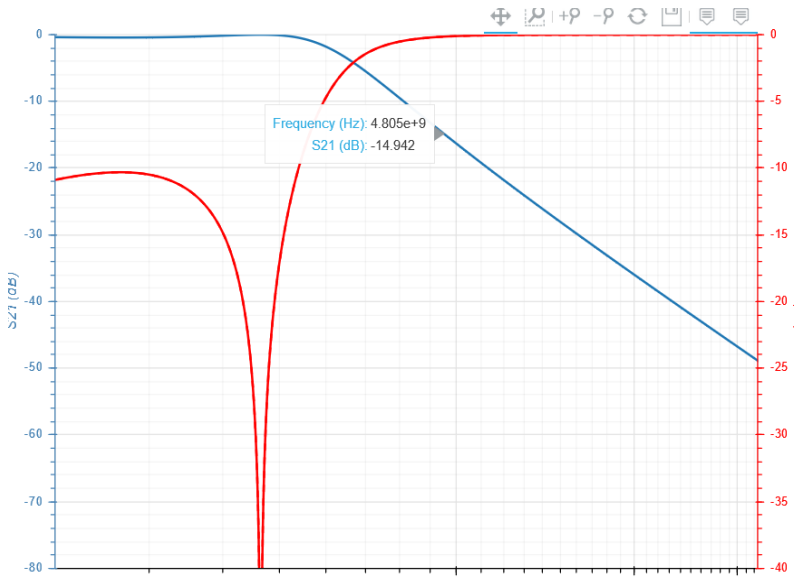

Figure 17. S21 simulated parameters

3.4.2 Conducted Performance

The measurements are done with a calibrated spectrum analyzer and RF cables. The levels are measured at the SMA output with the DUT.

All measurements are calibrated for cable losses.

3.4.2.1 TX Measurements

The test was done at ch19, room temperature, normal operating conditions. Measurements are done in burst mode, modulated signal.

Table 15. Fundamental power and harmonics, Conducted mode, PA in 3 dBm mode

	Fundamental	2nd harm	3rd harm	4th harm	5th harm
Without RFIO filter	4.29	-43.56	-42.03	-47.85	-36.17
With RFIO filter	3.79	-58.8	-72.6	-74.3	-65.5

Note 1 All values are in dBm.

Note 2 Measurement accuracy < ± 0.3 dB.

3.4.2.2 RX Measurements

The test was done at ch19, measurement frequency 2*(2440+1 MHz) = 4882 MHz.

Table 16. LO leakage, Conducted mode results

	Without RFIO filter	With RFIO filter
LO leakage power	-39.26	-55.26

Note 1 All values are in dBm.

Note 2 Measurement accuracy < ± 0.3 dB.

3.4.2.3 Antenna and Current Measurements

The antenna's transmit power is received from the RF circuitry through the TX line (matched to an impedance of 50 Ω). Matching the input impedance of the antenna to 50 Ω is required to ensure that the maximum power is transferred from the RF circuity to the antenna with only a negligible amount being reflected. However, the matching circuits are not always perfect, and the components present tolerances.

Also, if a printed antenna is in contact or close to other surfaces (especially conductive materials), it is detuned, and a lot of RF energy is not radiated, but reflected to the RF transmitter.

Peak current measurements depend on the antenna matching. A not perfectly matched antenna results in a higher power consumption during RF transmission.

The safest way to measure the peak power consumption of the system (hardware and software) is to have instead of the antenna a 50 Ω termination (dummy load).

4. PCB Layout Guidelines

PCB guidelines for the DA14533 are presented in this section using the daughterboards of the Pro-Devkit as reference: DA14533-db-qfn22(610-05)

4.1 PCB Layout of DA14533

The implemented PCB layout is based on the schematic shown in Figure 18. The same layout can be used for buck, boost, and bypass configurations (for bypass, L1 must be removed from the circuit).

A low-pass filter was added on the RFIOp trace, which presents impedance on both sides, equal to 50 Ω. The antenna is not shown in the schematic in Figure 18.

Finally, Y2, 32.768 kHz can be omitted.

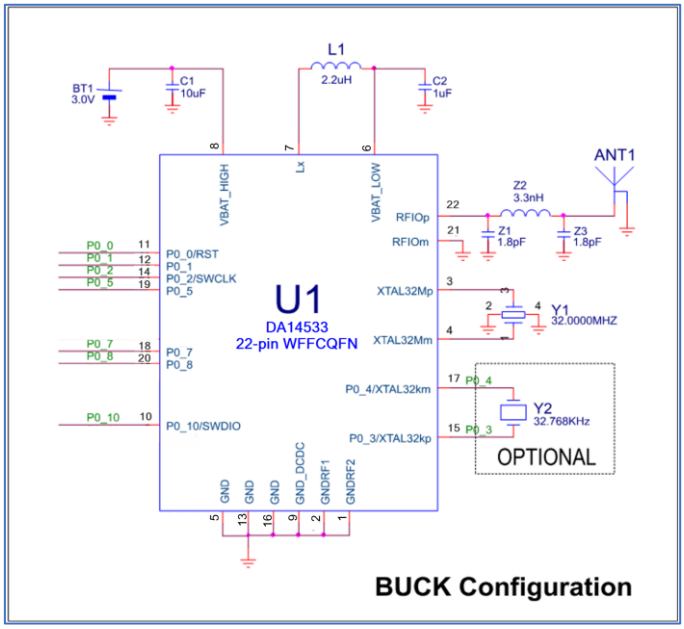

Figure 18. DA14533 WFFCQFN22 reference circuit

PCB rules applied on the Pro-Daughterboard:

- Number of layers: 4
- Material: FR-4 – no microvias
- Vias: Mechanical
- Under chip: Diameter 0.45 mm/drill 0.15 mm
- Rest PCB areas: Diameter 0.5 mm/drill 0.15 mm
- Copper clearance: 0.1 mm
- Copper width: 0.1 mm.

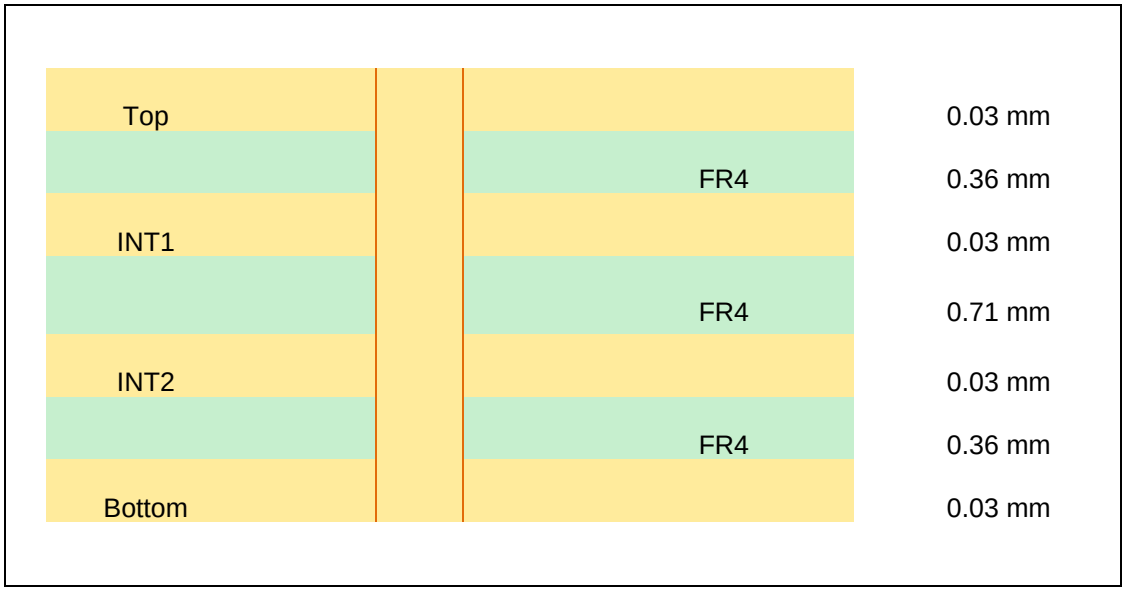

Figure 19. PCB cross section

PCB Layout guidelines

Grounding:

- Use INT1 layer free of routing and assign it as reference ground.
- Separate RF ground pins of DA14533 from the rest ground pins.
- Connect pin 19 to GND with vias as shown in Figure 20.
- Short 20, 21, 23 GND pins together and use two GND vias, as shown in Figure 20.
- Add GND stitching vias to increase the performance of the system.

Power management:

- Put capacitors C1 and C2 close to the pins of DA14533. Apply a GND per capacitor next to the GND pin.
- Put L1 as close as possible to the chip. Remove grounding under the inductor to minimize any possible coupling from reference ground.

XTALs:

- Put XTALs close to the chip.
- Try to have a ground shield around XTALs.
- There is no need to route the two XTAL traces differentially.

Remove the area on the INT1 ground layer under the pads of XTAL to reduce coupling as shown in Figure 21. Use the 3rd or 4th layer to shield the XTAL pads.

RF strip:

Calculate and route a 50 Ω RF stripline between DA14533 RFIOp pin and antenna. A low-pass filter, consisting of three components (Z1, Z2, Z3) must be put as close as possible to the chip. Both capacitors must be grounded on the same side of the RF stripline preferably to RFIOm, which is the RF reference ground.

In case the antenna needs matching, put a matching circuit next to the antenna. Ground the components on the same side of RF trace, same as in the low-pass filter.

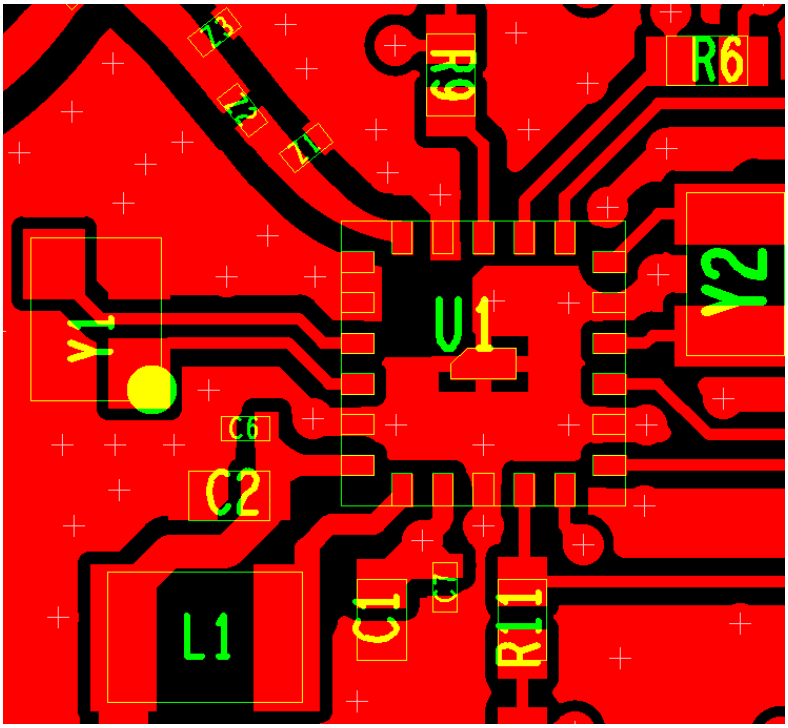

Figure 20. PCB placement and routing – top layer

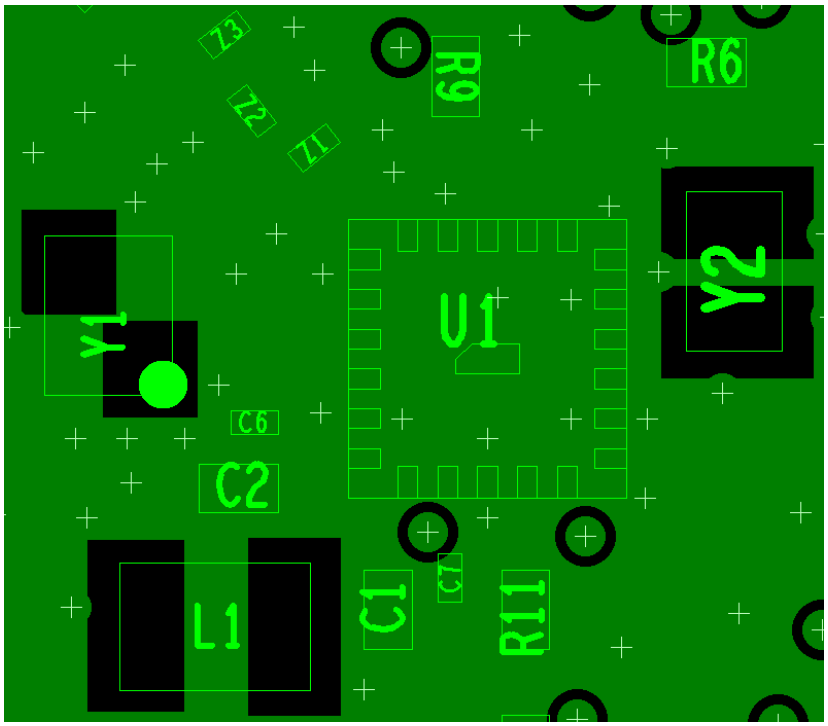

Figure 21. FCGQFN24 PCB placement and routing – GND plane - INT1 layer

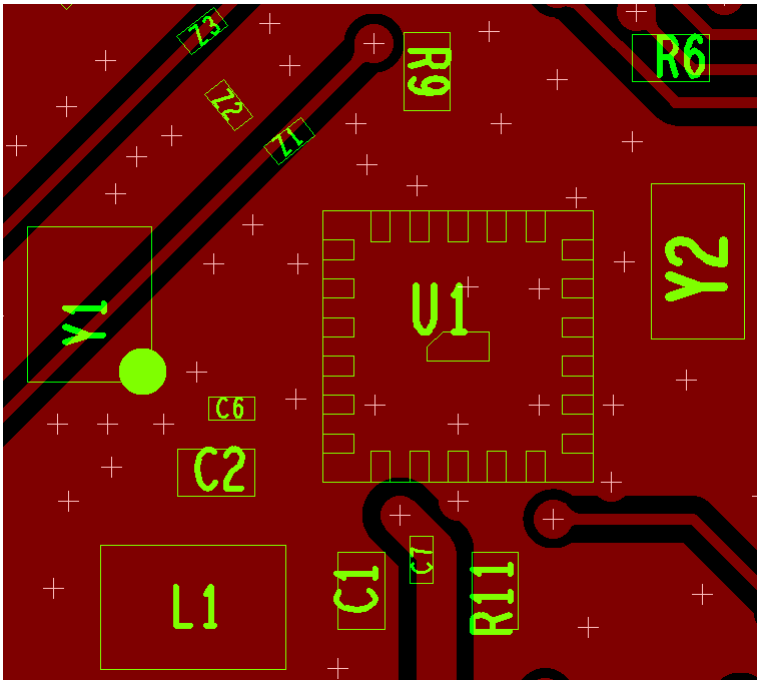

Figure 22. FCGQFN24 PCB placement and routing – INT2 layer

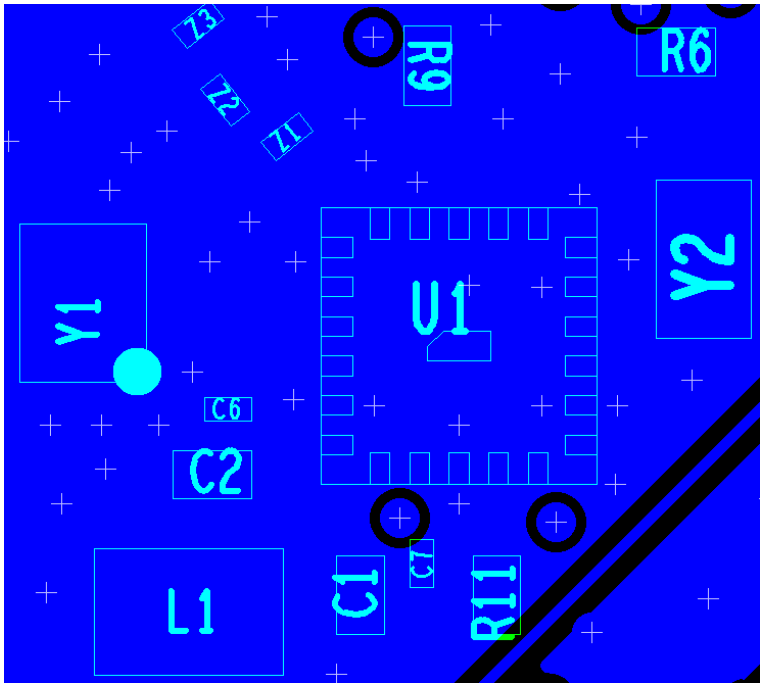

Figure 23. FCGQFN24 PCB placement and routing – GND bottom layer

4.1.1 Minimal System PCB Layout

An example of the PCB layout occupied from the DA14533 system is shown in Figure 25.

The implemented system uses the necessary components. Crystal 32 kHz is omitted. The inductor is the same as on the Pro-Devkit whereas all signals are fanned out. Component placement is much more efficient than the Pro-Devkit, as there is no need for signals multiplexing. Dimensions of the area are 5.8 mm x 7.6 mm.

The PCB can have either two or four layers. For a two-layer design, close the openings under the XTAL pads on the second layer.

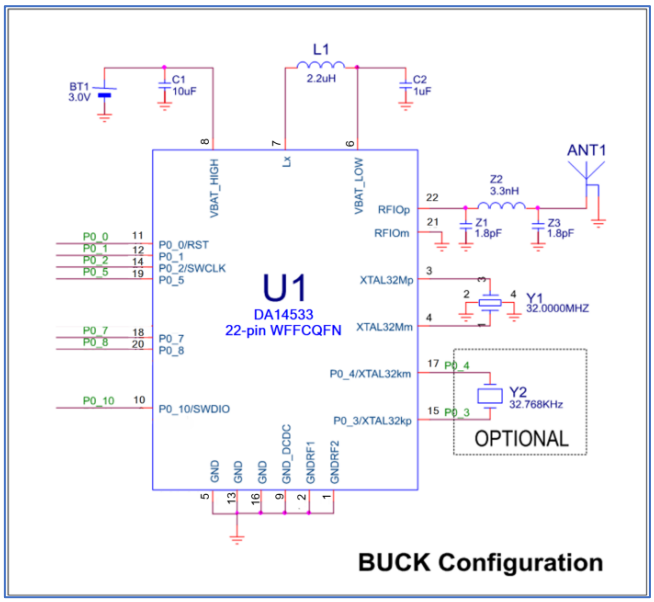

Figure 24. PCB occupied area for DA14533 system (the schematic)

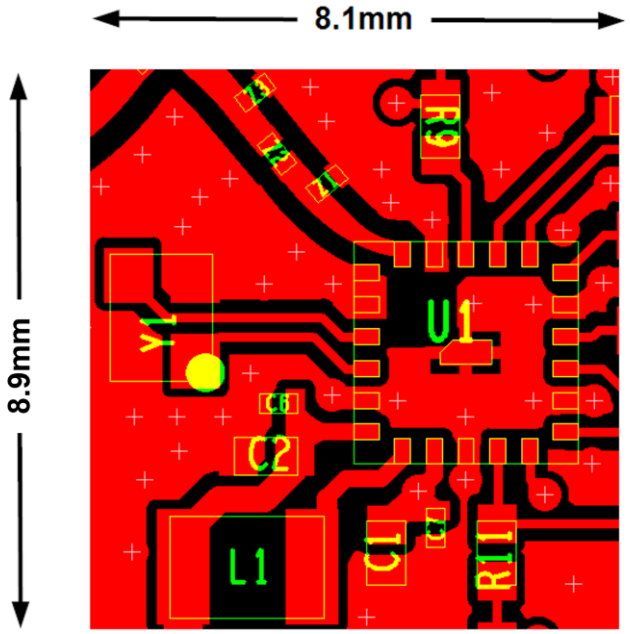

Figure 25. PCB occupied area for DA14533 system

Appendix A Special Considerations for Reset Functionality

There are three main reset signals in the DA14533:

- The hardware reset: it is optional and triggered by the RST pad (P0_0) when it becomes active for a short period of time (less than the programmable delay for POR).
- The Power-On Reset (POR): it is optional and triggered by a GPIO set as the POR source with a selectable polarity and/or the RST pad (P0_0) after a programmable time delay.
- The software reset: it is triggered by writing the SYS_CTRL_REG[SW_RESET] bit.

For more detailed description, see DA14533 Datasheet in Ref. [1].

Special considerations should be taken when using reset functionality, because:

- RST pad is multiplexed with P0_0 pin (Figure 27).
- P0_0 is also used during boot sequence (Figure 28).
- P0_0 is connected to SPI Flash (as MOSI (SPI_DO)) in many cases.

These cases are discussed in detail in A.1, A.2, and A.3.

A.1 Reset Pad (P0_0)

The DA14533 comprises a reset (RST) pad which is active high. It contains an RC filter with a resistor of 465 kΩ and a capacitor of 3.5 pF to suppress spikes. It also contains a 25 kΩ pull-down resistor (see Figure 26). This pad should be driven externally by a field-effect transistor (FET) or a single button connected to VBAT. The typical latency of the RST pad is in the range of 2 µs.

Features:

- RC spike filter on RST to suppress external spikes (465 kΩ, 3.5 pF)
- Three different reset lines (software, hardware, and POR)
- Latching the cause of a reset operation (RESET_STAT_REG)
- Configurable POR circuitry.

This reset pad is multiplexed with P0_0.

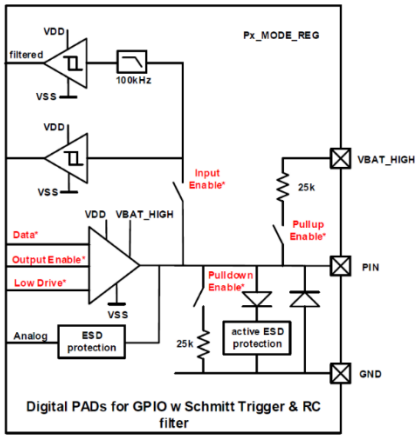

Figure 26. Type B GPIO Pad-GPIO with Schmitt Trigger and RC filter

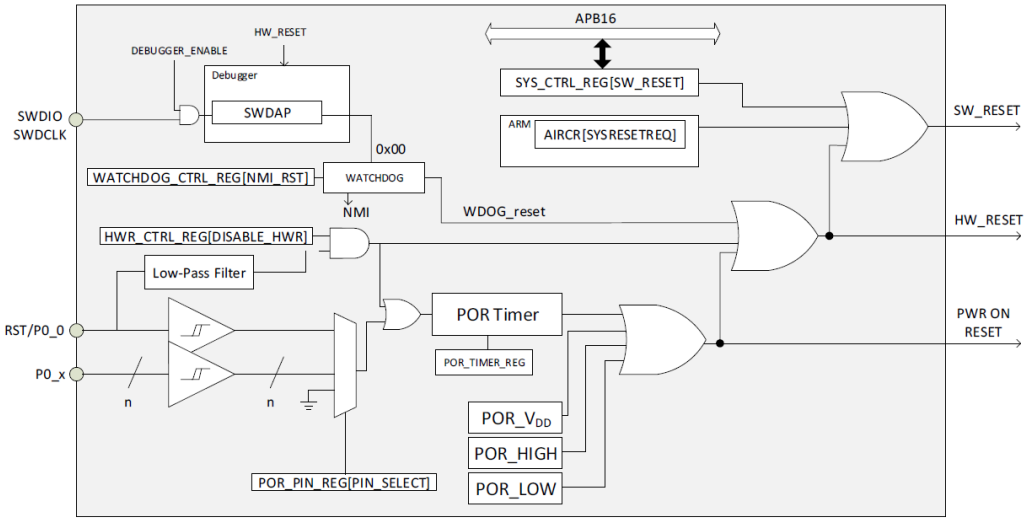

Figure 27. Reset block diagram

A.2 Booting Sequence and P0_0

P0_0 is used as booting pin in the steps shown in Figure 28.

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6
	Boot from ext SPI Master	**Boot from 1 wire UART (1st option)**	**Boot from 1 wire UART (2nd option)**	**Boot from 2 wire UART**	**Boot from ext SPI Slave**	**Boot from I2C**
P0_0/RST	MISO			Tx	MOSI	
P0_1	MOSI			Rx	SCS	
P0_2						
P0_3	SCS		RxTx		MISO	SDA
P0_4	SCK				SCK	SCL
P0_5		RxTx				

Note: The booter will try to boot from the above serial interfaces in the order from Step 1 to step 6.

Figure 28. Booting sequence and booting pins for DA14533

During power on and before booting, the reset pin is active high and is assigned on P0_0. This is the hardware reset. After booting, reset assignment and operation is handled by software.

During boot, the reset functionality POR or hardware reset on P0_0 is multiplexed with SPI Slave MISO (Boot Step 1), UART TX (Boot Step 4) and MOSI (Boot Step 5). During this time reset functionality is disabled. At the end of each boot step, the reset functionality on P0_0 is restored.

Table 17. P0_0 assignment during boot

Pin	Booting sequence	State	Comments
P0_0	Before boot	RST	Input with pull down
	During boot	MISO, (Boot Step 1) UTX, (Boot Step 4) MOSI. (Boot Step 5) RST	P0_0 is handled from Booting sequence. At the end of each step, and before next

Pin	Booting sequence	State	Comments
			booting step, P0_0 is assigned to Reset
	After boot	RST/GPIO	Handled by the software.

The RST functionality on P0_0 can be disabled by setting the HWR_CTRL_REG[DISABLE_HWR] bit.

During start-up sequence the RST pin inputs with pull-down keeping the chip out of reset. After application initialization the RST pin can be switched into GPIO mode. In case an external microcontroller does not drive P0_0, it is recommended to use it as an output to not permit external devices to interfere with the power-up sequence of the chip.

A.3 SPI Flash

P0_0 in many cases is connected to SPI_MOSI of SPI Flash. In this case RST/P0_0 pin should not be driven while the device is booting from the SPI Flash. Any external circuit that triggers hardware reset should not be used during this time.

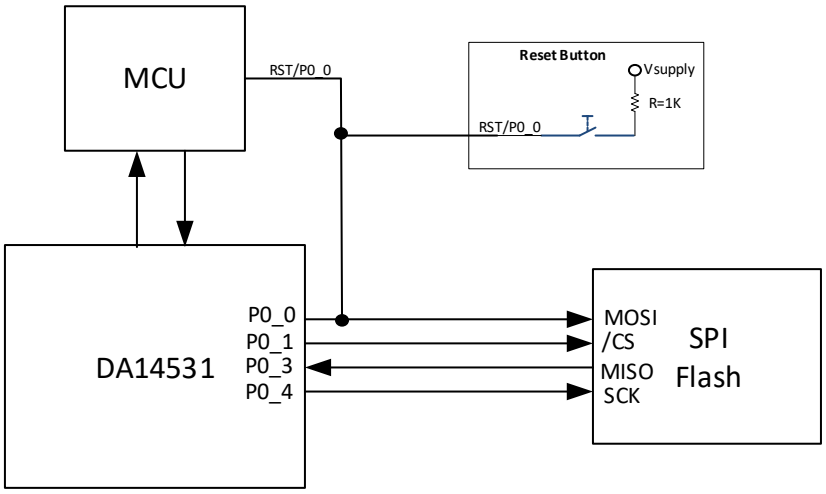

Figure 29. P0_0 connected to SPI_MOSI

A.4 Examples

A.4.1 Example 1: Booting from two-wire UART

Since the idle state of the UART lines are default high, FTDI devices and microcontrollers tend to have a pull-up resistor on their RX line to avoid continuous break. Since P0_0 is used as a TX while booting and also as hardware reset, connecting a device might continuously reset the DA14533 due to this external pull-up.

When booting from two-wire UART (Figure 28, Step 4), the TX is mapped to P0_0 which is also used as Reset pin. The device starting its boot sequence detects UART on P0_0/P0_1. After the boot sequence is finished the P0_0 is automatically restored to Reset mode. If a connected external microcontroller or FTDI USB to UART bridge pulls this port high, it triggers a continuous reset.

A valid solution would be to use a stronger R pull-down resistor connected to P0_0 overriding the effect of the receiver's pull-up, as shown in Figure 30.The value of R depends on the pull-up on the receiver's side. This solution is acceptable if there is no constant voltage from an external device on P0_0 to leak through the strong pull-down.

In case that the application requires constant connection on the P0_0/P0_1 due to external interface you must make sure that during booting process of DA14533, the external controller does not drive its RX pin to high state. If the external controller can handle continuous break conditions, due to low state because its RX line then the external pull-down can be omitted.

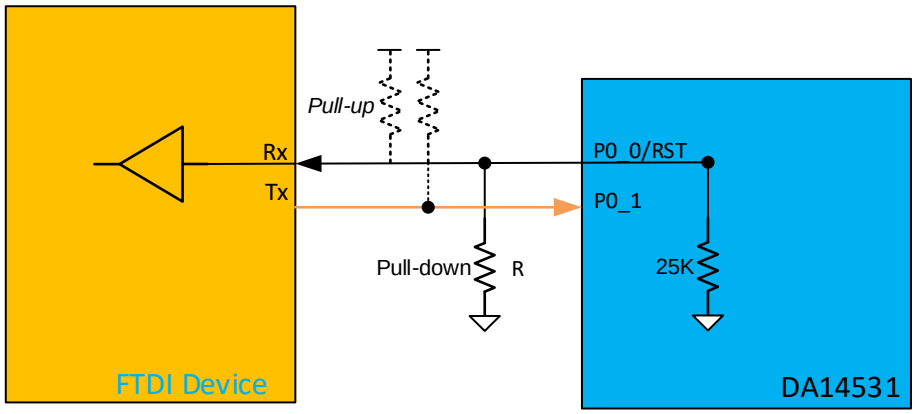

Figure 30. FTDI and DA14533 connection circuit for Reset

Using permanently P0_0 as TX means that reset function of P0_0 is disabled. DA14533 can be reset from external controller by either enabling the reset again through a command or set a GPIO pin to act as a POR source. An alternative solution would be to burn a secondary booter in the OTP and boot from different pins and keep the P0_0 as a reset.

A.4.2 Example 2: RST/P0_0 signal shared with Flash

Special considerations should be taken when RST/P0_0 is shared with a SPI Flash Memory. RST/P0_0 pin should not be driven while the device is booting from the SPI Flash. When the Flash is in use the reset functionality is not available. To access the flash and have the reset functionality of reset pin, follow the steps:

1. Disable RST functionality on P0_0 by setting HWR_CTRL_REG[DISABLE_HWR] bit.
2. Set P0_0 to SPI_MOSI.
3. Access Flash.
4. Enable hardware reset.

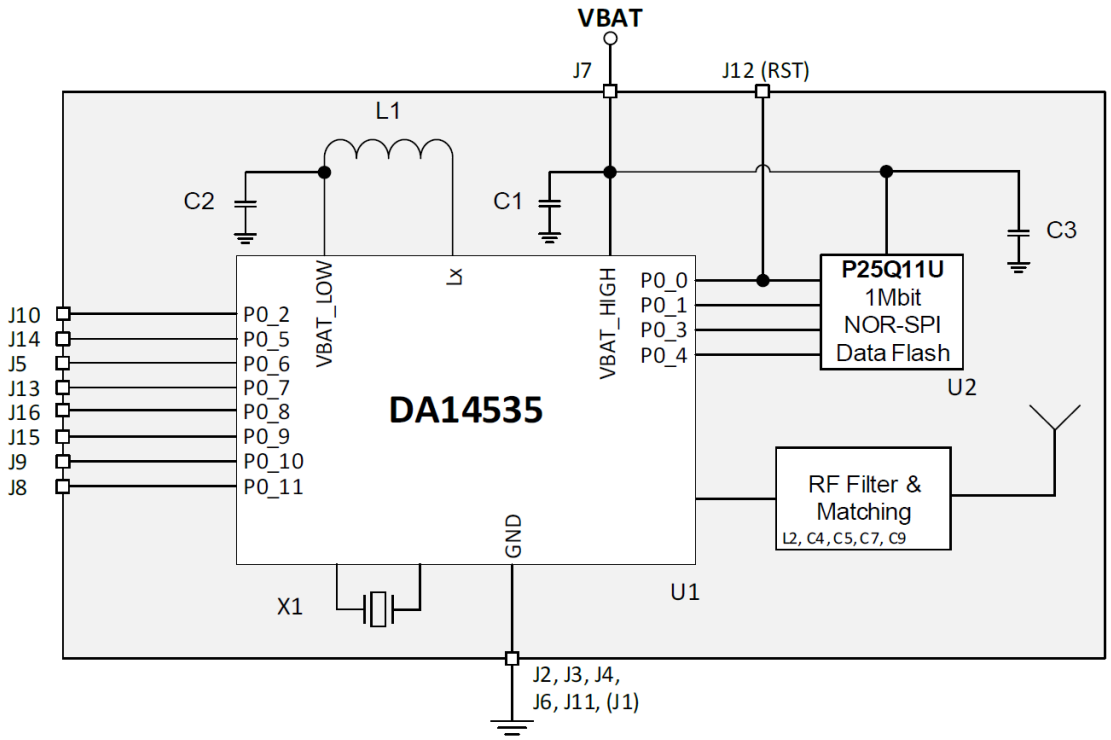

Figure 31. Example of connecting a sensor to the SPI BUS and an MCU to RST and UART of DA14535 SmartBond TINY™ module [376-25-C]

NOTE
DA14535 SmartBond TINY™ module comes with a preloaded demo. See Ref. [12].

Appendix B External Filtering for Quadrature Decoder

DA14533 has an integrated Quadrature decoder that can automatically decode the signals for the X, Y, Z axes of a HID input device, reporting step count and direction. For more information about the decoder, see Ref. [1].

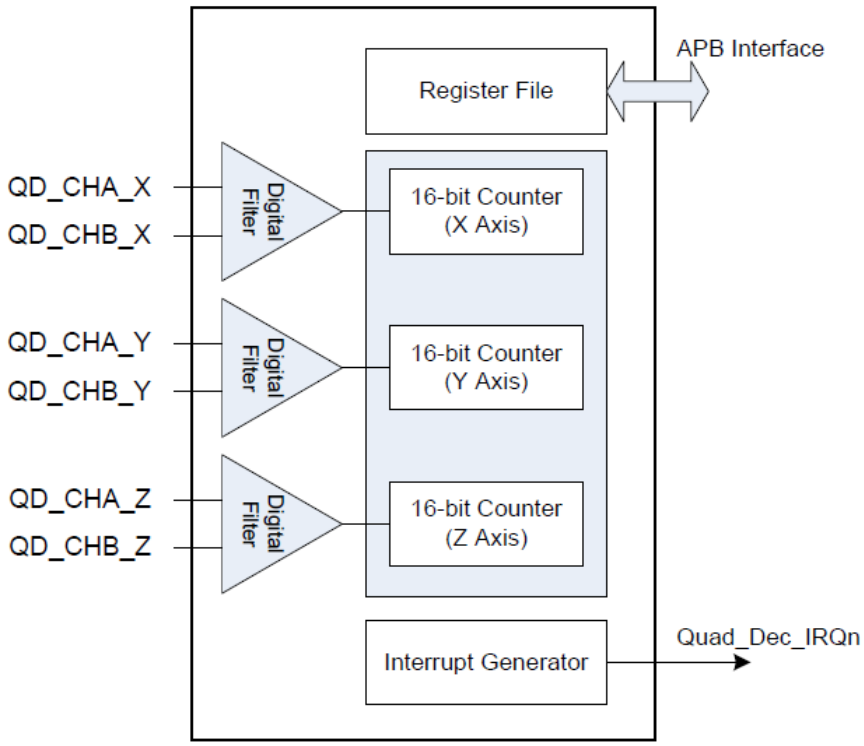

Figure 32. Quadrature decoder block diagram

The decoder is equipped with digital filtering which eliminates the spikes shorter that three clock periods. This means that for sys_clk=16 MHz and maximum time setting QDEC_CLOCKDIV=0x3FF, the decoder can handle bounces in the order of 200 µs. However, bouncing in encoders is relevant and depends on the mechanical characteristics. It can be in the order of some hundreds µs up to a few ms. These long bounces require external filtering. Usually, relevant filtering information can be found in the encoder's manufacturer datasheet. It is suggested to follow manufacturer instructions or apply a generic RC filter like the one shown in Figure 33.

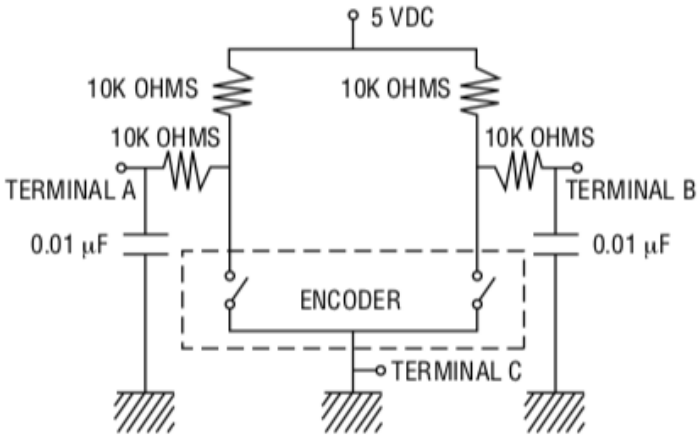

Figure 33. Suggested filter for mechanical incremental encoder

5. Revision History

Revision	Date	Description
1.01	July 16, 2025	Updated figures.
1.00	Mar 11, 2025	Initial version.

STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
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