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Application Note

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Controlling Fluorescent Lamp Ballasts by Using 78K0/Ix2

This application note describes how to control fluorescent lamp ballasts by using the various features of the 78K0/Ix2 microcontroller. Details about <u>power factor correction (PFC)</u> controlled by using a PWM timer that operates in conjunction with internal comparators, <u>half-bridge control with dead time</u> performed by using the PWM timer, protection performed by detecting an overcurrent or overvoltage by using the internal comparators, and DALI communication are provided.

Target devices
78K0/IY2 microcontroller
78K0/IA2 microcontroller
78K0/IB2 microcontroller

CONTENTS

CHAPTER 1 OVERVIEW

This application note describes how to control fluorescent lamp ballasts by using the 78K0/Ix2 microcontroller.

The features for controlling fluorescent lamp ballasts by using the 78K0/Ix2 microcontroller are as follows.

- Power factor correction (PFC) can be controlled by using a PWM timer that operates in conjunction with internal comparators. Therefore, no IC is required for controlling PFC.
- Inverter output with dead time is available. Therefore, no IC is required for performing half-bridge control.
- A 99% power factor can be achieved when the load is about 90 W[Note 1].
- The dimming of fluorescent lamps can be controlled.
- Timer output can be stopped immediately when an overvoltage, overcurrent, or installation or uninstallation of a fluorescent lamp is detected.
- Slave transmission and reception using the DALI communication protocol are supported[Note 2].
- The widths of pulses can be measured to easily receive infrared rays.
- A buzzer can be sounded and the dimming of LEDs can be controlled.

Notes 1. This is measured by using HIOKI 3332 POWER HiTESTER.
2. Peripheral hardware units that support DALI communication are mounted on the 78K0/IA2 and 78K0/IB2 microcontrollers.

Figure 1-1 shows an example of the system block diagram for controlling a ballast by using the 78K0/Ix2 microcontroller. Table 1-1 shows an example of the assignment of the microcontroller pins. Chapter 2 and the following chapters describe how to control a ballast when a ballast board is created according to this block diagram and pin assignment.

Figure 1-1. Example of the System Block Diagram for Controlling a Ballast by Using the 78K0/Ix2 Microcontroller

78K0/Ix2 microcontroller
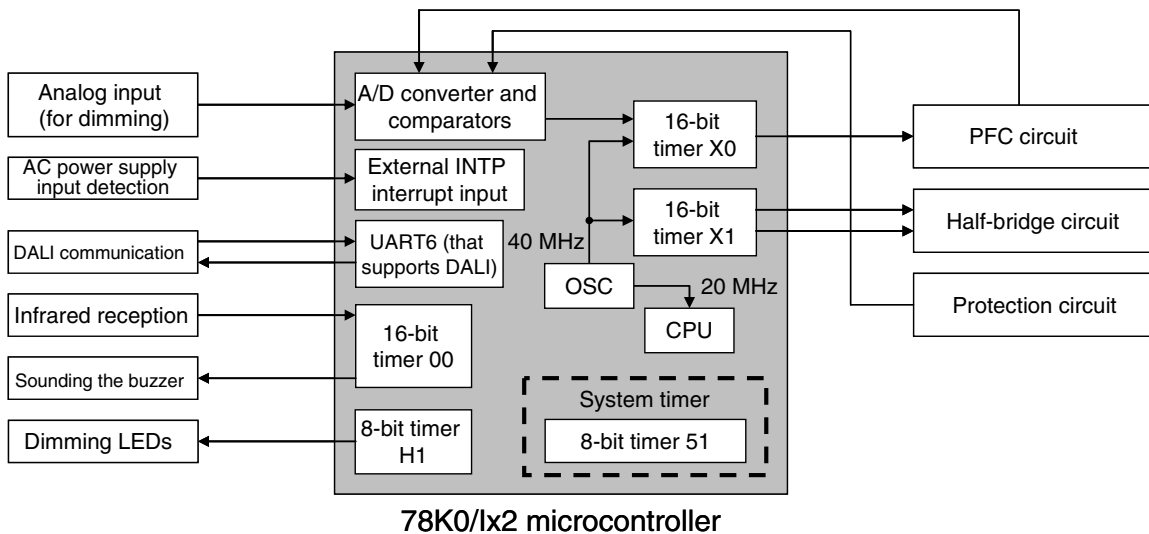
Table 1-1. Example of the Pin Assignment of the 78K0/IB2 Microcontroller

Port Name	Name of the Used Function Pin	I/O	Function
P00	TI000	Input	Infrared signal input
P01	TO00	Output	Sounding the buzzer
P20	ANI0	Input	Analog input for monitoring the boosted DC voltage
P21	ANI1/PGAIN	Input	Analog input for protecting the lamp or operational amplifier input
P22	ANI2	Input	Analog input for protecting the lamp
P23	CMP2+	Input	Comparator input for detecting zero currents (to control PFC)
P24	CMP0+	Input	Comparator input for detecting installation or uninstallation of a fluorescent lamp
P25	CMP1+	Input	Comparator input for detecting overcurrents
P26	ANI6	Input	Analog input for detecting the AC power supply voltage
P27	ANI7	Input	Analog input for switching the dimming mode
P30	TOH1	Output	Lighting LEDs
P31	TOX00	Output	Output for PFC
P33	TOX10	Output	Half-bridge output (low side)
P34	TOX11	Output	Half-bridge output (high side)
P37	P37	Input	Switch input for switching the infrared reception channel
P60	TxD6	Output	Output for DALI transmission
P61	RxD6	Input	Input for DALI reception
P70	ANI8	Input	Analog input for dimming

CHAPTER 2 CONTROLLING THE FEATURES

2.1 PFC and Half-Bridge Control

2.1.1 PFC control

Figure 2-1 (a) shows ideal waveforms of the AC power supply voltage and current. Here, the voltage and current have the same phase, are sine waves, and have a power factor of 100%. Figure 2-1 (b) shows the waveforms of the actual supply voltage and supply current of a power supply for which PFC control is not performed. Here, the conduction time is short and the peak current is large. Moreover, this causes the peak of the voltage waveform to flatten out. When the power factor decreases in this way, the following problems occur.

- High harmonic waves are generated that might prevent the compliance of products with regulations and their shipment.
- Excessively thick electric wires are required due to the large peak current.
- Breakers trip more easily.

Due to the above problems, PFC control is required for improving the power factor. For controlling PFC, the fluorescent lamp ballast board has relatively few components and generally uses the critical conduction mode (CRM) because there is little switching noise. Figure 2-1 (c) shows the waveforms of the AC power supply voltage and current when PFC control is used. The supply current is alternated and the average value of the distributed current values is controlled to have the same phase as the supply voltage and to be a sine wave. PFC can be controlled in the critical conduction mode by using the 78K0/Ix2 microcontroller.

Figure 2-1. Waveforms of the Supply Voltage and Current and PFC Control
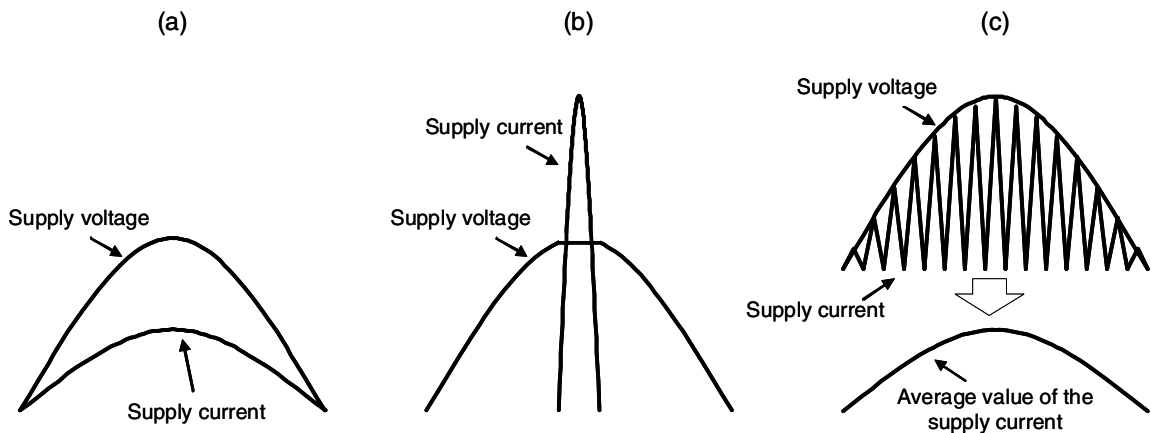
2.1.2 Overview of PFC control

Figure 2-2 shows a schematic example of a boost PFC circuit that uses the 78K0/Ix2 microcontroller. Pins for PFC output (TOX00 pin), zero-current detection input (CMP2+ pin), and DC output voltage monitoring input (ANI0 pin) are required for PFC control. A pin for AC power supply voltage monitoring input (the ANI6 pin), which is indicated by the broken line, is required only if using the 78K0/Ix2 in an environment where the AC power supply voltage differs over time.

Figure 2-3 shows the waveform generated when PFC control is performed using this configuration. If PFC output (TOX00 output) is enabled, I_{ON} is equal to (V_{IN}/L) multiplied by t_{ON}. Therefore, by fixing the t_{ON} output time, I_{ON} becomes proportional to V_{IN}, and the waveform of the I_{ON} peak current I_{PEAK} will have the same phase as V_{IN} and be a sine wave. In addition, because the current waveform is triangular, the average current $I_{AVERAGE}$ is equal to $I_{PEAK}/2$, which is also proportional to V_{IN}. Therefore, the waveforms of the average current and supply voltage will have the same phase and be sine waves and a waveform whose power factor is close to 100% can be generated.

Figure 2-2. Configuration Example of a Boost PFC Circuit
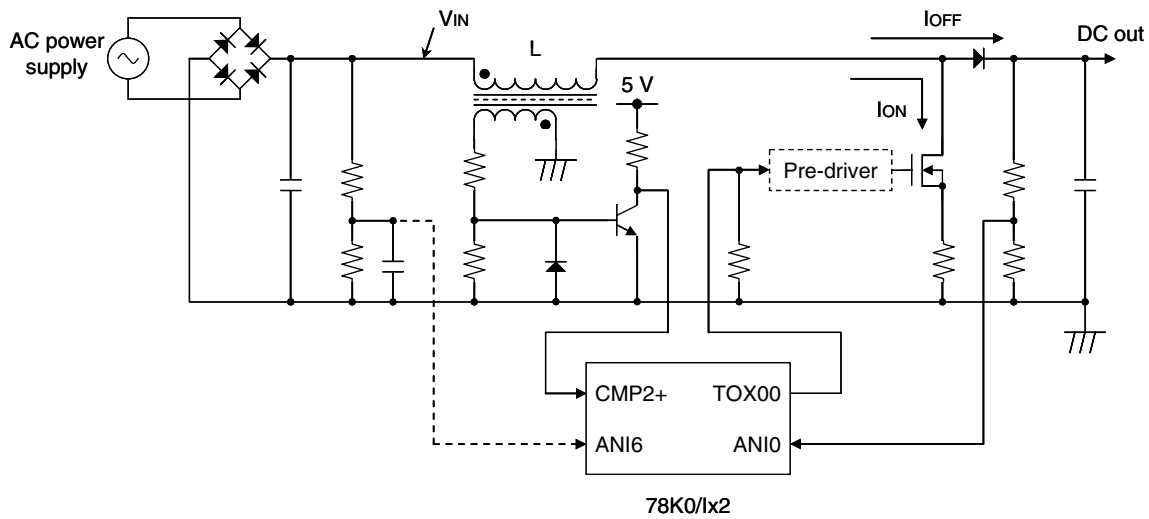
Figure 2-3. PFC Control Waveforms Generated by Using the 78K0/Ix2

Application Note U19665EJ2V0AN
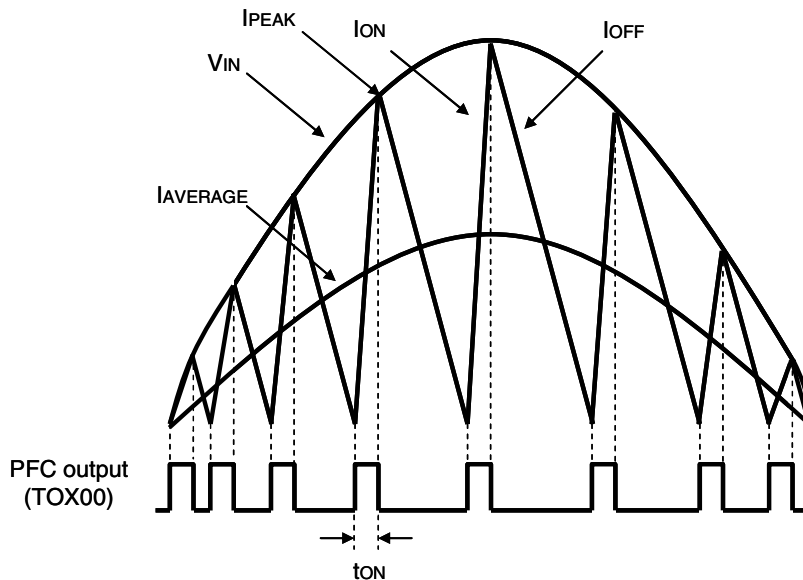
The peripheral hardware units of the 78K0/Ix2 microcontroller used for PFC control and their features are described below.

- 16-bit timer X0: PFC output
- Comparators: Zero-current detection
- A/D converter: DC output voltage monitoring and AC power supply voltage monitoring[Note]

Note   This is used if the 78K0/Ix2 is used in an environment where the AC power supply voltage differs over time.

The features of PFC control performed by using these peripheral hardware units are as follows:

- By using 16-bit timer X0 with the internal comparators, PFC output can be automatically enabled when a zero current is detected (without software processing).
- 40 MHz can be selected for the count clock of 16-bit timer X0 and the time during which PFC output is enabled can be controlled in 25 ns units.
- The time during which PFC output is enabled can be changed without stopping 16-bit timer X0.
- The DC output voltage and AC power supply voltage can be monitored by using an A/D converter that has a 10-bit resolution.

(1) Initialization before starting PFC control
    The peripheral hardware units of the 78K0/Ix2 microcontroller must be initialized before starting PFC control. An example of the setup for initializing 16-bit timer X0 and the internal comparators, which are the main peripheral hardware units to control PFC, is provided below.

```
/* 16-bit timer X0 setup */
TX0CTL0 = 0b00000000;  /* Sets the count clock to 40 MHz[Note]. */
TX0CTL1 = 0b00000000;  /* Specifies single output.  (Only the TOX00 pin performs output.) */
TX0CTL3 = 0b01100010;  /* Completely rewrites TX0CRn upon a restart by comparator 2 output
                          and restarts the timer when comparator 2 output is detected. */
TX0IOC0 = 0b00000100;  /* Sets the default status of TOX00 output to low level and enables
                          TOX00 output. */
TX0CR1  = 10000 - 1;   /* Sets the PFC output restart cycle for when a zero current is not
                          detected to 250 us. */

/* Comparator setup */
C2RVM  = 0b00011111;   /* Sets internal reference voltage DA2 to 1.6 V. */
C2CTL  = 0b00010000;   /* Specifies internal reference voltage DA2 as the reference voltage
                          and does not use the noise filter. */
```

Note   This applies if PLL clock mode is used and 40 MHz is specified for the clock supplied to 16-bit timer X0.

However, during the actual initial setup, the clock, ports, and interrupts must be set up. For details, see the 78K0/Ix2 User's Manual.

(2) Starting PFC control

Figure 2-4 shows the waveform generated when PFC control starts.

Figure 2-4. Waveform Generated When PFC Control Starts
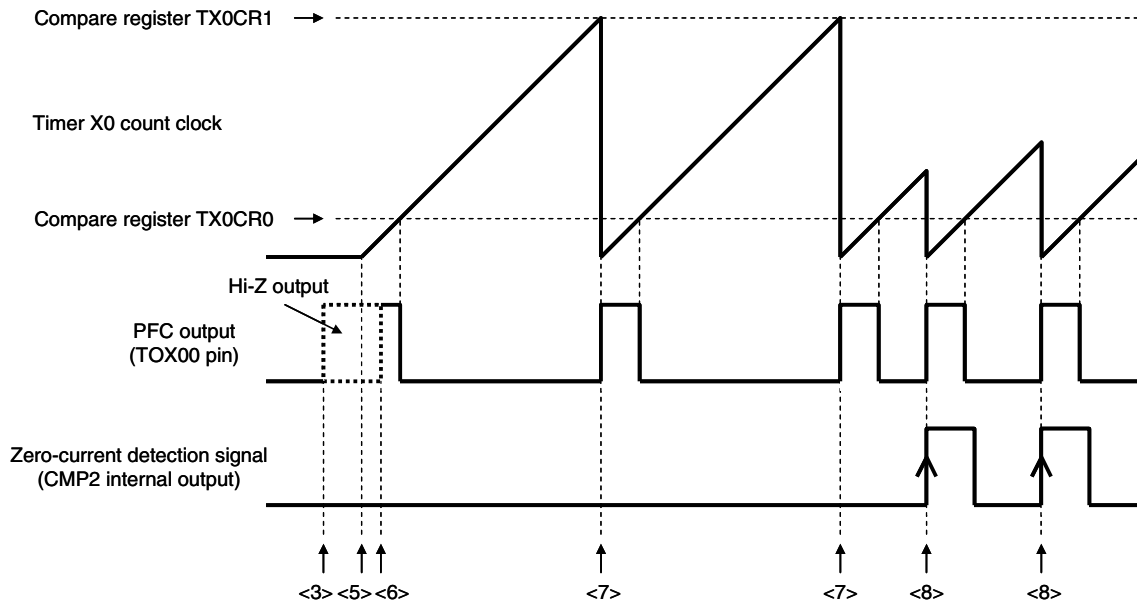
The operations are summarized below.

<1> The internal comparators start.

<2> The time PFC output is enabled is specified.

<3> The PFC output pin is set to input. This sets PFC output to high impedance and the MOSFET is disabled by an external pull-down resistor.

<4> The default status of PFC output is set to high level.

<5> 16-bit timer X0 starts.

<6> The PFC output pin is set to output. This cancels high-impedance output and PFC output starts.

<7> While a zero current cannot be detected, PFC output restarts in the cycle specified by using compare register TX0CR1 and the MOSFET is repeatedly enabled for a fixed period.

<8> When a zero current is detected, PFC output starts and the MOSFET is enabled for a fixed period.

Remark Controlling high-impedance output as in operations <3> and <6> is not required, but recommended to be set up for safety if interrupt servicing that takes a relatively long time might occur between operations <4> and <5>.

After PFC output starts in operation <6>, PFC output restarts before a zero current is detected and PFC output is enabled immediately when a zero current is detected by hardware, without performing software processing. Therefore, there is no delay due to CPU processing or CPU load for these operations.

Sample code for operations <1> to <6> is shown below.

```
/* Comparator setup */
CVRE   = 1;          /* <1> Enables the generation of the internal reference voltage. */
CMP2EN = 1;          /* <1> Enables comparator 2. */
C2OE   = 1;          /* <1> Enables internal output for comparator 2. */

/* 16-bit timer X0 setup */
TX0CR0  = 80 – 1;    /* <2> Sets the time PFC output is enabled when PFC control starts to 2 us. */
PM3.1   = 1;         /* <3> Sets the PFC output port to input.*/
TX0TOL0 = 1;         /* <4> Sets the default status of TOX00 output to high level.*/
TX0TMC = 1;          /* <5> Enables the timer to count. */
PM3.1   = 0;         /* <6> Sets the PFC output port to output. */
```

(3) PFC control if the load changes

Figure 2-5 shows the PFC control waveform generated when the load changes, such as during the time from the fluorescent lamp being preheated until it lights up or when the dimming frequency is changed after the voltage is boosted. When the load changes due to dimming and by how much the load changes can be estimated, because the 78K0/Ix2 microcontroller is used for dimming. Therefore, even if the load changes significantly due to dimming, PFC output according to the dimming can be performed easily and fluctuation in the DC output voltage and drastic decreases in the power factor can be prevented.

Figure 2-5. PFC Control Waveform Generated When the Load Changes
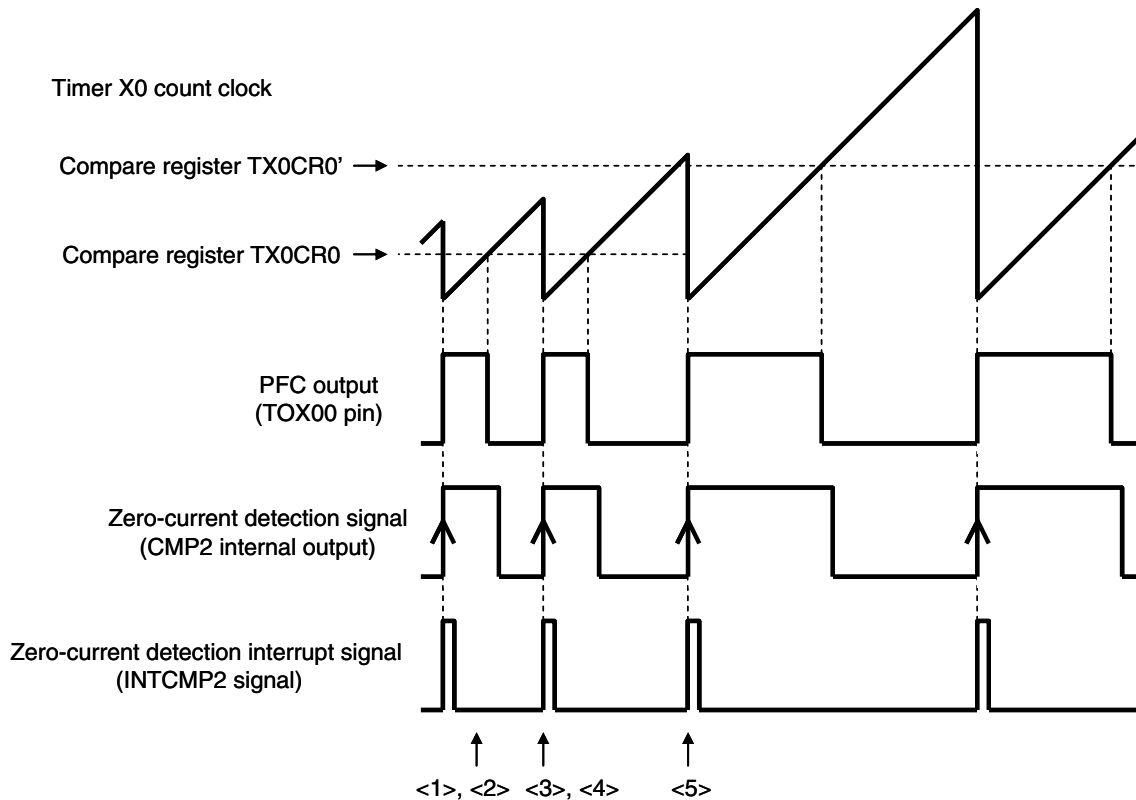
The operations are summarized below.

<1> The period of time PFC is enabled (TX0CR0 in Figure 2-5) is changed to a value according to the load (TX0CR0' in Figure 2-5).

<2> The zero-current detection interrupt (INTCMP2) is unmasked[Note].

<3> The pulse cycle (TX0CR1) value is rewritten or the same value is written immediately after a zero-current detection interrupt occurs.

<4> The zero-current detection interrupt (INTCMP2) is masked[Note].

<5> The period of time PFC output is enabled is updated when the next zero-current detection interrupt occurs.

Note Specifying the masking of zero-current detection interrupt is not required. Masking of zero-current detection interrupt must be specified if performing operation <3> during zero-current detection interrupt servicing.

Sample code for operations <1> to <4> is shown below.

<The following processing is executed around when the load changes.>

```
TX0CR0 += 100;          /* <1> Increases the period of time PFC output is enabled by 2.5 us. */
CMPIF2 = 0;             /* <2> Clears the comparator 2 interrupt request flag. */
CMPMK2 = 0;             /* <2> Unmasks comparator 2 interrupt. */
```

<The following processing is executed during the interrupt servicing immediately after an INTCMP2 interrupt occurs.>

```
TX0CR1 = 10000 - 1;   /* <3> Writes the same value to the PFC output restart cycle (250 us). */
CMPMK2 = 1;            /* <4> Masks comparator interrupt. */
```

(4) DC output voltage feedback

To make sure that the DC output voltage is constant, it must be monitored using the A/D converter, and the period of time PFC output is enabled must be controlled. The DC output voltage can be fed back by calculating the average DC output voltage by using the A/D converter and changing the period of time PFC output is enabled, such as at every half cycle of the AC power supply (10 ms at 50 Hz), because changes in the DC output voltage are moderate except when the load is intentionally changed. In addition, the period of time TOX00 output is enabled can be controlled in 25 ns units and the DC output voltage can be finely controlled, because 40 MHz can be selected for the count clock of 16-bit timer X0. Figure 2-6 shows an example in which feeding back the DC output voltage is controlled.

Figure 2-6. Example of Controlling the Feeding Back of the DC Output Voltage
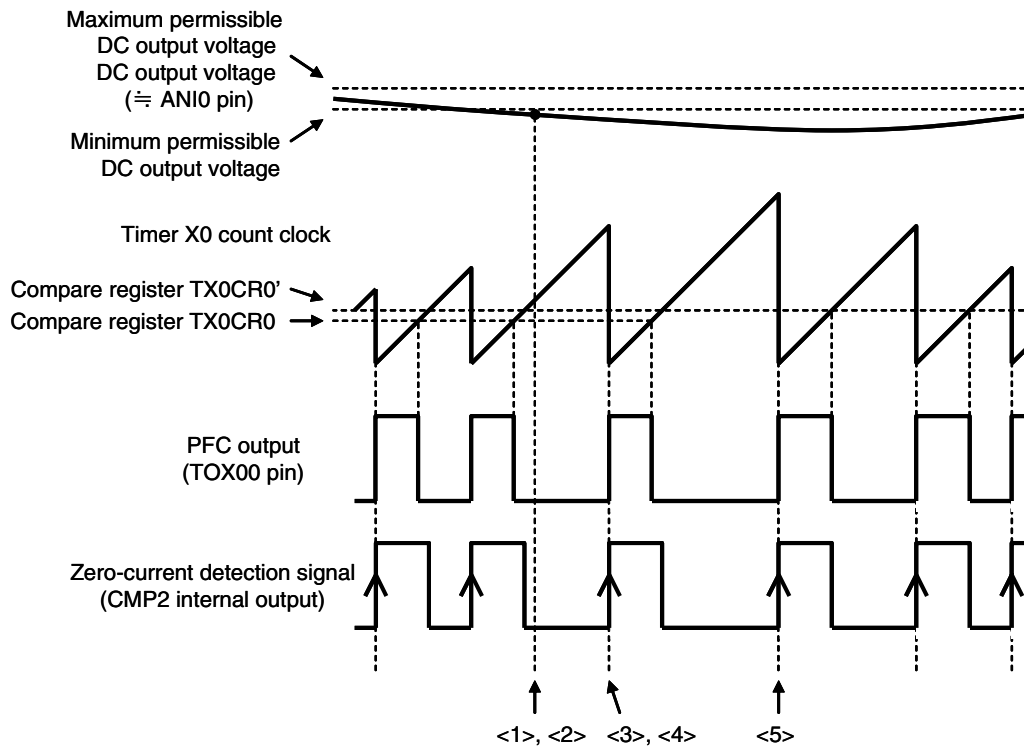
The operations are summarized below.

<1> It is detected that the average ANI0 input is the minimum permissible DC output voltage or less and that the voltage is falling, and the value of the compare register TX0CR0 is incremented by 1 (which adds 25 ns) by software.

<2> The zero-current detection interrupt (INTCMP2) is unmasked[Note].

<3> The pulse cycle (TX0CR1) value is rewritten or the same value is written immediately after a zero-current detection interrupt occurs.

<4> The zero-current detection interrupt (INTCMP2) is masked[Note].

<5> The period of time PFC output is enabled is updated when the next zero-current detection interrupt occurs.

Note Specifying the masking of zero-current detection interrupt is not required. Masking of zero-current detection interrupt must be specified if performing operation <3> during zero-current detection interrupt servicing.

Sample code for operations <1> to <4> is shown below.

<The following processing is executed around when the load changes.>

```
TX0CR0 += 1;        /* <1> Increases the period of time PFC output is enabled by 25 ns. */
CMPIF2 = 0;         /* <2> Clears the comparator 2 interrupt request flag. */
CMPMK2 = 0;         /* <2> Unmasks comparator 2 interrupt. */
```

<The following processing is executed during the interrupt servicing immediately after an INTCMP2 interrupt occurs.>

```
TX0CR1 = 10000 - 1;    /* <3> Writes the same value to the PFC output restart cycle (250 us). */
CMPMK2 = 1;            /* <4> Masks comparator interrupt. */
```

(5) Detecting the AC power supply voltage

To support different AC input voltages (AC 100 V to 240 V) by using the same control program, the parameters for PFC output must be changed according to the AC power supply voltage level. This can be achieved by detecting the rectified AC power supply voltage level by using the A/D converter and specifying these parameters when the power is turned on or at every fixed period after the power is turned on. However, supporting different AC input voltages and A/D converter input is not required for a ballast board that uses only one AC power supply.

A control example is provided below.

<1> After the power is turned on, the AC power supply voltage level is detected for a fixed period by using the A/D converter (ANI6 input) and the average value is calculated.

<2> The parameters for PFC output are specified according to the average value calculated in <1>.

<3> Hereafter, the AC power supply voltage level is detected at fixed periods by using the A/D converter (ANI6 input) and, if this voltage changes significantly, the parameters for PFC output are changed accordingly.

(6) Stopping PFC control

To stop PFC control, use the following procedure.

<1> Set the PFC output pin to input. This sets PFC output to high impedance and the MOSFET is disabled by an external pull-down resistor.

<2> Stop 16-bit timer X0.

<3> Set the default status of PFC output to low level.

<4> Set the PFC output pin to output. This cancels high-impedance output and a low-level signal is output from the PFC output pin.

<5> Stop the internal comparators.

Controlling high-impedance output as in steps <1> and <4> is not required, but recommended to be set up for safety if interrupt servicing that takes a relatively long time might occur between steps <2> and <3>. The comparators do not have to be stopped as in step <5>, either, but the power consumption of the microcontroller can be reduced by doing so.

Sample code for steps <1> to <5> is shown below.

```
/* 16-bit timer X0 setup */
PM3.1   = 1;       /* <1> Sets the PFC output port to input.*/
TX0TMC  = 0;       /* <2> Disables the timer from counting. */
TX0TOL0 = 0;       /* <3> Sets the default status of TOX00 output to low level.*/
PM3.1   = 0;       /* <4> Sets the PFC output port to output. */

/* Comparator setup */
CMP2EN = 0;        /* <5> Disables comparator 2. */
CVRE   = 0;        /* <5> Disables the generation of the internal reference voltage. */
C2OE   = 0;        /* <5> Disables internal output for comparator 2.*/
```

2.1.3 Overview of half-bridge control

Figure 2-7 shows an example of the configuration of a half-bridge circuit that uses the 78K0/Ix2 microcontroller. Pins for low-side output (TOX10 pin) and high-side output (TOX11 pin) are required for half-bridge control.

Figure 2-8 shows an example of the waveform generated when half-bridge control is performed by using this configuration. As shown below, inverter output can be performed from the MOSFET by alternately enabling low-side output and high-side output with a fixed dead time (without enabling both at the same time).

Figure 2-7. Half-Bridge Circuit Configuration Example
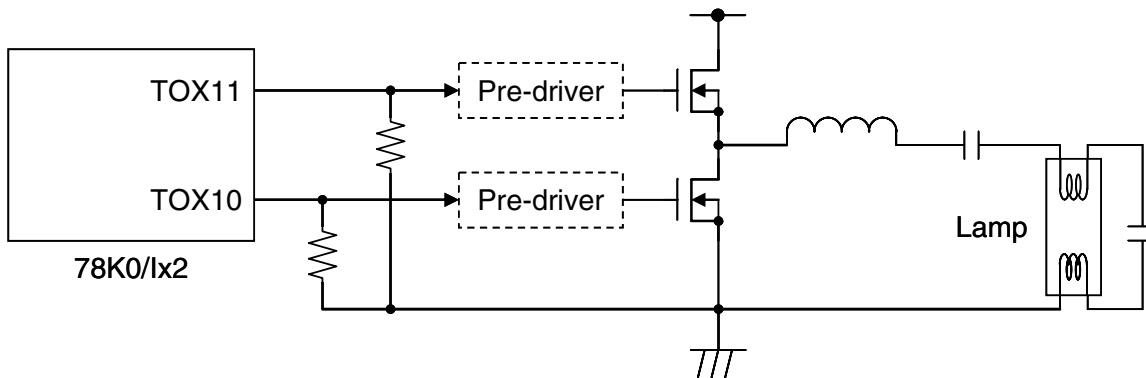
Figure 2-8. Half-Bridge Control Waveform Example
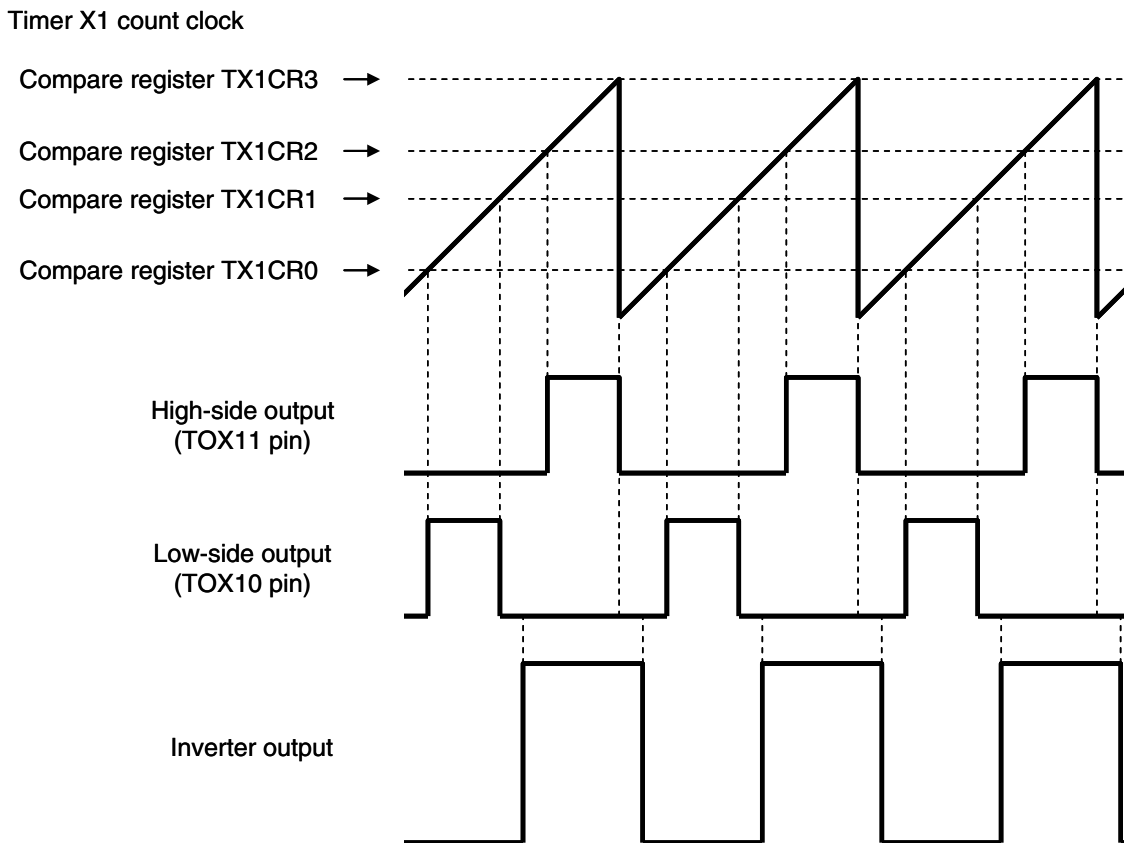
The peripheral hardware unit of the 78K0/Ix2 microcontroller used for half-bridge control and the features are described below.

- 16-bit timer X1: Low-side output and high-side output for half-bridge control

The features of half-bridge control performed by using this peripheral hardware unit are as follows:

- Synchronous 2-channel PWM output with dead time and flexible half-bridge control can be easily performed by using the dual output of 16-bit timer X1 (TOX10 and TOX11 output) and four compare registers (TX1CR0, TX1CR1, TX1CR2, and TX1CR3).
- 40 MHz can be selected for the count clock of 16-bit timer X1, the dead time can be controlled in 25 ns units, and the half-bridge output cycle can be controlled in 50 ns units.
- The inverter output frequency and dead time can be changed without stopping 16-bit timer X1.

(1) Initialization before starting half-bridge control
The peripheral hardware units of the 78K0/Ix2 microcontroller must be initialized before starting half-bridge control. An example of the setup for initializing 16-bit timer X1, which is typical for half-bridge control, is provided below.

```
/* 16-bit timer X1 setup */
TX1CTL0 = 0b00000000;  /* Sets the count clock to 40 MHz^Note. */
TX1CTL1 = 0b00001000;  /* Dual output (TOX10 and TOX11 pin output), TMX1 only start mode */
TX1IOC0 = 0b00001100;  /* Sets the default output statuses of TOX10 and TOX11 to low level
                          and enables TOX10 and TOX11 output.*/
```

Note This applies if PLL clock mode is used and 40 MHz is specified for the clock supplied to 16-bit timer X1.

However, during the actual initial setup, the clock, ports, and interrupts must be set up. For details, see the 78K0/Ix2 User's Manual.

(2) Starting half-bridge control

Figure 2-9 shows the waveform generated when half-bridge control starts.

Figure 2-9. Waveform Generated When Half-Bridge Control Starts
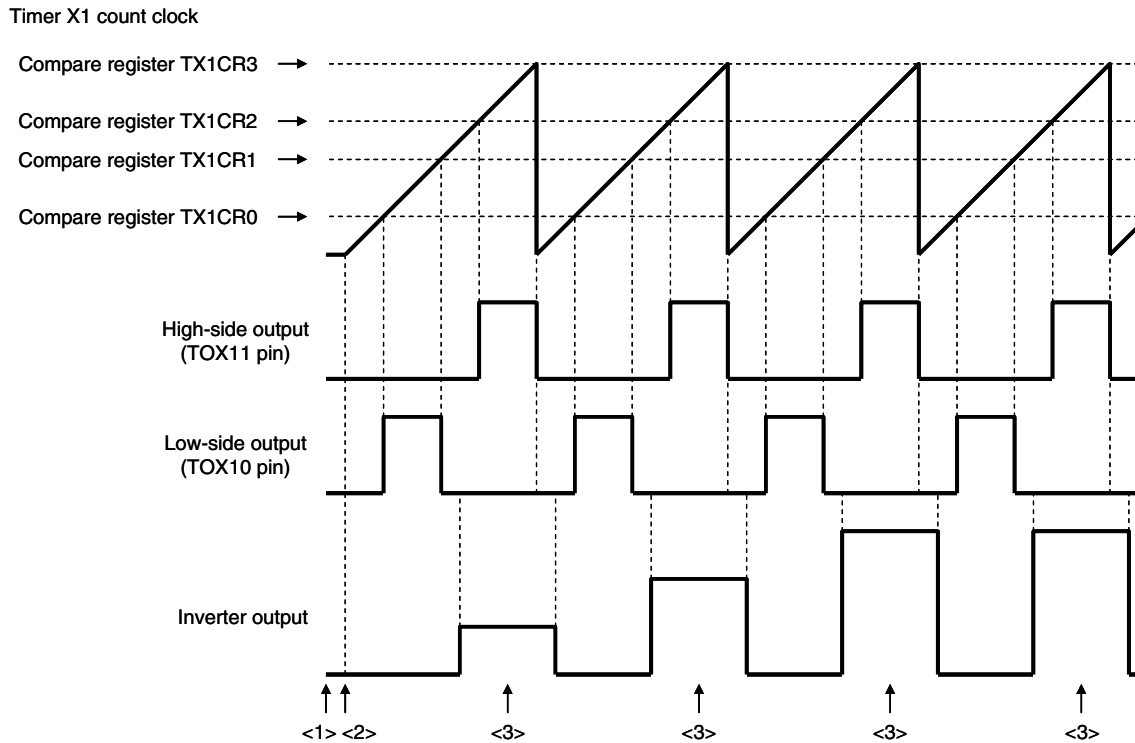
The operations are summarized below.

<1> The dead time and frequency of half-bridge control are specified.

<2> Half-bridge control starts.

<3> The inverter output voltage gradually increases and it becomes a fixed voltage when it reaches the DC output voltage generated by PFC control.

After half-bridge control is started in operations <1> and <2>, half-bridge control is executed by hardware. Therefore, there is no delay due to CPU processing or CPU load for these operations.

Sample code for operations <1> and <2> is shown below.

```
TX1CR0 = 40 – 1;            /* <1> Sets the dead time to 1 us.*/
TX1CR1 = 200 – 1;           /* <1> Sets the duty factor to 50%. */
TX1CR2 = 200 + 40 – 1;      /* <1> Sets the dead time to 1 us.*/
TX1CR3 = 400 – 1;           /* <1> Sets the frequency to 100 kHz. */
TX1TMC = 1;                 /* <2> Enables the timer to count. */
```

(3) Changing the half-bridge output cycle (to control dimming and sweep the frequency during preheating)

Figure 2-10 shows an example of the waveform generated when the half-bridge output cycle changes, such as during the time from the fluorescent lamp being preheated until it lights up or when it is dimmed.

Figure 2-10. Waveform When the Half-Bridge Output Cycle Changes
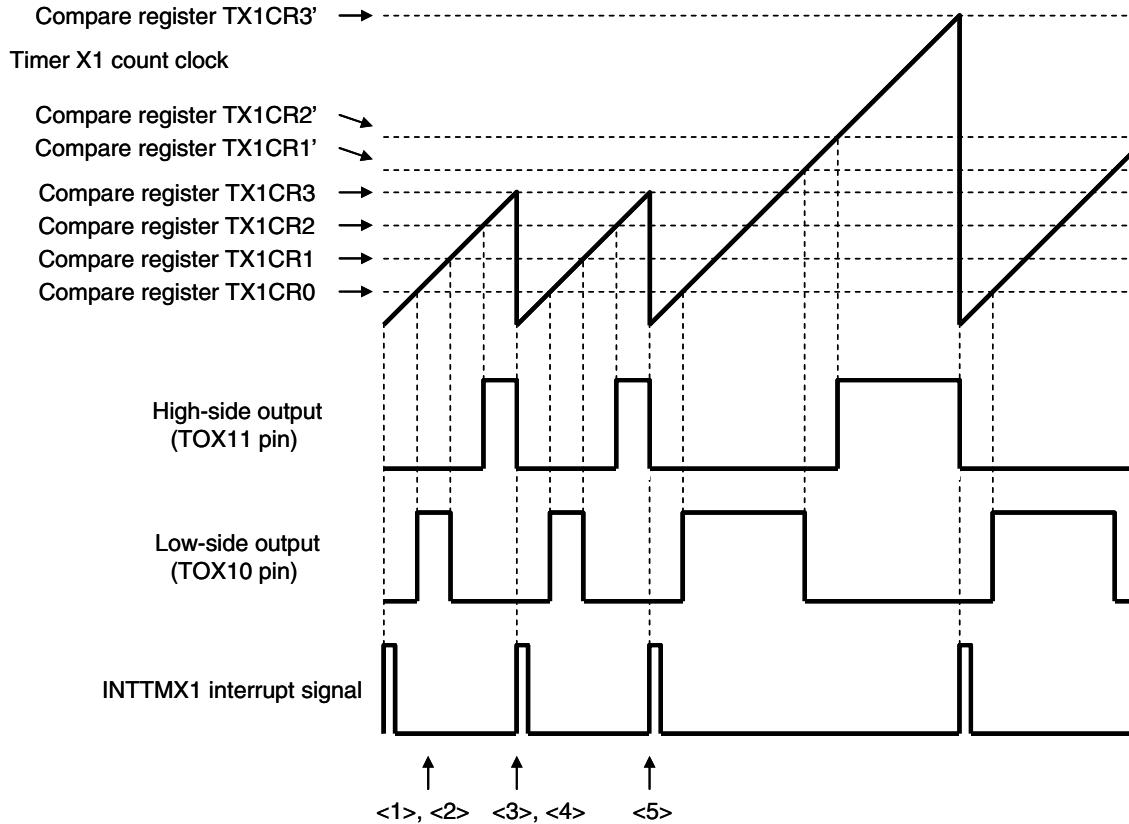
The operations are summarized below.

<1> The settings of the dead time and duty factor 50% are changed according to the new half-bridge output frequency.

<2> The INTTMX1 interrupt is unmasked[Note].

<3> The pulse cycle (TX1CR3) value is rewritten immediately after an INTTMX1 interrupt occurs.

<4> The INTTMX1 interrupt is masked[Note].

<5> When the next INTTMX1 interrupt occurs, the half-bridge output frequency is changed, but the dead time and duty factor 50% are maintained.

Note Specifying the masking of INTTMX1 interrupt is not required. Masking of INTTMX1 interrupt must be specified if performing operation <3> during INTTMX1 interrupt servicing.

Sample code for operations <1> to <4> is shown below.

<The following processing is executed around when the load changes.>

```
TX1CR1 = 400 - 1;          /* <1> Sets the duty factor of the new frequency to 50%. */
TX1CR2 = 400 + 40 - 1;     /* <1> Maintains the dead time of 1 us. */
TMIFX1 = 0;                /* <2> Clears the INTTMX1 interrupt request flag. */
TMMKX1 = 0;                /* <2> Unmasks INTTMX1 interrupt. */
```

Remark   The value of TX1CR0 must also be changed when changing the dead time.

<The following processing is executed during the interrupt servicing immediately after an INTTMX1 interrupt occurs.>

```
TX1CR3 = 800 - 1;          /* <3> Changes the half-bridge output frequency to 50 kHz. */
TMMKX1 = 1;                /* <4> Masks INTTMX1 interrupt. */
```

(4) Stopping half-bridge control
Specify the following setting to stop half-bridge control.

<1> Stop 16-bit timer X1.

Sample code for this specification is shown below.

```
TX1TMC = 0;                /* Disables the timer from counting. */
```

2.1.4 Software flowchart for PFC control and half-bridge control
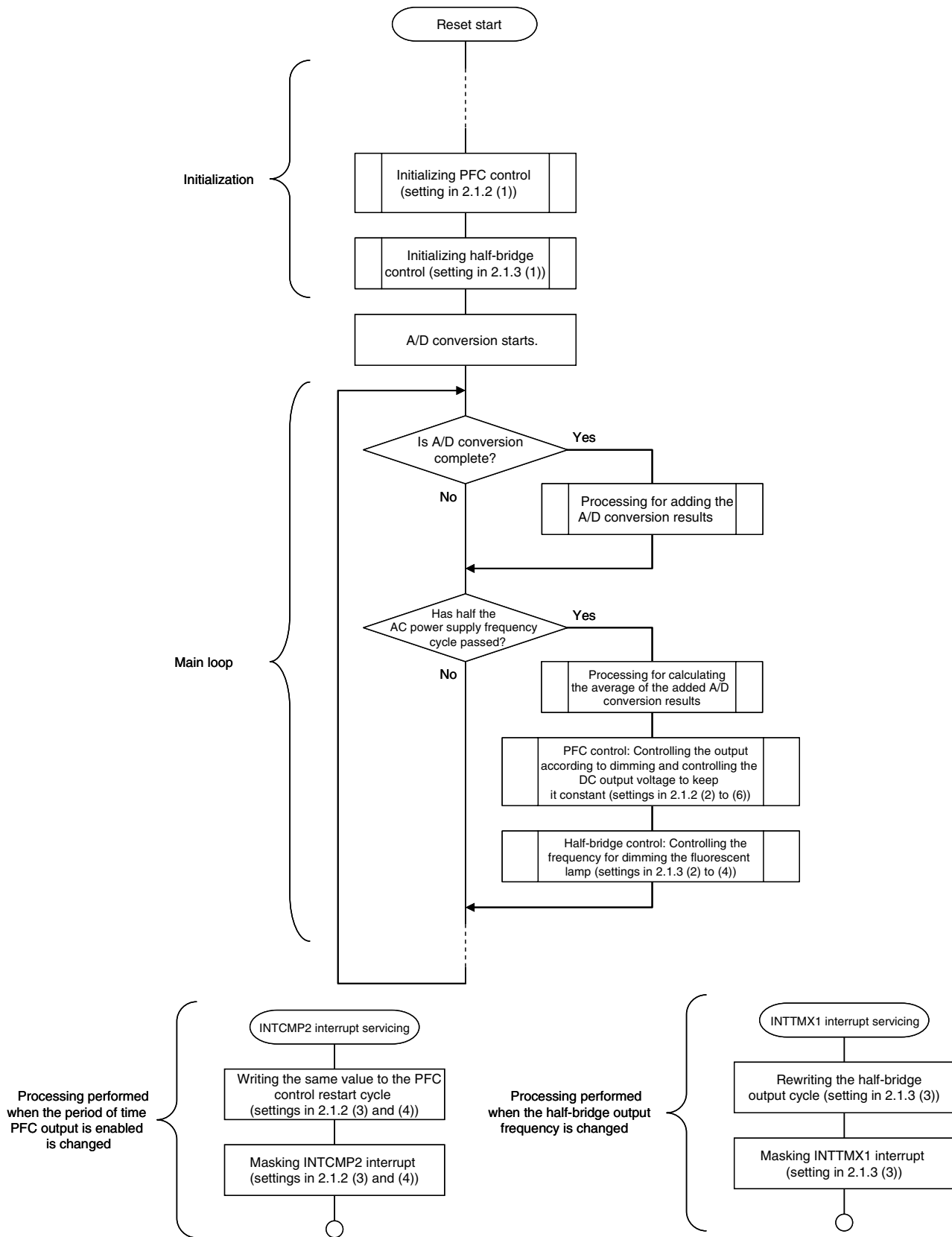
2.2 Protection

2.2.1 Overview of protection

The outputs of 16-bit timers X0 and X1 can be changed immediately by using them with an internal comparator or INTP0 input. This operation enables PFC output and half-bridge output to be stopped immediately when an overvoltage or overcurrent is detected or the lamp is installed or uninstalled. No delay due to software processing or CPU load occurs because this operation is performed by hardware.

Figure 2-11 shows an example of a circuit in which PFC output and half-bridge output are stopped immediately when the internal comparator detects an overcurrent flowing to the MOSFET for PFC control. Figure 2-12 shows an example of the waveform generated when an overcurrent is detected in this circuit.

Figure 2-11. Example of the Circuit When Timer Output Is Stopped Immediately When an Overcurrent Is Detected by the Internal Comparators
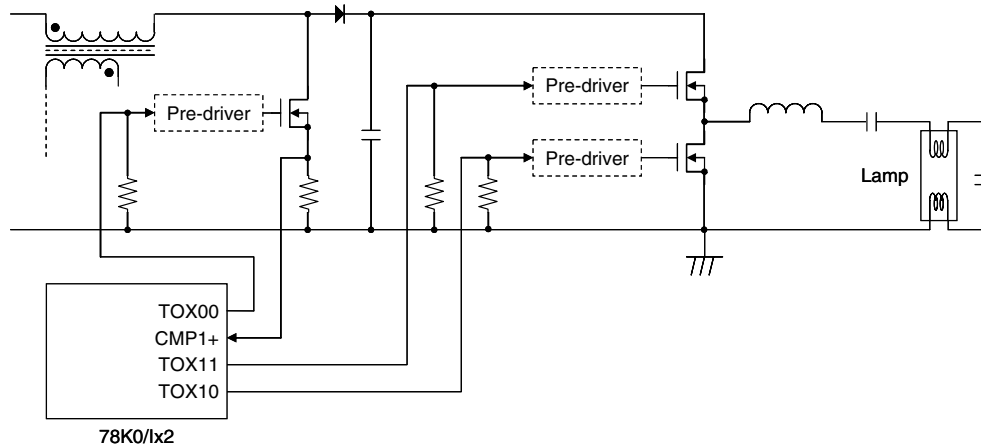
Figure 2-12. Example of the Waveform When Timer Output Is Switched to High Impedance When an Overcurrent Is Detected
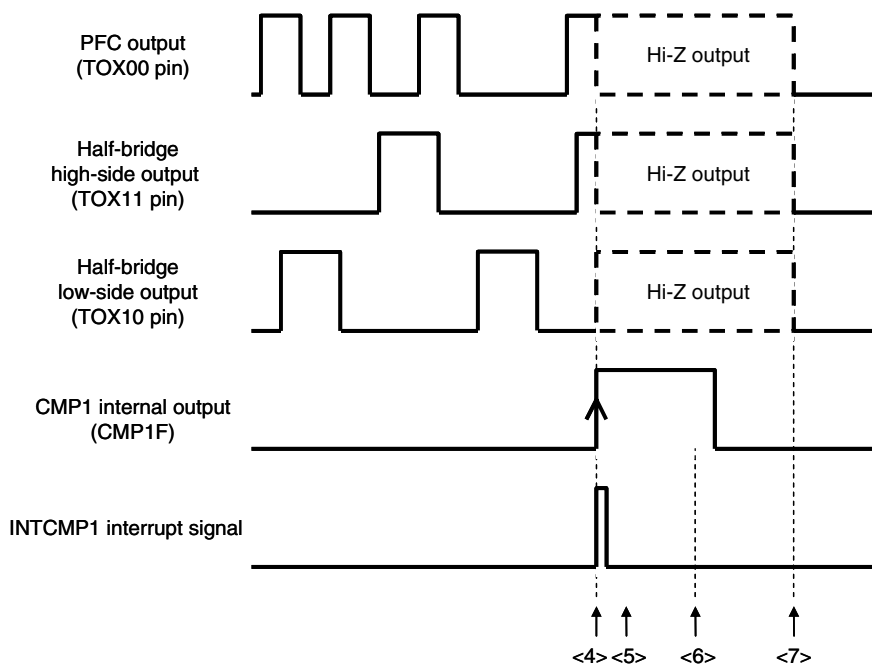
The operations are summarized below.

(1) Initialization

<1> The pins that perform PFC output (TOX00 pin) and half-bridge output (TOX10 and TOX11 pins) are specified as the pins controlling high-impedance output[Note 1] and internal comparator 1 is selected as the trigger.

<2> A setting is specified so that the high-impedance status cannot be canceled while the input signal of internal comparator 1 has an abnormal detection level[Note 2].

<3> Trigger signal input and high-impedance output control are enabled.

(2) Immediate high-impedance output when an abnormality is detected

<4> PFC output (TOX00 pin) and half-bridge output (TOX10 and TOX11 pins) change to high-impedance output when the CMP1+ pin input signal exceeds the reference voltage of the internal comparator.

<5> PFC output (TOX00 pin) and half-bridge output (TOX10 and TOX11 pins) are stopped, such as by INTCMP1 interrupt servicing, and these timer outputs are set to low level[Note 3].

(3) Canceling high-impedance output

<6> If HZA0DCC0 is set to 1 by mistake while the input signal of internal comparator 1 has an abnormal detection level, the setting is invalid and high-impedance output is not canceled.

<7> If HZA0DCC0 is set to 1 while the input signal of internal comparator 1 does not have an abnormal detection level, high-impedance output is canceled.

Notes 1. Whether to use high-impedance control can be specified for each pin.

2. A setting that enables cancellation of the high-impedance status can be specified regardless of the input signal.

3. When high-impedance output is canceled using this setting, a low-level signal is output from the pins. A setting that restarts control when high-impedance output is canceled, without stopping the PFC control timer, can also be used.

Sample code for operations <1> to <3>, <6>, and <7> is shown below.

<Initialization>

```
HIZTRS  = 0b10001101;  /* <1> Selects TOX00, TOX10, and TOX11 as the high-impedance output
                               pins and comparator 1 as the trigger. */
HZA0CTL0 = 0b01010000;  /* <2> Specifies that the HZA0DCC0 bit[Note] setting is invalid while the
                               signal to use has an abnormal detection level. */
HIZTREN0 = 1;           /* <3> Enables trigger signal input. */
HZA0DCE0 = 1;           /* <3> Enables high-impedance output control. */
```

Note Setting the HZA0DCC0 bit to 1 cancels the high-impedance status of the target pins (the TOX00, TOX10, and TOX11 pins in this example) and enables the output of the pins.

<Canceling high-impedance output>

```
HZA0DCC0 = 1;          /* <6> <7> Cancels the high-impedance output status. */
```

2.2.2 Software flowchart for protection
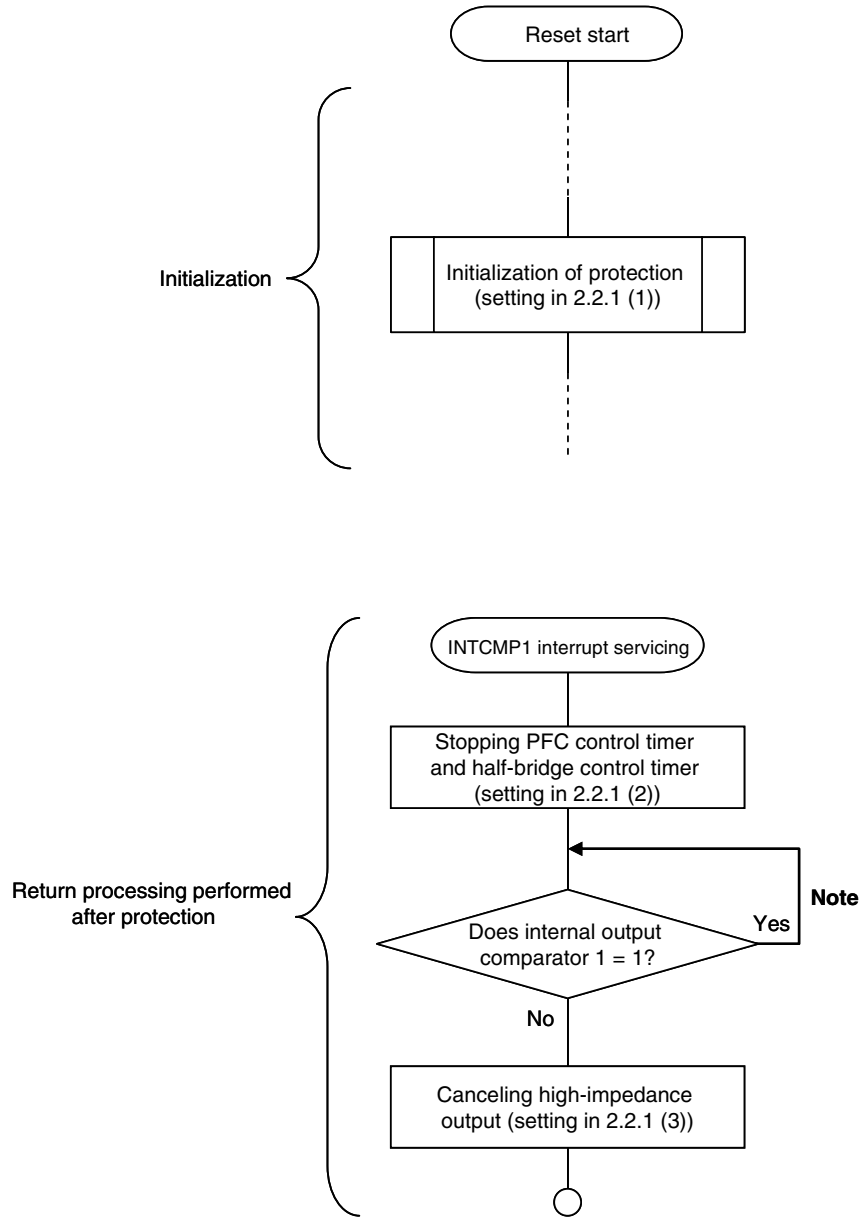
Note When performing these operations, processing that exits the loop if this loop is repeated for a specific period of time must be added, because this loop might be an infinite loop.

2.3 Communication

2.3.1 DALI communication

DALI (Digital Addressable Lighting Interface) is a communication protocol for controlling lighting, standardized in accordance with international open standards, and is mainly used to control the dimming of multiple fluorescent lamps and LEDs. DALI is used in a network consisting of up to 64 short addresses and 16 group addresses that performs half-duplex command communication between one master and one or more slaves. DALI commands are used to specify the dimming level in 8-bit accuracy, save any dimming level as a scene and switch between different scenes, and specify other settings. The communication speed is 1,200 Hz $\pm 10\%$.

The main specifications are described below.

(1) Data structure

<1> Bit definitions

DALI communication uses Manchester code. Therefore, bits are defined as 0 at falling edges and as 1 at rising edges and fixed to high level when no communication is performed.

Figure 2-13. Bit Definitions
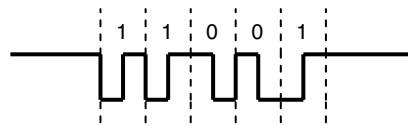
<2> Frames

- Forward frame

A forward frame is a frame transmitted from the master to a slave. Such a frame has 19 bits.

Figure 2-14. Structure of a Forward Frame
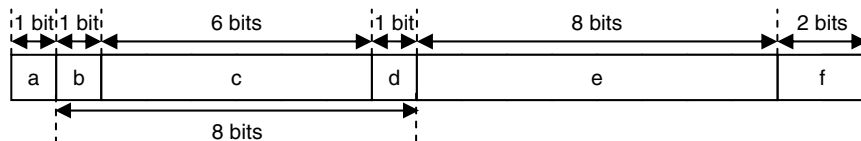
a: Start bit

This bit indicates the start of the frame. The waveform of this bit is always equal to 1.

b to d: Address byte

This byte specifies where to transmit the frame.

e: Data byte

This byte specifies a command.

f: Stop bits

These bits indicate the end of the frame. These bits are fixed to high level.

• Backward frame

A backward frame is a frame transmitted from a slave to the master. Such a frame has 11 bits.

Figure 2-15. Structure of a Backward Frame
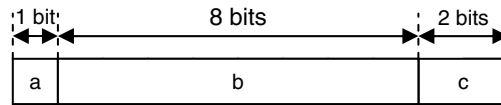
a: Start bit

This bit indicates the start of the frame. The waveform of this bit is always equal to 1.

b: Data byte

This byte replies to the master.

c: Stop bits

These bits indicate the end of the frame. These bits are fixed to high level.

(2) Specifying the transmission and reception timing

<1> Timing within a frame

1 bit width in DALI is 833.3 μs ±10% for both forward and backward frames.

Figure 2-16. Timing Within a Frame
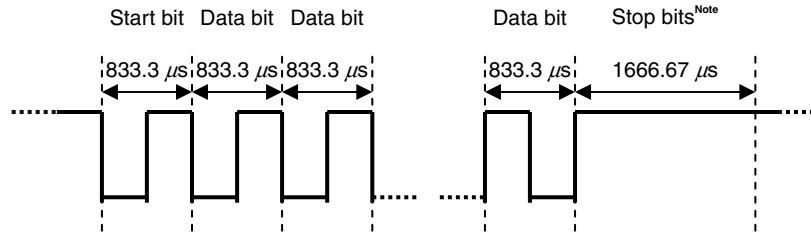
Note Because there are two stop bits, their timing is 1666.67 μs.

<2> Timing between frames

The following timing control is required in frame units in DALI.

- Forward frame width: 15.83 ms ±10%
- Backward frame width: 9.17 ms ±10%
- Communication interval between a forward and backward frame: 2.92 to 9.17 ms
- Interval between a forward frame and the next forward frame: At least 9.17 ms
- Interval between a backward frame and the next forward frame: At least 9.17 ms

Figure 2-17. Timing Between Frames

From the start of a forward frame to the start of a backward
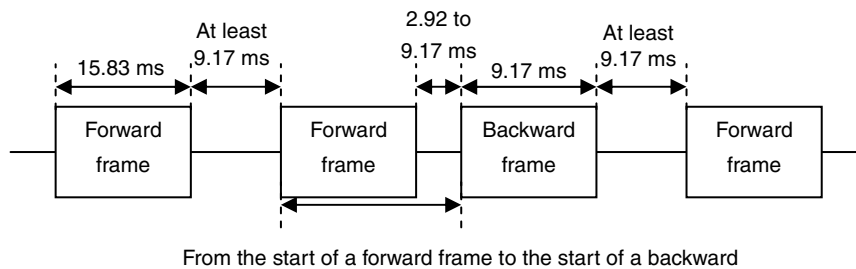
2.3.2 Overview of DALI communication

The 78K0/IA2 and 78K0/IB2 microcontrollers are provided with the serial interface UART6/DALI to transmit and receive data as a slave of DALI communication by using hardware. Therefore, no CPU load due to software processing occurs when data is transmitted or received via DALI.

Figure 2-18 shows a schematic example of a DALI communication circuit. Pins for DALI reception input (RxD6 pin) and DALI transmission output (TxD6 pin) are required for performing DALI communication.

Figure 2-18. Schematic Example of a DALI Communication Circuit
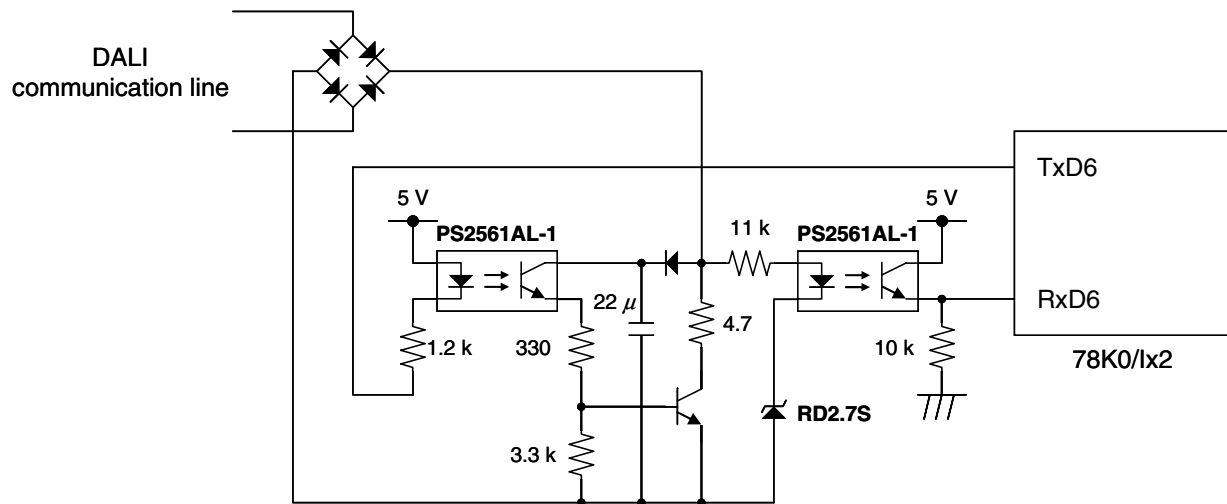
Remarks 1. PS2561AL-1 is a photocoupler made by NEC Electronics.
    2. RD2.7S is a Zener diode made by NEC Electronics.

(1) Initialization

An example of initializing the serial interface UART6/DALI when performing DALI communication is shown below.

```
UADLSEL = 1;          /* Specifies DALI mode. */
ASICL6.1 = 0;         /* Specifies that the MSB is first. */
CKSR6 = 5;            /* Sets the count clock to 625 kHz^Note 1. */
BRGC6 = 130;          /* Sets the baud rate to 1,200 bps^Note 1. */
ASIM6.0 = 0;          /* Specifies INTSRE6^Note 2 as the interrupt generated when a reception
                         error occurs.*/
```

Notes 1. This applies if PLL clock mode is used and 20 MHz is specified for the clock supplied to the peripheral hardware units.
    2. The interrupt generated when data is received successfully (INTSR6) can also be specified.

(2) Timing chart when receiving data

Figure 2-19 shows an example of the timing chart when data is received from the master during DALI communication.

Figure 2-19. Timing Chart When Receiving Data During DALI Communication
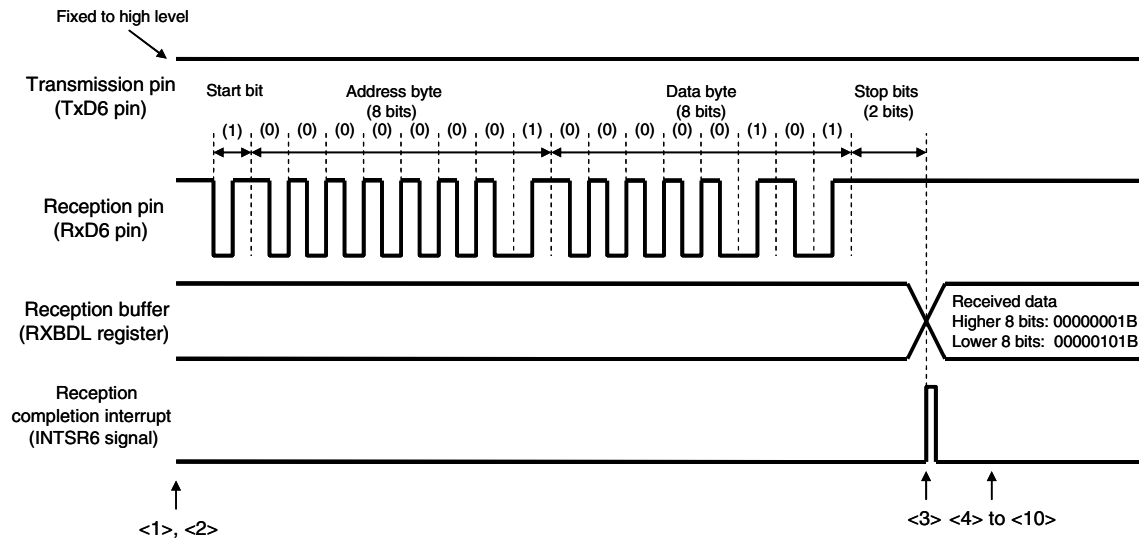
The operations are summarized below.

<Enabling reception>
<1> The internal operation clock of the serial interface UART6/DALI is enabled.
<2> Reception is enabled and a status in which reception can be performed is specified.
<3> If data is received successfully from the master during DALI communication, the interrupt INTSR6 is generated and received data is stored into the RXBDL register. If a reception error occurs, an INTSRE6 interrupt is generated and the reception error status is stored into the ASIS6 register. (Figure 2-19 shows a timing chart for when data was received successfully.)

<Processing after an INTSR6 interrupt is generated when data was received successfully>
<4> The received data (16 bits) is saved.
<5> Reception is disabled.
<6> The internal operation clock of the serial interface UART6/DALI is disabled.

<Processing after an INTSRE6 interrupt is generated when a reception error occurred>
<7> The reception error status is read.
<8> The received data (16 bits) is discarded.
<9> Reception is disabled.
<10> The internal operation clock of the serial interface UART6/DALI is disabled.

Sample code for operations <1>, <2>, and <4> to <10> is shown below.

<Enabling reception>

```
POWER6 = 1;                /* <1> Enables the internal operation clock. */
RXE6 = 1;                  /* <2> Enables reception. */
```

<Processing after an INTSR6 interrupt is generated when data was received successfully>

```
ushRxCode = RXBDL;         /* <4> Saves the received data^Note 1. */
RXE6 = 0;                  /* <5> Disables reception. */
POWER6 = 0;                /* <6> Disables the internal operation clock. */
```

<Processing after an INTSRE6 interrupt is generated when a reception error occurred>

```
ucRxeCode = ASIS6;         /* <7> Reads the reception error status^Note 2. */
ushTemp = RXBDL;           /* <8> Discards the received data^Note 1. */
RXE6 = 0;                  /* <9> Disables reception. */
POWER6 = 0;                /* <10> Disables the internal operation clock. */
```

Notes 1. ushRxCode and ushTemp are 16-bit variables.

2. ucRxeCode is an 8-bit variable.

(3) Timing chart when transmitting data

Figure 2-20 shows an example of the timing chart when data is transmitted to the master during DALI communication.

Figure 2-20. Timing Chart When Transmitting Data During DALI Communication
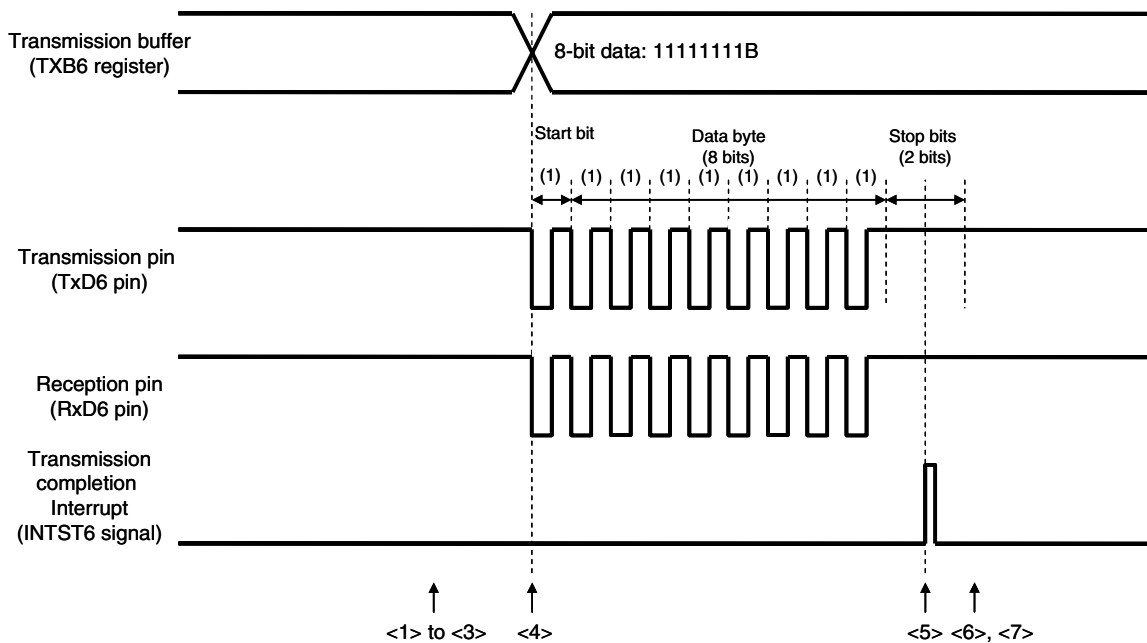
The operations are summarized below.

<Starting transmission>

<1> The internal operation clock of the serial interface UART6/DALI is enabled.

<2> Transmission is enabled and a status in which reception can be performed is specified.

<3> An NOP instruction (which consumes two clocks) is executed so that the system waits at least one base clock cycle.

<4> The data to transmit is stored into the TXB6 register and transmission starts[Note].

<5> An INTST6 interrupt is generated when transmission ends.

<Processing after an INTST6 interrupt is generated when transmission ends>

<6> Transmission is disabled.

<7> The internal operation clock of the serial interface UART6/DALI is disabled.

Note As shown in Figure 2-20, the transmitted data is directly input to the reception pin during DALI communication. Therefore, preventing the generation of reception error interrupts is recommended by disabling reception (RXE6 = 0) before starting transmission.

Sample code for operations <1> to <4>, <6>, and <7> is shown below.

<Starting transmission>

```
POWER6 = 1;              /* <1> Enables the internal operation clock. */
TXE6 = 1;                /* <2> Enables transmission. */
NOP();                   /* <3> Waits at least 1 base clock. */
TXB6 = 0b11111111;       /* <4> Starts transmitting the data 11111111. */
```

<Processing after an INTST6 interrupt is generated when transmission ends>

```
TXE6 = 0;                /* <6> Disables transmission. */
POWER6 = 0;              /* <7> Disables the internal operation clock. */
```

2.3.3 Software flowcharts for DALI communication

```
                              ┌─────────────┐
                              │ Reset start │
                              └─────────────┘
                                     ┆
                              ┌──┬──────────────┬──┐
                              │  │ Initializing  │  │
              Initialization  │  │ DALI          │  │
                              │  │ communication │  │
                              │  │ (setting in   │  │
                              │  │ 2.3.2 (1))    │  │
                              └──┴──────────────┴──┘

                              ┌──┬──────────────┬──┐
                              │  │ Enabling DALI │  │
                              │  │ reception     │  │
                              │  │ (setting in   │  │
                              │  │ 2.3.2 (2))    │  │
                              └──┴──────────────┴──┘

                                  ◇ Has a DALI command          Yes
                                    been received? ◇───────────────┐
                                         No                        │
                              ┌──┬──────────────────┬──┐
                              │  │ DALI command      │  │
                              │  │ identification    │  │
                              │  │ processing        │  │
                              └──┴──────────────────┴──┘
                                  ◇ Is a reply required? ◇    Yes
                                         No
                              ┌──────────────────────┐
                              │ Enabling DALI         │
                              │ transmission          │
                              │ (setting in 2.3.2 (3))│
                              └──────────────────────┘
                              ┌──────────────────────┐
                              │ Waiting at least 1    │
                              │ base clock            │
                              │ (setting in 2.3.2 (3))│
                              └──────────────────────┘
                              ┌──────────────────────┐
                              │ Transferring the      │
                              │ transmitted data to   │
                              │ the TXB6 register     │
                              │ (setting in 2.3.2 (3))│
                              └──────────────────────┘

              Main loop
```

Processing performed when data is successfully received
```
        ( INTSR6 interrupt servicing )
                    |
        ┌───────────────────────────┐
        │     Saving received data   │
        │     (setting in 2.3.2 (2)) │
        └───────────────────────────┘
                    |
        ┌───────────────────────────┐
        │     Disabling reception    │
        │     (setting in 2.3.2 (2)) │
        └───────────────────────────┘
                    |
                   ( )
```

Processing performed when a reception error occurred
```
        ( INTSRE6 interrupt servicing )
                    |
        ┌─────────────────────────────┐
        │  Saving reception error status│
        │     (setting in 2.3.2 (2))   │
        └─────────────────────────────┘
                    |
        ┌─────────────────────────────┐
        │   Discarding received data   │
        │     (setting in 2.3.2 (2))   │
        └─────────────────────────────┘
                    |
        ┌─────────────────────────────┐
        │     Disabling reception      │
        │     (setting in 2.3.2 (2))   │
        └─────────────────────────────┘
                    |
                   ( )
```

Processing performed when transmission ends
```
        ( INTST6 interrupt servicing )
                    |
        ┌───────────────────────────┐
        │    Disabling transmission  │
        │    (setting in 2.3.2 (3))  │
        └───────────────────────────┘
                    |
                   ( )
```

Table B-1. Reference Parts Table (1/3)

Part	Part Number	Product Name and Specifications	Function	Manufacturer	Manufacturer Product Name
IC	771	UPD78F0756MC-CAB-AX	Microcontroller	NEC Electronics Corporation	UPD78F0756MC-CAB-AX
IC	773	UPC78M05AHF-AZ	3-pin regulator	NEC Electronics Corporation	UPC78M05AHF-AZ
PC	301	PS2561AL-1	Photocoupler	NEC Electronics Corporation	PS2561AL-1
PC	302	PS2561AL-1	Photocoupler	NEC Electronics Corporation	PS2561AL-1
ZD	301	RD2.7S-T1-A	Zener diode	NEC Electronics Corporation	RD2.7S-T1-A
LF	1	SU10VD-20010	AC 250 V 2 A line filter	NEC TOKIN Corporation	SU10VD-20010
LF	2	SS24H-R20045-CH	AC 250 V 2 A line filter	NEC TOKIN Corporation	SS24H-R20045-CH
BZ	0	PS1440P02BT	Buzzer	TDK Corporation	PS1440P02BT
C	101	2KV 1000p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33D102KB3B
C	102	2KV 1000p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33D102KB3B
C	103	50V 470p	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM2162C1H471JA01D
C	104	25V 0.47u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM219B31E474KA88D
C	105	50V 470p	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM2162C1H471JA01D
C	111	400V 0.18u	Film capacitor	Panasonic Corporation	ECWF4184JB
C	112	4700p 2KV	Film capacitor	Nippon Chemi-Con Corporation	FHACD202V472JKLDZ0
C	211	400V 0.18u	Film capacitor	Panasonic Corporation	ECWF4184JB
C	212	4700p 2kV	Film capacitor	Nippon Chemi-Con Corporation	FHACD202V472JKLDZ0
C	220	50V 0.1u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM21BR11H104KA01L
C	301	25V 22u	Electrolytic capacitor	NICHICON CORPORATION	UPS1E220MDD
C	401	25V 10u	Electrolytic capacitor	NICHICON CORPORATION	UPS1E100MDD
C	513	10V 100u	Electrolytic capacitor	NICHICON CORPORATION	UPS1A101MDD
C	601	50V 0.1u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM21BR11H104KA01L
C	602	10V 1u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM216B11A105KA01
C	701	250VAC 0.33u	Film capacitor	NISSEI ELECTRIC CO., LTD.	MMDF 0250 K 334 0000 0150
C	702	250VAC 0.33u	Film capacitor	NISSEI ELECTRIC CO., LTD.	MMDF 0250 K 334 0000 0150
C	703	50V 0.1u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM21BR11H104KA01L
C	704	2kV 1000p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33D102KB3B
C	705	2kV 1000p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33D102KB3B
C	706	2kV 1000p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33D102KB3B
C	711	450V 1u	Film capacitor	Rubycon Corporation	450MMK105K
C	712	450V 1u	Film capacitor	Rubycon Corporation	450MMK105K
C	713	1KV 470p	Ceramic capacitor	Murata Manufacturing Co., Ltd.	DEHR33A332KA3B
C	714	450V 47u	Electrolytic capacitor	Rubycon Corporation	450BXA47MCC(18×31.5)
C	717	25V 22u	Electrolytic capacitor	NICHICON CORPORATION	UPS1E220MDD
C	719	50V 100u	Electrolytic capacitor	NICHICON CORPORATION	UPS1H101MPD
C	723	10V 1u	Monolithic ceramic capacitor	Murata Manufacturing Co., Ltd.	GRM216B11A105KA01
C	775	25V 47u	Electrolytic capacitor	NICHICON CORPORATION	UPS1E470MPDDD
CN	101	B5P-VH (LF)(SN)	Connector	J.S.T. Mfg. Co., Ltd.	B5P-VH (LF)(SN)
CN	201	B5P-VH (LF)(SN)	Connector	J.S.T. Mfg. Co., Ltd.	B5P-VH (LF)(SN)
CN	301	ML-800-S1V-2P	Connector	SATO PARTS CO., LTD.	ML-800-S1V-2P
CN	302	ML-800-S1V-2P	Connector	SATO PARTS CO., LTD.	ML-800-S1V-2P
CN	701	B2P3-VH (LF)(SN)	Connector	J.S.T. Mfg. Co., Ltd.	B2P3-VH (LF)(SN)
D	101	EP04RA60	FRD	Nihon Inter Electronics Corporation	EP04RA60
D	102	EP04RA60	FRD	Nihon Inter Electronics Corporation	EP04RA60
D	103	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	104	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	105	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	106	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	301	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	501	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	702	D1N60 5060	Diode	Shindengen Electric Manufacturing Co., Ltd.	D1N60 5060
D	703	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	704	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	707	D5L60 7000	FRD	Shindengen Electric Manufacturing Co., Ltd.	D5L60 7000
D	708	30PUB60	FRD	Nihon Inter Electronics Corporation	30PUB60
D	709	30PUB60	FRD	Nihon Inter Electronics Corporation	30PUB60
D	710	1SS133	Diode	ROHM Co., Ltd.	1SS133
D	711	1SS133	Diode	ROHM Co., Ltd.	1SS133
DB	1	D4SB60 L 7000	D bridge (AC)	Shindengen Electric Manufacturing Co., Ltd.	D4SB60 L 7000
DB	2	S1NBC60-7101	D bridge	Shindengen Electric Manufacturing Co., Ltd.	S1NBC60-7101
F	1	3.0A	Glass tube fuse	YOUBON Corporation	2MF-3
F	1	F-105	Fuse holder	SATO PARTS CO., LTD.	F-105
IC	772	MIP0221SU	IPD	Panasonic Corporation	MIP0221SU
IC	401	GP1UX511QS 38KHz	Remote light receiving unit	Sharp Corporation	GP1UX511QS 38KHz
JMP	401A	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401B	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401C	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401D	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401E	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401F	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401G	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401H	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401I	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
JMP	401J	DSP02-002-431G	Short plug	KEL Corporation	DSP02-002-431G
L	101	77-L002	Inductor 1mH	Tashiro Densetsu Corporation	77-L002
L	201	77-L002	Inductor 1mH	Tashiro Densetsu Corporation	77-L002
L	701	2200uH	Inductor	TDK Corporation	TSL1112-2222JR33
LED	1	SLR332VR3F	LED	ROHM Co., Ltd.	SLR332VR3F
LED	2	SLR332VR3F	LED	ROHM Co., Ltd.	SLR332VR3F
MOV	0	ERZV09D511	Absorber	Panasonic Corporation	ERZV09D511

Table B-1. Reference Parts Table (2/3)

Part	Part Number	Product Name and Specifications	Function	Manufacturer	Manufacturer Product Name
NTC	0	NTPAJ100LDKB0	NTC thermistor	Murata Manufacturing Co., Ltd.	NTPAJ100LDKB0
Q	101	RJK5012DPP-00-T2	Power MOSFET	Renesas Technology Corp.	RJK5012DPP-00-T2
Q	102	RJK5012DPP-00-T2	Power MOSFET	Renesas Technology Corp.	RJK5012DPP-00-T2
Q	103	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	104	2SA1037AKT146R	PNP transistor	ROHM Co., Ltd.	2SA1037AKT146R
Q	105	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	106	2SA1037AKT146R	PNP transistor	ROHM Co., Ltd.	2SA1037AKT146R
Q	107	IRFR430APbF	Power MOSFET	Vishay Intertechnology, Inc.	IRFR430APbF
Q	108	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	109	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	110	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	301	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	401	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	402	2SA1037AKT146R	PNP transistor	ROHM Co., Ltd.	2SA1037AKT146R
Q	703	RJK5012DPP-00-T2	Power MOSFET	Renesas Technology Corp.	RJK5012DPP-00-T2
Q	704	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	705	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	706	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	707	2SA1037AKT146R	PNP transistor	ROHM Co., Ltd.	2SA1037AKT146R
Q	708	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
Q	709	2SC2412KT146R	NPN transistor	ROHM Co., Ltd.	2SC2412KT146R
R	101	10Ω 3216	Chip resistor	KOA Corporation	RK73B2BTTD100G
R	102	5.1K 2W	Coat insulation metal film resistor	KOA Corporation	MOS2C(T52A)512J
R	103	2.4K 3216	Chip resistor	KOA Corporation	RK73B2BTTD242G
R	104	2.4K 3216	Chip resistor	KOA Corporation	RK73B2BTTD242G
R	105	200 2125	Chip resistor	KOA Corporation	RK73B2ATTD201G
R	106	10K 2W	Coat insulation metal film resistor	KOA Corporation	MOS2C(T52A)103J
R	107	20 2125	Chip resistor	KOA Corporation	RK73B2ATTD200G
R	108	6.8K 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	109	1K 2125	Chip resistor	KOA Corporation	RK73B2ATTD102G
R	110	24K 2125	Chip resistor	KOA Corporation	RK73B2ATTD243G
R	111	200 2125	Chip resistor	KOA Corporation	RK73B2ATTD201G
R	112	6.8K 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	113	430 2125	Chip resistor	KOA Corporation	RK73B2ATTD431G
R	114	20 2125	Chip resistor	KOA Corporation	RK73B2ATTD200G
R	115	6.8K 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	117	51 2125	Chip resistor	KOA Corporation	RK73B2ATTD510G
R	119	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	120	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	121	4.7K 2125	Chip resistor	KOA Corporation	RK73B2ATTD472G
R	123	4.7K 2125	Chip resistor	KOA Corporation	RK73B2ATTD472G
R	124	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	125	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	126	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	301	1.2K 2125	Chip resistor	KOA Corporation	RK73B2ATTD122G
R	302	330 2125	Chip resistor	KOA Corporation	RK73B2ATTD331G
R	303	3.3k 2125	Chip resistor	KOA Corporation	RK73B2ATTD332G
R	304	4.7 2125	Chip resistor	KOA Corporation	RK73B2ATTD4R7G
R	305	11k 2125	Chip resistor	KOA Corporation	RK73B2ATTD113G
R	306	0 2125	Chip resistor	KOA Corporation	RK73Z2ATTD
R	307	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	308	0 2125	Chip resistor	KOA Corporation	RK73Z2ATTD
R	402	33K 2125	Chip resistor	KOA Corporation	RK73B2ATTD333G
R	403	33K 2125	Chip resistor	KOA Corporation	RK73B2ATTD333G
R	404	22K 2125	Chip resistor	KOA Corporation	RK73B2ATTD223G
R	405	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	406	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	407	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	408	3.3K 2125	Chip resistor	KOA Corporation	RK73B2ATTD332B
R	409	1K 2125	Chip resistor	KOA Corporation	RK73B2ATTD102G
R	410	1K 2125	Chip resistor	KOA Corporation	RK73B2ATTD102G
R	411	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	413	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	414	2.2k 2125	Chip resistor	KOA Corporation	RK73B2ATTD222G
R	415	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	416	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	418	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	419	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	421	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	422	100k 2125	Chip resistor	KOA Corporation	RK73B2ATTD104G
R	423	330k 2125	Chip resistor	KOA Corporation	RK73B2ATTD334G
R	424	330k 2125	Chip resistor	KOA Corporation	RK73B2ATTD334G
R	521	100 2125	Chip resistor	KOA Corporation	RK73B2ATTD101G
R	522	1k 2125	Chip resistor	KOA Corporation	RK73B2ATTD102G
R	523	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	701	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	702	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	703	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	704	0.1 3W	Coat insulation metal film resistor	KOA Corporation	MOSX3C(T52A)R10J
R	705	10 2W	Coat insulation metal film resistor	KOA Corporation	MOS2C(T52A)100G
R	706	330K 3216	Chip resistor	KOA Corporation	RK73B2BTTD334G

Table B-1. Reference Parts Table (3/3)

Part		Part Number	Product Name and Specifications	Function	Manufacturer	Manufacturer Product Name
R	707	330K 3216	Chip resistor	KOA Corporation	RK73B2BTTD334G
R	708	6.8K 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	709	47k 3216	Chip resistor	KOA Corporation	RK73B2BTTD473G
R	710	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	711	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	712	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	713	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	714	4.7K 2125	Chip resistor	KOA Corporation	RK73B2ATTD472G
R	715	10K 2125	Chip resistor	KOA Corporation	RK73B2ATTD103G
R	716	4.7K 2125	Chip resistor	KOA Corporation	RK73B2ATTD472G
R	717	220 2125	Chip resistor	KOA Corporation	RK73B2ATTD221G
R	718	220 2125	Chip resistor	KOA Corporation	RK73B2ATTD221G
R	719	220 2125	Chip resistor	KOA Corporation	RK73B2ATTD221G
R	720	10 2125	Chip resistor	KOA Corporation	RK73B2ATTD100G
R	721	6.8k 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	722	330k 3216	Chip resistor	KOA Corporation	RK73B2BTTD334G
R	723	330k 3216	Chip resistor	KOA Corporation	RK73B2BTTD334G
R	724	6.8k 2125	Chip resistor	KOA Corporation	RK73B2ATTD682G
R	725	47k 3216	Chip resistor	KOA Corporation	RK73B2BTTD473G
R	762	2.2k 2125	Chip resistor	KOA Corporation	RK73B2ATTD222G
SW	1	M2T-12AAP1	Power switch	NIHON KAIHEIKI IND. CO., Ltd.	M2T-12AAP1
SW	401	SSSF014800	Selector switch	ALPS ELECTRIC CO., LTD.	SSSF014800
SW	402	SS-12SDP2	Slide switch	NIHON KAIHEIKI IND. CO., Ltd.	SS-12SDP2
SW	502	SKHRAAA010	Tact switch	ALPS ELECTRIC CO., LTD.	SKHRAAA010
T	1	77-L001	Inductor	Tashiro Densetsu Corporation	77-L001
TP	1	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	2	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	3	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	4	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	5	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	6	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	7	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	11	LC-2-G -black	Test pin	Mac-Eight Co., Ltd.	LC-2-G -black
TP	12	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	13	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	14	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	15	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	16	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	17	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	19	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	20	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	21	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	22	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	23	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	24	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	25	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	26	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	29	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	30	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	31	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	32	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	33	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	34	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	35	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	36	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
TP	37	LC-2-G -green	Test pin	Mac-Eight Co., Ltd.	LC-2-G -green
VR	401	100K	Volume dial	Bourns Inc.	3386F-1-104TLF
ZD	201	4.7V	Zener diode	ROHM Co., Ltd.	MTZJ T-77 4.7B
ZD	701	7.5V	Zener diode	ROHM Co., Ltd.	MTZJ T-77 7.5B