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## H8/300L SLP Series

### Connecting a Cadmium-Sulfide Photocell

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#### Introduction

A CdS cell is connected to the analog input pin, and the results of A/D conversion are displayed on seven-segment LEDs.

#### Target Device

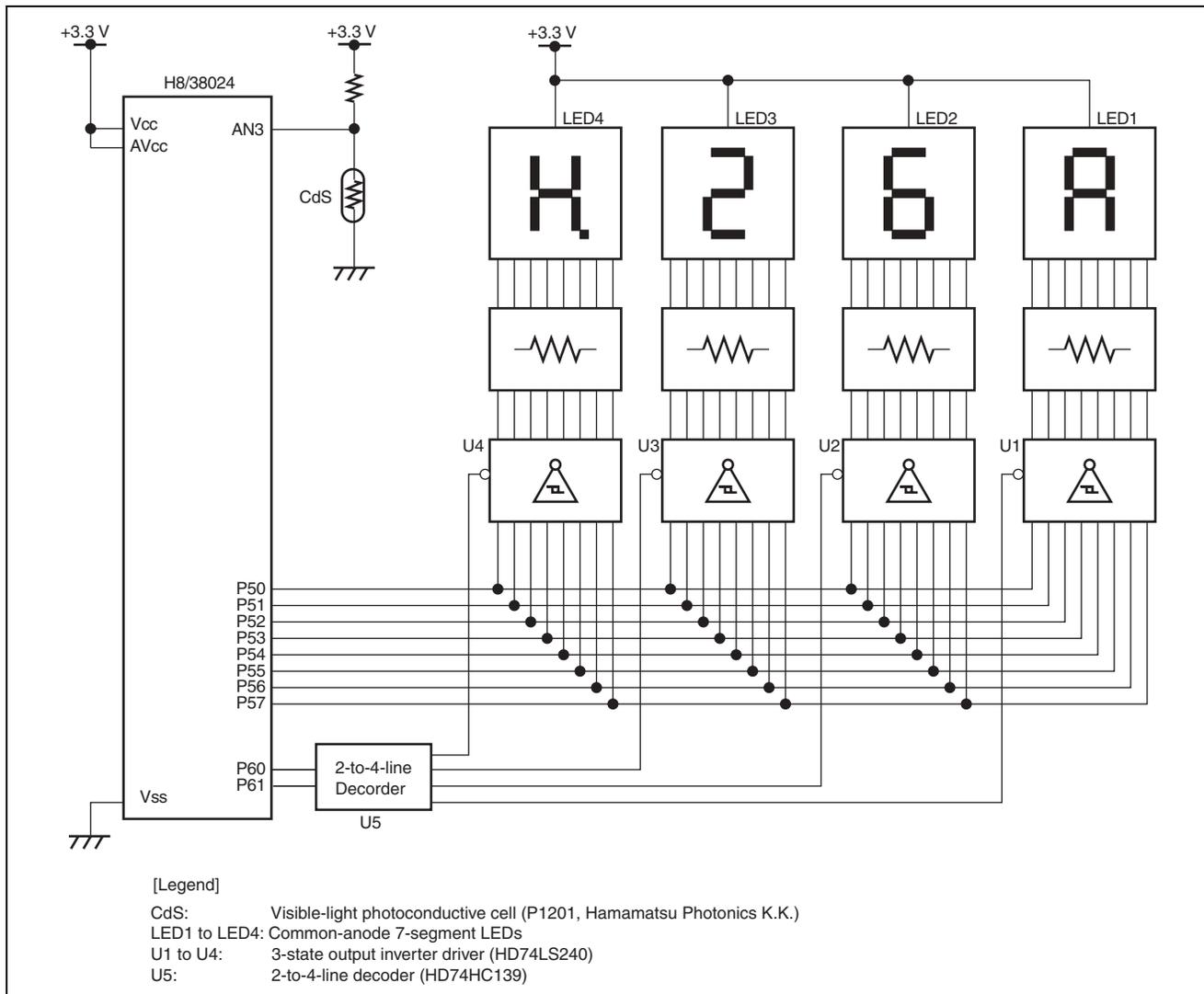
H8/38024

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### 1. Specifications

- Figure 1.1 shows the hardware configuration example of connecting a visible-light photoconductive cell. A resistor and visible-light photoconductive cell: CdS cells are connected to the analog input pin 3 (AN3 pin) as shown in the figure.
- The signal on the AN3 pin is A/D converted, after which the results of A/D conversion are displayed on the 7-segment LED connected to the I/O port.
- The 7-segment LED display shows the 10-bit result of A/D conversion as a hexadecimal value in the range from H'000 to H'3FF.
- A/D conversion is performed at 0.5-s intervals.



**Figure 1.1 Hardware Configuration**

- In this sample task, the H8/38024's operating voltage (Vcc) and analog power supply voltage (AVcc) are 3.3 V, the oscillation frequency of the system clock is 10 MHz and that of the sub-clock is 32.768 kHz.

6. The visible-light photoconductive cell, CdS cell, used in this sample task is a product of Hamamatsu Photonics K.K. (model P1201). The specifications of this CdS cell are as follows.

Table 1.1 lists the absolute maximum ratings and characteristics of the CdS cell (P1201).

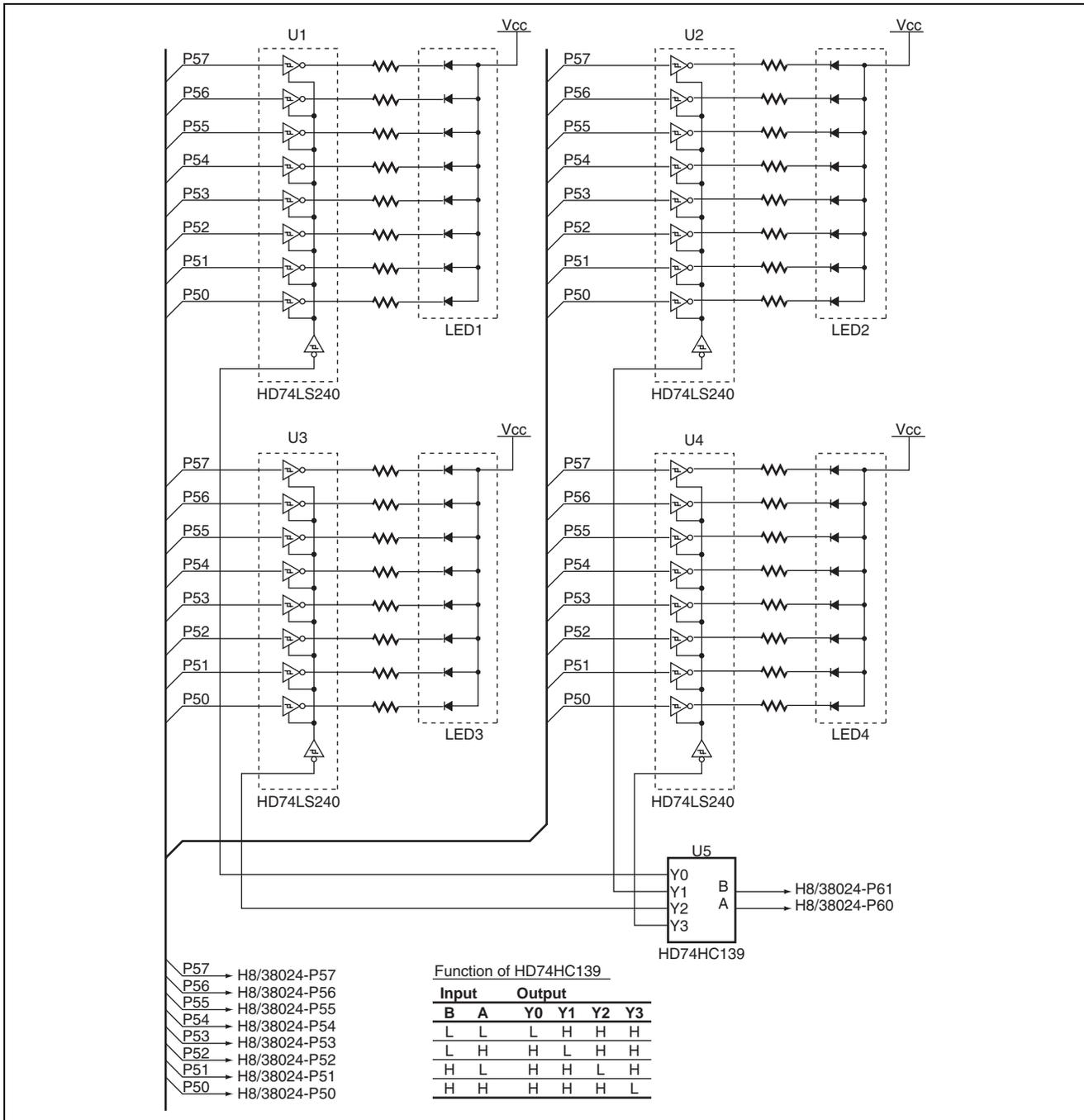
**Table 1.1 Absolute Maximum Ratings and Characteristics**

Maximum Absolute Ratings			Characteristics*1						
Applied Voltage (Vdc)	Allowable Dissipation (mW)	Ambient Temperature (°C)	Maximum Sensitivity Wave Length (nm)	Resistance Value*2				Response Time 10 I <sub>x</sub> *5	
				10 I <sub>x</sub> , 2856K		0 I <sub>x</sub> *3		γ <sub>10</sub> <sup>100</sup> *4	100 to 10 lx
Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
100	70	-30 to +80	540	20	60	5.0	0.75	40	30

- Notes: 1. All values were measured after exposure to light (100 to 500 I<sub>x</sub>) for one to two hours.  
 2. The light source is standard tungsten light bulb with a color temperature of 2856K.  
 3. Measured 10 seconds after shutting off the 10-I<sub>x</sub> incident light.  
 4. Typical gamma characteristics (within ±0.10 variations) between 10 I<sub>x</sub> and 100 I<sub>x</sub>.

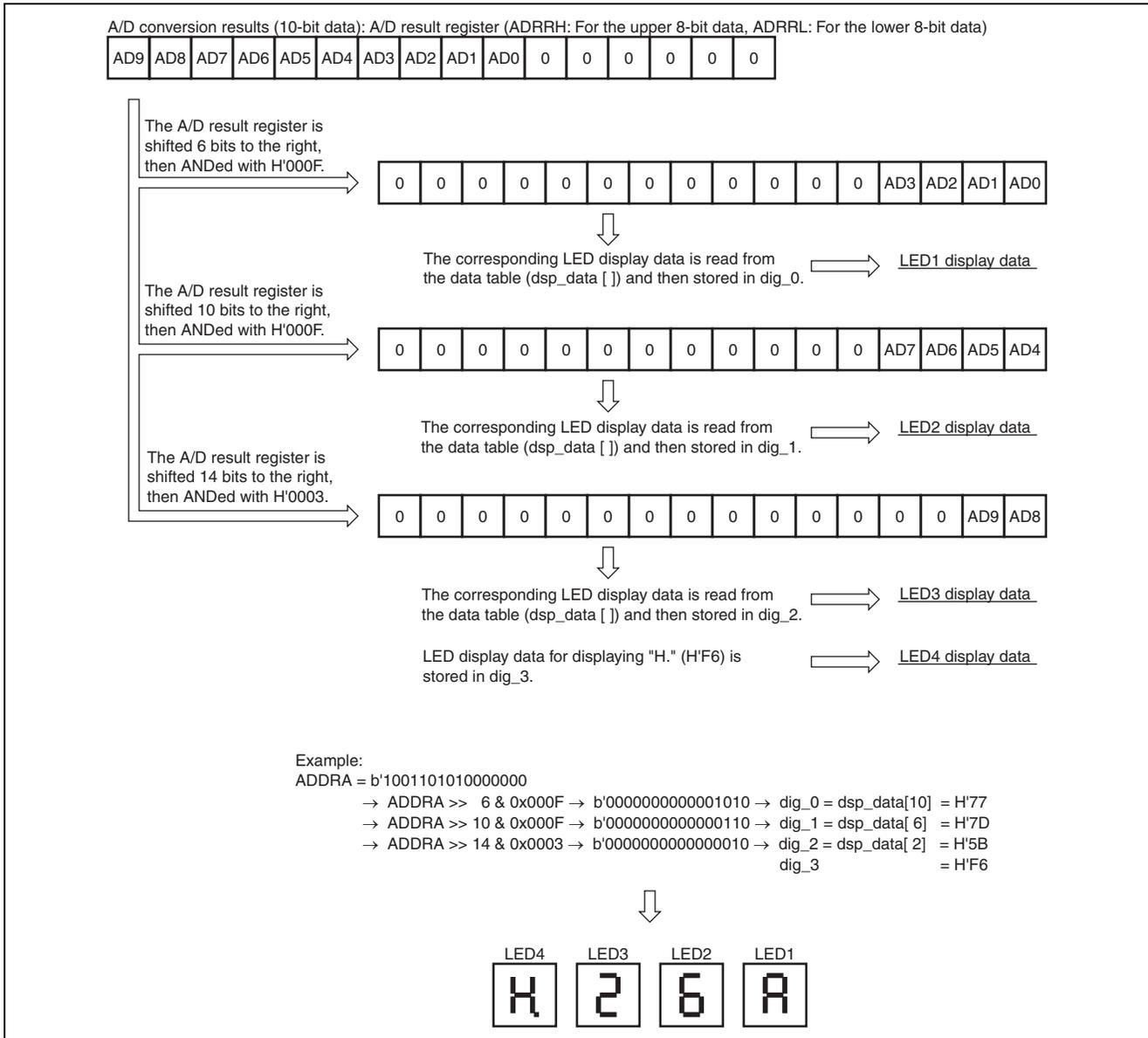
$$\gamma_{10}^{100} = \left| \frac{\log(R100) - \log(R10)}{\log(E100) - \log(E10)} \right|$$

5. The rise time is the time for the sensor resistance to reach 63% of saturation conductance level (when fully illuminated). The fall time is the time for the sensor resistance to decay from the saturation conductance level to 37%.
7. In this sample task, display on the 7-segment LED is handled by attaching port outputs to the inputs to the tri-state-output inverter drivers (HD74LS240), and the driver outputs are in turn connected to the cathodes of the 7-segment LEDs. The port outputs are connected to each of the four 7-segment LEDs to control the display on the LEDs. The enable pins of the tri-state inverter driver control switching of display on the 7-segment LEDs. The signals used to switch the display are generated by the 2-to-4-line decoder (HD74HC139), which is controlled by two port-pin outputs. Figure 1.2 shows how the 7-segment LEDs are controlled.



**Figure 1.2 7-Segment LED Control**

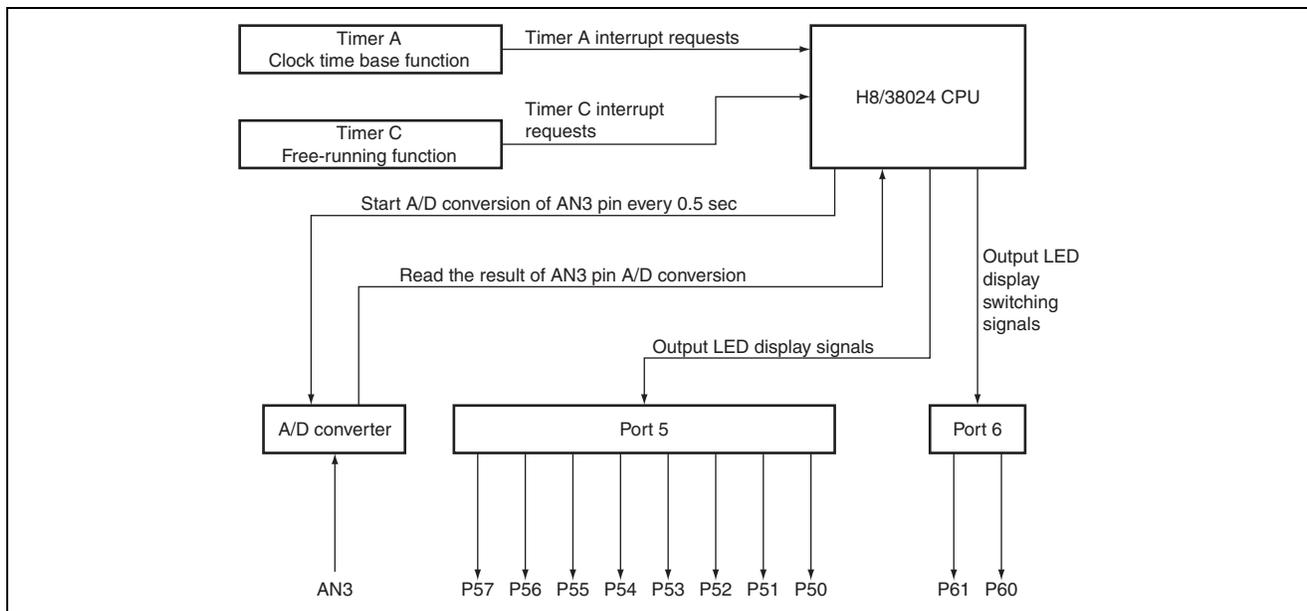
8. In this sample task, the results of A/D conversion are displayed in hexadecimal format (H'3FF to H'000) on the 7-segment LEDs. Figure 1.3 shows how this is done.



**Figure 1.3 How A/D Conversion Results are Displayed on the LEDs**

### 2. Description of Function

1. Figure 2.1 is a block diagram of the H8/38024 functions used in this sample task. Table 2.1 shows function allocations.

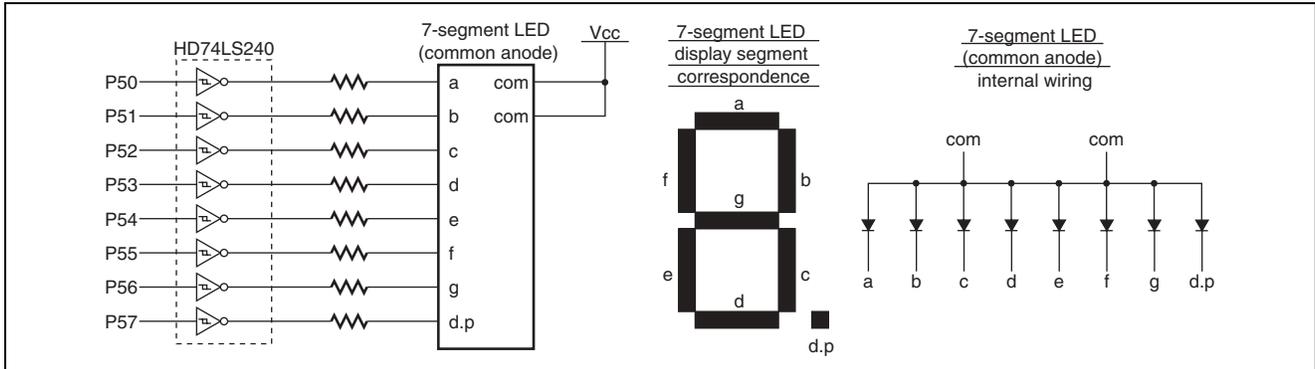


**Figure 2.1 Block Diagram of Functions Used**

**Table 2.1 Function Allocation**

Function	Function Allocation
Timer A	The timer A's clock time base function is used to measure 0.5 s, which is the period for A/D conversion of the signal on the analog input pin 3 (AN3). The timer A interrupt is used for each A/D conversion period.
Timer C	Timer C's free-running function is used to control switching of the 7-segment LED display. Each of the four 7-segment LEDs is lit in sequence at an interval of 3.2768 ms, which is the time taken for timer C to overflow. This obtains dynamic illumination from the LEDs.
A/D converter	This unit A/D-converts the result of dividing the voltage between the AVcc and GND planes by the fixed resistance and the resistance that varies according to the amount of light accepted by the CdS cell connected to analog input pin 3 (AN3) of the A/D converter.
Port 6	The four 7-segment LED display is switched by the P60 and P61 output pins of port 6. These pins are connected to the input/output pins of the 2-to-4-line decoder.
Port 5	The 7-segment LEDs are displayed by the P50 to P57 output pins of port 5. The 10 bits of data produced by A/D conversion of the value on the AN3 pin are converted to 3 digits of hexadecimal data for display, this is then output to the LED.

2. Figure 2.2 shows how the 7-segment LED used in this task is connected. A high output from port 5 lights up the corresponding segment as shown by the figure. Table 2.2 shows the relationship between the output from port 5 and the display on the LED.



**Figure 2.2 7-Segment LED Connection Diagram and Internal Wiring**

Table 2.2 Relation between Port 5 Outputs and 7-Segment LED Display Data

LED Display	LED DisplayPort 5 Output Data								LED Display	LED DisplayPort 5 Output Data							
	P57	P56	P55	P54	P53	P52	P51	P50		P57	P56	P55	P54	P53	P52	P51	P50
	0	0	1	1	1	1	1	1		0	1	1	1	0	1	1	1
	0	0	0	0	0	1	1	0		0	1	1	1	1	0	0	1
	0	1	0	1	1	0	1	1		0	0	1	1	1	0	0	1
	0	1	0	0	1	1	1	1		0	1	0	1	1	1	1	0
	0	1	1	0	0	1	1	0		0	1	1	1	1	0	0	1
	0	1	1	0	1	1	0	1		0	1	1	1	0	0	0	1
	0	1	1	1	1	1	0	1		0	1	0	0	0	0	0	0
	0	0	1	0	0	1	1	1		1	1	1	1	0	1	1	0
	0	1	1	1	1	1	1	1									
	0	1	1	0	1	1	1	1									

### 3. Principles of Operation

- Figure 3.1 shows the principle of operation in the use of timer A and A/D conversion carried out on the AN3 pin. The A/D conversion interrupt is not used in this sample task. Instead, the completion of A/D conversion is detected in the tmra interrupt processing routine.

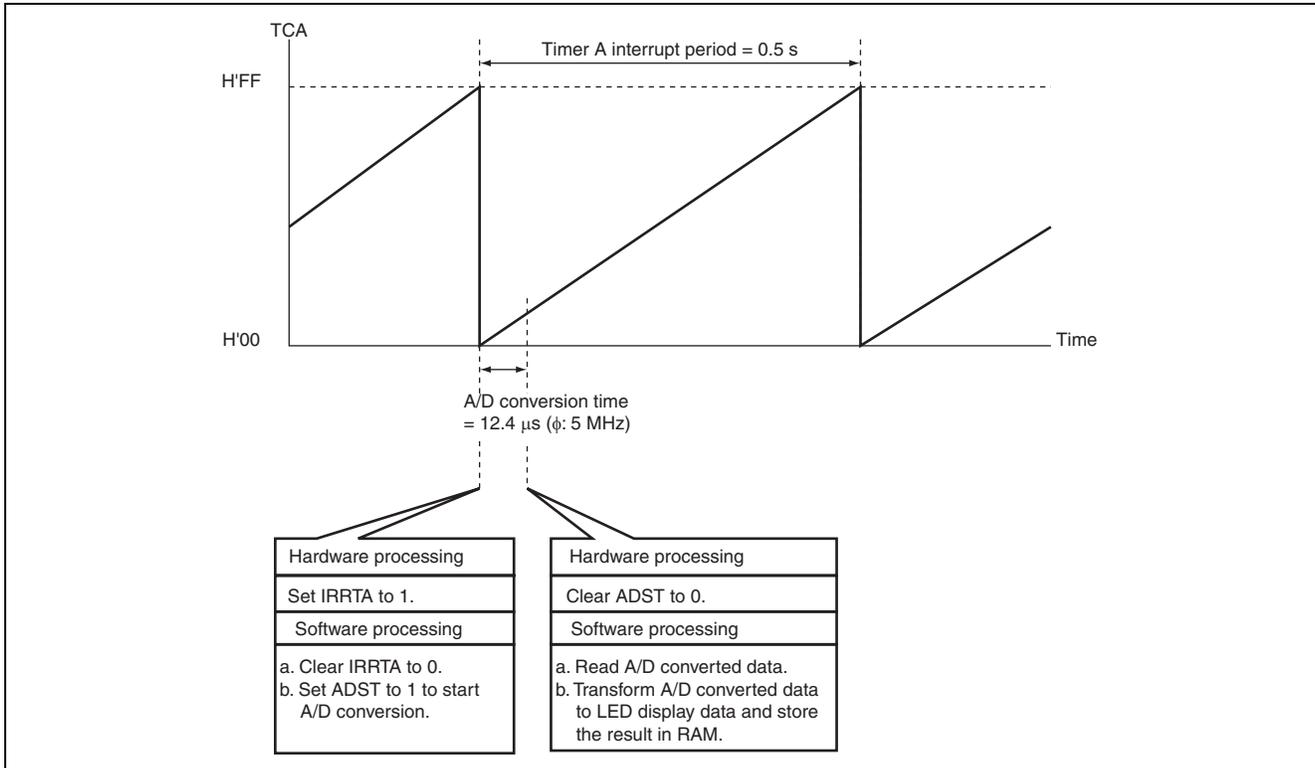


Figure 3.1 Operation Principle of A/D Conversion of AN3-Pin Signal Using Timer A

2. The principle applied in controlling the 7-segment displays is explained below. Figure 3.2 depicts the situation where "3210" is being displayed on LED4 to LED1. As the figure shows, the next display in sequence of LED1 to LED4 is lit up each time a timer-C overflow period elapses, creating a dynamic display on the 7-segment LEDs

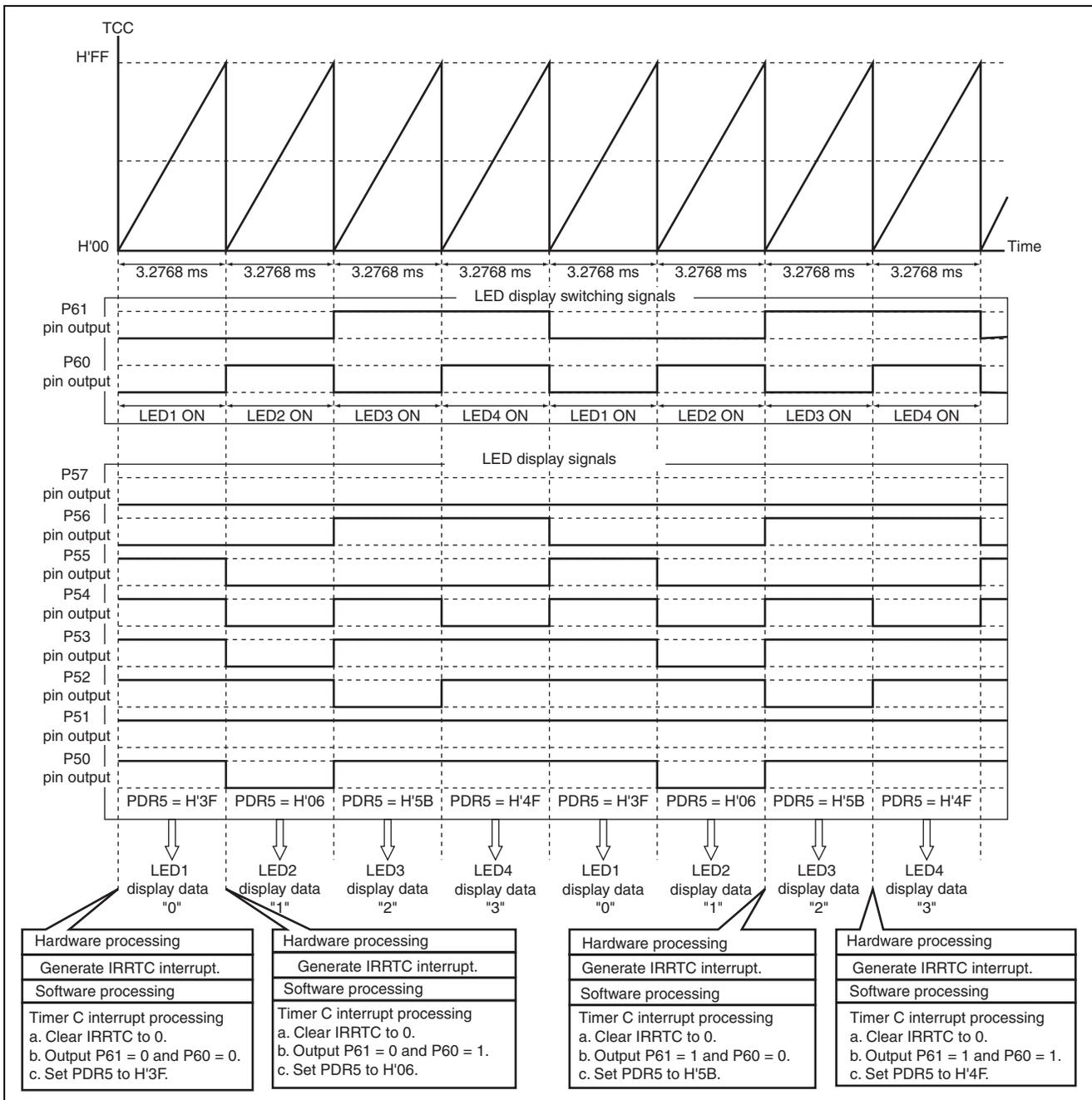


Figure 3.2 Operation Principle of 7-Segment LED Display Control

## 4. Description of Software

### 4.1 Modules

Table 4.1 describes the modules used in this sample task.

**Table 4.1 Description of Modules**

Module	Label	Function
Main routine	main	Makes initial settings and enables interrupts.
Timer A interrupt processing routine	tmra	Clears the interrupt flags, transforms A/D-converted data into LED-display data, and stores the result in RAM.
Timer C interrupt processing routine	tmrc	Clears the interrupt flags and controls output of LED-display data and switching of LED display.

### 4.2 Arguments

This sample task uses no arguments.

### 4.3 Internal Registers

The internal registers used in this sample task are described in table 4.2.

**Table 4.2 Description of Internal Registers**

Register	Function	Address	Setting
TMA	Timer mode register A Selects prescaler and input clock.	H'FFB0	H'0C (initial setting)
TMA3	Internal Clock Select 3 Selects the operating mode for timer A. When TMA3 = 1, timer A functions as the clock time base by counting the output from prescaler W.	Bit 3	1
TMA2	Internal Clock Select 2 to 0	Bit 2	0/1
TMA 1	When TMA3 = 1, clock time base (32.768 kHz) operation is selected. When TMA2 = 1, TMA1 = 0 and TMA0 = 0, TCA is reset. When TMA2 = 0, TMA1 = 0 and TMA0 = 1, TCA overflow period is 0.5 s.	Bit 1	0
TMA 0		Bit 0	0/1
TMC	Timer Mode Register C Selects the automatic reloading function, controls counting upward/downward of the counter, and controls input clock.	H'FFB4	H'1B
TMC7	Automatic Reloading Select When TMC7 = 0, the interval timer function is selected.	Bit 7	0
TMC6	Counter Upward/Downward Control	Bit 6	0
TMC5	When TMC6 = 0 and TMC5 = 0, TCC is an up-counter.	Bit 5	0
TMC2	Clock Select	Bit 2	0
TMC1	When TMC2 = 0, TMC1 = 1 and TMC0 = 1, counts on the internal clock $\phi/64$ .	Bit 1	1
TMC0		Bit 0	1
TLC	Timer Load Register C Sets TCC reload value.	H'FFB5	H'00

Register	Function	Address	Setting
AMR	A/D Mode Register Sets A/D conversion speed, selects use of external trigger, and specifies analog input pin.	H'FFC6	H'37
CKS	A/D Conversion Speed Setting When $\phi = 5$ MHz: CKS = 0 selects 12.4 $\mu$ s.	Bit 7	0
TRGE	Trigger Enable When TRGE = 0, starting of A/D conversion in response to an external trigger input is disabled.	Bit 6	0
CH3	Channel Select Bits 3 to 0	Bit 3	0
CH2	When CH3 = 0, CH2 = 1, CH1 = 1 and CH0 = 1, AN3 is selected.	Bit 2	1
CH1		Bit 1	1
CH0		Bit 0	1
ADSR	A/D Start Register Sets to start or stop A/D conversion.	H'FFC7	—
ADSF	A/D Conversion Start/Completion Check When read: ADSF = 0 indicates that A/D conversion is complete. ADSF = 1 indicates that A/D conversion is in progress. When written: Writing ADSF = 0 forcibly terminates A/D. Writing ADSF = 1 starts A/D conversion.	Bit 7	0/1
ADRRH	A/D Result Register Stores the upper 8 bits of the results of A/D conversion.	H'FFC4	—
ADRRL	A/D Result Register Stores the lower two bits of the results of A/D conversion in bits 7 and 6.	H'FFC5	—
PUCR6	Port Pull-Up Control Register 6 Provides bit-by-bit control of the MOS pull-up for the pins of port 6 that have been set as inputs. When PUCR6 = H'00, the MOS pull-up for the P67 to P60 pins are turned off.	H'FFE3	H'00
PDR6	Port Data Register 6 General-purpose I/O port data register for port 6	H'FFD9	H'00
PCR6	Port Control Register 6 Provides bit-by-bit control of input/output selection for the pins of port 6 that have been set as general-purpose I/O pins. When PCR6 = H'FF, the pins P67 to P60 function as general-purpose output pins.	H'FFE9	H'FF

Register	Function	Address	Setting
PMR5	Port Mode Register 5 Sets the port 5 pin functions	H'FFCC	H'00
WKP7	P57/WKP7/SEG7 Pin Function Switching WKP7 = 0 selects the general-purpose I/O port function for P57.	Bit 7	0
WKP6	P56/WKP6/SEG6 Pin Function Switching WKP6 = 0 selects the general-purpose I/O port function for P56.	Bit 6	0
WKP5	P55/WKP5/ADTRG Pin Function Switching WKP5 = 0 selects the general-purpose I/O port function for P55.	Bit 5	0
WKP4	P54/WKP4 Pin Function Switching WKP4 = 0 selects the general-purpose I/O port function for P54.	Bit 4	0
WKP3	P53/WKP3 Pin Function Switching WKP3 = 0 selects the general-purpose I/O port function for P53.	Bit 3	0
WKP2	P52/WKP2 Pin Function Switching WKP2 = 0 selects the general-purpose I/O port function for P52.	Bit 2	0
WKP1	P51/WKP1 Pin Function Switching WKP1 = 0 selects the general-purpose I/O port function for P51.	Bit 1	0
WKP0	P50/WKP0 Pin Function Switching WKP0 = 0 selects the general-purpose I/O port function for P50.	Bit 0	0
PUCR5	Port Pull-Up Control Register 5 Provides bit-by-bit control of the MOS pull-up for the pins of port 5 that have been set as inputs. When PUCR5 = H'00, the MOS pull-up for the P57 to P50 pins are turned off.	H'FFE2	H'00
PDR5	Port Data Register 5 General-purpose I/O port data register for port 5	H'FFD8	H'00
PCR5	Port Control Register 5 Provides bit-by-bit control of input/output selection for the pins of port 5 that have been set as general-purpose I/O pins. When PCR5 = H'FF, the pins P57 to P50 function as general-purpose output pins.	H'FFE8	H'FF
IENR1	Interrupt Enable Register 1 Enables/disables interrupt requests.	H'FFF3	—
IENTA	Timer A Interrupt Request Enable When IENTA = 1, the timer A overflow interrupt request is enabled.	Bit 5	1
IRR1	Interrupt Request Register 1 If an interrupt request is generated by the timer A, IRQ4, IRQ3, IRQAEC, IRQ1 or IRQ0, the corresponding flag is set to 1.	H'FFF6	—
IRRTA	Timer A Interrupt Request Flag This is set to 1 when the timer A counter has overflowed (H'FF → H'00). This is cleared to 0 when 0 is written to.	Bit 7	0/1
IENR2	Interrupt Enable Register 2 Enables/disables interrupt requests.	H'FFF4	—
IENTC	Timer C Interrupt Request Enable When IENTC = 1, the timer A overflow/underflow interrupt request is enabled.	Bit 1	1

Register	Function	Address	Setting
IRR2	Interrupt Request Register 2 If an interrupt request is generated by a direct transition, A/D converter, timer G, timer FH, timer FL, timer C or asynchronous event counter, the corresponding flag is set to 1.	H'FFF7	—
IRRTC	Timer C Interrupt Request Flag This is set to 1 when the timer C counter has overflowed (H'FF → H'00) or underflowed (H'00 → H'FF). This is cleared to 0 when 0 is written to.	Bit 7	0/1

#### 4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

**Table 4.3 Description of RAM**

Label	Function	Address	Used in
dig_0	Stores LED1 display data. (1 byte)	H'FB80	main, tmra
dig_1	Stores LED2 display data. (1 byte)	H'FB81	main, tmra
dig_2	Stores LED3 display data. (1 byte)	H'FB82	main, tmra
dig_3	Stores LED4 display data. (1 byte)	H'FB83	main, tmra
cnt	8-bit counter used in switching display from LED1 to LED4. (1 byte)	H'FB84	main, tmrc

#### 4.5 Description of Data Table

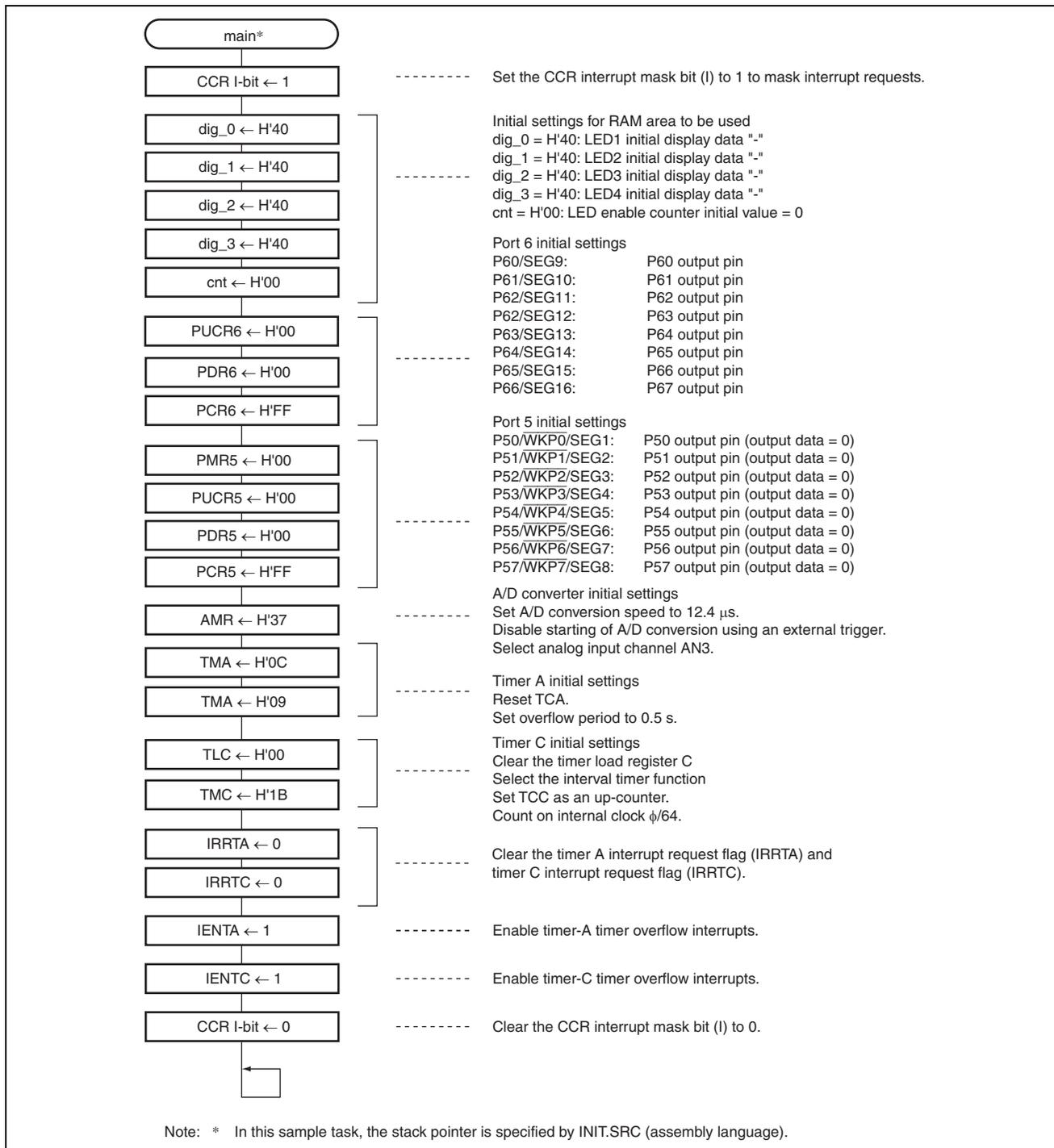
In this sample task, display data for the 7-segment LED displays are stored in the ROM as a 1-dimensional array (data table). Table 4.4 describes the table of display data (dsp\_data [ ]).

**Table 4.4 Description of 7-Segment LED Display Data Table (dsp\_data[ ])**

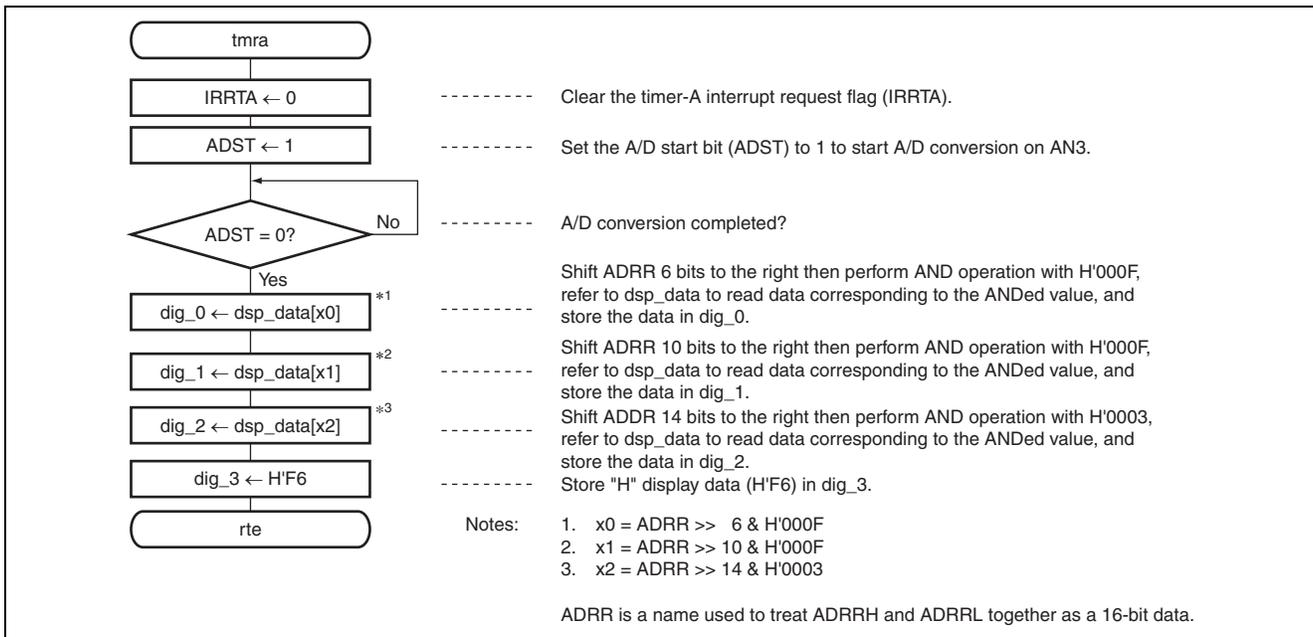
Array Name	Data	Data Description	Data Size	Address
dsp_data[0]	H'3F	Data output from port 5 to display "0"	1 byte	H'01EC
dsp_data[1]	H'06	Data output from port 5 to display "1"	1 byte	H'01ED
dsp_data[2]	H'5B	Data output from port 5 to display "2"	1 byte	H'01EE
dsp_data[3]	H'4F	Data output from port 5 to display "3"	1 byte	H'01EF
dsp_data[4]	H'66	Data output from port 5 to display "4"	1 byte	H'01F0
dsp_data[5]	H'6D	Data output from port 5 to display "5"	1 byte	H'01F1
dsp_data[6]	H'7D	Data output from port 5 to display "6"	1 byte	H'01F2
dsp_data[7]	H'27	Data output from port 5 to display "7"	1 byte	H'01F3
dsp_data[8]	H'7F	Data output from port 5 to display "8"	1 byte	H'01F4
dsp_data[9]	H'6F	Data output from port 5 to display "9"	1 byte	H'01F5
dsp_data[10]	H'77	Data output from port 5 to display "A"	1 byte	H'01F6
dsp_data[11]	H'7C	Data output from port 5 to display "b"	1 byte	H'01F7
dsp_data[12]	H'39	Data output from port 5 to display "C"	1 byte	H'01F8
dsp_data[13]	H'5E	Data output from port 5 to display "d"	1 byte	H'01F9
dsp_data[14]	H'79	Data output from port 5 to display "E"	1 byte	H'01FA
dsp_data[15]	H'71	Data output from port 5 to display "F"	1 byte	H'01FB

### 5. Flowchart

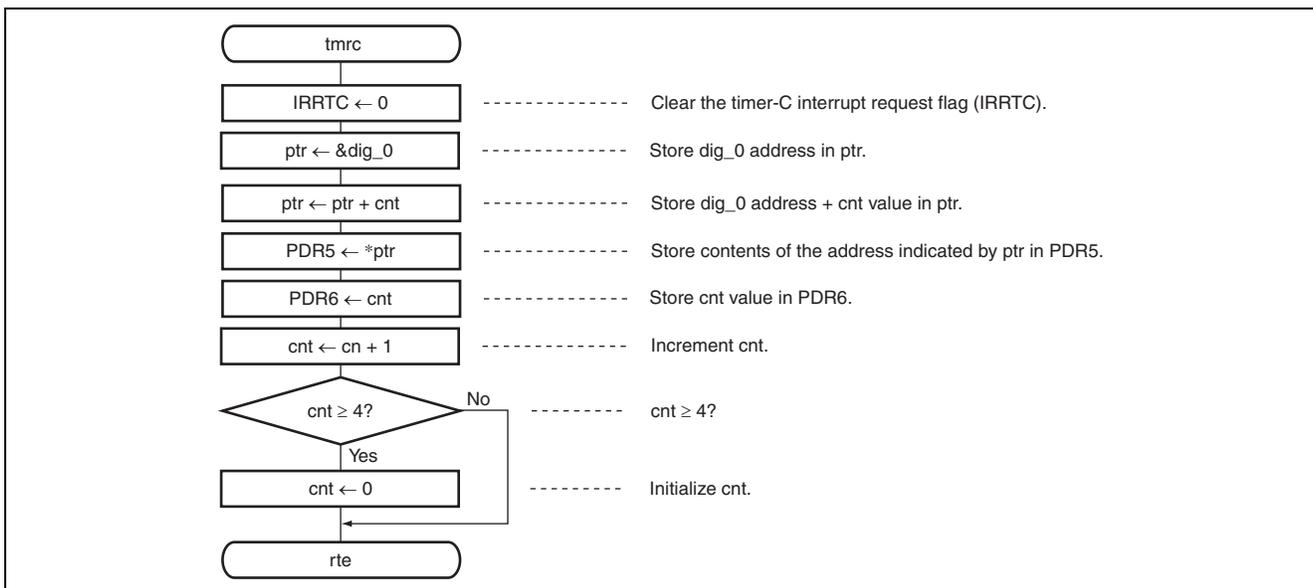
#### 1. Main routine (main)



### 2. Timer A interrupt processing routine (tmra)



### 3. Timer C interrupt processing routine (tmrc)



## 6. Program Listing

INIT.SRC (Program listing)

```

.EXPORT  _INIT
.IMPORT  _main
;
.SECTION P, CODE
_INIT:
MOV.W   #H'FF80, R7
LDC.B   #B'10000000, CCR
JMP     @_main
;
.END

/*****
/*
/* H8/300L Super Low Power Series
/* -H8/38024 Series-
/* Application Note
/* ' Application example '
/* ' Connecting a CdS cell '
/*
/* Function
/* : Connecting a CdS cell
/*
/* External Clock : 10MHz
/* Internal Clock : 5MHz
/* Sub Clock      : 32.768kHz
/*
*****/

#include <machine.h>

/*****
/* Symbol Definition
*****/
struct BIT {
    unsigned char  b7:1;    /* bit7 */
    unsigned char  b6:1;    /* bit6 */
    unsigned char  b5:1;    /* bit5 */
    unsigned char  b4:1;    /* bit4 */
    unsigned char  b3:1;    /* bit3 */
    unsigned char  b2:1;    /* bit2 */
    unsigned char  b1:1;    /* bit1 */
    unsigned char  b0:1;    /* bit0 */
};

#define PUCR6      *(volatile unsigned char *)0xFFE3    /* Port pull-up control register 6 */
#define PDR6      *(volatile unsigned char *)0xFFD9    /* Port data register 6 */
#define PCR6      *(volatile unsigned char *)0xFFE9    /* Port control register 6 */

#define PMR5      *(volatile unsigned char *)0xFFCC    /* Port mode register 5 */
#define PUCR5     *(volatile unsigned char *)0xFFE2    /* Port pull-up control register 5 */
#define PDR5      *(volatile unsigned char *)0xFFD8    /* Port data register 5 */
#define PCR5      *(volatile unsigned char *)0xFFE8    /* Port control register 5 */

```

```

#define TMA      *(volatile unsigned char *)0xFFB0      /* Timer mode register A      */
#define CKSTPR1  *(volatile unsigned char *)0xFFFA      /* Clock stop register 1      */

#define TMC      *(volatile unsigned char *)0xFFB4      /* Timer mode register C      */
#define TLC      *(volatile unsigned char *)0xFFB5      /* Timer Load register C      */

#define ADDR     *(volatile unsigned int *)0xFFC4       /* A/D result register (word access) */
#define ADDRH    *(volatile unsigned int *)0xFFC4       /* A/D result register (byte access) */
#define ADDRRL   *(volatile unsigned int *)0xFFC5       /* A/D result register (byte access) */
#define AMR      *(volatile unsigned char *)0xFFC6       /* A/D mode register          */
#define ADSR     *(volatile unsigned char *)0xFFC7       /* A/D start register         */
#define ADSR_BIT (*(struct BIT *)0xFFC7)
#define ADST     ADSR_BIT.b7                             /* A/D start                  */

#define IRR1     *(volatile unsigned char *)0xFFF6       /* Interrupt request register 1 */
#define IRR1_BIT (*(struct BIT *)0xFFF6)
#define IRRTA    IRR1_BIT.b7                             /* Timer A interrupt request flag */
#define IENR1    *(volatile unsigned char *)0xFFF3       /* Interrupt enable register 1 */
#define IENR1_BIT (*(struct BIT *)0xFFF3)
#define IENTA    IENR1_BIT.b7                             /* Timer A interrupt enable     */

#define IRR2     *(volatile unsigned char *)0xFFF7       /* Interrupt request register 2 */
#define IRR2_BIT (*(struct BIT *)0xFFF7)
#define IRRTC    IRR2_BIT.b1                             /* Timer C interrupt request flag */
#define IENR2    *(volatile unsigned char *)0xFFF4       /* Interrupt enable register 2 */
#define IENR2_BIT (*(struct BIT *)0xFFF4)
#define IENTC    IENR2_BIT.b1                             /* Timer C interrupt enable     */

#pragma interrupt (tmra)
#pragma interrupt (tmrc)

/*****
/* Function Definition
*****/
extern void INIT(void); /* Stack pointer set */
void main(void); /* main routine */
void tmra(void); /* Timer A interrupt routine */
void tmrc(void); /* Timer C interrupt routine */

```

```

/*****
/* Data Table */
/*****
const unsigned char dsp_data[16] =
{
    0x3f,          /* LED display data = "0" */
    0x06,          /* LED display data = "1" */
    0x5b,          /* LED display data = "2" */
    0x4f,          /* LED display data = "3" */
    0x66,          /* LED display data = "4" */
    0x6d,          /* LED display data = "5" */
    0x7d,          /* LED display data = "6" */
    0x27,          /* LED display data = "7" */
    0x7f,          /* LED display data = "8" */
    0x6f,          /* LED display data = "9" */
    0x77,          /* LED display data = "A" */
    0x7c,          /* LED display data = "B" */
    0x39,          /* LED display data = "C" */
    0x5e,          /* LED display data = "D" */
    0x79,          /* LED display data = "E" */
    0x71,          /* LED display data = "F" */
};

/*****
/* RAM Define */
/*****
unsigned char dig_0;          /* Dig-0 LED display data store */
unsigned char dig_1;          /* Dig-1 LED display data store */
unsigned char dig_2;          /* Dig-2 LED display data store */
unsigned char dig_3;          /* Dig-3 LED display data store */
unsigned char cnt;           /* LED enable counter */

/*****
/* Vector Address */
/*****
#pragma section V1          /* Vector section set */
void (*const VEC_TBL1[])(void) = {
    INIT          /* 0x0000 Reset vector */
};
#pragma section V2          /* Vector section set */
void (*const VEC_TBL2[])(void) = {
    tmra          /* 0x0016 Timer A interrupt vector */
};
#pragma section V3          /* Vector section set */
void (*const VEC_TBL3[])(void) = {
    tmrc          /* 0x001A Timer C interrupt vector */
};
#pragma section          /* P */

```

```

/*****
/* Main Program
/*****
void main(void)
{
    set_imask_ccr(1);                /* CCR I-bit = 1                */

    dig_0 = 0x40;                    /* Used RAM area initialize    */
    dig_1 = 0x40;                    /* Used RAM area initialize    */
    dig_2 = 0x40;                    /* Used RAM area initialize    */
    dig_3 = 0x40;                    /* Used RAM area initialize    */
    cnt   = 0x00;                    /* Used RAM area initialize    */

    PUCR6 = 0x00;                    /* Port 6 initialize          */
    PDR6  = 0x00;
    PCR6  = 0xFF;

    PMR5  = 0x00;                    /* Port 5 initialize          */

    PUCR5 = 0x00;
    PDR5  = 0x00;
    PCR5  = 0xff;

    AMR   = 0x37;                    /* A/D converter initialize (AN3) */

    TMA   = 0x0c;                    /* Clear Timer Counter A to 0   */
    TMA   = 0x09;                    /* Timer A initialize           */
    TLC   = 0x00;                    /* Clear Timer Load register C to 0 */
    TMC   = 0x1b;                    /* Timer C initialize           */

    IRRTA = 0;                       /* Clear IRRTA to 0            */
    IRRTC = 0;                       /* Clear IRRTC to 0            */
    IENTA = 1;                       /* Timer A interrupt enable     */
    IENTC = 1;                       /* Timer C interrupt enable     */

    set_imask_ccr(0);                /* CCR I-bit = 0                */

    while(1);
}

/*****
/* Timer A Interrupt
/*****
void tmra(void)
{
    IRRTA = 0;                       /* Clear IRRTA to 0            */
    ADST  = 1;                       /* A/D converter start         */
    while(ADST == 1);                /* A/D converter end ?        */
    dig_0 = dsp_data[ADRR >> 6 & 0x000f]; /* Dig-0 LED display data set */
    dig_1 = dsp_data[ADRR >> 10 & 0x000f]; /* Dig-1 LED display data set */
    dig_2 = dsp_data[ADRR >> 14 & 0x0003]; /* Dig-2 LED display data set */
    dig_3 = 0xf6;                    /* Dig-3 LED display data set */
}

```

```

/*****
/* Timer C Interrupt
/*****
void tmrc(void)
{
    unsigned char *ptr;                /* Pointer set */
    IRRTC = 0;                         /* Clear IRRTC to 0 */
    ptr = &dig_0;                      /* LED display data store address set */
    ptr += cnt;                        /* LED display data read */
    PDR5 = *ptr;                       /* LED display data output */
    PDR6 = cnt;                        /* LED enable data output */
    cnt++;                             /* "cnt" increment */
    if (cnt >= 4){                    /* 4 times end ? */
        cnt = 0;                      /* "cnt" initialize */
    }
}

```

**Link address specifications**

Section Name	Address
CV1	H'0000
CV2	H'0016
CV3	H'001A
P	H'0100
B	H'FB80

**Revision Record**

Rev.	Date	Description	
		Page	Summary
1.00	Dec.19.03	—	First edition issued

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