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R32C/100 Series

Configuring Wait Mode

1. Abstract

This document describes the settings to enter wait mode.

2. Introduction

The application described in this document applies to the following MCU:

- MCU: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

3. Overview

Wait mode is a low power mode in which the MCU's base clock is stopped. In wait mode, as the MCU's base clock is stopped, the CPU clock and peripheral bus clock, both of which are generated by the base clock, are stopped as well. As a result, the CPU and watchdog timer are stopped.

Execute the WAIT instruction to enter wait mode from PLL self-oscillation mode, low speed mode, or low power mode.

Use a hardware reset, NMI, or peripheral function interrupt to exit wait mode.

This document explains the settings necessary to enter wait mode, as well as shows an example of using the timer A1 interrupt to exit wait mode.

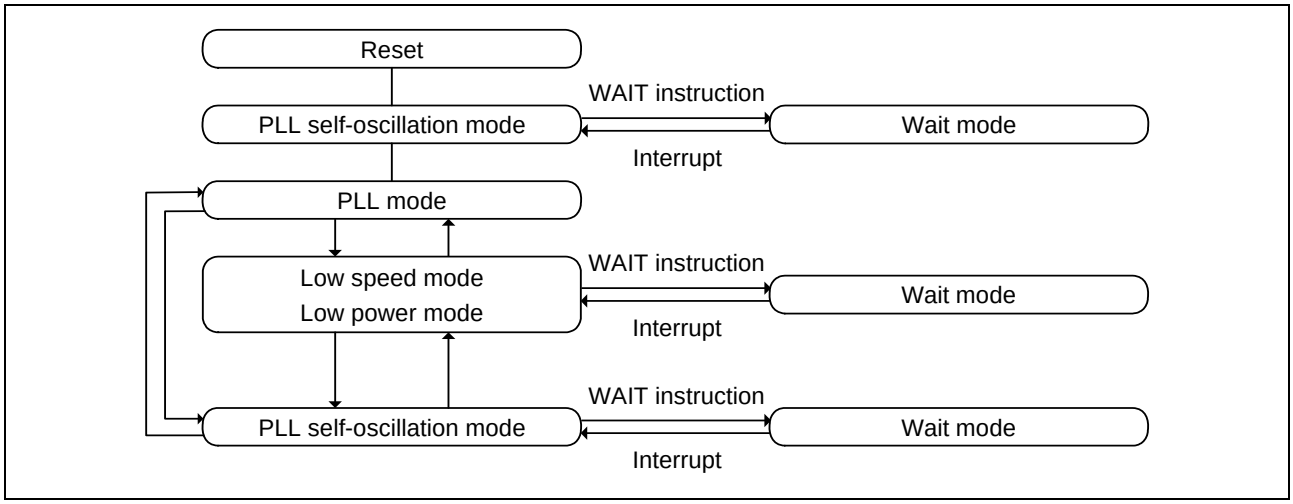

Figure 3.1 Entering Wait Mode

4. Settings

This section describes the settings to enter wait mode.

4.1 Notes

The following are precautions that should be taken when building a program using a wait mode.

4.1.1 Using Wait Mode

The MCU enters wait mode by executing the WAIT instruction. When using wait mode, there are necessary steps to be taken for the initial settings, necessary steps before entering the WAIT instruction, and necessary steps for exiting wait mode. These steps are listed below.

Initial Settings

Set individual request levels after setting the wake-up interrupt priority level (RLVL2 to RLVL0 bits in the RIPL1 and RIPL2 registers) to 7.

Before Entering the Wait mode

(1) Set the I flag to 0.
(2) Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.
(3) Perform a dummy read of any interrupt control registers.
(4) Set the processor interrupt priority level (IPL) in the flag register (FLG) to 0.
(5) Enable interrupts temporarily by executing the following instructions:
FSET I
NOP
NOP
FCLR I
(6) Set the interrupt request level for the interrupt to exit wait mode. Do not rewrite the interrupt control register after this step.
(7) Set the IPL in the flag register.
(8) Set the interrupt priority level for resuming to the same level as the IPL.
Interrupt request level of the interrupt used to exit wait mode > IPL = Interrupt priority level for resuming.
(9) Change the current operation mode to another to move to wait mode (1).
When using the oscillation stop function:
Set the CM20 bit in the CM2 register to 0 (oscillation stop detection function).
Set the CM20 bit to 0 before stopping the main clock.
This setting can be performed at any point before step (9).
(10) Set the I flag to 1.
(11) Execute the WAIT instruction.

Note:
1. The following modes can be switched to wait mode.
- Low speed mode
- Low power mode
- PLL self-oscillation Mode

After Exiting Wait Mode

After exiting wait mode, immediately set the wake-up interrupt priority level to 7.

4.1.2 Setting the I Flag and IPL

This application note uses the asm function to set the I flag and IPL. The following figures show how to set the I flag and IPL using asm function in C. Figure 4.1 shows the Setting the I Flag, Figure 4.2 shows the Setting IPL and Figure 4.3 shows the Executing the WAIT Instruction.

```
asm("FCLR   I") ;
        Sets the I flag to 0

asm("FSET   I") ;
        Sets the I flag to 1
```

Figure 4.1 Setting the I Flag

```
asm("LDIPL   #3") ;
        Sets IPL to 3
```

Figure 4.2 Setting IPL

```
asm("WAIT") ;
        Executes the WAIT instruction
```

Figure 4.3 Executing the WAIT Instruction

4.1.3 Stopping the Peripheral Function Clock

If the CM02 bit in the CM0 register is set to 1 (when peripheral function clock source stops in wait mode), the peripheral clock stops in wait mode. This further reduces power consumption.
Note that fC32 and f2n (when the main clock is selected as the clock source) do not stop.

4.1.4 Exiting Wait Mode

Use a hardware reset, NMI, or peripheral function interrupt (from software interrupts 0 to 63) to exit wait mode.

The following table lists settings for exiting wait mode.

Table 4.1 Interrupts for Exiting Wait Mode

Interrupt	CM02 Bit is 0	CM02 Bit is 1
NMI	Applicable	Applicable
External interrupt (excluding INT6, INT7, and INT8)	Applicable	Applicable
Key input interrupt	Applicable	Applicable
Low voltage detect interrupt	Applicable	Applicable
Timer A interrupt Timer B interrupt	Applicable in all modes	Applicable in event counter mode, or when the count source is fC32 or f2 (main clock selected as clock source)
Serial interface interrupt (excluding UART7 and UART8)	Applicable with both external and internal clocks	Applicable when using an external clock or f2n (main clock selected as clock source)
A/D conversion interrupt	Applicable in one-shot mode or single sweep mode	Do not use
Intelligent I/O interrupt	Applicable	Do not use
I^2C-bus interface interrupt	Applicable	Do not use
I^2C-bus line interrupt	Applicable	Applicable
CAN wake-up interrupt	Applicable	Applicable

4.1.5 Notes on Setting Protected Registers

Registers set in this application note (PM2, CM0, CM3, and CCR) are protected by the protect register. (see table below for details). The protect function protects important registers from being unintentionally rewritten due to a program runaway. After disabling the protect function, protected registers can be rewritten.

Table 4.2 The Protect Register and Protected Registers

Register	Write Disabled/Enabled	Protected Registers
PRCR	PRC0 Bit 0: Write disabled 1: Write enabled	CM0 to CM2, and PM3
	PRC1 Bit 0: Write disabled 1: Write enabled	PM0, PM2, CSOP0 to CSOP2, INVC0, INVC1, IOBC, and I2CMR
	PRC2 Bit 0: Write disabled 1: Write enabled	PD9, P9_iS (i = 0 to 7), PLC0, and PLC1
PRCR2	PRC27 Bit 0: Write disabled 1: Write enabled	CM3
PRCR3	PRC31 Bit 0: Write disabled 1: Write enabled	VRCR, LVDC, and DVCR
PRR	b7 to b0 Value Other than AAh: Write disabled AAh: Write enabled	CCR, FMCR, PBC, FEBC0, and FEBC3, EBC0 to EBC3, CB01, CB12, and CB23

4.2 Setting Overview

The figure below shows the procedure for entering wait mode. Refer to section **4.3 "Detailed Settings"** for detailed settings.

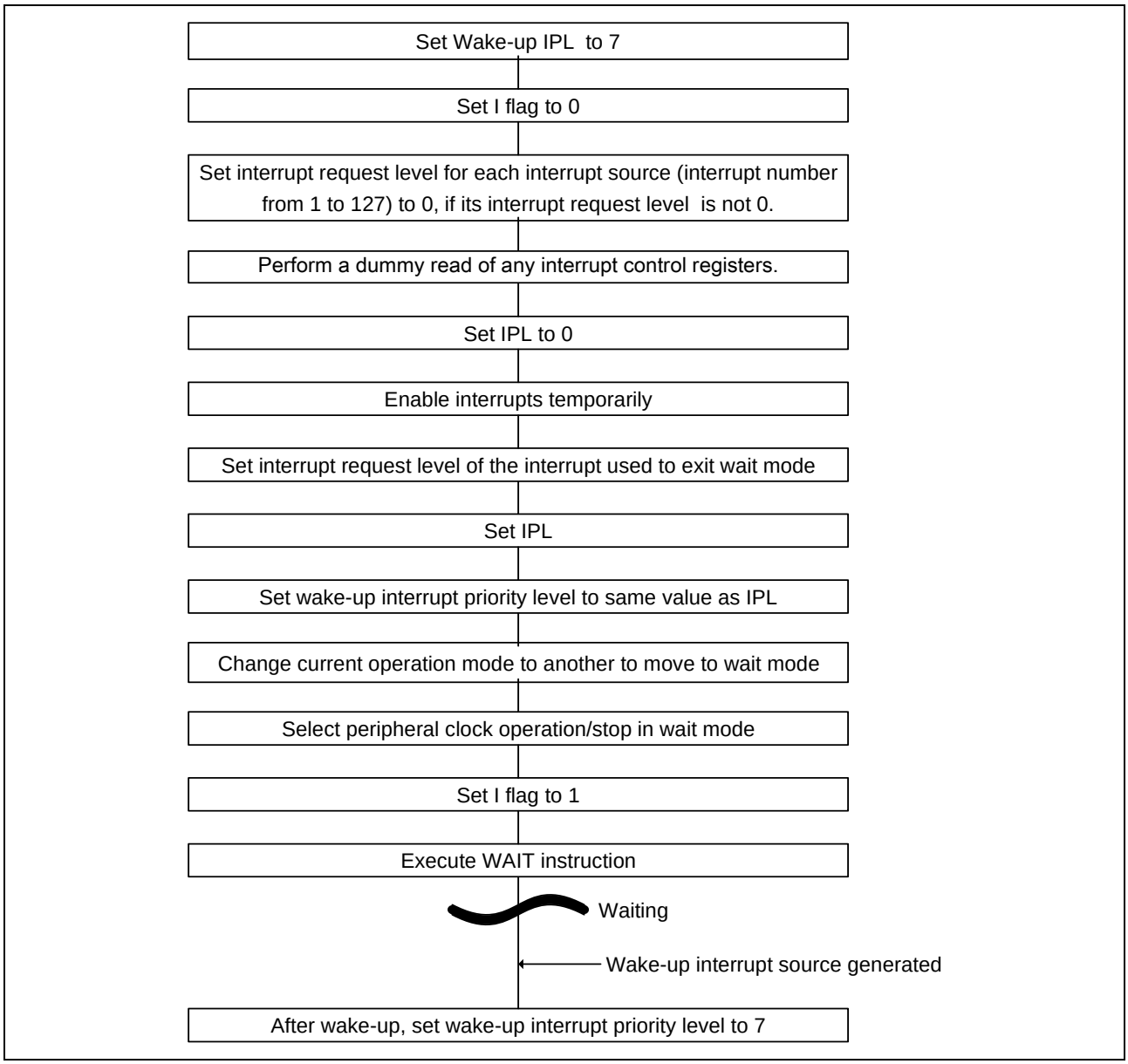

Figure 4.4 Procedures for Entering Wait Mode

4.3 Detailed Settings

Set the wake-up interrupt priority level to 7.

b7 b0

X	X	0	X	0	1	1	1

Wake-up Interrupt Priority Level Set Register i (RIPLi) (i = 1, 2)

RLVL2 to RLVL0	Stop/Wait Wake-up Interrupt Priority Level Select Bit 111b: Level 7
FSIT	Fast Interrupt Select Bit 0: Use interrupt priority level 7 for normal interrupt
b4	Set to 0.
DMAII	DMAII Select Bit 0: Use interrupt priority level 7 for interrupt
b7 to b6	Set to 0.

Set the I flag to 0.

Asm(“FCLR I”)

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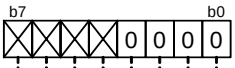
Set the interrupt request level for each interrupt source (interrupt number from 1 to 127) to 0, if its interrupt request level is not 0.

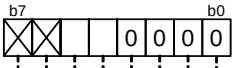


Interrupt Control Register

TA0IC to TA4IC, TB0IC to TB5IC, S0TIC to S8TIC, S0RIC to S8RIC, BCN0IC to BCN6IC, DM0IC to DM3IC, AD0IC, KUPIC, IIO0IC to IIO11IC, I2CIC, I2CLIC, C0FTIC to C1FTIC, C0FRIC to C1FRIC, C0TIC to C1TIC, C0RIC to C1RIC, C0EIC to C1EIC, C0WIC to C1WIC

- ILV2 to ILV0 — Interrupt Reqeust Level Select Bit
  000b: level 0 (Interrupt disabled)
- IR — Interrupt Request Flag
  0: No interrupt requested
- b7 to b4 — Set to 0.

Set the IR bit to 0.



Interrupt Control Register (INT0IC to INT8IC)

- ILV2 to ILV0 — Interrupt Request Level Select Bit
  000b: level 0 (Interrupt disabled)
- IR — Interrupt Request Flag
  0: No interrupt requested
- POL — Polarity Switch Bit
  0: Select the falling edge or a low level signal
  1: Select the rising edge or a high level signal
- LVS — Level Sense/Edge Sense Switch Bit
  0: Edge sense
  1: Level sense
- b7 to b6 — Set to 0.

Set the IR bit to 0.

Perform a dummy read of any interrupt control registers.

Set IPL to 0.

```
asm (“LDIPL#0”) ;
```

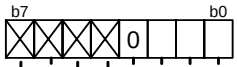
Continued on next page

Continued from previous page

Interruption is temporarily permitted.

```
asm("FSET I");
asm("NOP");
asm("NOP");
asm("NOP");
asm("FCLR I")
```

Set interrupt request level of the interrupt used to exit wait mode.

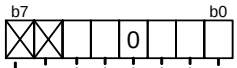


Interrupt Control Register

TA0IC to TA4IC, TB0IC to TB5IC, S0TIC to S8TIC, S0RIC to S8RIC, BCN0IC to BCN6IC, DM0IC to DM3IC, AD0IC, KUPIC, IIO0IC to IIO11IC, I2CIC, I2CLIC, C0FTIC to C1FTIC, C0FRIC to C1FRIC, C0TIC to C1TIC, C0RIC to C1RIC, C0EIC to C1EIC, C0WIC to C1WIC

ILV2 to ILV0	Interrupt Reqeust Level Select Bit Select the level.
IR	Interrupt Request Flag 0: No interrupt requested
b7 to b4	Set to 0

Set the IR bit to 0.



Interrupt Control Register (INT0IC to INT8IC)

ILV2 to ILV0	Interrupt Request Level Select Bit Select the level.
IR	Interrupt Request Flag 0: No interrupt requested
POL	Polarity Switch Bit 0: Select the falling edge or a low level signal 1: Select the rising edge or a high level signal
LVS	Level Sense/Edge Sense Switch Bit 0: Edge sense 1: Level sense
b7 to b4	Set to 0

Set the IR bit to 0.

Set the IPL.

```
asm("LDIPL #3")
```

Set wake-up interrupt priority level to same value as IPL.

Interrupt request level of the interrupt used to exit wait mode > IPL = Interrupt priority level for resuming.

Continued on next page

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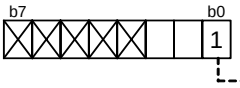
Change the current operation mode to another to move to wait mode.
Low speed mode, low power mode, or PLL self-oscillation mode can be used.
When using the oscillation stop function, disable the oscillation stop detection function after making the settings below.
Set the CM20 bit to 0 before stopping the main clock.

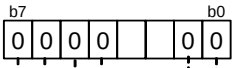
When the oscillation stop function is used:



Protect Register (PRCR)

PRC0 — Protect Bit 0

1: Write enabled for registers CM0, CM1, CM2, and PM3

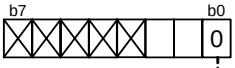


Oscillator Stop Detection Register (CM2)

CM20 — Oscillator Stop Detection Enable Bit
0: Disabled

b1 — Set to 0.

b7 to b4 — Set to 0.



Protect Register (PRCR)

PRC0 — Protect Bit 0

0: Write enabled for registers CM0, CM1, CM2, and PM3

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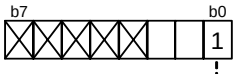
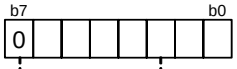
Set interrupt request level of the interrupt used to exit wait mode.



Protect Register (PRCR)

PRC0 Protect bit 0

1: Write enabled for registers CM0, CM1, CM2, and PM3



System Clock Control Register 0 (CM0)

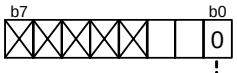
CM02 WAIT peripheral function clock stop bit

0: Do not stop peripheral function clock in wait mode

1: Stop peripheral function clock in wait mode

Set to 0.

When the PM21 bit in the PM2 register is set to 1, the CM02 bit is not changed by a write operation.



Protect Register (PRCR)

Set the PRC0 bit to 0 (write disabled) after this bit is set to 1 (write enabled).

PRC0 Protect bit 0

0: Write disabled for registers CM0, CM1, CM2, and PM3

Set the I flag to 1.
asm("FSET 1")

Execute the WAIT instruction.
asm("WAIT")

Wait mode

← Source for interrupt wake-up generated

After wake-up, set wake-up interrupt priority level to 7.

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.

5.1 Explanation

In the sample program, after exiting low speed mode in which the sub clock is used, the MCU enters low-power mode. From that point on, the MCU repeatedly enters and, by using a timer A1 interrupt, exits wait mode. This program is based on the assumption that the sub clock is used.

Refer to the hardware manual for more information on the settings to enter low speed mode and sub clock oscillation.

Table 5.1 lists Clock Operation in Low speed Mode, Low Power Mode, and Wait Mode
Table 5.2 lists Timer A1 Settings
Table 5.3 lists Priority Level of Interrupt Used for Wake-up and IPL Settings
Figure 5.1 shows Sample Program Mode Change
Figure 5.2 shows Sample Program Operation

Table 5.1 Clock Operation in Low speed Mode, Low Power Mode, and Wait Mode

Clock	Low Speed Mode	Low Power Mode	Wait Mode
Main clock	Oscillated	Stopped	
Sub clock	Oscillated		
On-chip oscillator	Stopped		
PLL clock	Oscillated	Stopped	
Base clock	Sub clock		
Peripheral function clock	All oscillated	Only fC32 oscillated	

Table 5.2 Timer A1 Settings

Operating Mode	Count Source Division Ratio	Count Source
Timer mode	1024	fC32 (1.024 kHz)

Table 5.3 Priority Level of Interrupt Used for Wake-up and IPL Settings

Set interrupt request level of the interrupt used to exit wait mode	IPL
7	3

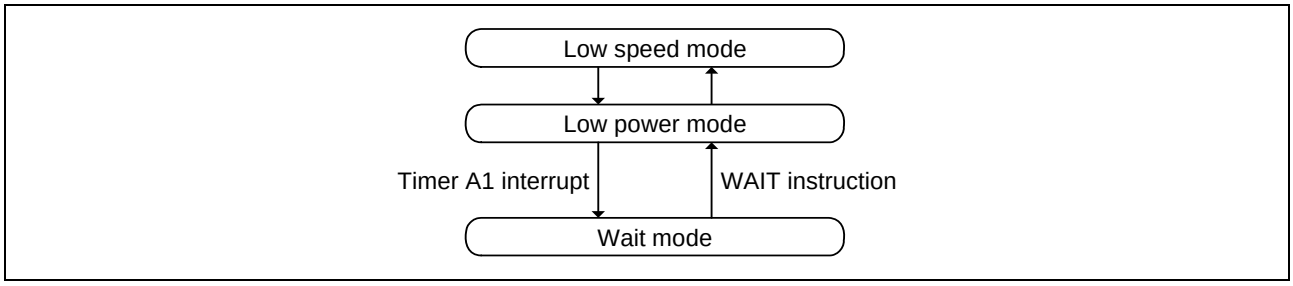


Figure 5.1 Sample Program Mode Change

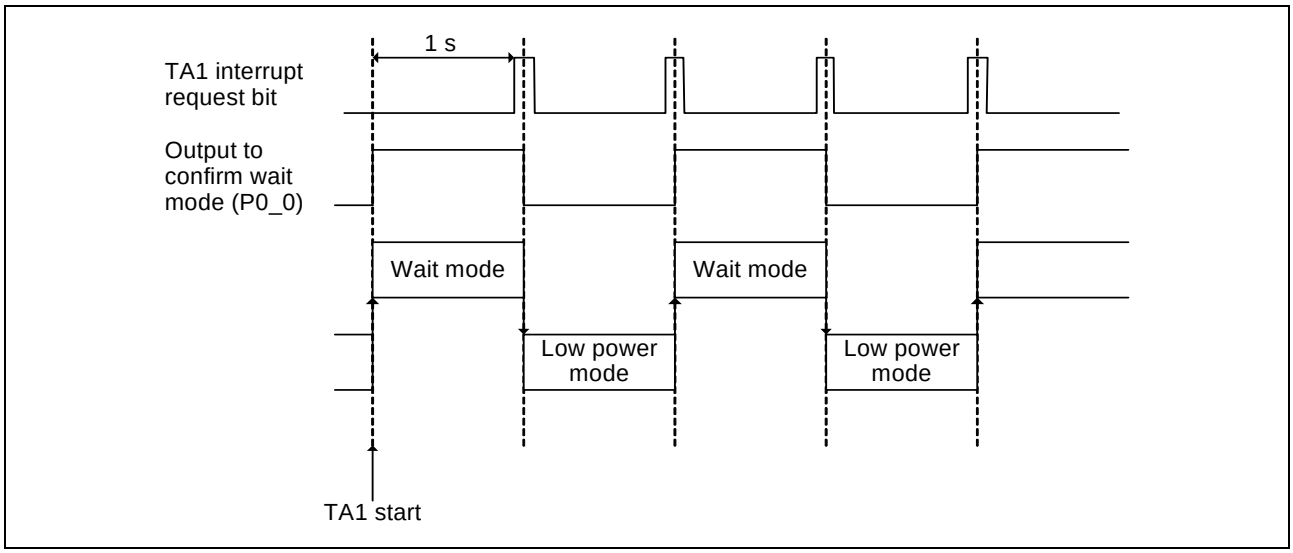


Figure 5.2 Sample Program Operation

5.2 Program Flow

The sample program is composed solely of a main function.
Figure 5.3 shows the Main Function Flowchart, Figure 5.4 shows the Wait Mode Transition Flowchart and Figure 5.5 shows the Exit Wait Mode Flowchart.
Items in parenthesis correspond to flow numbers in the sample program: (a) to (d) in Figure 5.3, (1) to (14) in Figure 5.4, and (1) to (6) in Figure 5.5.

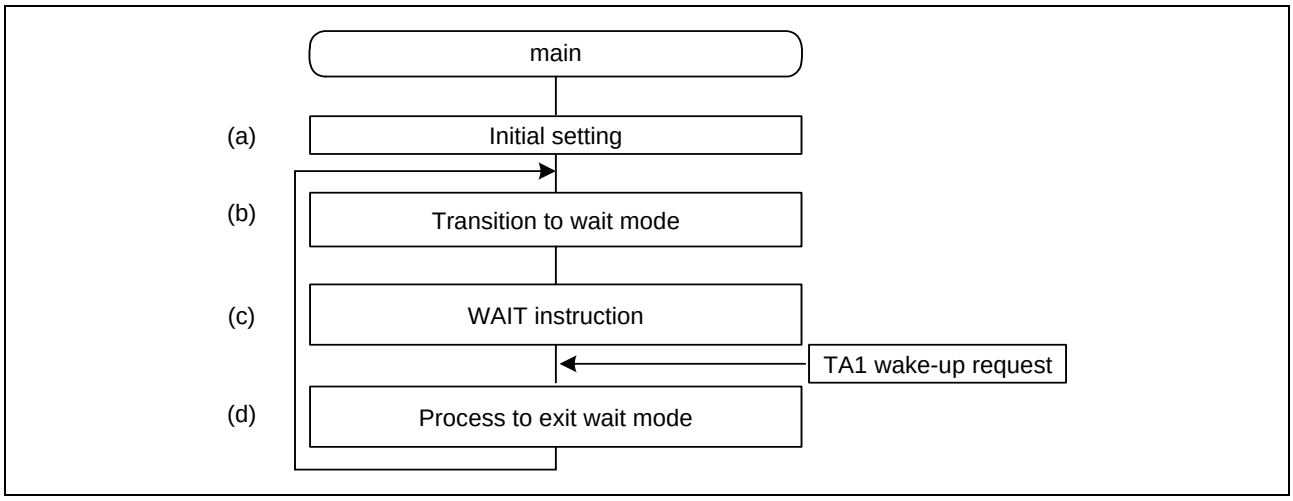


Figure 5.3 Main Function Flowchart

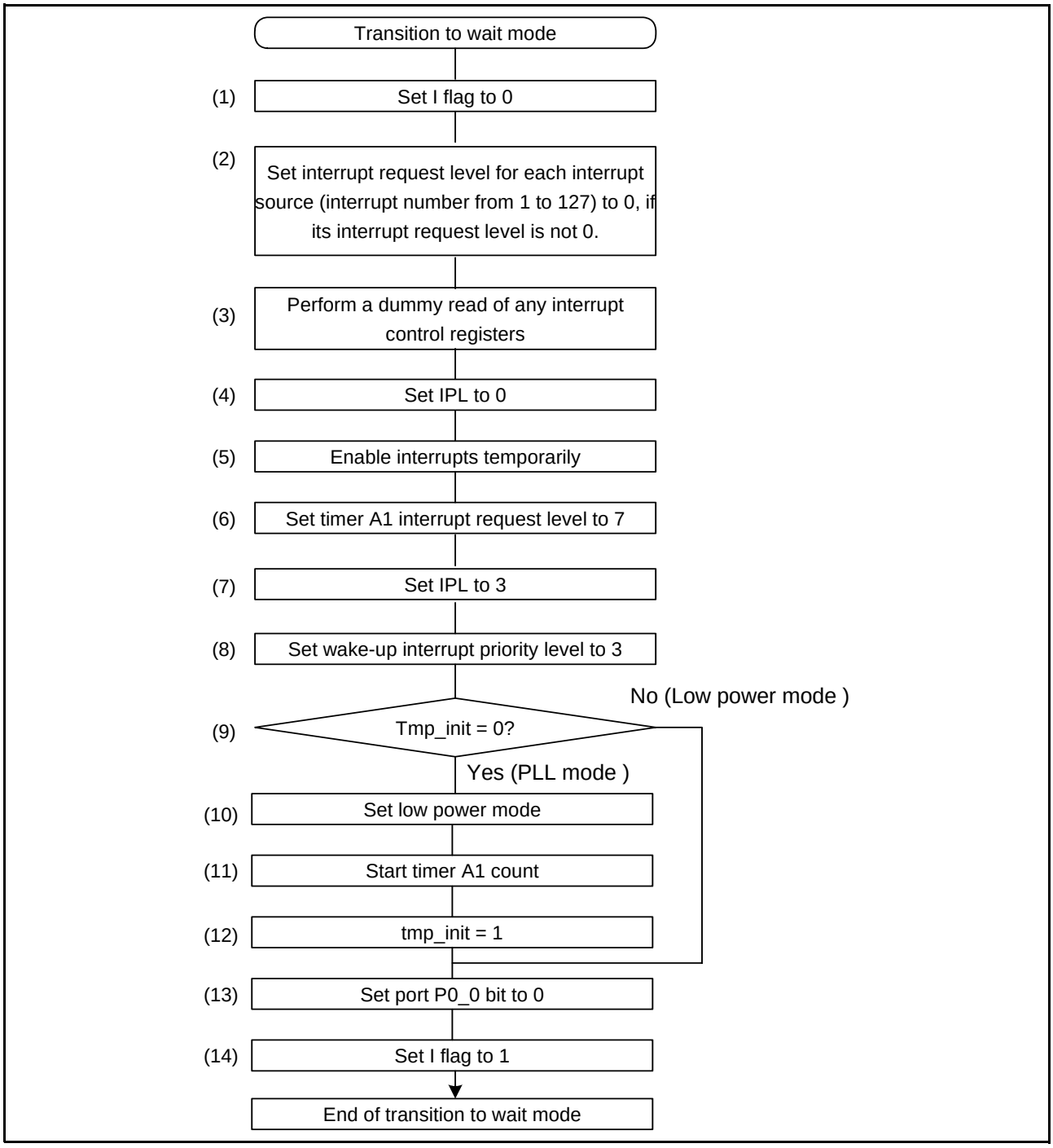


Figure 5.4 Wait Mode Transition Flowchart

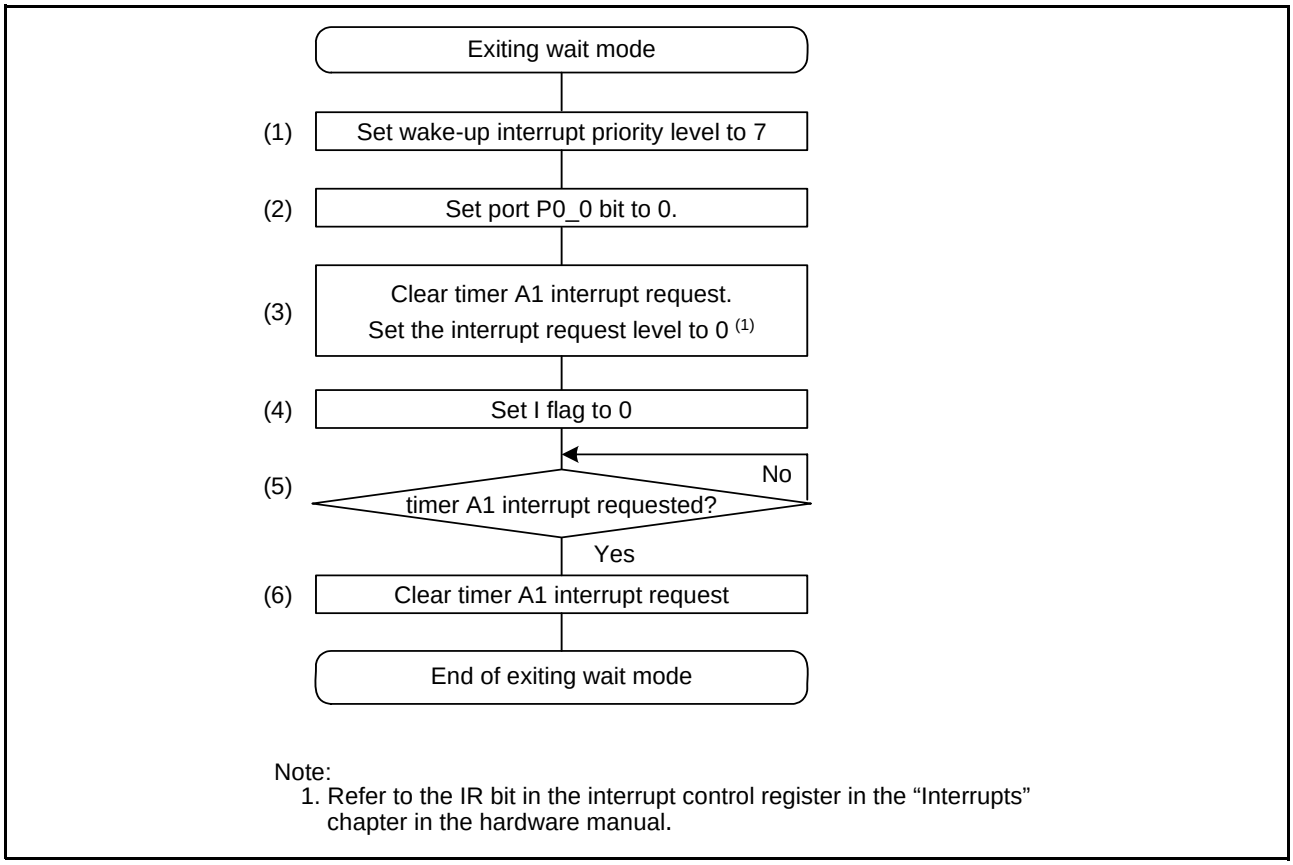


Figure 5.5 Exit Wait Mode Flowchart

6. Reference Documents

Hardware Manual: R32C/118 Group Hardware Manual Rev. 1.00
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

C Compiler Manual: R32C/100 Series C Compiler Ver. 1.02 User's Manual Rev. 1.00
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Revision History	Configuring Wait Mode

Revision	Date	Page	Summary
1.00	Feb. 26, 2010	—	Initial release

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