RX Family

Comparison of the Differences Among the RSCAN, CAN, and CAN FD modules

Introduction

This application note is a reference material for confirming the differences among the following modules: the RSCAN module of the RX140 Group, the CAN module of the RX671 Group, and the CAN FD module of the RX26T Group. The differences covered include general differences and register differences.

Target Devices

RX Family

When applying this application note to another MCU, make modifications according to the specifications of that MCU, and then perform careful evaluation.

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1. Comparison of Differences Between the CAN Module and the CAN FD Module

1.1 Comparison of General Differences

Table 1.1 shows Comparison of General Differences Between the CAN Module and the CAN FD Module.

Table 1.1 Comparison of General Differences Between the CAN Module and the CAN FD Module

Item	CAN	CAN FD
Protocol	Conforming to the ISO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (CAN) Data transfer rate (CAN FD)	The bit rate can be programmed at a maximum of 1 Mbps (fCAN ≥ 8 MHz). — fCAN: CAN clock source	• Arbitration phase: 1 Mbps, max. • Data phase: 8 Mbps, max. *1
Operating frequency	PCLKB: 60 MHz, max. CANMCLK: 24 MHz, max.	• Register block: 60 MHz, max. (PCLKB) • Message buffer RAM: 120 MHz, max. (PCLKA)
Operating clock for the data link layer (DLL clock)	—	60 MHz, max. (selectable from CANFDMCLK and CANFDCLK)
Message box (CAN) Message buffer (CAN FD)	32 mailboxes: Selectable from two mailbox modes • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. For the rest of mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	• Receive message buffer: 32 buffers • Transmit message buffer: 4 buffers • Transmit queue: 1 queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD *1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	CAN	CAN FD
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes *1
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field (data length) The protection function when the payload size is exceeded is provided. • Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Channel transmission interrupt can be enabled and disabled.

Item	CAN	CAN FD
FIFO	• 24 mailboxes can be configured for transmission or reception. • Of the other mailboxes, four FIFO stages can be configured for transmission and four FIFO stages for reception.	The FIFO size is programmable. • Receive FIFO queue: 2 queues • Common FIFO queue: 1 queue (Whether to use it as a receive or transmit FIFO queue can be selected.)
Automatic transmission interval adjustment	—	• Available when the common FIFO queue is configured as a transmit FIFO queue • The interval between messages sent from the FIFO queue can be adjusted.
Method of recovery from the bus-off state	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when the bus-off state starts. • The mode automatically changes to CAN Halt mode when the bus-off state ends. • The mode programmatically changes to CAN Halt mode. • The state programmatically changes to the Error Active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when the bus-off state starts. • Automatically enters CH_HALT mode when the bus-off state ends. • Enters CH_HALT mode by software (during the period of recovery from the bus-off state). • The state programmatically changes to the Error Active state.
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition among error states (the error warning state, error passive state, start of the bus-off state, and recovery from the bus-off state) can be detected. • The error counter can be read.	—
Timestamp function	• Timestamp function with a 16-bit counter • Number of bit times that can be selected for the reference clock: 1, 2, 4, or 8	Transmission and reception timestamp function
Interrupt function	• Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO receive interrupt Receive message buffer interrupt

Item	CAN	CAN FD
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support units • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback)
Low power consumption function (CAN) Power down function (CAN FD)	Ability to specify the module-stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to the module-stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

1.2 Comparison of Operating Modes

Table 1.2 shows Comparison of Operating Modes Between the CAN Module and the CAN FD Module.

Table 1.2 Comparison of Operating Modes Between the CAN Module and the CAN FD Module

CAN	CAN FD	
CAN reset mode	Channel modes	CH_RESET mode
CAN Halt mode		CH_HALT mode
CAN sleep mode		CH_SLEEP mode
CAN operation mode (not in the bus-off state)		CH_OPERATION mode (not in the bus-off state)
CAN operation mode (in the bus-off state)		CH_OPERATION mode (in the bus-off state)
—	Global modes	GL_SLEEP mode
—		GL_RESET mode
—		GL_HALT mode
—		GL_OPERATION mode

1.3 Comparison of Register Differences

Table 1.3 shows Comparison of Register Differences Between the CAN Module and the CAN FD Module.

Table 1.3 Comparison of Register Differences Between the CAN Module and the CAN FD Module

Register	Bit	CAN	CAN FD
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison registers 0 and 1	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 31)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register

Register	Bit	CAN	CAN FD
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFO n status register (n = 0, 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0

Register	Bit	CAN	CAN FD
TMIER0	—	—	Transmit message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2. Comparison of Differences Between the RSCAN Module and the CAN FD Module

2.1 Comparison of General Differences

Table 2.1 shows Comparison of General Differences Between the RSCAN Module and the CAN FD Module.

Table 2.1 Comparison of General Differences Between the RSCAN Module and the CAN FD Module

Item	RSCAN	CAN FD
Protocol	Conforming to the ISO 11898-1 standard	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RSCAN) Data transfer rate (CAN FD)	1 Mbps, max.	Arbitration phase: 1 Mbps, max. Data phase: 8 Mbps, max. *1
Operating frequency	PCLKB: 40 MHz, max. CANMCLK: 20 MHz, max.	Register block: 60 MHz, max. (PCLKB) Message buffer RAM: 120 MHz, max. (PCLKA)
Operating clock for the data link layer (DLL clock)	—	60 MHz, max. (either CANFDMCLK or CANFDCLK can be selected)
Buffer (RSCAN) Message buffer (CAN FD)	A total of 20 buffers • Channel-specific buffer: 4 buffers (per channel) Transmit buffer: 4 buffers per channel • Channel-shared buffer: 16 buffers Receive buffer: 0 to 16 buffers Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)	• Transmit message buffer: 4 buffers • Transmit queue: 1 queue Automatic transfer of messages to the transmit queue is supported. • Receive message buffer: 32 buffers
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD *1 • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RSCAN	CAN FD
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Interrupts can be enabled or disabled for each FIFO buffer. • Mirror function (to receive messages transmitted from the own CAN node) • Time stamp function (recording of 16-bit timer value indicating time message received)	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes *1
Receive filter function (RSCAN) Acceptance filter (CAN FD)	• Receive messages can be selected according to 16 receive rules. • The number of receive rules (0 to 16) can be set for each channel. • Acceptance filter processing: ID and mask can be set for each receive rule. • DLC filter processing: A DLC check value can be set for each receive rule.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Receive message transfer function	• Routing function A function that transfers received messages to arbitrary destination buffers (Maximum number of destination buffers: 2) Transfer destination: Receive buffer, receive FIFO buffer, and transmit/receive FIFO buffer • Label addition function Label information can be stored together when storing a message in a receive buffer and FIFO buffer.	—

Item	RSCAN	CAN FD
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or transmit buffer number priority transmission mode can be selected. • Transmission can be aborted. (Completion of abort can be confirmed with a flag.) • Interrupt can be enabled or disabled individually for each transmit buffer and for each transmit/receive FIFO buffer.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted. (Completion of abort can be confirmed with a flag.) • Channel transmission interrupts can be enabled or disabled.
FIFO	• Receive FIFO buffer: 2 FIFO buffers (up to 16 buffers allocatable to each) • Transmit/receive FIFO buffer: A FIFO buffer per a channel (up to 16 buffers allocatable to each)	The FIFO size is programmable. • Receive FIFO buffer: 2 FIFO buffers • Common FIFO buffer: 1 FIFO buffer (Whether to use the FIFO buffer as a receive FIFO buffer or transmit FIFO buffer can be selected.)
Interval transmission function (RSCAN) Automatic transmission interval adjustment (CAN FD)	The message transmission interval time can be set. (transmit mode of transmit/receive FIFO buffers)	Available when the common FIFO queue is configured as a transmit FIFO queue The interval between messages sent from the FIFO queue can be adjusted.
Transmit history function	Stores the history information of transmitted messages.	—

Item	RSCAN	CAN FD
Method of recovery from the bus-off state	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to channel halt mode when the bus-off state starts. • The mode automatically changes to channel halt mode when the bus-off state ends. • The mode programmatically changes to channel halt mode. • The mode programmatically changes to the Error Active state (forcible recovery from the bus-off state).	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when the bus-off state starts. • Automatically enters CH_HALT mode when the bus-off state ends. • Enters CH_HALT mode by software (during the period of recovery from the bus-off state). • The state programmatically changes to the Error Active state.
Timer	Time stamp function (recording of 16-bit timer value indicating time message received)	Transmission and reception timestamp function
Interrupt function	• Global (2 sources) — Global receive FIFO interrupt — Global error interrupt • Channel (3 sources/channel) — Channel transmission interrupt Transmit complete interrupt Transmit abort interrupt Transmit/receive FIFO transmit complete interrupt Transmit history interrupt — Channel error interrupt — Transmit/receive FIFO receive interrupt	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO receive interrupt Receive message buffer interrupt
Software support	—	Label information is automatically added to received messages.
Test modes	Test function for user evaluation • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback) • RAM test (read/write test)	• Basic test mode • Listen-only mode • Self-test mode 0 (external loopback mode) • Self-test mode 1 (internal loopback mode)
Low power consumption function (RSCAN) Power down function (CAN FD)	Ability to specify the module-stop state	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Ability to transition to the module-stop state
RAM	—	RAM with ECC protection

Note: 1. This is only available for products that support the CAN FD protocol.

2.2 Comparison of Operating Modes

Table 2.2 shows Comparison of Operating Modes Between the RSCAN Module and the CAN FD Module.

Table 2.2 Comparison of Operating Modes Between the RSCAN Module and the CAN FD Module

RSCAN		CAN FD	
Channel modes	Channel reset mode	Channel modes	CH_RESET mode
	Channel halt mode		CH_HALT mode
	Channel stop mode		CH_SLEEP mode
	Channel communication mode (not in the bus-off state)		CH_OPERATION mode (not in the bus-off state)
	Channel communication mode (in the bus-off state)		CH_OPERATION mode (in the bus-off state)
Global modes	Global stop mode	Global modes	GL_SLEEP mode
	Global reset mode		GL_RESET mode
	Global test mode		GL_HALT mode
	Global operation mode		GL_OPERATION mode

2.3 Comparison of Register Differences

Table 2.3 shows Comparison of Register Differences Between the RSCAN Module and the CAN FD Module.

Table 2.3 Comparison of Register Differences Between the RSCAN Module and the CAN FD Module

Register	Bit	RSCAN	CAN FD
CFGL	—	Bit configuration register L	—
CFGH	—	Bit configuration register H	—
CTRL	—	Control register L	—
CTRH	—	Control register H	—
STSL	—	Status register L	—
STSH	—	Status register H	—
ERFLL	—	Error flag register L	—
ERFLH	—	Error flag register H	—
GCFGL	—	Global configuration register L	—
GCFGH	—	Global configuration register H	—
GCTRL	—	Global control register L	—
GCTRH	—	Global control register H	—
GSTS	—	Global status register	—
GERFLL	—	Global error flag register	—
GTINTSTS	—	Global transmit interrupt status register	—
GTSC	—	Timestamp register	—
GAFLCFG	—	Receive rule number configuration register	—
GAFLIDLj	—	Receive rule entry register jAL (j = 0 to 15)	—
GAFLIDHj	—	Receive rule entry register jAH (j = 0 to 15)	—
GAFLMLj	—	Receive rule entry register jBL (j = 0 to 15)	—
GAFLMHj	—	Receive rule entry register jBH (j = 0 to 15)	—
GAFLPLj	—	Receive rule entry register jCL (j = 0 to 15)	—
GAFLPHj	—	Receive rule entry register jCH (j = 0 to 15)	—
RMNB	—	Receive buffer number configuration register	—
RMND0	—	Receive buffer receive complete flag register	—
RMIDLn	—	Receive buffer register nAL (n = 0 to 15)	—
RMIDHn	—	Receive buffer register nAH (n = 0 to 15)	—
RMTSn	—	Receive buffer register nBL (n = 0 to 15)	—
RMPTRn	—	Receive buffer register nBH (n = 0 to 15)	—

Register	Bit	RSCAN	CAN FD
RMDF0n	—	Receive buffer register nCL (n = 0 to 15)	—
RMDF1n	—	Receive buffer register nCH (n = 0 to 15)	—
RMDF2n	—	Receive buffer register nDL (n = 0 to 15)	—
RMDF3n	—	Receive buffer register nDH (n = 0 to 15)	—
RFCCm	—	Receive FIFO control register m (m = 0, 1)	—
RFSTSm	—	Receive FIFO status register m (m = 0, 1)	—
RFPCTRm	—	Receive FIFO pointer control register m (m = 0, 1)	—
RFIDLm	—	Receive FIFO access register mAL (m = 0, 1)	—
RFIDHm	—	Receive FIFO access register mAH (m = 0, 1)	—
RFTSm	—	Receive FIFO access register mBL (m = 0, 1)	—
RFPTRm	—	Receive FIFO access register mBH (m = 0, 1)	—
RFDF0m	—	Receive FIFO access register mCL (m = 0, 1)	—
RFDF1m	—	Receive FIFO access register mCH (m = 0, 1)	—
RFDF2m	—	Receive FIFO access register mDL (m = 0, 1)	—
RFDF3m	—	Receive FIFO access register mDH (m = 0, 1)	—
CFCCL0	—	Transmit/receive FIFO control register 0L	—
CFCCH0	—	Transmit/receive FIFO control register 0H	—
CFSTS0	—	Transmit/receive FIFO status register 0	—
CFPCTR0	—	Transmit/receive FIFO pointer control register 0	—
CFIDL0	—	Transmit/receive FIFO access register 0AL	—
CFIDH0	—	Transmit/receive FIFO access register 0AH	—
CFTS0	—	Transmit/receive FIFO access register 0BL	—
CFPTR0	—	Transmit/receive FIFO access register 0BH	—
CFDF00	—	Transmit/receive FIFO access register 0CL	—

Register	Bit	RSCAN	CAN FD
CFDF10	—	Transmit/receive FIFO access register 0CH	—
CFDF20	—	Transmit/receive FIFO access register 0DL	—
CFDF30	—	Transmit/receive FIFO access register 0DH	—
RFMSTS	—	Receive FIFO message lost status register	—
CFMSTS	—	Transmit/receive FIFO message lost status register	—
RFISTS	—	Receive FIFO interrupt status register	—
CFISTS	—	Transmit/receive FIFO receive interrupt status register	—
TMCp	—	Transmit buffer control register p (p = 0 to 3)	—
TMSTSp	—	Transmit buffer status register p (p = 0 to 3)	—
TMTRSTS	—	Transmit buffer transmit request status register	—
TMTCSTS	—	Transmit buffer transmit complete status register	—
TMTASTS	—	Transmit buffer transmit abort status register	—
TMIEC	—	Transmit buffer interrupt enable register	—
TMIDLp	—	Transmit buffer register pAL (p = 0 to 3)	—
TMIDHp	—	Transmit buffer register pAH (p = 0 to 3)	—
TMPTRp	—	Transmit buffer register pBH (p = 0 to 3)	—
TMDF0p	—	Transmit buffer register pCL (p = 0 to 3)	—
TMDF1p	—	Transmit buffer register pCH (p = 0 to 3)	—
TMDF2p	—	Transmit buffer register pDL (p = 0 to 3)	—
TMDF3p	—	Transmit buffer register pDH (p = 0 to 3)	—
THLCC0	—	Transmit history buffer control register	—
THLSTS0	—	Transmit history buffer status register	—
THLACC0	—	Transmit history buffer access register	—
THLPCTR0	—	Transmit history buffer pointer control register	—
GRWCR	—	Global RAM window control register	—
GTSTCFG	—	Global test configuration register	—
GTSTCTRL	—	Global test control register	—
GLOCKK	—	Global test protection unlock register	—
RPGACCr	—	RAM test register r (r = 0 to 127)	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register

Register	Bit	RSCAN	CAN FD
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0, 1)
RFSRn	—	—	Receive FIFO n status register (n = 0, 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0, 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)

Register	Bit	RSCAN	CAN FD
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	Transmit message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GFDCFG	—	—	Global CAN FD configuration register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

3. Reference Documents

User's Manuals: Hardware

RX671 Group User's Manual: Hardware (R01UH0899EJ)
RX140 Group User's Manual: Hardware (R01UH0905EJ)
RX26T Group User's Manual: Hardware (R01UH0979EJ)

If you use a product of a group for which none of the above manuals are applicable, refer to the applicable hardware manual ("User's Manual: Hardware" for the relevant group).
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.28.23	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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