Implementing an Analog Clock with SLG47003V

SLG47003V

This application note describes how to use the Renesas SLG47003V to implement an analog clock.

The application note comes complete with a design file that can be found in the Reference section.

Contents

1. Terms and Definitions

ACMP	Analog Comparator
CNT/DLY	Counter-Delay
DFF	D Flip-flop
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
LDR	Light-dependent resistor
LED	Light Emitting Diode
LUT	Look-up Table
MF	Multi-function Macrocell
OSC	Oscillator
PCB	Printed Circuit Board

2. References

For related documents and software, please visit:

SLG47003 - AnalogPAK Programmable Mixed-Signal IC, VDD Range: 2.3-5.5V, 15 GPIOs, 1 ACMPs, 2 Op Amps, 2 Rheostats, I2C | Renesas

Download our free Go Configure Software Hub [1] to open the .aap files [2] and view the proposed circuit design. Use the AnalogPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-424 Implementing an Analog Clock with SLG47003V.aap, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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3. Introduction

The Analog Clock is a timekeeping device that uses analog measuring instruments (microammeters) to display time.

An ammeter, typically used to measure electric current, can be designed with an analog display resembling a clock face, where the needle movement indicates current levels instead of time. These "analog ammeters" often use a moving coil, moving magnet, moving iron, or electrodynamic mechanism to deflect a needle across a calibrated scale, showing current flow.

Figure 1. Visual Example and Time Representation on the Analog Clock

In this application note, we will explore the implementation of an Analog Clock using AnalogPAK SLG47003V chips. The SLG47003V combines analog and digital functionality in a compact, low-power package, making it ideal for a wide range of embedded applications.

Any electronic clock consists of the following essential building blocks:

- A stabilized pulse generator (Crystal Oscillator 32768 Hz)
- A divide-by-32768 circuit / seconds pulse generator
- A divide-by-60 circuit / seconds counter
- A divide-by-60 circuit / minutes counter
- A divide-by-24 circuit / hours counter
- Time setting and control circuitry

To be able to read time from an analog microammeter, we need to extend the basic building blocks of the electronic clock with additional modules that will convert digital signals into a stepwise-changing voltage.

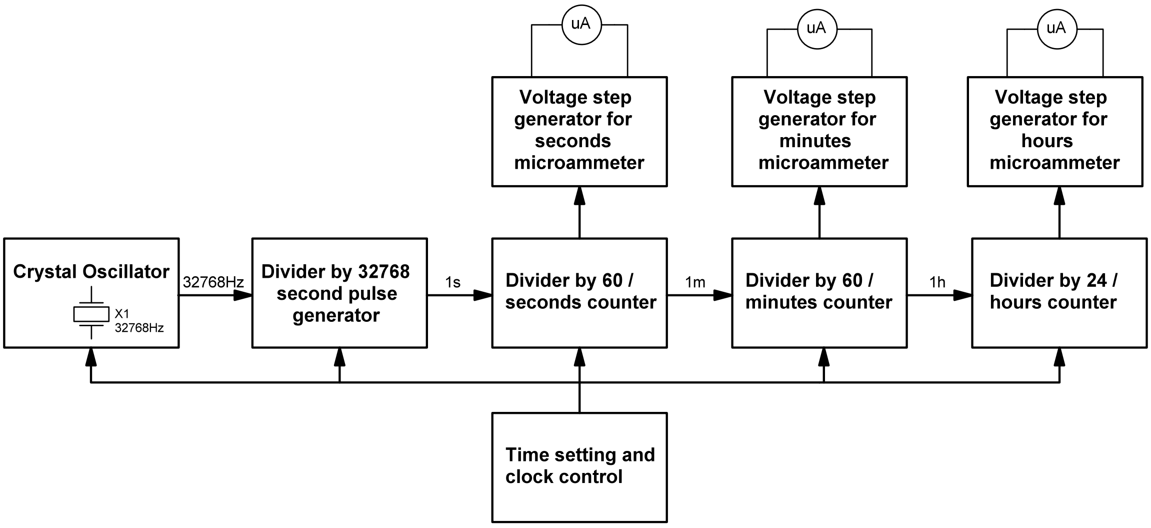


Figure 2. Analog Clock Block Diagram

4. The Design

4.1 Circuit Design

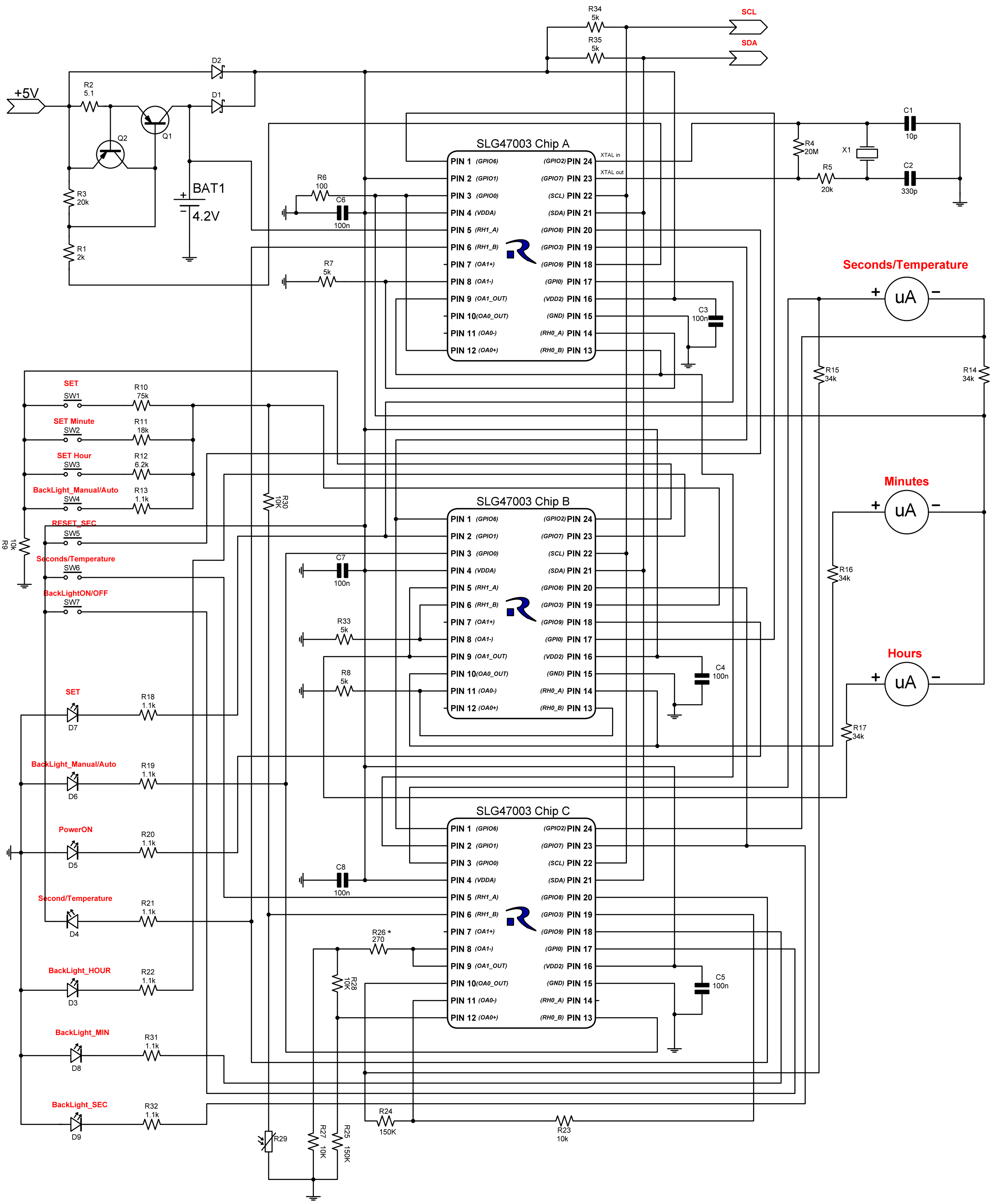


Figure 3. Analog Clock Electrical Schematic

Clock Features

The Analog Clock is built using three SLG47003V chips and provides the following functionalities:

- Timekeeping with hour, minute, and second indication using three analog ammeters.
- Ambient temperature measurement (range: 10 °C to 40 °C) using the chip's internal temperature sensor, with the measured temperature displayed via the analog ammeter normally used for seconds.
- Backlight control for the microammeters, operable in manual or automatic mode (based on a photoresistor signal).
- Battery charging management for the backup power supply.

Clock Control and User Interface

The clock is operated using seven buttons:

- **SET** – enters time setting mode.
- **Set Minutes** – adjusts the minutes value.
- **Set Hours** – adjusts the hours value.
- **RESET_SEC** – resets the seconds counter.
- **Second/Temperature** – toggles between time and temperature display.
- **BackLight ON/OFF** – controls backlight activation.
- **BackLight Manual/Auto** – switches between manual and automatic backlight modes.

Switching to temperature measurement mode is triggered by a short press of the Second/Temperature button. An LED labeled "Second/Temperature" indicates the active temperature mode.

The backlight (LEDs "BackLight_HOUR", "BackLight_MIN", "BackLight_SEC") is activated by a long press of the BackLight ON/OFF button. Brightness has four levels and can be adjusted with short presses of the same button.

In automatic mode, brightness adjusts based on ambient light intensity detected by a photoresistor. Switching between manual and automatic modes is done via the BackLight Manual/Auto button.

The clock is powered by a 5 V main power source and includes a 4.2 V backup battery. When operating on battery power, the display and backlight are disabled to conserve energy. The "PowerON" LED indicates main power operation and turns off when the main power is lost.

The clock circuitry also monitors the battery charging voltage and disables charging when the battery reaches 4.2 V.

To set the time:

- Hold the **SET** button for ~0.5 seconds to enter time setting mode (indicated by the **"SET"** LED).
- Time setting mode pauses the seconds counter.
- Use **Set Minutes** and **Set Hours** to adjust the time (only incrementing is available).
- Use **RESET_SEC** to reset the seconds.
- To exit time setting mode and resume normal operation, hold **SET** again for ~0.5 seconds.

Let's consider the designs in which this version of the clock is implemented.

On Chip A, the following are implemented:

- Crystal Oscillator.
- Divide-by-32768/second pulse generator.
- Divide-by-60 circuit / seconds counter.
- Second voltage step generator.
- Time setting and clock control (RESET_SEC, power source control).

On Chip B, the following are implemented:

- Divide-by-60 circuit / minutes counter.
- Minute voltage step generator.
- Divide-by-24 circuit / hours counter.
- Hour voltage step generator.
- Time setting and clock control (clock control button monitoring).

On Chip C, the following are implemented:

- Temperature measurement.
- Backlight control.
- Switching of the analog indicator “Second/Temperature”.

4.2 Design of Chip A for the Analog Clock

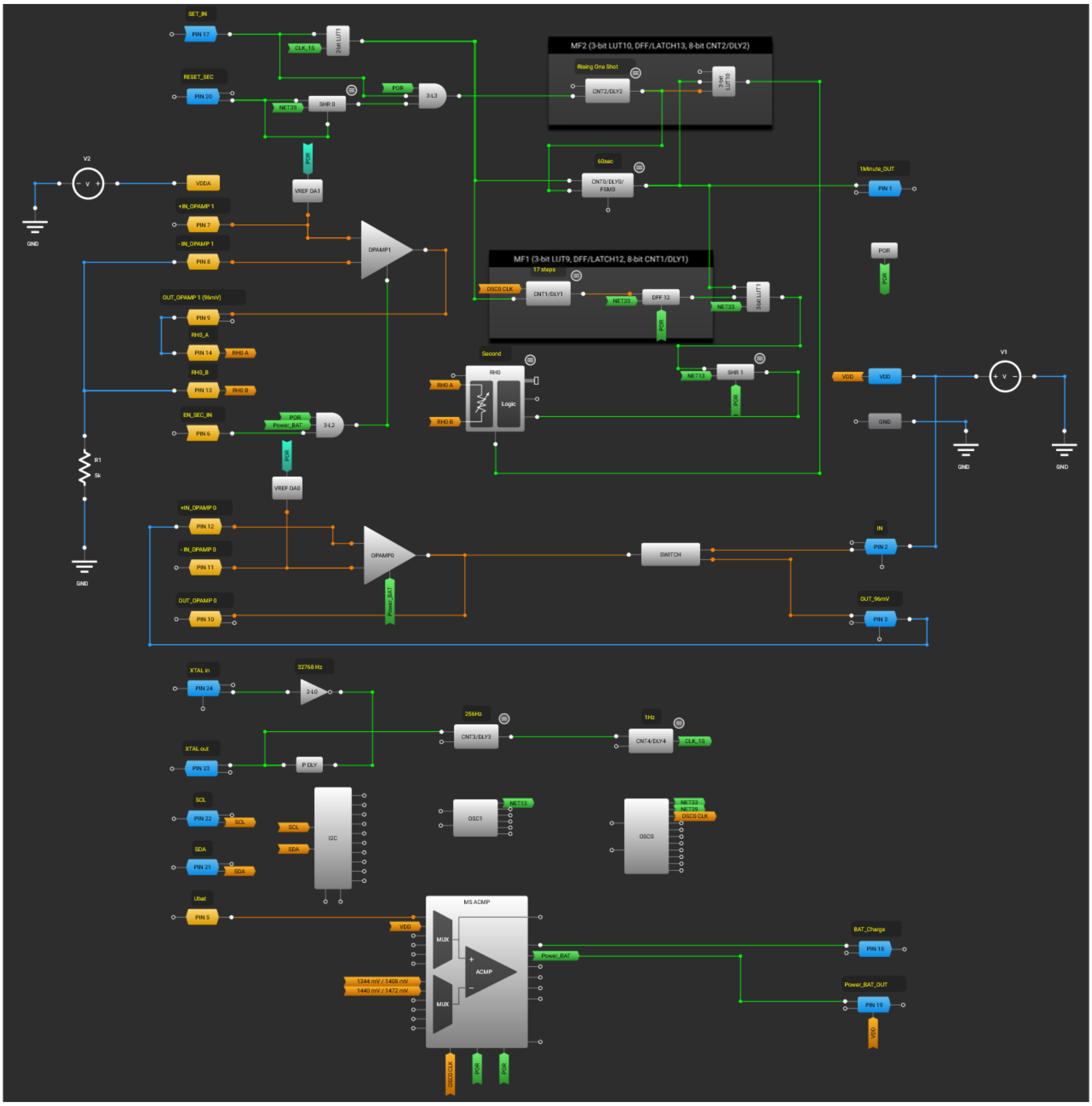


Figure 4. Design of Chip A for the Analog Clock

Crystal Oscillator

The stable pulse generator responsible for generating one-second timing pulses is built using the Crystal Oscillator module, which is specifically designed to operate with external quartz resonators.

Figure 5 shows the circuit configuration for connecting the quartz resonator. For this clock, we will use a standard "watch" quartz crystal resonator with a frequency of 32.768 kHz.

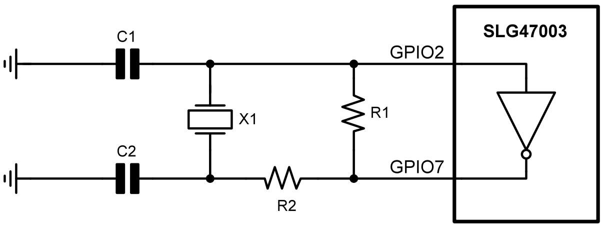


Figure 5. Circuit Diagram for Connecting the Quartz Resonator

Divide-by-32768/second pulse generator

To obtain stable one-second intervals, the 32.768 kHz frequency generated by the Crystal Oscillator needs to be divided by 32768. A 16-bit CNT1/DLY1/FSM1 is used as the divider, configured as a counter (see Figure 6).

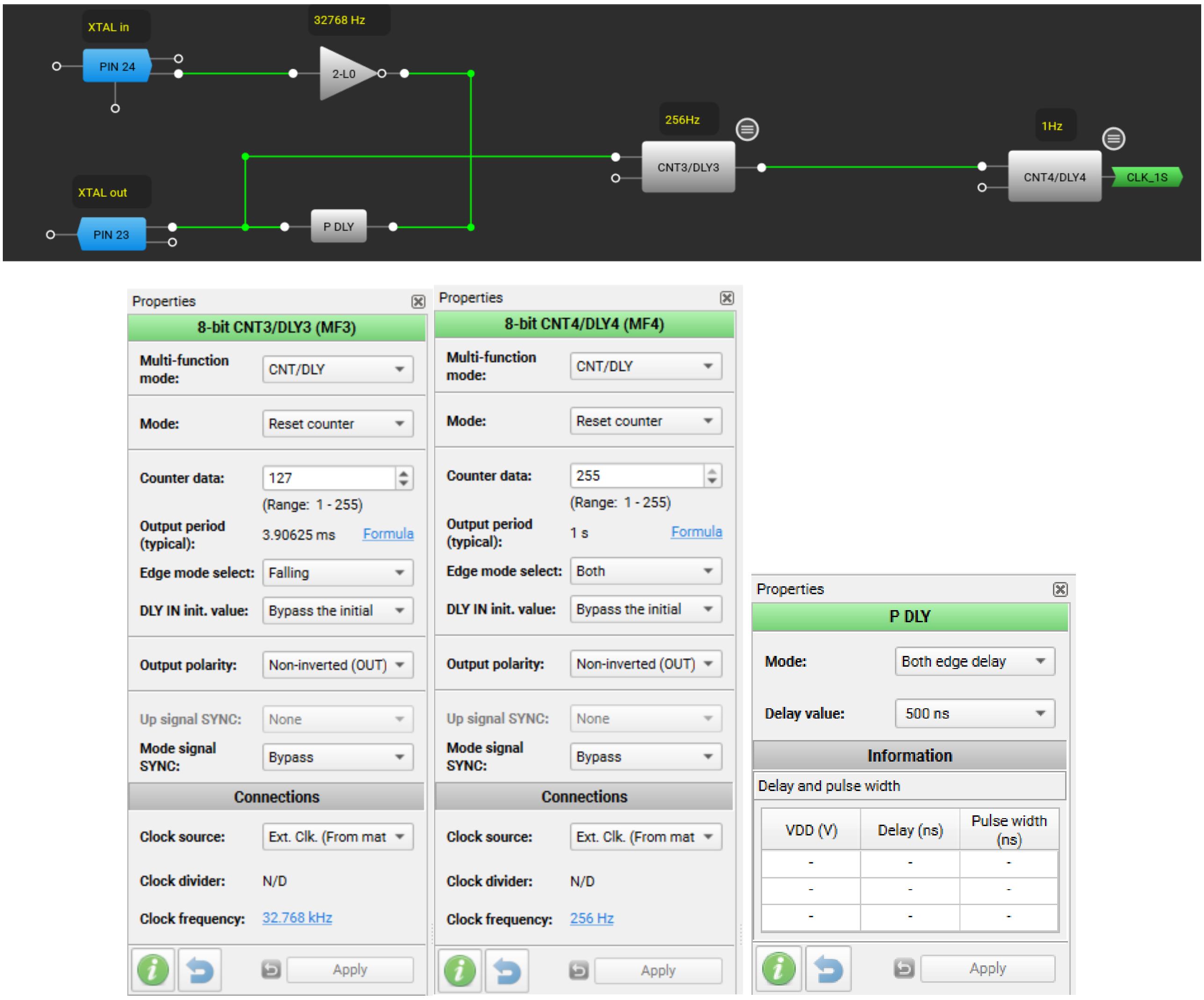


Figure 6. Second Pulse Generator and Configuration of CNT3, CNT4, P DLY

Divide by 60 / Seconds Counter

The conversion of seconds pulses into minutes pulses is handled by the Divide by 60 / seconds counter.

The Divide by 60 / seconds counter consists of an 8-bit CNT0/DLY0, which is configured as a divide-by-60 frequency divider (see Figure 7).

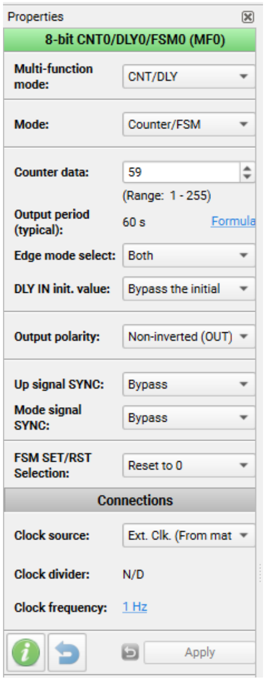


Figure 7. Settings for 8-bit CNT0/DLY0

Seconds voltage step generator

The voltage step generator in this design is built using OPAMP1, VREF OA1, digital rheostat RH0, 8-bit CNT1/DLY1, DFF12, 3-bit LUT1, and Shift Register1.

OPAMP1 is configured as a non-inverting amplifier, with its gain controlled by the digital rheostat RH0 (see Figure 8).

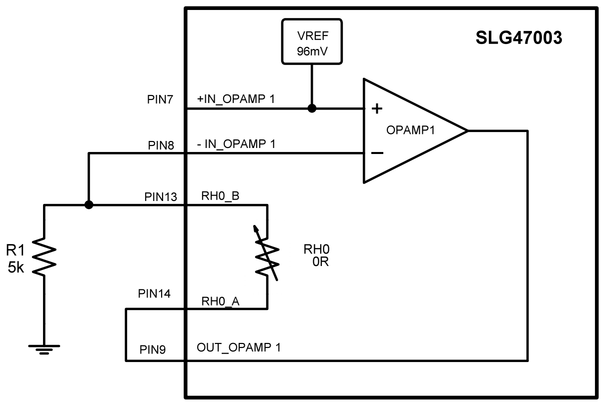


Figure 8. Circuit configuration of OPAMP1 as a step voltage generator

A stable voltage of 96 mV from VREF OA1 is applied to the +IN input of OPAMP1. Thus, OPAMP1 amplifies the input voltage with a gain coefficient equal to K. The gain coefficient is calculated by the formula:

$$K = 1 + \frac{RH0}{R1}$$

The digital rheostat RH0 has a maximum resistance of approximately 100 kΩ, and a minimum resistance close to 0 Ω. By varying the resistance of the digital rheostat from 0 to 100 kΩ, the gain of OPAMP1 (assuming R1 = 5 kΩ) changes from 1 to nearly 21. Accordingly, the output voltage of OPAMP1 will vary from 96 mV to approximately 2000 mV. By dividing the entire resistance range of the rheostat into 60 equal steps and increasing the resistance by 1/60 of its range every second, we can generate a stepwise increasing voltage at the output of OPAMP1.

The digital rheostat RH0 has 1023 switching steps. To utilize the rheostat's full range, RH0 must be incremented by 17 steps every second. This means that a burst of 17 pulses must be generated every second. The components 8-bit CNT1/DLY1, DFF12, and 3-bit LUT1 are responsible for generating this pulse burst (the configuration of these elements is shown in Figure 9).

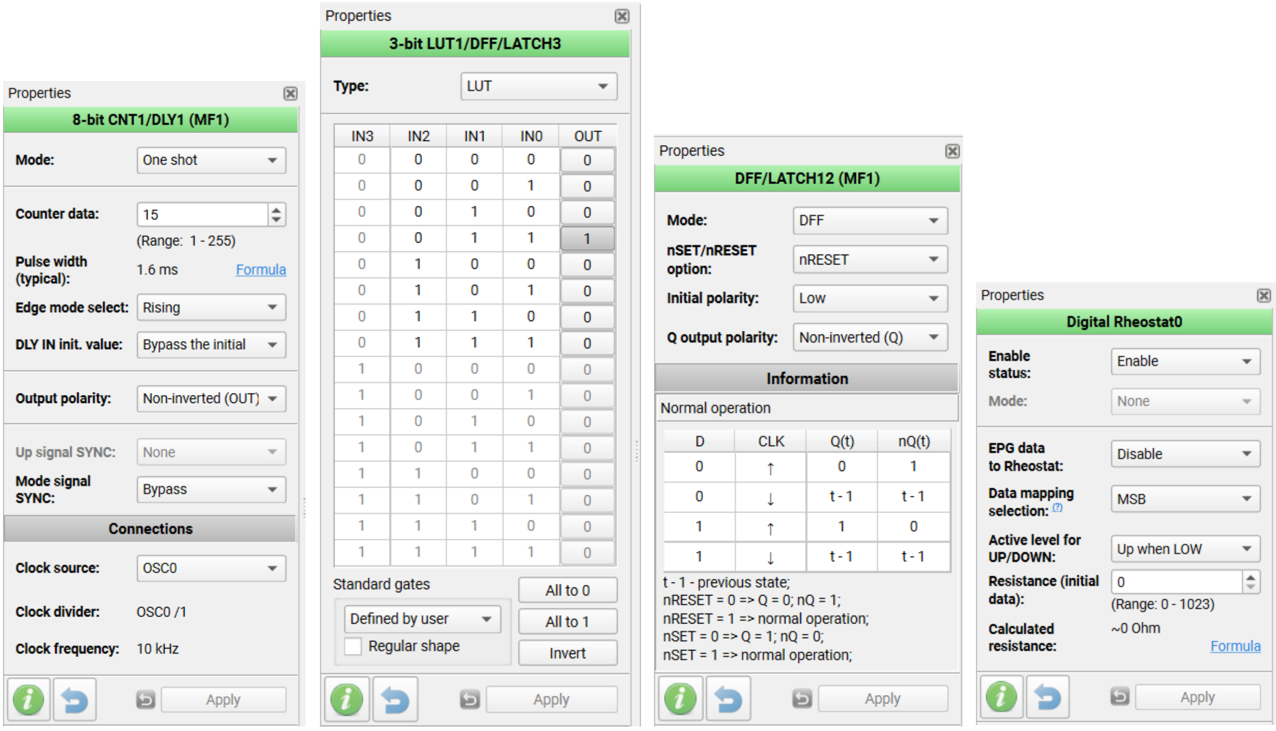
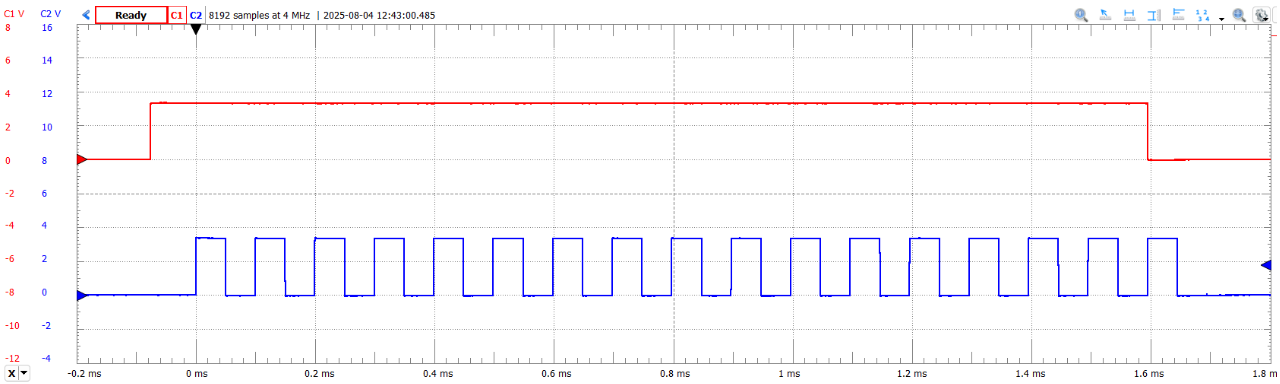


Figure 9. Settings for 8-bit CNT1/DLY1, DFF12, RH0 and 3-bit LUT1

The 8-bit CNT1/DLY1 generates a pulse of approximately 1.6 ms on each rising edge of the seconds pulses. DFF12 synchronizes this pulse with the clock pulses from OSC0, and using the 3-bit LUT1, the resulting pulse is filled with 17 clock pulses from OSC0 (see the oscilloscope waveform in Figure 10).



C1 (red) – 8-bit CNT1/DLY1 output
C2 (blue) – 3-bit LUT1 output

Figure 10. The pulse burst generation circuit waveform

After the resistance of RH0 has increased from 0 to its maximum value, it must be quickly reset back to the minimum. This is done using the Reload input of the RH0 rheostat. The initial value of RH0 is set to 0 (see Figure 9). CNT0/DLY0 and 3-bit LUT10 generate this signal at the beginning of each minute (when CNT0/DLY0 counts to 60). Shift Register1 introduces a slight delay to the clock pulses for RH0, ensuring that the Reload process completes before the next clock pulses arrive.

At the output of OPAMP1 we receive a cyclic step signal, which can be displayed using an analog microammeter (see Figure 11).

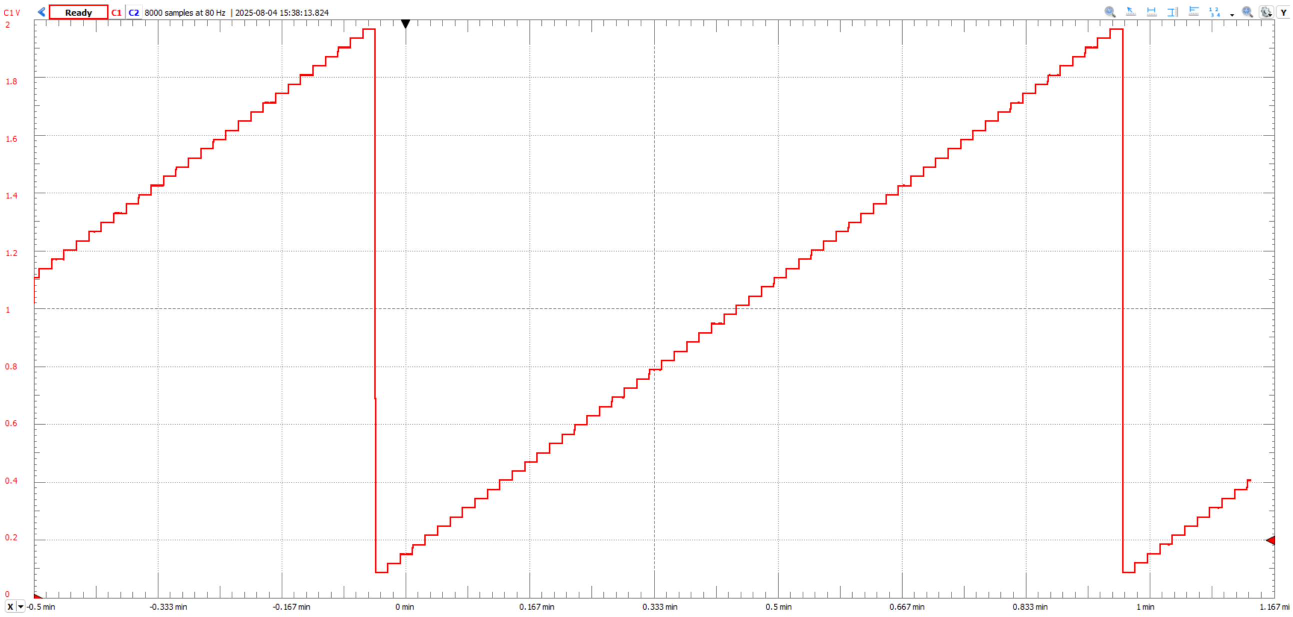


Figure 11. The seconds' step signal generation circuit waveform

The step voltage changes from 96 mV, so part of the microammeter scale will not be involved (the arrow will not return to the 0-scale mark); to remove this unwanted effect, the design uses a circuit on OPAMP0 and Analog SWITCH (see Figure 12). This circuit is a voltage stabilizer of which at the output we get a voltage of 96 mV. Thus, if we turn on the microammeter between the output of this stabilizer and the output of OPAMP1, this will compensate for the offset of the step voltage and the microammeter arrow will return to the zero-scale value.

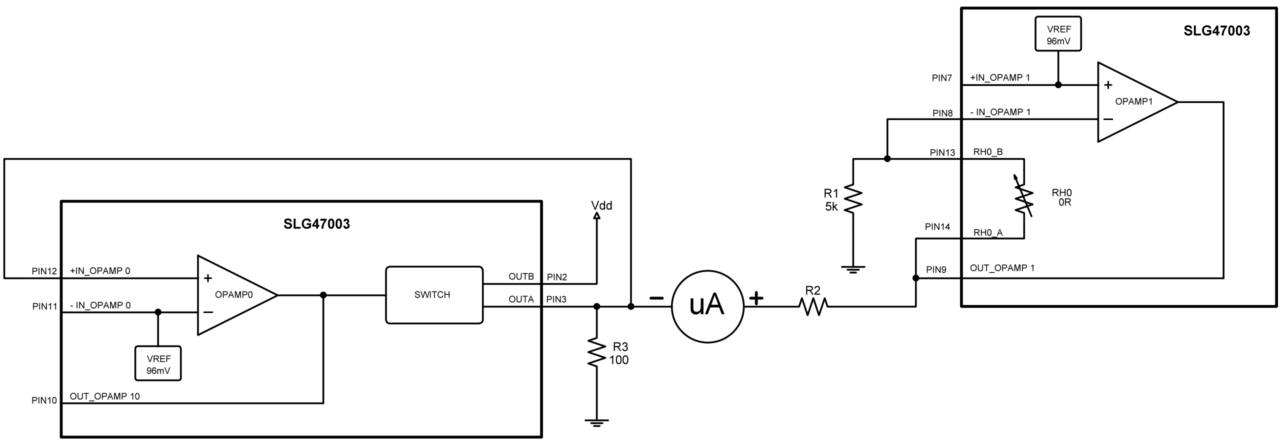


Figure 12. Circuit configuration for connecting the microammeter

Time Setting and Clock Control

Time setting and clock control refers to the processing of button signals, monitoring of power supply voltage levels, and monitoring the charge level of the backup battery (see Figure 13).

Shift Register0 functions as a debounce filter for the "RESET_SEC" button. Together with the configuration of PIN 20 as a digital input with Schmitt trigger and a pull-down resistor, this setup ensures protection against false triggering caused by contact bounce.

3-bit LUT3 and 8-bit CNT2/DLY2 are responsible for resetting the seconds value during time setting. 2-bit LUT1 blocks the passage of seconds pulses from the seconds pulse generator when the clock is in time-setting mode. The configuration of the elements responsible for handling the "RESET_SEC" button press is shown in Figure 14.

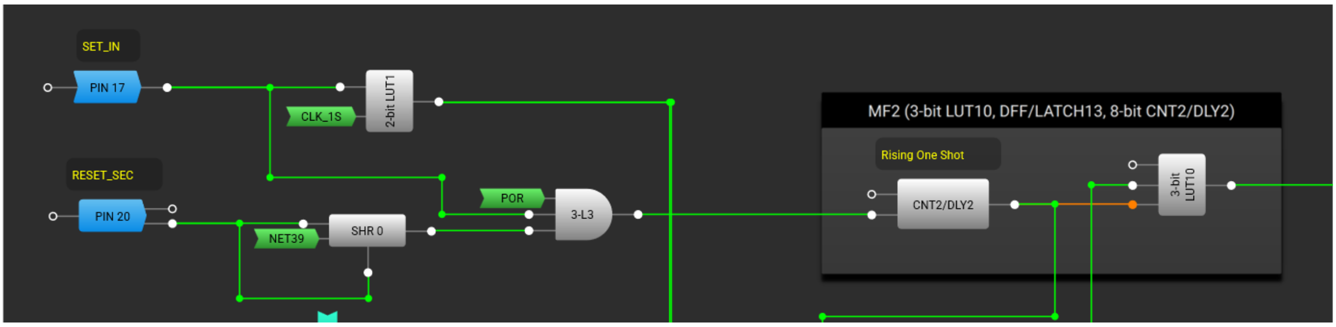


Figure 13. Part of the design responsible for button press handling

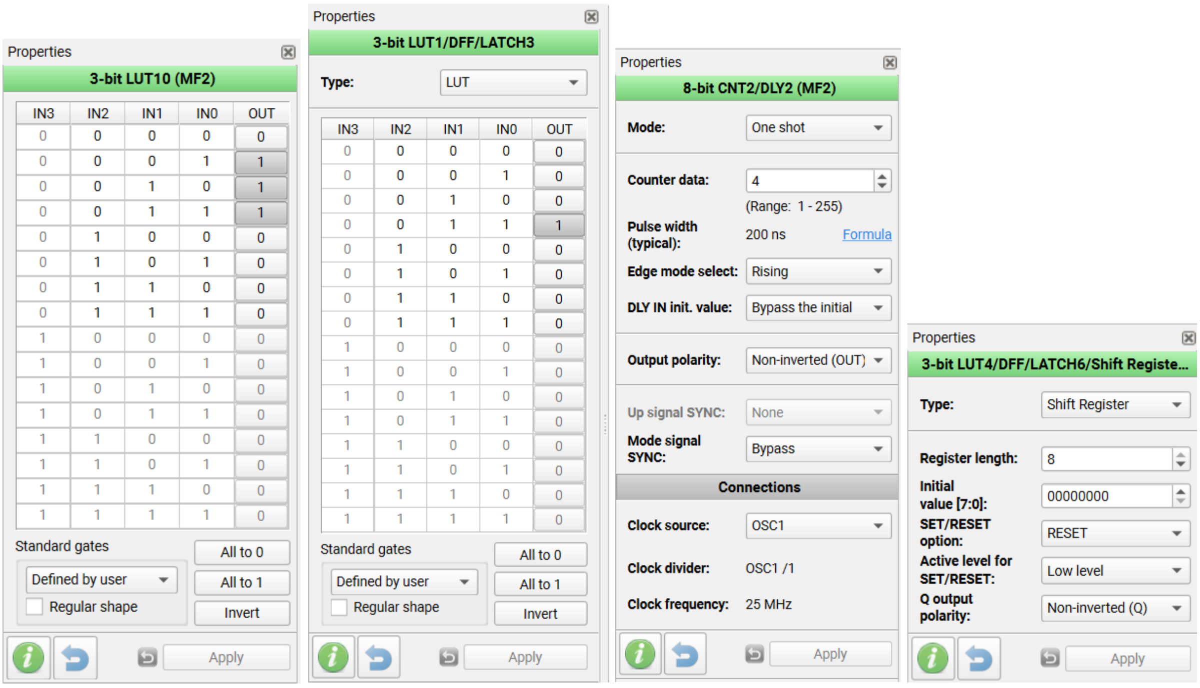


Figure 14. Configuration of the elements responsible for button press handling

The MS ACMP monitors the power supply voltage level (Channel 1, configuration shown in Figure 16) and the backup battery charge level (Channel 0).

When Vdd exceeds 4.4 V, the MS ACMP outputs a HIGH level on OUT_CH1. This HIGH level keeps the time display active on the clock as long as the supply voltage remains above 4.3 V, i.e., while the clock is connected to a stationary power source.

Channel 0 of the MS ACMP monitors the backup battery voltage level (configuration is shown in Figure 15). When the voltage exceeds 4.2 V, it outputs a HIGH level on OUT_CH0 which disables the external battery charging circuit and stops the charging process.

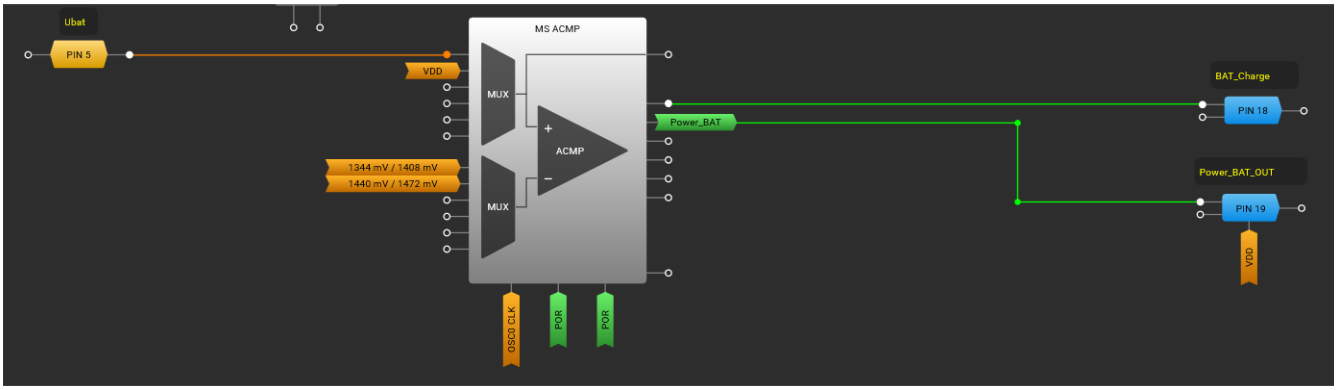


Figure 15. Part of the design responsible for monitoring the power supply voltage level

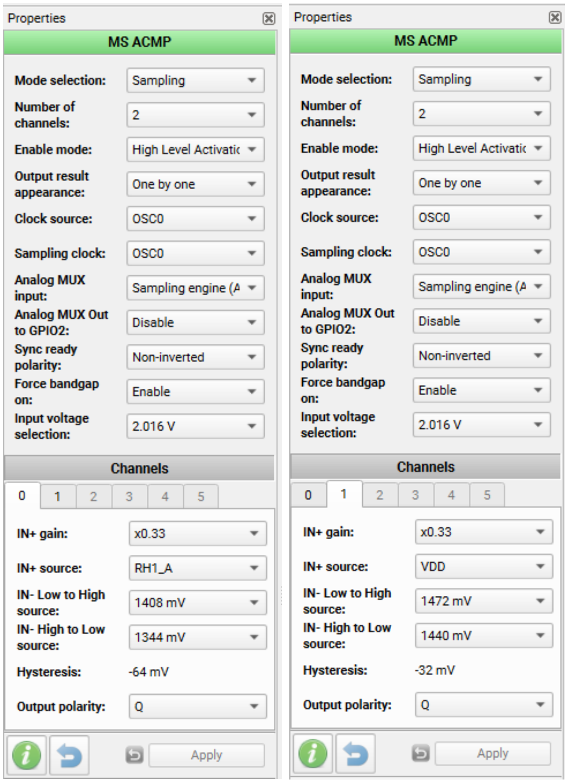


Figure 16. Configuration of the elements responsible for monitoring the power supply voltage level

4.3 Design of Chip B for the Analog Clock

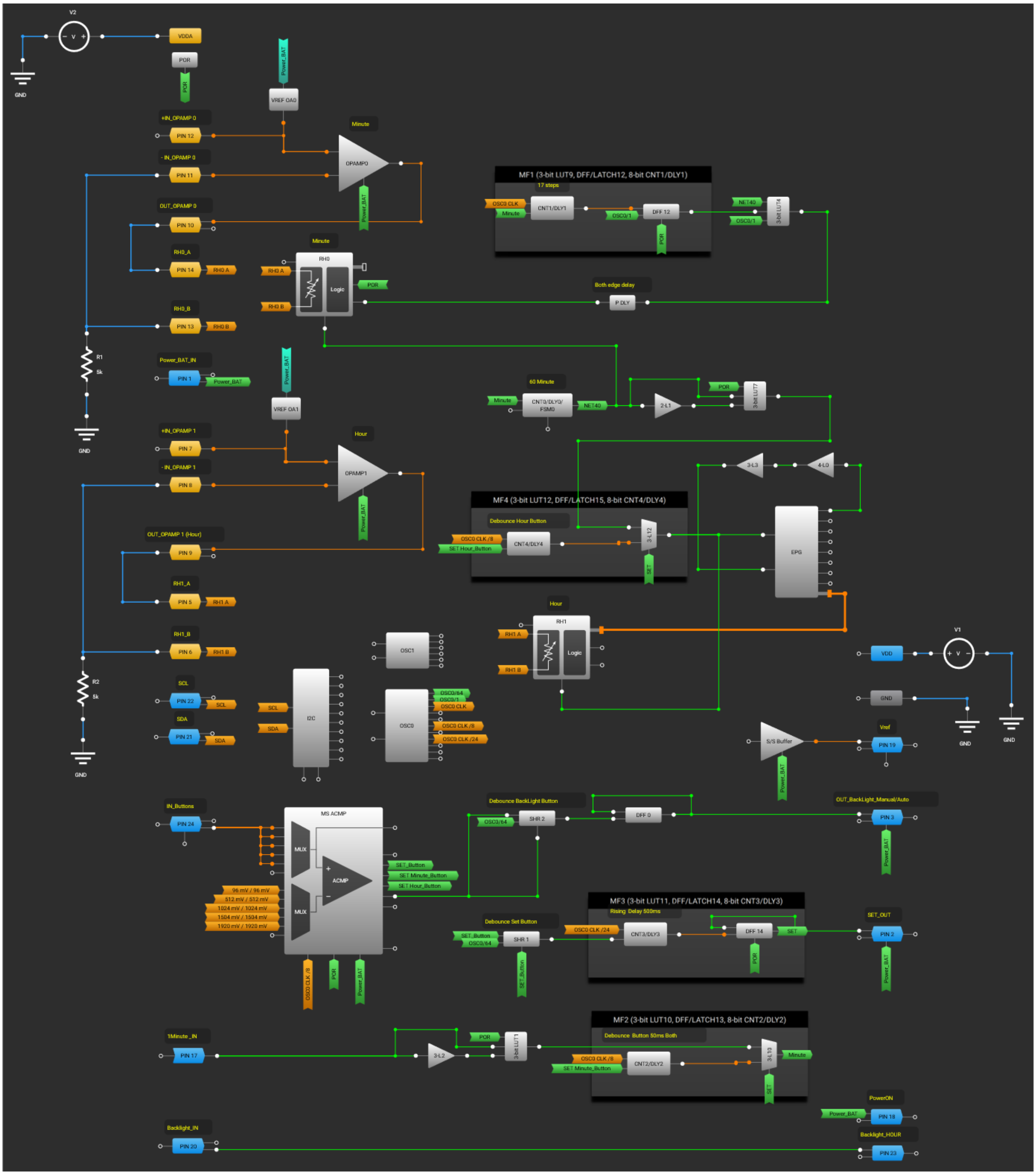


Figure 17. Design of Chip B for Analog Clock

Let's take a closer look at the operation of the Chip B design of the clock.

Divide by 60 / Minutes Counter

The counting of minutes pulses and the generation of hours pulses is performed using an 8-bit CNT0/DLY0, which is configured as a divide-by-60 frequency divider, following a similar scheme to the Divide by 60 / Seconds Counter used in Chip A.

Minutes voltage step generator

The voltage step generator for minutes in this design is built using OPAMP0, VREF OA0, digital rheostat RH0, 8-bit CNT1/DLY1, DFF12, 3-bit LUT4, and P DLY. It operates similarly to the voltage step generator for seconds in Chip A.

Divide by 24 / hours counter and hours voltage step generator

Division by 24 and counting of hours pulses is performed using the EPG (Extended Pattern Generator). In this design, the EPG also controls the hours voltage step generator. The digital rheostats can be driven by the EPG. In rheostat mode, the 8-bit data from the EPG will be loaded into the activated rheostat counters at the rising edge of the corresponding RELOAD signal.

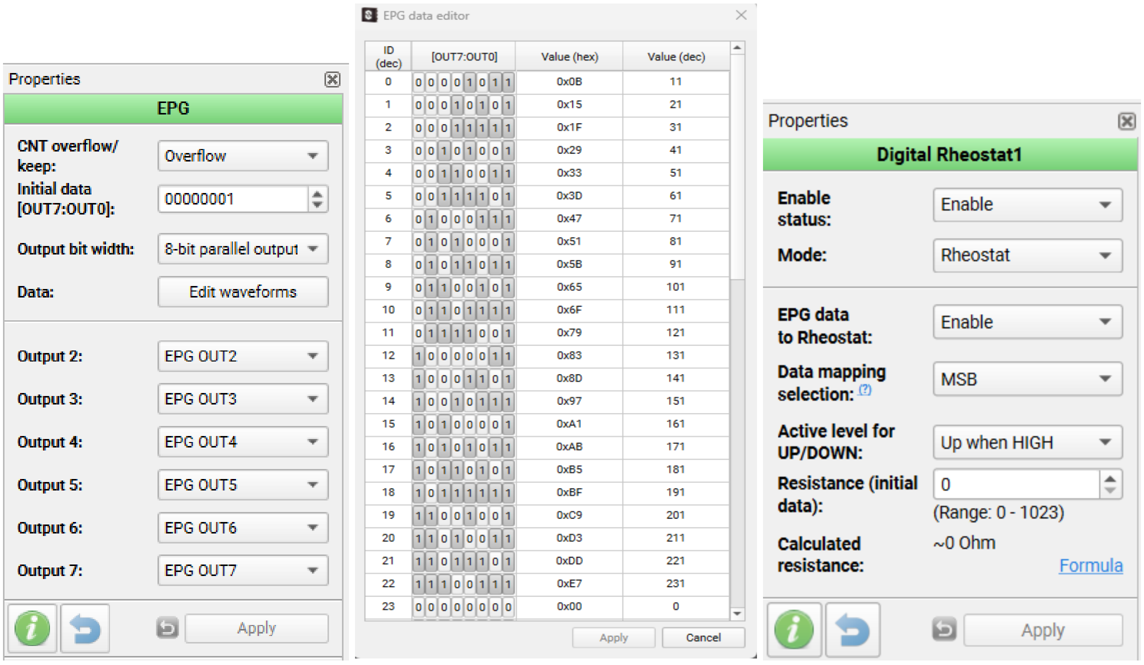


Figure 18. Configuration of the EPG and digital rheostat RH1

Data corresponding to the resistance values of the digital rheostat RH1 have been added to memory cells 0 through 22. RH1 sequentially accepts these values upon receiving pulses at the CLK EPG input. The EPG remains active when a high level is present at the nRESET input. The data is selected such that for memory cells 0 through 22, the OUT0 output always holds a logical 1. The signal from OUT0 is fed to the nRESET input through two buffers (3-bit LUT3, 4-bit LUT0), and as soon as the EPG reaches cell 23 (where OUT0 has a logical 0), the EPG is reset to the Initial state. Upon reset, RH1 is loaded with the Initial data from the EPG, and subsequent pulses at the CLK EPG input cycle through the memory cells from 0 to 22. This process repeats cyclically with each incoming pulse at CLK EPG. This setup allows for division by 24 and control of the hours Voltage Step Generator using a single EPG.

The hours voltage step generator in this design is built using OPAMP1, VREF OA1, the digital rheostat RH1, and the EPG. The operating principle of the generator is just like those used for the minutes and seconds. An example of the circuit operation for generating a stepped control signal for the microammeter displaying hours is shown in Figure 19. To simplify the acquisition of the oscilloscope trace, the frequency of pulses at the CLK EPG input has been significantly increased to approximately 156 Hz.

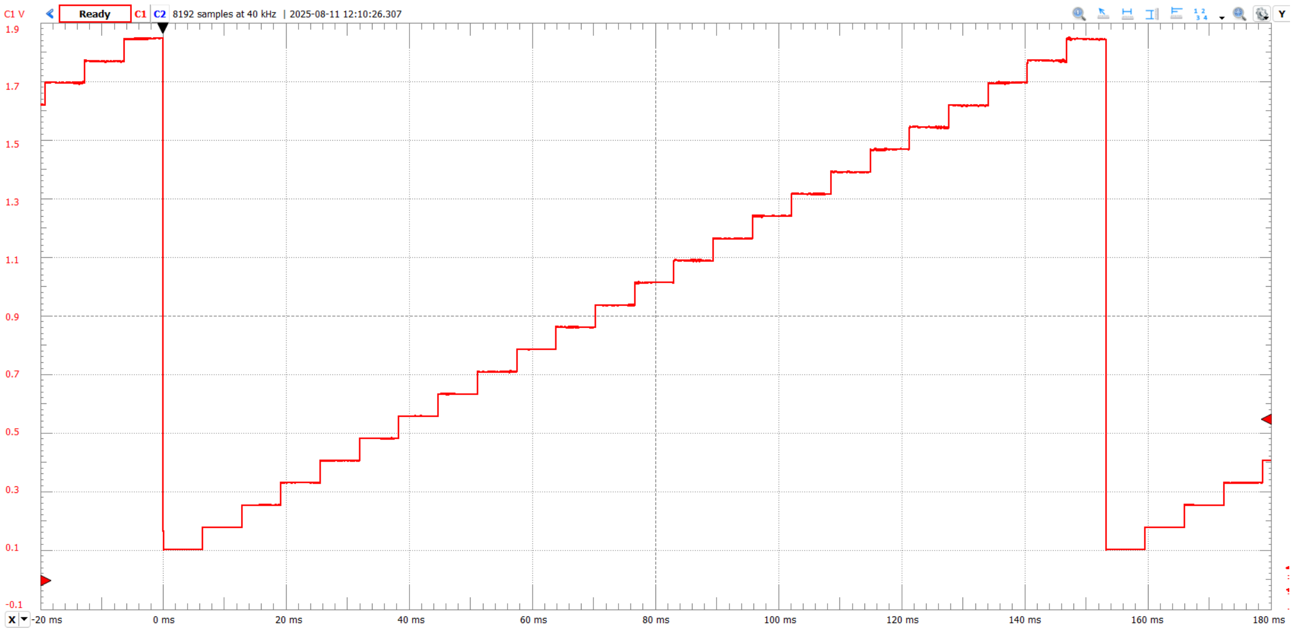


Figure 19. The hours' step signal generation circuit waveform

Time Setting and Clock Control

To process button presses for clock control – SET, Set Minutes, Set Hours and the button for switching the backlight mode between BackLight_Manual and Auto, this design uses the MS ACMP in Range mode. The circuit's operating principle is based on measuring the voltage across resistor R4 (see Figure 20), which is formed by voltage dividers on resistors R5–R8 when buttons SW1–SW4 are pressed. The dividers are powered by a stable voltage of 2016 mV from the SS Buffer output (PIN19).

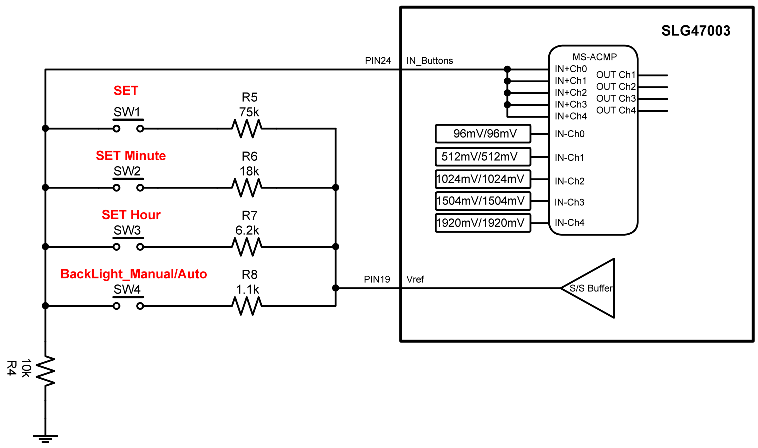


Figure 20. Part of the circuit responsible for processing clock control button presses

The configuration of the MS ACMP is shown in Figure 21.

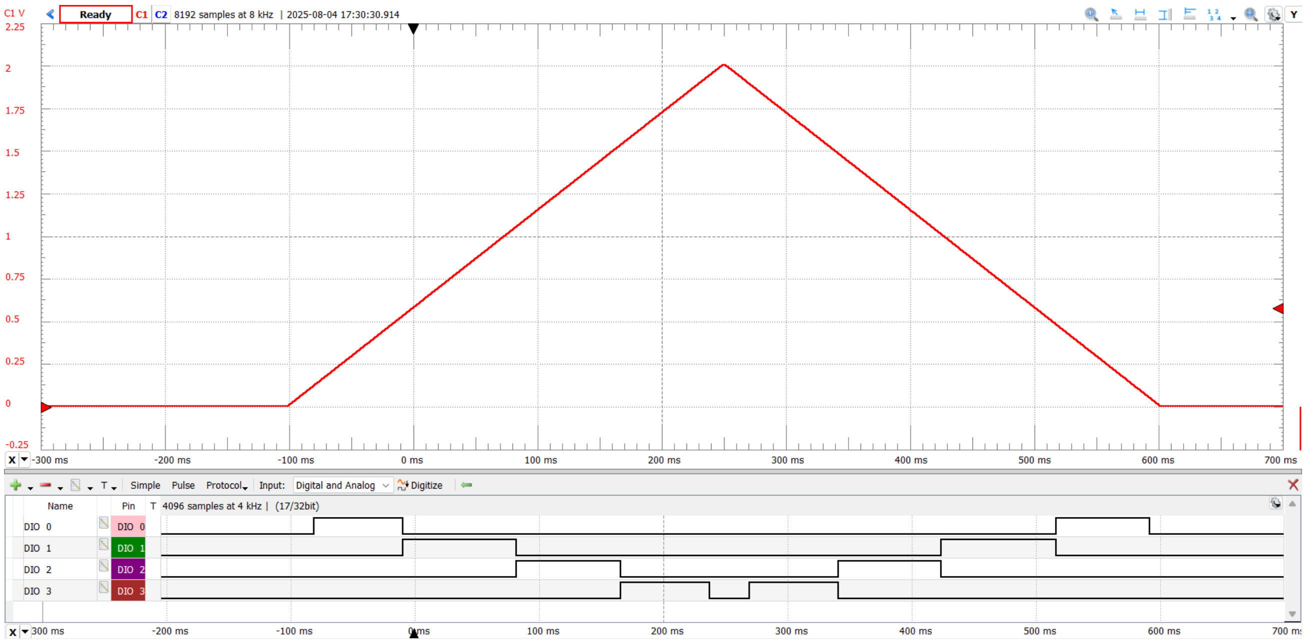
Figure 21. MS ACMP Configuration

The operating principle behind the MS ACMP in Range mode is illustrated by the oscilloscope trace shown in Figure 22. A high level appears at the output OUT CH1 of the MS ACMP when the voltage at the IN_Buttons input (PIN24) (based on the configuration shown in Figure 21) is within the range of 96 mV to 512 mV. Similarly, a high level appears at the output OUT CH2 when the input voltage is between 512 mV and 1024 mV. At the output OUT CH3, a high level corresponds to an input voltage range of 1024 mV to 1504 mV. At the output OUT CH4, a high level corresponds to an input voltage range of 1504 mV to 2016 mV.

The voltage dividers are designed in such a way that pressing each button generates a voltage at resistor R4 that falls in the middle of each of the above ranges, so that we can obtain distinct high-level signals at the MS ACMP outputs corresponding to each individual button.

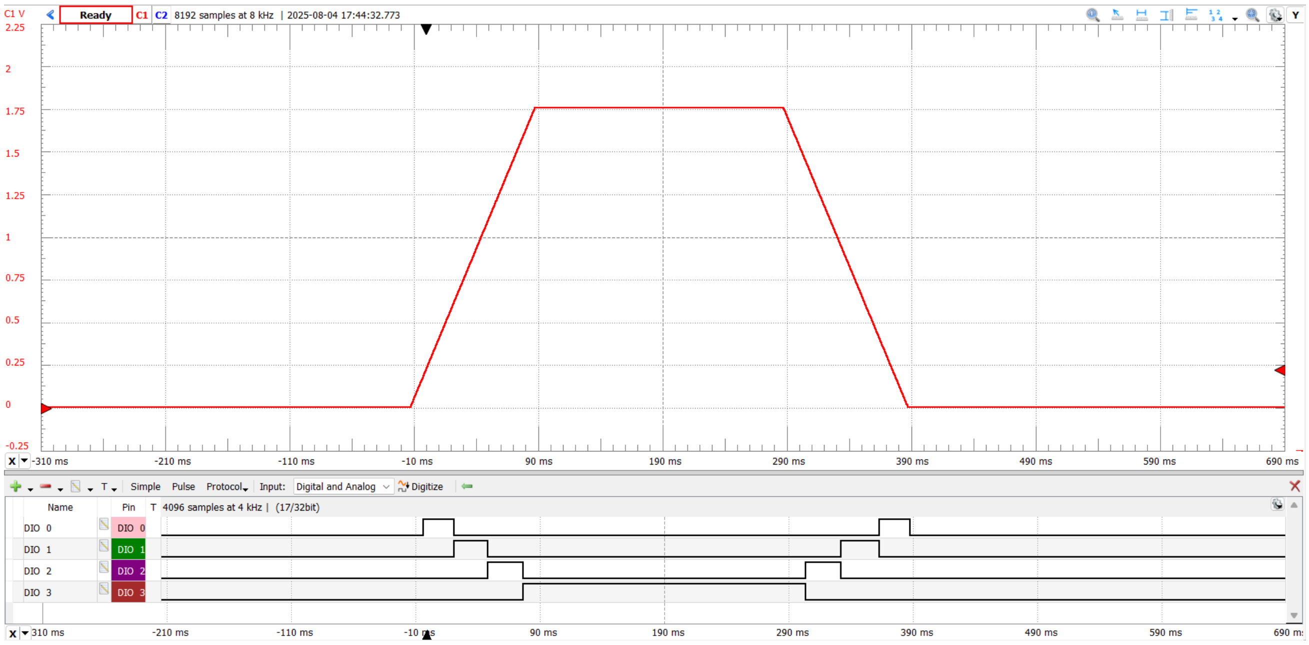
Thus, using only one chip pin, we can process four independent buttons.

However, due to button contact bounce and the specific behavior of the MS ACMP (during signal rise and fall at the MS ACMP input, other button outputs that were not pressed may also trigger), there is a high risk of incorrect operation of this circuit (see Figure 23).



C1 (red) – PIN24 (IN_Buttons)
DIO 0 – OUT CH1 MS ACMP
DIO 1 – OUT CH2 MS ACMP
DIO 2 – OUT CH3 MS ACMP
DIO 3 – OUT CH4 MS ACMP

Figure 22. MS ACMP operation in Range mode waveform



C1 (red) – PIN24 (IN_Buttons)
DIO 0 – OUT CH1 MS ACMP
DIO 1 – OUT CH2 MS ACMP
DIO 2 – OUT CH3 MS ACMP
DIO 3 – OUT CH4 MS ACMP

Figure 23. The button press processing waveform when the BackLight_Manual/Auto button is pressed

To eliminate the effects of button contact chatter and spurious signals, this design uses debounce filters built on Shift Register 1 (3-bit LUT5), Shift Register 2 (3-bit LUT6), CNT2/DLY2, and CNT4/DLY4. The settings of these components are shown in Figure 24.

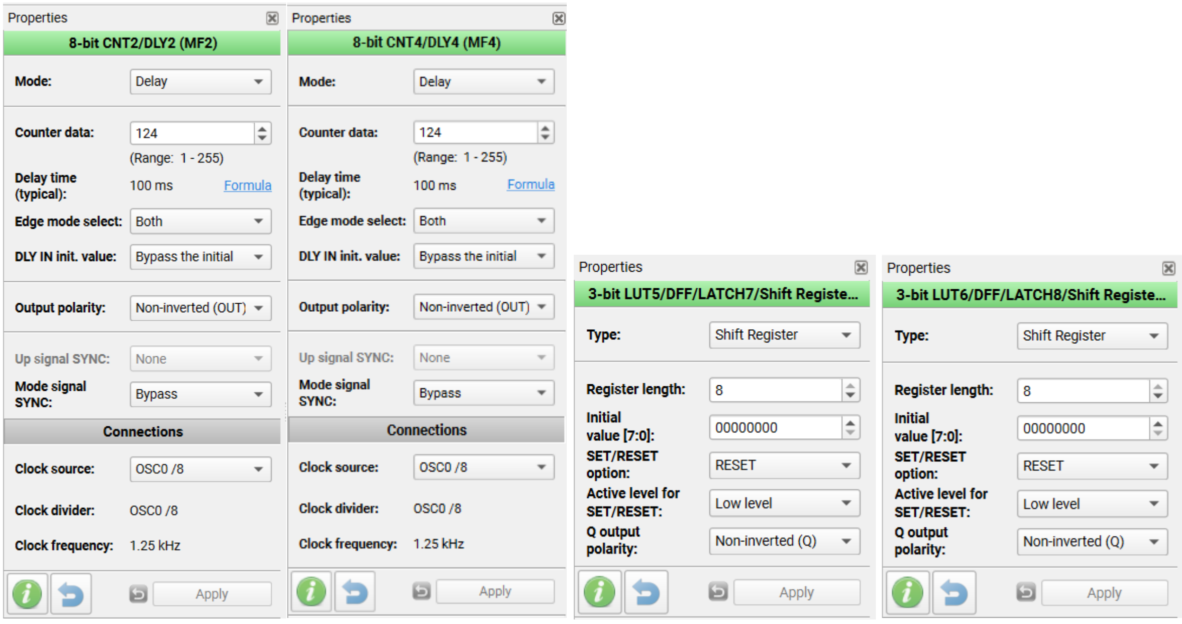
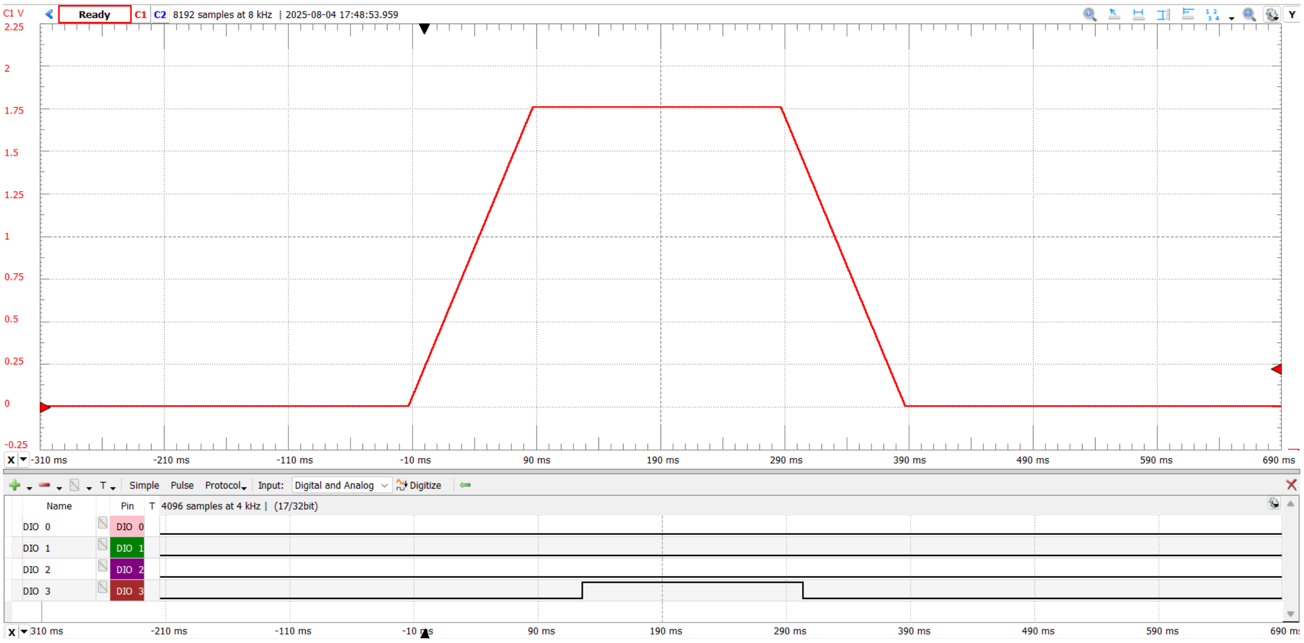


Figure 24. Configuration of Shift Register 1 (3-bit LUT5), Shift Register 2 (3-bit LUT6), CNT2/DLY2, CNT4/DLY4

Figure 25 shows the oscilloscope waveform of the signals from the outputs of the debounce filters when pressing the BackLight_Manual/Auto button. As can be seen, false triggering is now absent during the transition of the signal rising to a steady state.

To eliminate false button triggering, the voltage dividers that generate voltages for each button are powered from a stable source with a voltage of 2016 mV. This voltage is generated using an SS Buffer and VREF.



C1 (red) – PIN24 (IN_Buttons)
DIO 0 – OUT Shift Register 1
DIO 1 – OUT CNT2/DLY2
DIO 2 – OUT CNT4/DLY4
DIO 3 – OUT Shift Register 2

Figure 25. The button press processing waveform when pressing the BackLight_Manual/Auto button (signals from the outputs of MS ACMP passed through debounce filters).

Multiplexers based on 3-bit LUT10 and 3-bit LUT12 switch signals from the SET Hour_Button, SET Minute_Button, and internal signals from the output of CNY0/DLY0 or PIN 17 “1Minute_IN” according to the control signal SET.

Rising Edge Detectors are implemented using 3-bit LUT7, 2-bit LUT1, 3-bit LUT1, and 2-bit LUT2. These detectors help eliminate false triggering of the hours counter and EPG during the transition from clock setup mode to normal operation, in cases where the output of CNY0/DLY0 or PIN 17 “1Minute_IN” is at a HIGH level.

4.4 Design of Chip C for the Analog Clock

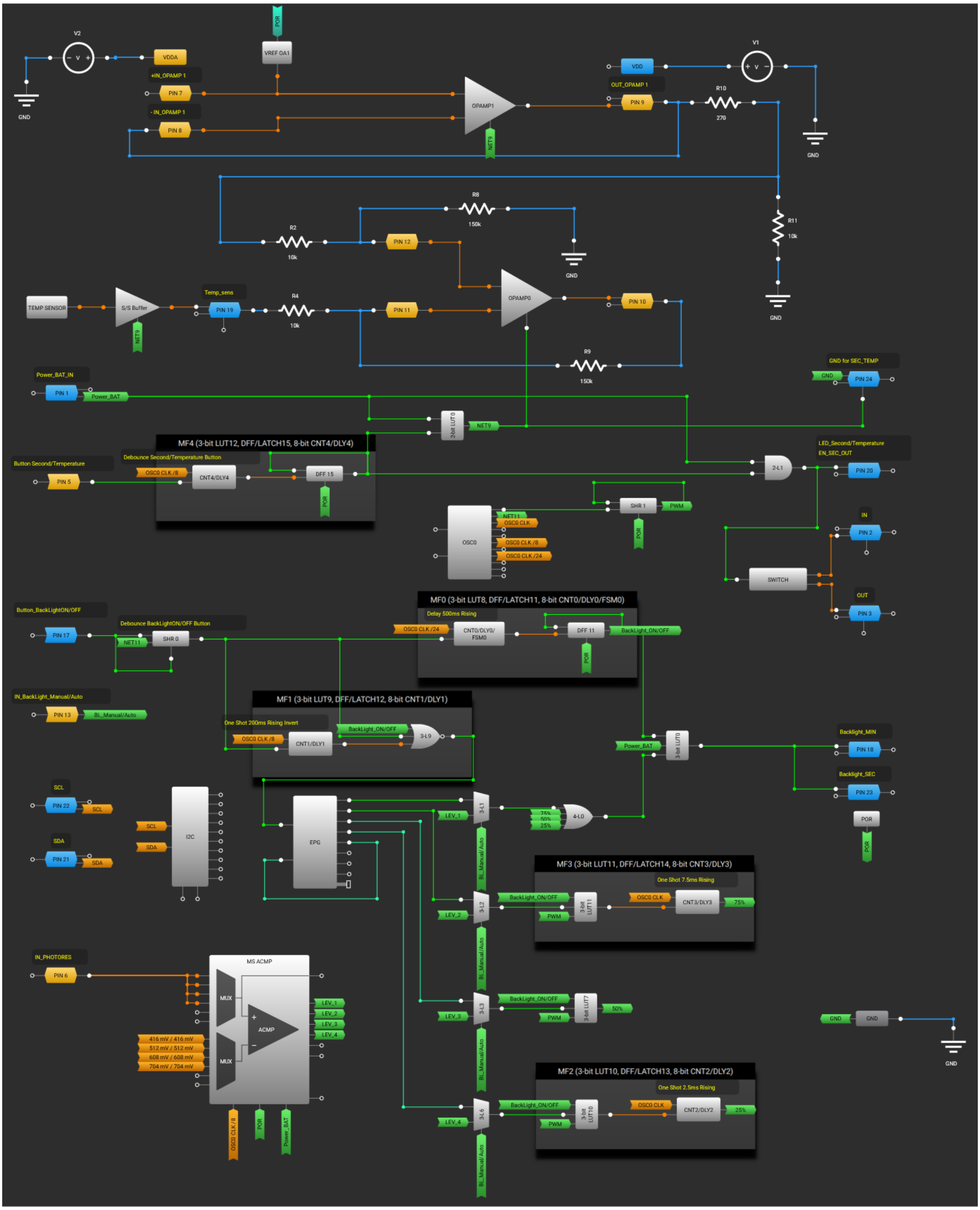


Figure 26. Design of Chip C for Analog Clock

Let's take a closer look at the operation of the Chip C design of the clock.

Temperature Measurement

The following components are used for temperature measurement in this design: TEMP SENSOR, Sink/Source BUFFER, OPAMP0, OPAMP1, and VREF OA1.

The structural diagram of the TEMP SENSOR is shown in Figure 27.

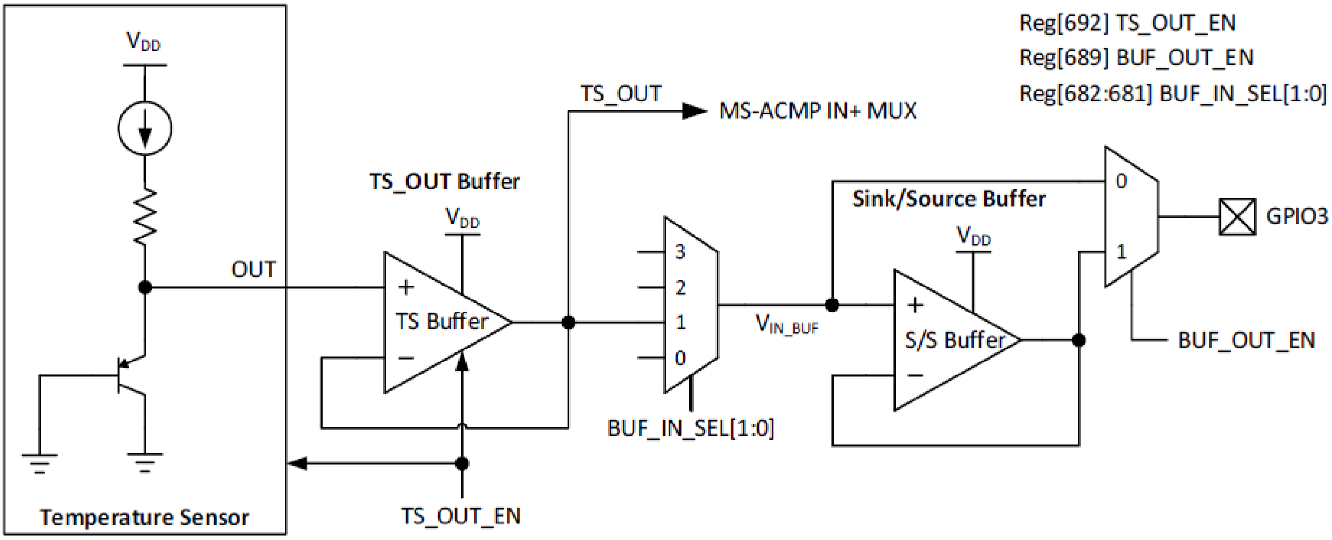


Figure 27. Analog Temperature Sensor Structure

The value of the analog voltage at the TEMP SENSOR output can be calculated using the following formula:

$$V_{TS\_OUT} = -4.8 \times T_J + 1825.2$$

Where:

V_{TS_OUT}: TS_OUT voltage in mV

T_J: Junction temperature in °C.

Thus, for the temperature ranging from 10 °C to 40 °C, the voltage at the output of the TEMP SENSOR will vary from approximately 1633 mV to 1777 mV. To achieve a thermometer range of 10 °C to 40 °C while utilizing the full scale of the microammeter, OPAMP0 is configured as a differential amplifier with a gain factor of 15. A reference voltage source is built using OPAMP1 and VREF OA1. OPAMP1, configured as a buffer (voltage follower), serves to buffer the VREF OA1. The voltage at the output of OPAMP1 sets the starting point of the temperature measurement range (10 °C).

The differential amplifier on OPAMP0 amplifies the difference between a stable reference voltage corresponding to a temperature of 10 °C and the voltage generated at the output of the TEMP SENSOR. As a result, the output of OPAMP0 provides a voltage ranging from 0 to approximately 2160 mV, which corresponds to a temperature range from 10 °C to 40 °C. The temperature measurement circuit is shown in Figure 28.

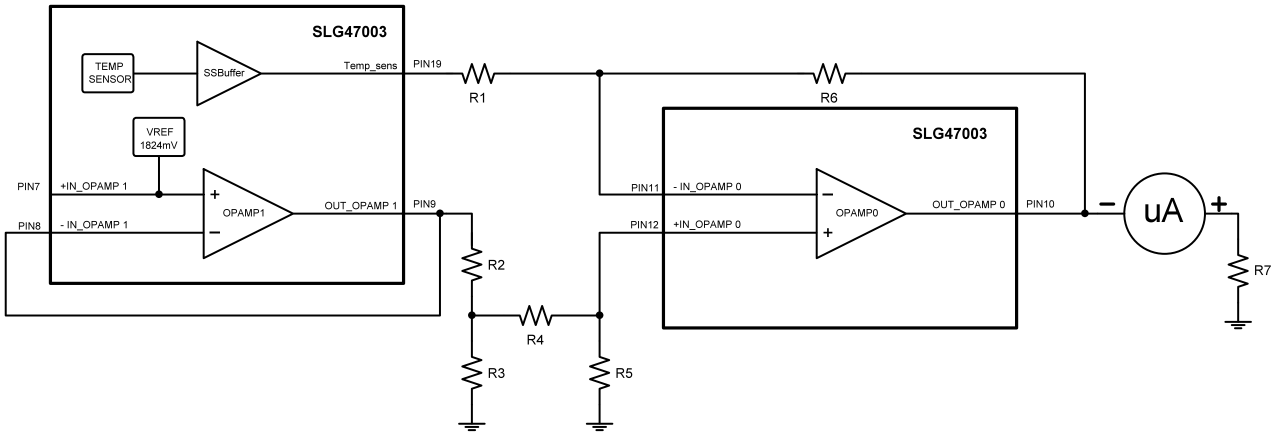


Figure 28. Temperature measurement scheme

The analog voltage value at the output of OPAMP0 can be calculated using the following formula:

$$V_{OUT} = \frac{R1}{R6} \times (V_{+IN} - V_{-IN})$$

Where:

V_{OUT}: Output voltage OPAMP0

V_{+IN}: +IN Input voltage OPAMP0

V_{-IN}: +IN Input voltage OPAMP0

and R1 = R4, R5 = R6

Switching the Analog Indicator "Second/Temperature"

Switching between the Second or Temperature display modes is done using the Second/Temperature button. CNT4/DLY4 functions as a debounce filter for the "Second/Temperature" button. Together with the configuration of PIN 5 as a digital input with a Schmitt trigger and a Pull Down resistor, it prevents false triggering due to contact bounce. DFF15 toggles and stores the state of Second or Temperature. 2-bit LUT0 controls the activation of OPAMP0 and changes the state of PIN 24 from a LOW level to HIGH-Z. 2-bit LUT1 generates the control signal EN_SEC_OUT at PIN 20 and controls the SWITCH.

The control circuit for the microammeter – the temperature and seconds indicator – is shown in Figure 29.

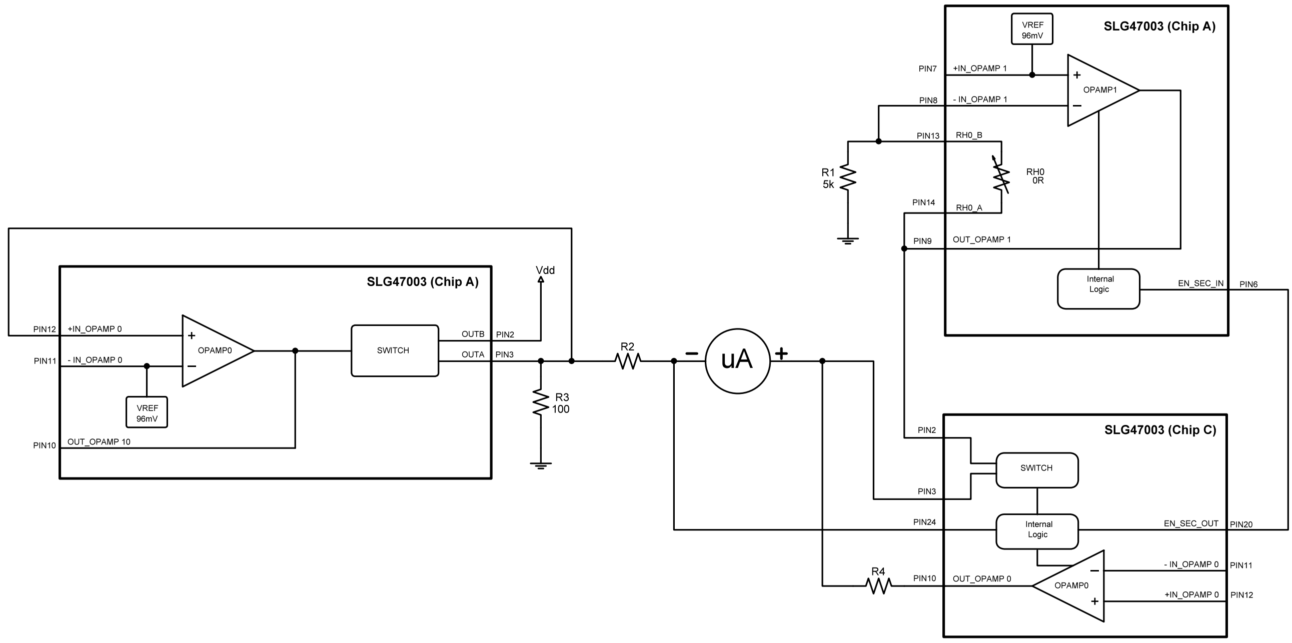


Figure 29. Control circuit for the microammeter – temperature and seconds indicator

In “Seconds” mode, the “−” terminal of the microammeter is connected through current-limiting resistor R2 to PIN 3 of chip A, while the “+” terminal of the microammeter is connected through the closed SWITCH of chip C to the output of OPAMP1 of chip A. At this time, OPAMP0 of chip C is turned off by a control signal from 2-bit LUT0, and its output is switched to HIGH-Z, as is the output of PIN 24. This ensures that the temperature measurement circuit does not interfere with the operation of the microammeter and does not affect the seconds display circuit. Meanwhile, OPAMP1 of chip A is active, and the microammeter displays the seconds value.

In “Temperature” mode, a LOW level appears on PIN 24, connecting the “−” terminal of the microammeter to the circuit’s GND. The SWITCH opens, disconnecting the output of OPAMP1 of chip A from the “+” terminal of the microammeter, and OPAMP1 of chip A is also turned off. OPAMP0 of chip C is activated and connected to the “+” terminal of the microammeter through the current-limiting resistor R4. As a result, the microammeter begins to display the temperature value.

Backlight Control

The backlight of the microammeters can operate in two modes: manual and automatic. The backlight is turned on by a long press (more than 500 ms) of the BackLight ON/OFF button. Switching between manual and automatic backlight control is done via the BL_Manual/Auto signal, which is generated by the BackLight_Manual/Auto button (see Design B).

In manual mode, short presses (less than 200 ms) are used to select one of four brightness levels.

In automatic mode, the brightness of the backlight changes depending on the intensity of ambient light falling on the clock. The ambient light intensity is monitored by an LDR (Light Dependent Resistor).

Shift Register0 functions as a debounce filter for the BackLight ON/OFF button. Together with the configuration of PIN 17 as a digital input with Schmitt trigger and a Pull Down resistor, it prevents false triggering due to contact bounce. CNT0/DLY0 and DFF11 detect long presses of the BackLight ON/OFF button. CNT1/DLY1 and 3-bit LUT9 detect short presses and block short press activation in case of a long press.

The configuration of these components is shown in Figure 30, and the oscilloscope waveform of this module's operation is presented in Figure 31.

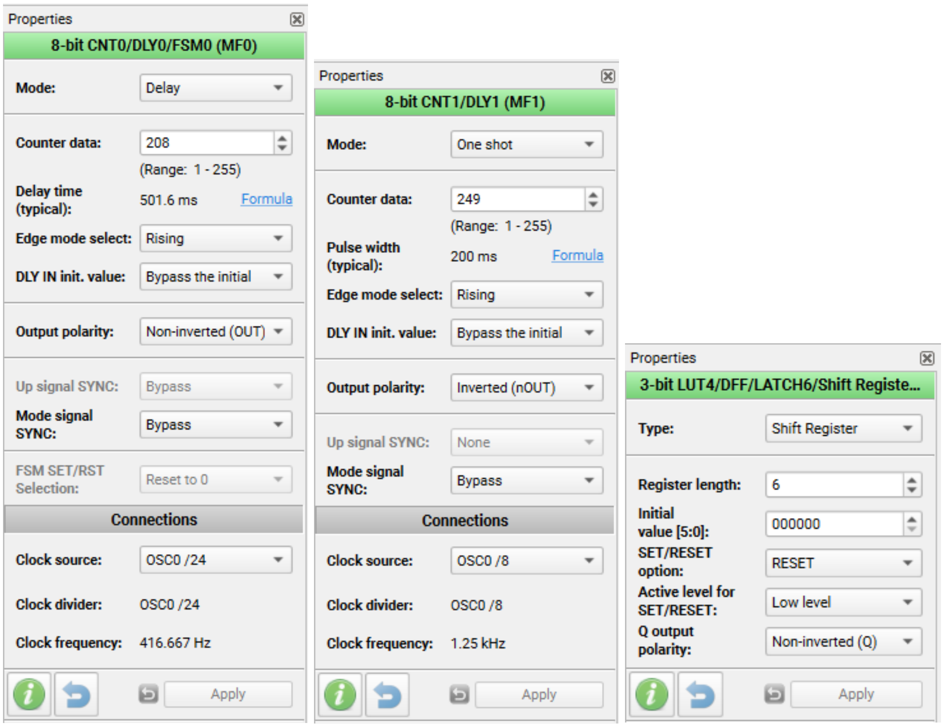


Figure 30. Setting CNT0/DLY0, CNT1/DLY1, Shift Register0

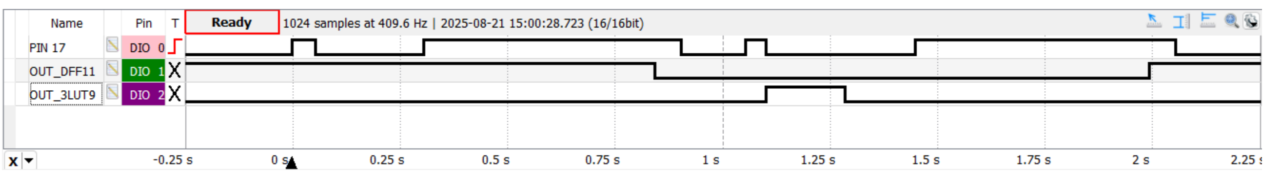


Figure 31. The BackLight ON/OFF button press processing waveform

Brightness Adjustment of the Backlight

Brightness adjustment is achieved by changing the duty cycle of the PWM signal controlling the backlight LEDs (100%, 75%, 50%, 25%).

The PWM signals are generated as follows:

Shift Register1, configured as a frequency divider by 4, generates the base PWM signal with a 50% duty cycle. PWM signals with 75% and 25% duty cycles are generated using CNT3/DLY3, 3-bit LUT11, CNT2/DLY2, and 3-bit LUT10, based on the 50% PWM signal. All PWM signals are combined using 4-bit LUT0.

The configuration of the components that generate the PWM signals is shown in Figure 32.

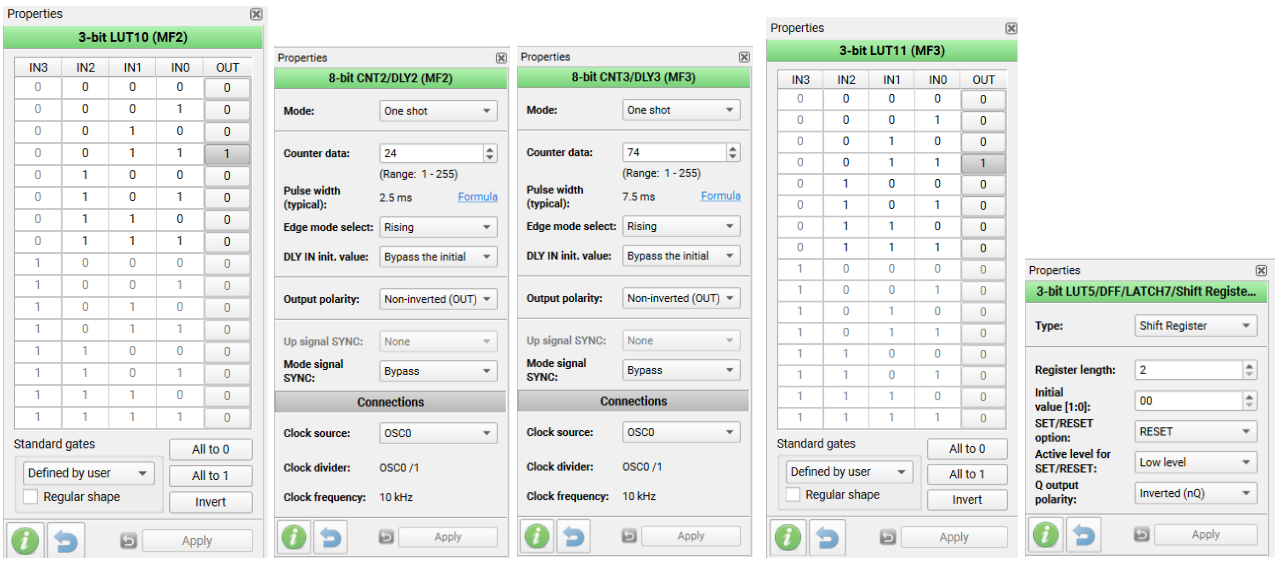


Figure 32. Configuration of CNT0/DLY0, CNT1/DLY1, 3-bit LUT10, 3-bit LUT11, Shift Register1

A 4-channel 2-to-1 multiplexer is implemented using the elements 3-bit LUT1, 3-bit LUT2, 3-bit LUT3, and 3-bit LUT6. This multiplexer selects the control signal source for the PWM signal generation circuit.

Manual Backlight Control

Switching between PWM signals in manual mode is performed using the EPG. The configuration of the EPG is shown in Figure 33.

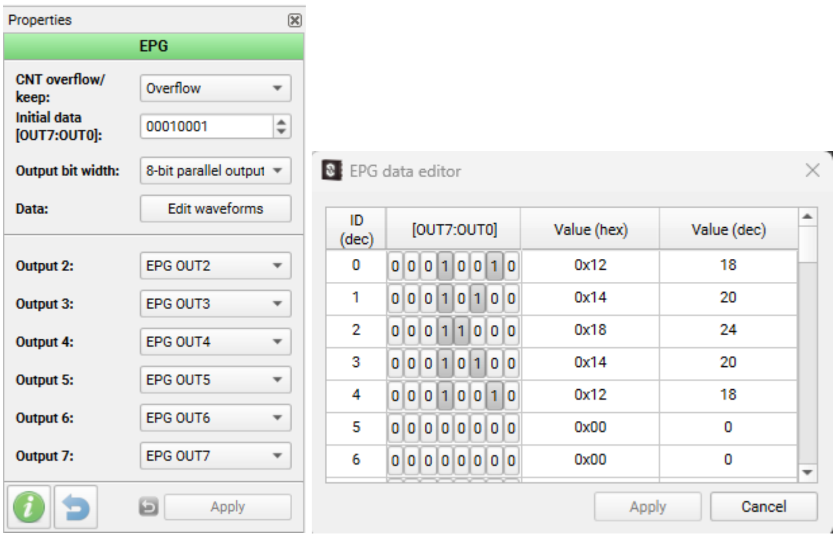


Figure 33. EPG Configuration

This EPG configuration allows cyclic switching between PWM signals according to the scheme shown in Figure 34.

The signal from output OUT4 is fed to the nRESET input and as soon as the EPG reaches state 5 (where OUT4 has a logical 0), the EPG is reset to the Initial state. Subsequent pulses at the CLK input of the EPG each cycle through states 0 to 4. This process repeats cyclically as pulses continue to arrive at the CLK input.

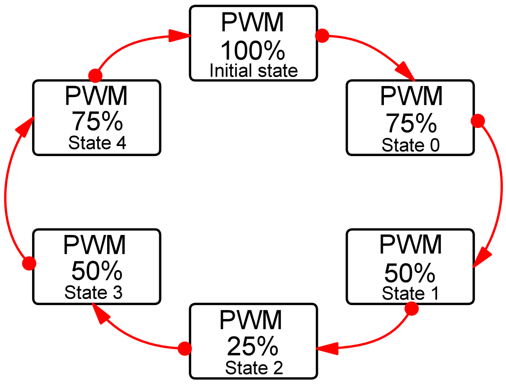
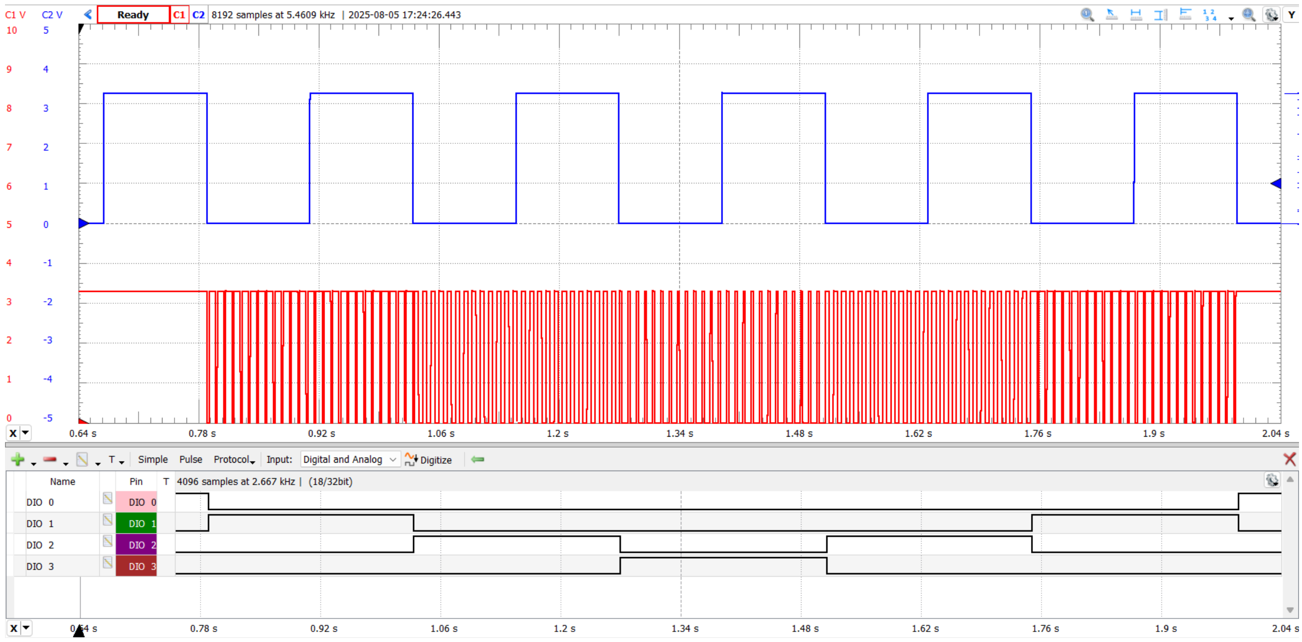


Figure 34. PWM Signal Switching Using EPG

The oscilloscope waveform of the manual backlight brightness control operation is shown in Figure 35.



C2 (blue) – PIN17 (Button_BackLightON/OFF)
C1 (red) – PIN18 (Backlight_MIN)
DIO 0 – OUT0 EPG
DIO 1 – OUT1 EPG
DIO 2 – OUT2 EPG
DIO 3 – OUT3 EPG

Figure 35. The manual brightness backlight control waveform

Automatic Backlight Control

In automatic mode, the brightness of the backlight changes depending on the intensity of ambient light falling on the clock. The ambient light intensity is monitored by an LDR. As the ambient light level decreases, the backlight brightness also decreases.

The automatic backlight control is built using the LDR and MS-ACMP (see Figure 36).

A voltage divider is formed using R1 and the LDR, powered by a stable Vref voltage. The voltage from the divider is fed to the input of the MS-ACMP. When the ambient light intensity increases, the voltage at the divider decreases; when the ambient light intensity decreases, the voltage increases.

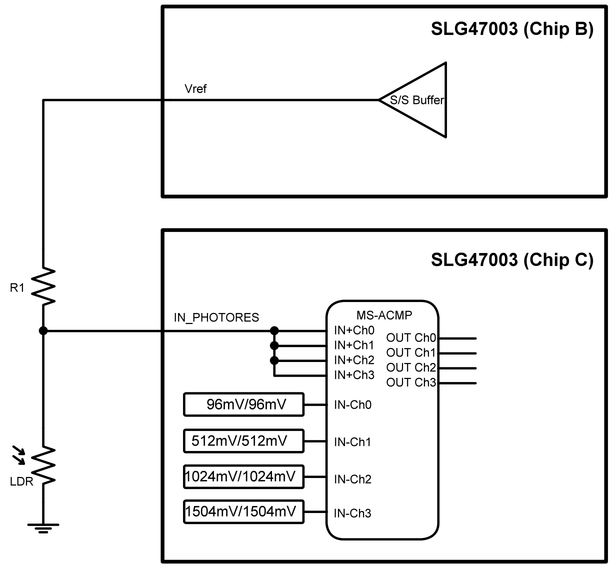


Figure 36. Automatic Backlight Control Circuit

The configuration of MS-ACMP is shown in Figure 37.

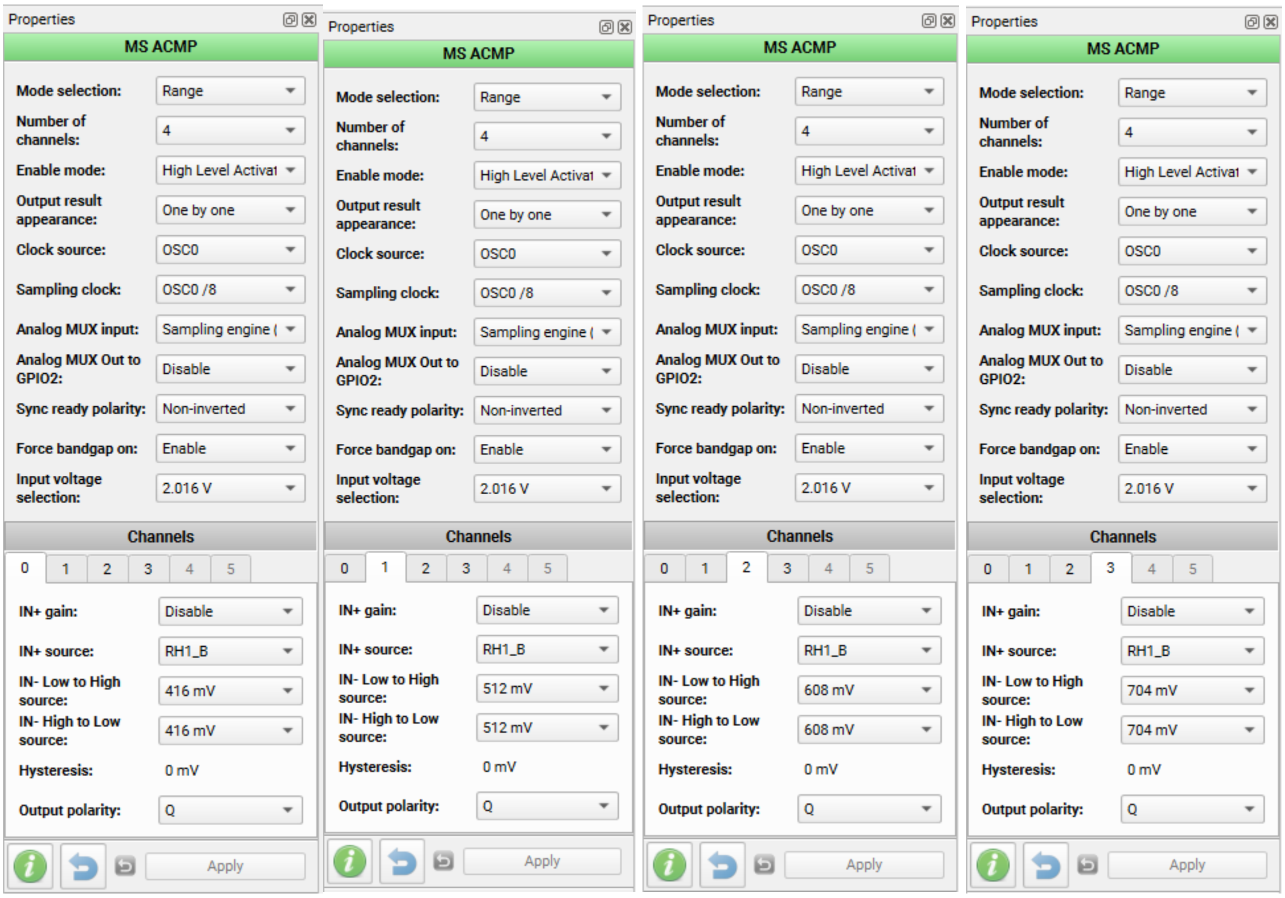
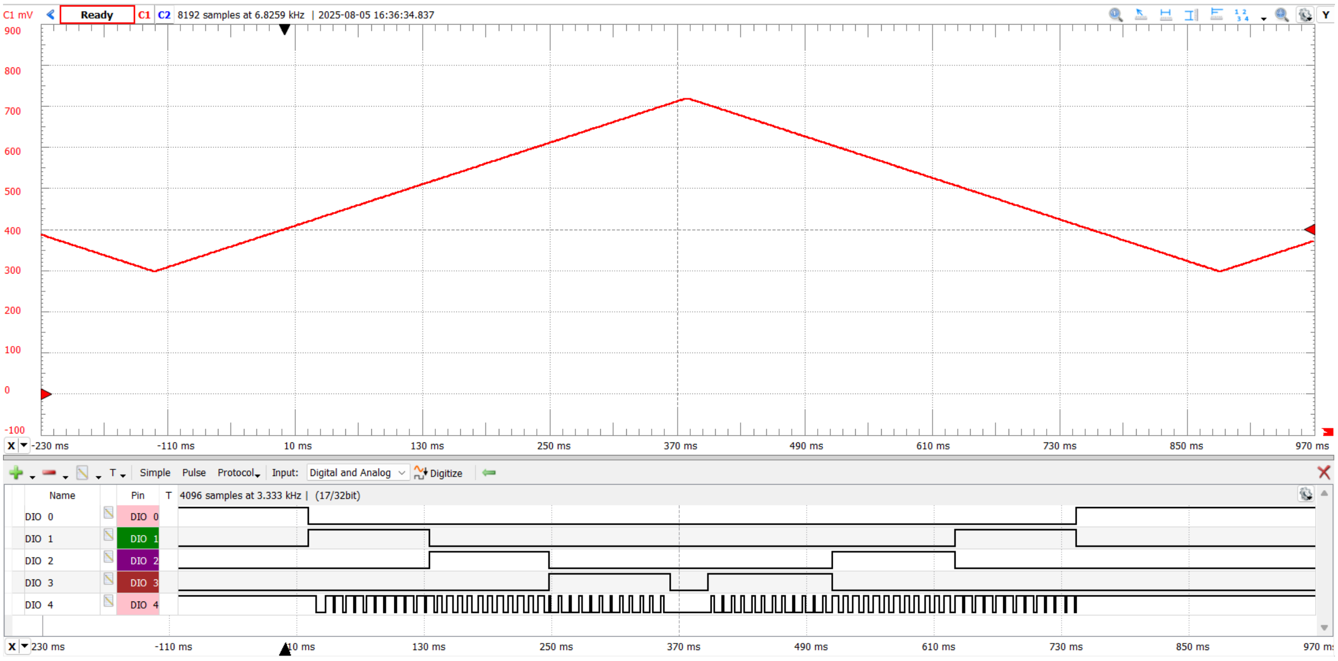


Figure 37. MS-ACMP Configuration

The oscilloscope waveform of the automatic backlight brightness control operation is shown in Figure 38.



C1 (red) – PIN6 (IN_PHOTORES)
DIO 0 – OUT CH0
DIO 1 – OUT CH1
DIO 2 – OUT CH2
DIO 3 – OUT CH3
DIO 4 – PIN18 (Backlight_MIN)

Figure 38. The automatic brightness backlight control waveform

5. PCB Design and Project Layout

For testing purposes a PCB was designed, and can be seen in Figure 39.

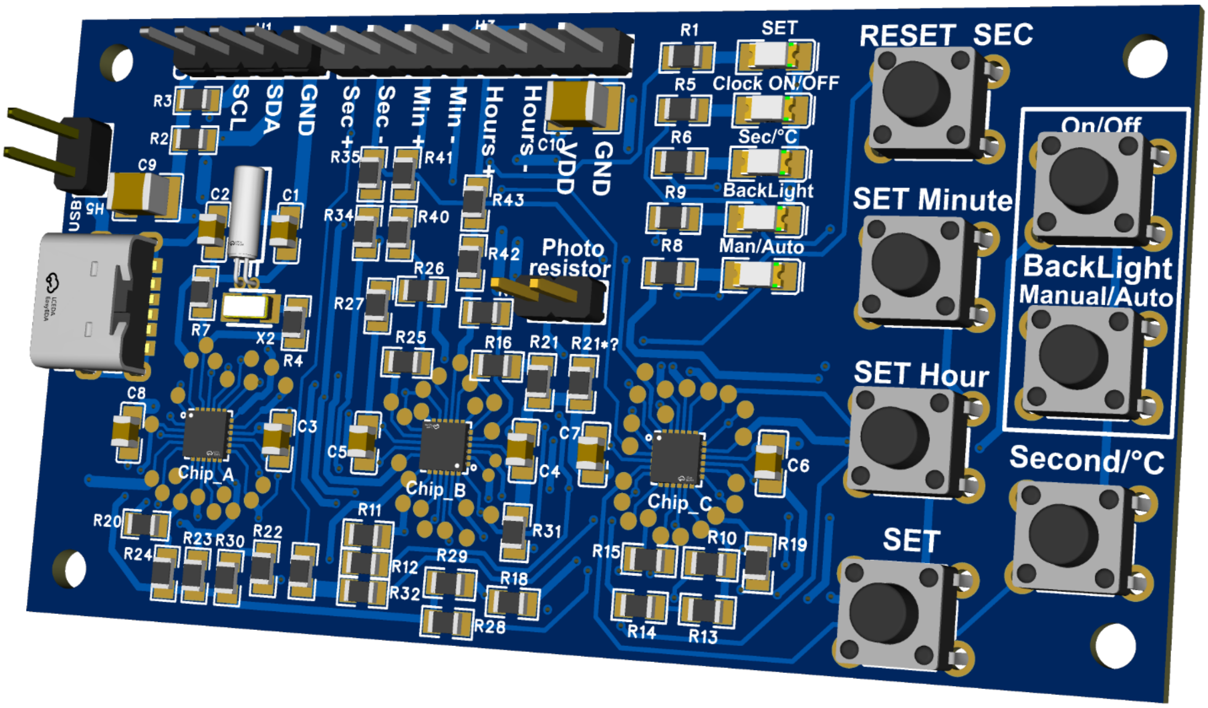


Figure 39. PCB for Analog Clock

SLG47003V chips feature an I²C module that enables control over these chips within a wide range. The use of I²C in this project significantly simplifies and accelerates configuration and debugging during development.

The operation of the prototype of the "Analog Clock" project in clock mode is shown on Figure 40. The first microammeter on the left displays the hours (50 μA = 24 hours), the microammeter in the middle displays the minutes (50 μA = 60 minutes), the microammeter on the right displays the seconds (50 μA = 60 seconds). In temperature measurement mode, the microammeter on the right displays the temperature.

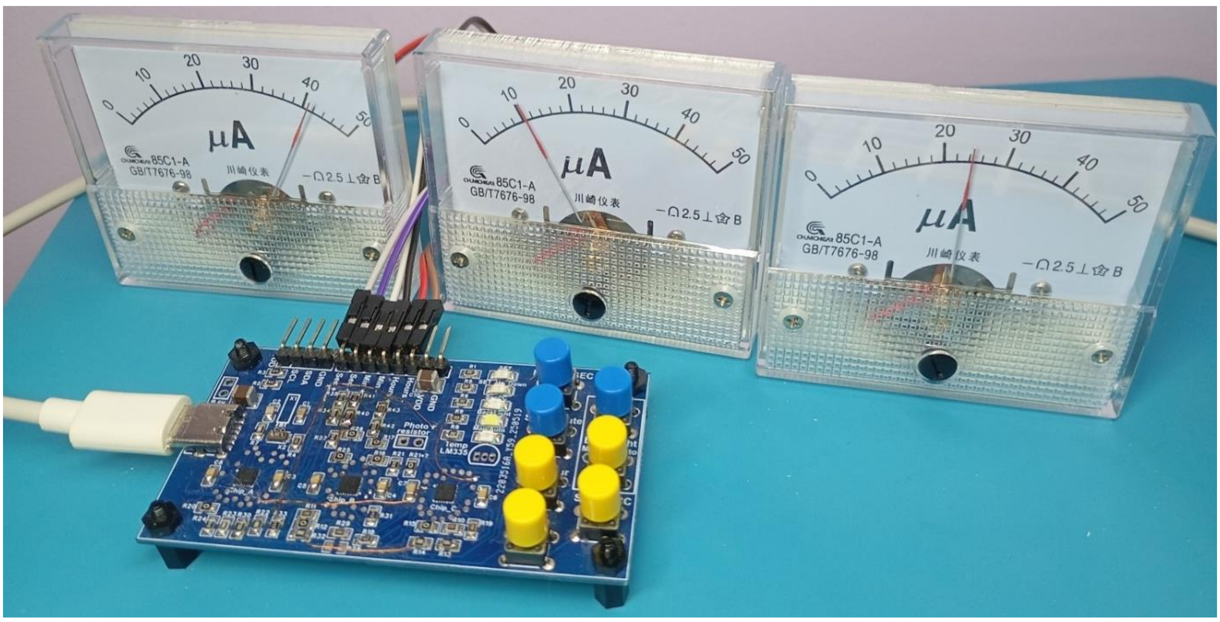


Figure 40. The prototype for the Analog Clock

6. Conclusions

By using three SLG47003V devices, a fully functional device was created that demonstrates the full capabilities of the SLG47003V chips. Examples of the operation of nearly all blocks included in these chips are shown, covering both the analog and digital components.

The analog clock built using microammeters is more of an engineering experiment or an art project than a practical device. It demonstrates the idea that a standard indicator (a microammeter) can be used in a completely unconventional way, made possible with Renesas GreenPAK chips.

Revision History

Revision	Date	Description
1.00	May 25, 2026	Initial release.

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