

SLG47115 and SLG46110 Isolated Flyback Controller

SLG47115, SLG46110

This application note describes how to design and build an isolated DC-DC flyback controller using the SLG47115 as a low-side N-MOSFET controller and using the SLG46110 for isolated feedback via an optocoupler.

Isolated power supplies are useful when electrical noise on a primary must be prevented from reaching the secondary. This isolation “barrier” can also be used to provide electrical safety, conforming to various safety standards, or be used to perform level-shifting between different electrical potentials.

The SLG47115 contains two half-bridge power stages that can be used to directly drive many different loads, such as the gate of a discrete power N-MOSFET. Depending on the size of the MOSFET and its proportional gate capacitance, a single half-bridge (or both half-bridges) can be used to drive the gate. The SLG47115 also includes a comparator with a fast response time designed for sensing current.

For non-isolated flyback (and other non-isolated topologies) the SLG47115’s analog comparators can be used to sense the output voltage. Together, the current comparator and the voltage comparator can be programmed to provide a control scheme that combines a fixed peak current with hysteretic, controlled on and off times.

The SLG46110 utilizes two voltage comparators that can each use independent reference voltages at their inverting inputs. In this design example, these comparators are used to sense both the output voltage and the output current on an isolated secondary side and then used to transmit a turn-off pulse through a RV1S6190A high-speed optocoupler.

This application note comes complete with GoConfigure design files that can be found in the References section as well as an Excel-based calculator tool for creating other flyback regulators with varying sets of input voltages, output voltages, output currents, and switching frequency ranges.

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Terms and Definitions

ACMP	Analog Comparator
BOM	Bill of Materials
CCMP	Current Comparator
CNT/DLY	Counter-Delay
DC	Direct current
DFF	D Flip-flop
EMI	Electro-magnetic Interference
ESR	Equivalent Series Resistance
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GPO	General Purpose Output
HV	High Voltage
IC	Integrated Circuit
I/O	Input / Output
I2C	Inter-Integrated Circuit Protocol
LUT	Look-up Table
MF	Multi-function Macrocell
OSC	Oscillator
OCP	Overcurrent Protection
PCB	Printed Circuit Board
POR	Power On Reset
PWM	Pulse Width Modulation
SMPS	Switch-mode Power Supply

References

For related documents and software, please visit:

[HVPAK™ | Renesas](#)

Download our free GreenPAK Designer software [1] to open the .app files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] [GreenPAK Go Configure Software Hub](#), Software Download and User Guide, Renesas Electronics

[2] [AN-CM-420 SLG47115 and SLG46110V Isolated Flyback Controller](#), Design file, Renesas Electronics

[3] [GreenPAK Development Tools](#), GreenPAK Development Tools Webpage, Renesas Electronics

[4] [GreenPAK Application Notes](#), GreenPAK Application Notes Webpage, Renesas Electronics

[5] [SLG47115](#) Datasheet, Renesas Electronics

[6] [SLG46110](#) Datasheet, Renesas Electronics

1. Introduction

Isolated DC-DC converters are widely used to produce a regulated voltage from a source on one (primary) side of an isolation barrier to a load on the other (secondary) side. Noise immunity, electrical safety, and common-mode level shifting are all applications that require isolation in a power supply. This application note introduces the simplest of all isolated DC-DC converters, the flyback, utilizing the SLG47115 for power switching and using the SLG46110 to send control signals back to the primary from the isolated secondary.

The design of this flyback converter is based on the buck-boost topology. As the name implies, both buck-boost and flyback converters can both generate regulated output voltages that are above, below, or equal to their input voltage. The flyback can also produce a negative output voltage, control output current rather than output voltage, or generate multiple outputs.

Flyback converters use a coupled inductor as their magnetic element. While the symbol looks like a transformer, a coupled inductor differs from a “true” transformer because it purposefully stores energy in its core like an inductor – something most other SMPS transformers avoid as much as possible. For simplicity, the magnetic element will be referred to as a “flyback transformer” in this application note (in keeping with common industry practice). The flyback transformer isolates, level-shifts, and stores energy. No additional magnetics are needed, and this is the key to the flyback topology’s simplicity.

2. Flyback Converter Design and Operation

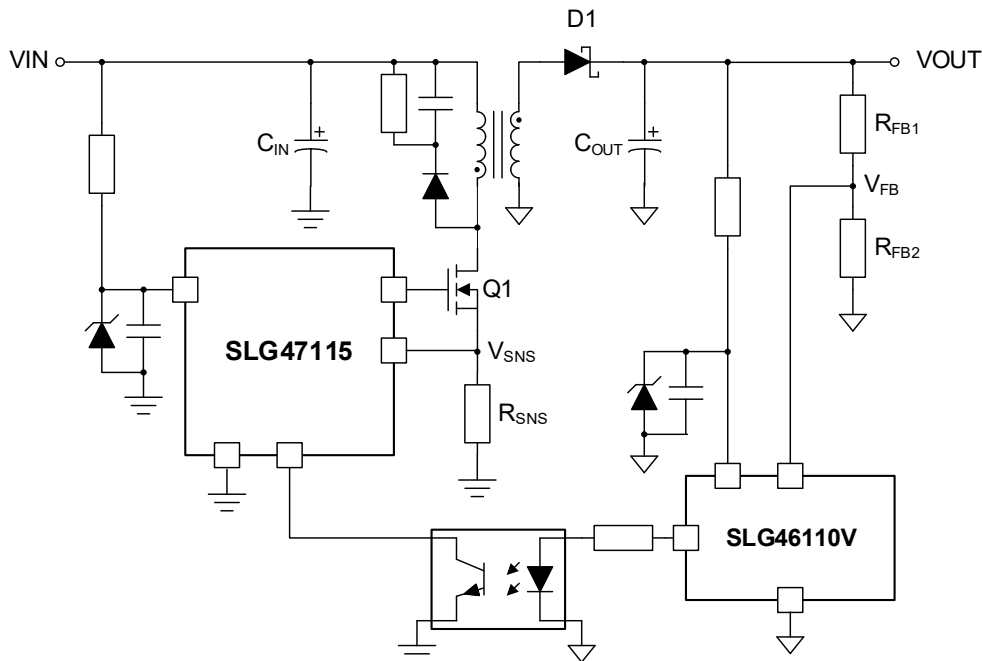


Figure 1. Simplified Flyback Converter Schematic

2.1 Theory of Operation

Each switching cycle begins when the voltage at the center tap (V_{FB}) of the output resistor divider R_{FB1} and R_{FB2} falls below the threshold of the voltage comparator specified in the SLG46110. A signal sent through the optocoupler to the SLG47115 turns on Q1 and current begins to ramp up in the primary of the flyback transformer. The polarity of the transformer keeps the D1 output diode reverse-biased while current flows in the primary side. The fast current comparator inside the SLG47115 senses the primary current through R_{SNS} at node V_{SNS} and turns Q1 off when the current reaches a peak value (set by the user). The voltage in the secondary reverses direction, forward biases D1, and current flows to the output. The instantaneous voltage across the output capacitor C_{OUT} initially rises but then falls as the load discharges C_{OUT} . This causes the output voltage (and hence V_{FB}) to fall until SLG46110’s comparator trips once again, starting the next switching cycle.

In this hysteretic control method with fixed peak primary current, the switching frequency varies in inverse proportion to the output power. This provides a natural increase in power efficiency at light loads but comes at the expense of having more complex EMI filtering because of the variable frequency.

2.2 Go Configure Software Hub Projects

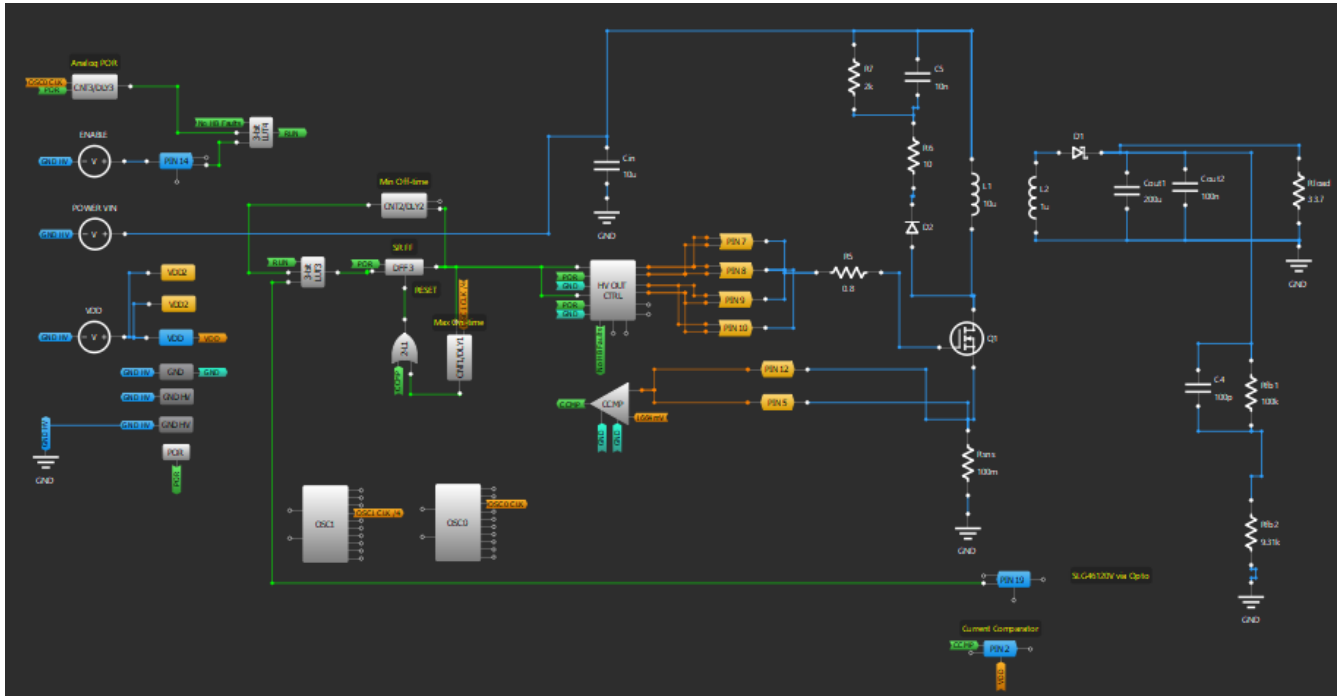


Figure 2. SLG47115 controlling an external N-MOSFET

The simulation in Figure 2 cannot be run as shown as the simulation of more than one GreenPAK IC in a single instance of Go Configure is not currently supported. The SLG47115+SLG46110 Flyback Evaluation Board comes with the programming file (shown in Figure 2) already programmed into its SLG47115 IC for standalone operation. Please see section 8 Emulation of Different Configurations for information on using the EVB with an Advanced Development Board or Development Board Lite in Emulation mode, where the control parameters can be changed for different input voltage, output voltage, operating frequency, and output power.

Please also see section 9 Non-isolated Flyback in Go Configure for Simulation in order to find details on a separate Go Configure programming file with a flyback regulator that is non-isolated, allowing simulation using only the SLG47115.

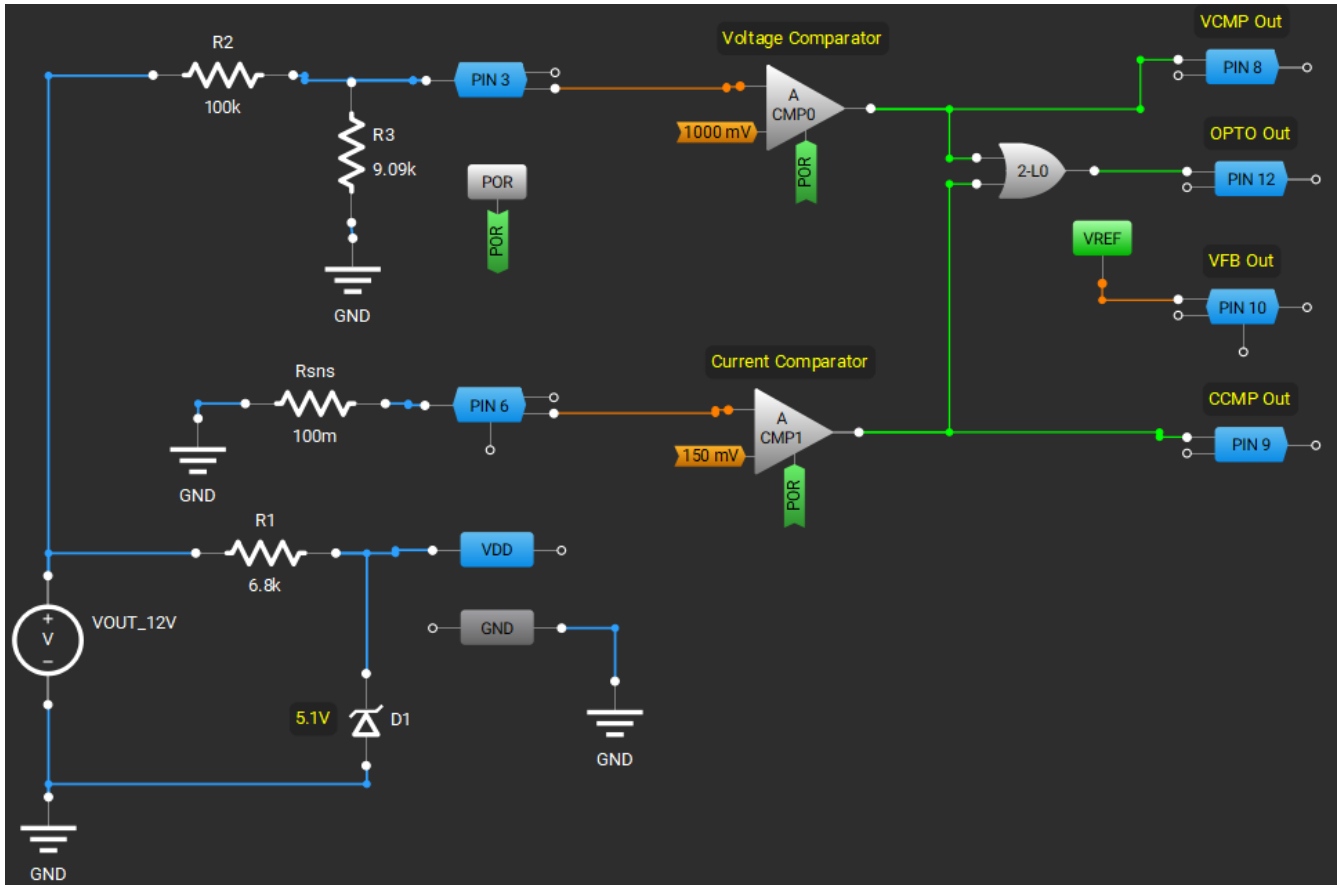


Figure 3. SLG46110 Sensing Output Voltage and Output Current

The simulation shown in Figure 3 comes programmed into the SLG46110 IC on the SLG46110-DIP evaluation board which can then be plugged into the SLG47115+SLG46110 Flyback Evaluation Board. Because each IC or DIP EVB can only be programmed once, the configurations of the Voltage Comparator and Current Comparator thresholds and gains cannot be modified.

However, the output voltage can be changed by modifying the values of R2 and R3, and the output current limit can be adjusted by changing the value of R1. For different voltage or feedback thresholds inside the SLG46110 IC, a fresh SLG46110-DIP can be programmed and substituted for the one that comes with the flyback EVB.

3. Standalone Mode Operation

The processes described in this section assume that the flyback evaluation board is being used in Standalone Mode, where the onboard linear regulator U1 provides power to both the VDD and VDD2 nets. Please ensure that Jumper J8 is installed for Standalone Mode, and refer to section 8 Emulation of Different Configurations for details on Emulation Mode.

3.1 Startup

To begin operation the SLG47115 and SLG46110 based flyback converter requires valid voltages to be present at the SLG47115's VDD and VDD2 pins as well as requires a voltage source connected at the VIN terminal. V_{DD} can range from 2.6 V up to 5.5 V and V_{DD2} can range from 4.5 V up to 26.4 V. For simplicity, a linear regulator takes the 10 V to 14 V input and generates 5.0 V to power both the VDD and VDD2 pins. V_{DD} governs all the logic functions of the SLG47115, whereas V_{DD2} is used for the input to the internal half-bridges, making it the gate drive voltage for Q1. See section 4.6 Selecting the Control MOSFET for advice on MOSFET selection for Q1 as well as selecting the appropriate gate drive voltage.

Timer block CNT3/DLY3 begins counting as soon as V_{DD} is up and valid. CNT3/DLY3 waits for one millisecond before providing a logic HIGH to LUT4 in order to make sure that CCMP is operational, as the analog blocks of the SLG47115 need several hundred additional microseconds after POR to become active. LUT4 also receives the “No HB Faults” signal from the HV OUT CTRL block, making sure that neither the internal Over Current Protection nor the Over Temperature Protection circuits have been tripped. The last input to LUT4 is an external signal from PIN 14 (ENABLE). PIN 14 is configured as a digital input with a Schmitt trigger, and an external logic HIGH is required to turn on the flyback converter. Switching commences when all the conditions for LUT4 have been met.

The SLG46110 is unpowered at startup as it relies on a 5.1 V zener diode and a dropping resistor from V_{OUT} to provide its V_{DD} . Until the SLG46110 becomes active, the switching duty cycle is governed by CCMP and the Minimum Off-time block of the SLG47115. Once the SLG46110 has a valid V_{DD} (1.71 V is the minimum) then its Voltage Comparator (CMP0) and Current Comparator (CMP1) begin monitoring the output voltage and output current respectively and can send control pulses to the primary side.

3.2 Steady State

The heart of the controller for this switching regulator is DFF3, which is configured as an SR flip flop where the CLK pin acts as the SET input and the RESET pin acts as the RESET input. In steady state operation, DFF3's output (Q) is set by the signal at PIN 19, which is the output of the SLG46110 coming in via an optocoupler. The logic HIGH from DFF3 turns on the high side FETs and turns off the low side FETs of the internal half-bridges, forcing the gate of external MOSFET Q1 to V_{DD2} . This turns on Q1's channel and allows current to begin rising in the primary of the flyback transformer.

Once DFF3 is set, the Maximum On-time counter (CNT1/DLY1) begins. Normally the fast current comparator CCMP resets DFF3, but if anything goes wrong and it fails to do so, CNT1/DLY1 is OR'd to DFF3's RESET pin which prevents the On-time from exceeding 20 μ s. The threshold that trips CCMP is set by the user. Between the programmable gain and the programmable threshold, voltages ranging from just 4 mV up to 504 mV are possible. The primary current sense resistor is also selected by the user, providing a wide range of peak currents. Please refer to section [4.2 Transformer Design and Peak Primary Current Selection](#) for guidance on selecting the peak current.

As soon as CCMP or CNT1/DLY1 have reset DFF3, the low side FETs of the internal half-bridges turn on and the high side FETs turn off, forcing the gate of Q1 to nearly zero volts. CCMP has a response time of 350 ns (typical) that serves as the blanking time, preventing CCMP from tripping accidentally right as Q1 turns on. Without this delay, the voltage transient resulting from the discharge of the capacitances at the switching node of the flyback converter can possibly turn Q1 off prematurely. There is an additional propagation delay after CCMP trips as the gates between CCMP and the HB block typically will add another 300 ns delay. For simplicity, this has been summed to a total of 650 ns (t_{CCMP}).

When CCMP has tripped, current flow in the primary is cut off. The magnetic field in the transformer reverses polarity and the current flows in the secondary. The logic LOW at DFF3's Q output also starts the Minimum Off-time block (CNT2/DLY2). CNT2/DLY2 prevents Off-times of less than 2.52 μ s and provides some noise immunity in case the SLG46110's circuitry is tripped inadvertently. CNT2/DLY2 also limits the maximum switching frequency by setting a minimum switching period which ensures that a minimum amount of energy is transferred to the output on every cycle.

During steady state, the SLG46110's voltage and current comparator outputs are OR'd together so that either one can send a signal through the optocoupler to turn Q1 back on.

3.3 Minimizing Propagation Delay Using a Fast Optocoupler

Most isolated flyback regulators use optocouplers with NPN-type phototransistors at their outputs to transfer an analog feedback (error) signal with a bandwidth less than 10 kHz. The PS2381-1 is a good example of such an optocoupler. For this pulse-based system the feedback is essentially digital and the PS2381-1's typical rise and fall times of 4 μ s and 5 μ s, respectively, can possibly use up an entire switching cycle. Furthermore, the pull-up

resistor needed for the emitter of the phototransistor can possibly consume power constantly, compromising the converter's light load power efficiency.

Renesas offers a family of high speed optocouplers with CMOS, push-pull output stages. The RV1S9160A is selected for this application as it operates at 3.3 V or 5 V on both sides of its isolation barrier and has a total propagation delay of 60 ns maximum (both HIGH to LOW and LOW to HIGH). Furthermore, its photodiode achieves those tiny delays with 3 mA of drive current, and no pull-up resistor is needed at its output. During startup when no drive current is available at the photodiode side, the RV1S9160A's output stage defaults to a logic HIGH. The SLG47115's LUTs can accommodate any logic polarity, so the logic HIGH to turn on the control FET Q1 makes the system straightforward by associating the optocoupler's "HIGH" with "increasing" energy transmission.

4. Designing with Peak Current Hysteretic Control

4.1 Electrical Specifications

The accompanying Excel worksheet for this application note is based upon control combining variable frequency with constant peak primary current and operation in continuous conduction mode (CCM) at maximum load, hence the term "peak current hysteretic control". The selected external characteristics are as follows:

- Input voltage range: $V_{IN_MIN} = 10\text{ V}$, $V_{IN_NOM} = 12\text{ V}$, $V_{IN_MAX} = 14\text{ V}$
- Target output voltage: $V_{O_TGT} = 12\text{ V} \pm 2\%$
- Maximum continuous output current: $I_{O_MAX} = 1.0\text{ A}$
- Estimated power efficiency: $\eta = 89\%$ (at maximum load)
- Target switching frequency at nominal V_{IN} and maximum load: $f_{SW_TGT} = 150\text{ kHz}$
- Maximum drain-source voltage of the primary power N-MOSFET, Q1: $V_{BR_DS} = 80\text{ V}$
- Maximum reverse blocking voltage of the secondary output Schottky diode: $V_{RRM_MAX} = 60\text{ V}$.

A note about the estimation for power efficiency – some allowances are made for this application note. The initial estimate was 80 % power efficiency, but the prototype performed surprisingly well, yielding 89 % efficiency at maximum load. As a result, the input currents changed by around 10%, with effects that trickled down the following calculations which yielded discrepancies between predictions and lab results. Therefore, a complete iteration was performed. In practice, the more power converters an engineer builds, the more accurate their initial estimates for everything will be, and the less iterations will be needed for satisfactory results.

The fixed internal parameters of the SLG47115 and SLG46110 that affect the timing of the hysteretic control are as follows:

- SLG47115 CCMP response time (typical): $t_{CCMP} = 650\text{ ns}$.

To make calculations more accurate, the forward voltage of the output Schottky diode when the maximum output current flows is estimated:

- Output diode forward voltage: $V_{F1} = 0.5\text{ V}$.

The next parameters are for the inverting inputs of the SLG46110's Voltage Comparator (CMP0) and Current Comparator (CMP1):

- Voltage Comparator CMP0 reference: $V_{FBV} = 1.0\text{ V}$
- Current Comparator CMP1 reference: $V_{FBC} = 150\text{ mV}$.

The voltage feedback divider resistors are then selected. If no other requirements exist, then 100 k Ω 1 % is a good compromise between power dissipation and noise immunity for the upper resistor:

- Upper voltage feedback resistor: $R_{FB1} = 100\text{ k}\Omega\ 1\%$.

The calculated lower feedback resistor is determined by:

$$R_{FB2_CALC} = R_{FB1} \times \left(\frac{V_{O_TGT}}{V_{FBV}} - 1 \right) = 100\text{ k}\Omega \times \left(\frac{12\text{ V}}{1\text{ V}} - 1 \right) = 9.09\text{ k}\Omega$$

EQ 4.1

One of the benefits of a user-selectable reference voltage is that adjustments can be made easily on a fresh GreenPAK IC. For example, a reference voltage can be selected to line up with standard values. 9.09 is an E96 1 % value, hence the SLG46110-DIP comes with 1.0 V for V_{FBV} :

- Lower voltage feedback resistor: $R_{FB2} = 9.09 \text{ k}\Omega$ 1 %.

Due diligence still requires that the actual output voltage is calculated with the selected feedback resistors:

$$V_{OUT} = V_{FBV} \times \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = 1.0 \text{ V} \times \frac{100 \text{ k}\Omega + 9.09 \text{ k}\Omega}{9.09 \text{ k}\Omega} = 12.0 \text{ V}$$

EQ 4.2

Now, the maximum output power is calculated as:

$$P_{O_MAX} = I_{O_MAX} \times (V_{OUT} + V_{F1}) = 1 \text{ A} \times (12 \text{ V} + 0.5 \text{ V}) = 12.5 \text{ W}$$

EQ 4.3

The maximum input power is then estimated. This will be used for various peak and RMS current calculations:

$$P_{IN_MAX} = \frac{P_{O_MAX}}{\eta} = \frac{12.5 \text{ W}}{0.89} = 14.1 \text{ W}$$

EQ 4.4

4.2 Transformer Design and Peak Primary Current Selection

The magnetic element is the foundation of any switching regulator. The following calculations provide the basic parameters for a flyback transformer that can be passed to a dedicated magnetics designer for refinement, prototyping, and production.

To begin, de-rating factors for the primary N-MOSFET and secondary diode are selected. For low voltages (< 100 V), typical de-ratings of 10 % are given for both:

- Primary MOSFET voltage de-rating: $K_{PRI} = 10 \%$
- Secondary rectifier voltage de-rating: $K_{SEC} = 10 \%$.

The maximum primary and secondary voltages for Q1 and D1 are calculated as follows:

$$V_{DS_MAX} = V_{BR_DS} \times \left(1 - \frac{K_{PRI}}{100}\right) = 80 \text{ V} \times \left(1 - \frac{10}{100}\right) = 72 \text{ V}$$

EQ 4.5

$$V_{D1_MAX} = V_{RRM} \times \left(1 - \frac{K_{SEC}}{100}\right) = 60 \text{ V} \times \left(1 - \frac{10}{100}\right) = 54 \text{ V}$$

EQ 4.6

Next, an estimate is needed for the transient voltage that appears across Q1 each time it turns off. The cause of this transient is the energy stored in the leakage inductance of the flyback transformer while current flows in the primary. A clamping circuit is needed in most cases to prevent this transient (often called the “leakage inductance spike”) from exceeding Q1’s V_{BR_DS} . These clamping circuits and their designs can take many forms, but for now a maximum is needed, regardless of how it is achieved. The following is one method of calculation that has proven effective for Renesas Applications Engineering. It is based upon setting the target clamp voltage to the midpoint between the maximum input voltage and the maximum permissible drain-to-source voltage of Q1:

$$V_{CLAMP_1ST} = \frac{V_{DS_MAX} - V_{IN_MAX}}{2} = \frac{72 \text{ V} - 14 \text{ V}}{2} = 29 \text{ V}$$

EQ 4.7

- Target value for leakage inductance clamp voltage: $V_{CLAMP_TGT} = 30 \text{ V}$.

The minimum permissible primary-to-secondary turns ratio is based on keeping the reverse voltage blocked by D1 from exceeding V_{D1_MAX} , and is calculated as follows:

$$N_{PS_MIN} = \frac{V_{IN_MAX} \times (1 + K_{SEC}/100)}{V_{D1_MAX} - V_{O1}} = \frac{14 V \times (1 + 0.1)}{54 V - 12 V} = 0.3$$

EQ 4.8

Preventing Q1 from overvoltage forms the basis of the maximum permissible turns ratio:

$$N_{PS_MAX} = \frac{V_{DS_MAX} - V_{IN_MAX} - V_{SPIKE_1ST}}{V_{OUT}} = \frac{72 V - 14 V - 30 V}{12 V} = 2.2$$

EQ 4.9

In most cases the best target primary-to-secondary turns ratio is right in the middle between the min and max value, which would be ~1.2:1. For this circuit, an off-the-shelf flyback transformer fitting the requirements for this flyback converter was found that has a ratio of 1.33:1.

- Target primary-to-secondary turns ratio: $N_{PS_TGT} = 1.33:1$.

Now the voltage reflected to the primary side of the transformer while the secondary conducts can be calculated:

$$V_{OR} = N_{PS_TGT} \times (V_{OUT} + V_{F1}) = 1.33 \times (12 V + 0.5 V) = 17 V$$

EQ 4.10

At this point it's important to compare and make sure that V_{OR} is less than the target leakage clamp voltage, V_{CLAMP_TGT} . Otherwise, this circuit will try to clamp the reflected voltage from the secondary during core demagnetization, which will always result in overheating and damage to the clamp components. As 17 V is less than 30 V, this is a non-issue.

A check of the peak predicted voltage across Q1 while it is off:

$$V_{DS_PK} = V_{IN_MAX} + V_{OR} + V_{CLAMP_1ST} = 14 V + 17 V + 30 V = 61 V$$

EQ 4.11

Power supply engineers familiar with flyback converters will agree that having some margin to spare for peak primary MOSFET voltage is always beneficial, particularly because the leakage inductance spike is a function of parasitics, making it very difficult to simulate accurately. A conservative peak primary voltage will ease the process of getting the converter working and then refined further in the lab.

The next flyback transformer parameter is its primary magnetizing inductance, which requires several calculations in sequence to determine, starting with the duty cycle. In continuous conduction mode (CCM) operation, the duty cycle varies little with respect to the output current or the frequency. This makes it possible to estimate the duty cycle over the input voltage range:

$$D_{MIN} = \frac{N_{PS_TGT} \times V_{OUT}}{V_{IN_MAX} + N_{PS_TGT} \times (V_{OUT} + V_{F1})} = \frac{1.0 \times 12 V}{14 V + 1.33 \times (12 V + 0.5 V)} = 0.54$$

EQ 4.12

$$D_{NOM} = \frac{N_{PS_TGT} \times V_{OUT}}{V_{IN_NOM} + N_{PS_TGT} \times (V_{OUT} + V_{F1})} = \frac{1.0 \times 12 V}{12 V + 1.33 \times (12 V + 0.5 V)} = 0.58$$

EQ 4.13

$$D_{MAX} = \frac{N_{PS_TGT} \times V_{OUT}}{V_{IN_MIN} + N_{PS_TGT} \times (V_{OUT} + V_{F1})} = \frac{1.0 \times 12 V}{10 V + 1.33 \times (12 V + 0.5 V)} = 0.62$$

EQ 4.14

Next, the average input currents at maximum load are evaluated over the complete V_{IN} range:

$$I_{IN_MIN} = \frac{P_{IN_MAX}}{V_{IN_MAX}} = \frac{14.1 W}{14 V} = 1.01 A$$

EQ 4.15

$$I_{IN_NOM} = \frac{P_{IN_MAX}}{V_{IN_NOM}} = \frac{14.1 W}{12 V} = 1.17 A$$

EQ 4.16

$$I_{IN_MAX} = \frac{P_{IN_MAX}}{V_{IN_MIN}} = \frac{14.1\text{ W}}{10\text{ V}} = 1.41\text{ A}$$

EQ 4.17

CCM flyback converters are characterized by the trapezoidal wave currents that flow through their primary windings. The secondary current also takes the shape of a trapezoid wave. In most CCM designs, the inductance is selected to achieve a target ratio of the average of the trapezoid's pedestal to the peak and valley of that pedestal. Figure 4 shows this concept visually for clarity.

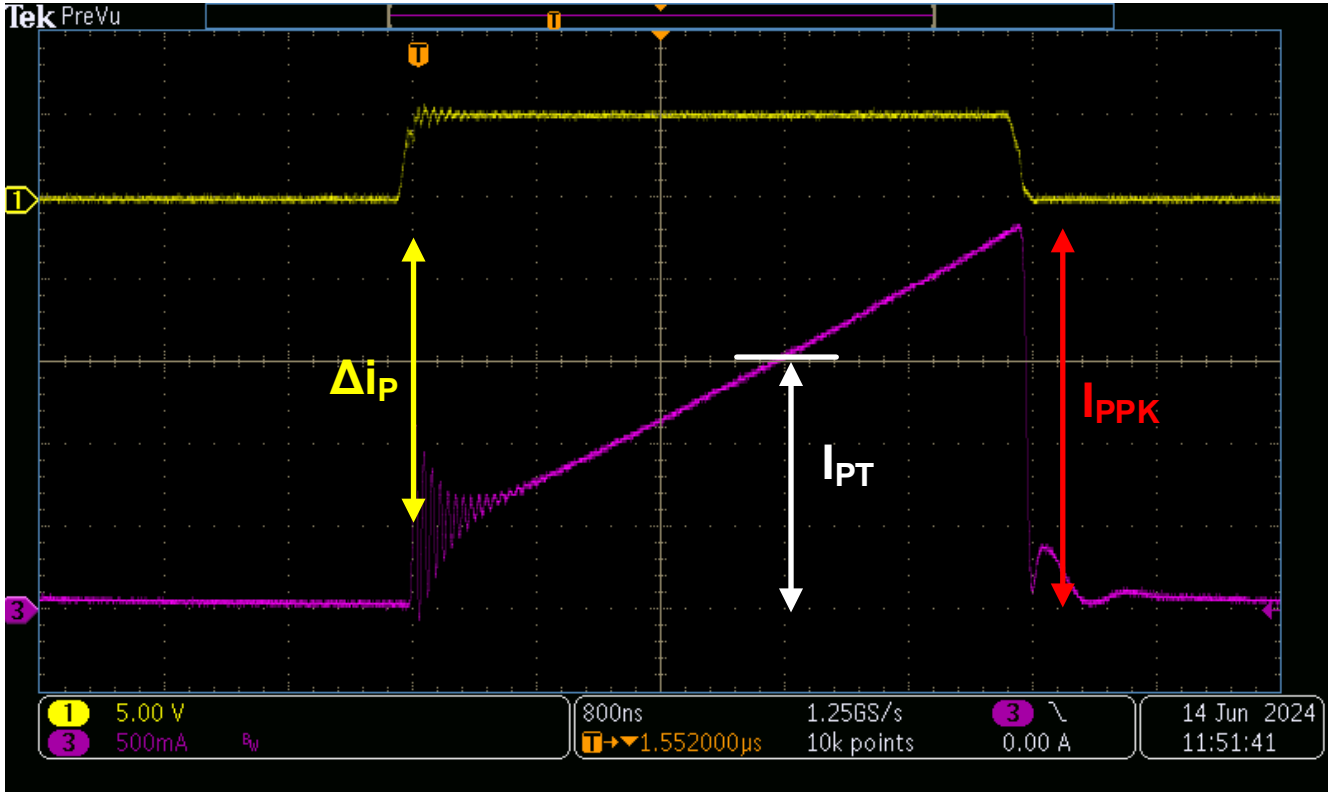


Figure 4. Ch.1 = Q1 V_{GS} , Ch.3 = Primary Current. I_{PT} is the Average of the Trapezoidal Pedestal

The primary current pedestals are calculated as follows:

$$I_{PT_MIN} = \frac{I_{IN_MIN}}{D_{MIN_CALC}} = \frac{1.01\text{ A}}{0.54} = 1.85\text{ A}$$

EQ 4.18

$$I_{PT_NOM} = \frac{I_{IN_NOM}}{D_{NOM_CALC}} = \frac{1.17\text{ A}}{0.58} = 2.02\text{ A}$$

EQ 4.19

$$I_{PT_MAX} = \frac{I_{IN_MAX}}{D_{MAX_CALC}} = \frac{1.41\text{ A}}{0.62} = 2.26\text{ A}$$

EQ 4.20

Next, the desired ripple current to pedestal current ratio needs to be selected. A common starting point is 40 %, and is used in the following:

- Target primary ripple-to-pedestal current ratio: $\Delta i_{P\%} = 40\%$.

$$\Delta i_{P_TGT} = I_{PT_NOM} \times \frac{\Delta i_{P\%}}{100} = \frac{2.02\text{ A} \times 40}{100} = 0.81\text{ A}$$

EQ 4.21

At this point the design philosophy diverges from fixed frequency converters with variable peak currents in favor of getting as close as possible to the target switching frequency at the nominal input voltage. The peak primary current needed to deliver the full output power at nominal input voltage is calculated by:

$$I_{PK_TGT} = I_{PT_NOM} + \frac{\Delta i_{PT_TGT}}{2} = 2.02 A + \frac{0.81 A}{2} = 2.43 A$$

EQ 4.22

The user programs the actual, fixed peak current that the converter will use by selecting the current sense voltage (the reference voltage for CCMP inside the SLG47115) and then selecting the value of the sense resistor itself. Starting with the next highest current above I_{PK_TGT} is recommended. Renesas Applications Engineering has found that a sense voltage ranging from 100 mV to 500 mV provides a balance between good accuracy and low power dissipation in the sense resistor. From a cost perspective, 100 mΩ is a very common value available with 1 % tolerance in a wide variety of sizes, power dissipations, and materials. Choosing this value also makes the math easy to calculate.

- Selected primary current sense resistor: $R_{SNS} = 100 \text{ m}\Omega$ 1 %, size and power will be determined later.

CCMP's reference voltage (V_{SNS}) is programmable in 32 mV steps and supports either 4 V/V or 8 V/V gain.

Figure 5 shows the selected combination, which yields a V_{SNS} of 288 mV. This value was determined from lab testing, which confirmed that having lower peak currents can prevent the flyback from reaching full output power at the minimum input voltage of 10 V.

Figure 5. Programming CCMP's Inverting Threshold, V_{SNS} , to 288 mV

With the peak primary current set:

$$I_{PK_PROG} = \frac{V_{SNS}}{R_{SNS}} = \frac{288 \text{ mV}}{100 \text{ m}\Omega} = 2.88 A$$

EQ 4.23

Finally, to calculate the desired primary inductance we use the formula:

$$L_{P_CALC} = \frac{V_{IN_NOM} \times D_{NOM_CALC}}{2 \times f_{SW_TGT} \times (I_{PK_PROG} - I_{PT_NOM})} = \frac{12 V \times 0.58}{2 \times 150 \text{ kHz} \times (2.88 A - 2.02 A)} = 17.3 \mu H$$

EQ 4.24

If using a custom transformer, then the target primary inductance can be set to exactly 17.3 μH with a typical tolerance of ±10 %.

In this case, an off-the-shelf part was selected, the Würth Elektronik 7491195212. This part has a primary inductance of 21 μH. Using a different inductance will affect the ripple current and therefore affect the frequency, but by selecting an off-the-shelf transformer, a large amount of development time is saved.

- Selected primary magnetizing inductance: $L_P = 21 \mu\text{H}, \pm 10 \%$.

The 650 ns (typical) total response time for the CCMP (which helps with noise immunity during the turn-on of Q1) becomes a source of error in the actual peak primary currents during turn-off. This 650 ns response time is added to the calculated on-time, resulting in a higher peak primary current. The following calculations account for the increase, which varies with the input voltage:

$$I_{PPK_VMIN} = I_{PK_PROG} + \frac{V_{IN_MIN} \times t_{CCMP}}{L_P} = 2.88 \text{ A} + \frac{10 \text{ V} \times 650 \text{ ns}}{21 \mu\text{H}} = 3.19 \text{ A} \quad \text{EQ 4.25}$$

$$I_{PPK_VNOM} = I_{PK_PROG} + \frac{V_{IN_NOM} \times t_{CCMP}}{L_P} = 2.88 \text{ A} + \frac{12 \text{ V} \times 650 \text{ ns}}{21 \mu\text{H}} = 3.25 \text{ A} \quad \text{EQ 4.26}$$

$$I_{PPK_VMAX} = I_{PK_PROG} + \frac{V_{IN_MAX} \times t_{CCMP}}{L_P} = 2.88 \text{ A} + \frac{14 \text{ V} \times 650 \text{ ns}}{21 \mu\text{H}} = 3.31 \text{ A} \quad \text{EQ 4.27}$$

More accurate calculations of the peak-to-peak primary ripple current can also be made in order to calculate the worst case (highest) RMS current flowing in the transformer primary and in MOSFET Q1:

$$\Delta i_{P_VMIN} = 2 \times (I_{PPK_VMIN} - I_{PT_MAX}) = 2 \times (3.19 \text{ A} - 2.26 \text{ A}) = 1.86 \text{ A} \quad \text{EQ 4.28}$$

$$\Delta i_{P_VNOM} = 2 \times (I_{PPK_VNOM} - I_{PT_NOM}) = 2 \times (3.25 \text{ A} - 2.02 \text{ A}) = 2.46 \text{ A} \quad \text{EQ 4.29}$$

$$\Delta i_{P_VMAX} = 2 \times (I_{PPK_VMAX} - I_{PT_MIN}) = 2 \times (3.31 \text{ A} - 1.85 \text{ A}) = 2.92 \text{ A} \quad \text{EQ 4.30}$$

In practice the highest RMS currents occur when V_{IN} is at the minimum. This calculation can be used to calculate the conduction losses in Q1 and can also be used to select the wire gauge and type for a custom transformer design:

$$I_{P_RMS_VMIN} = \sqrt{D_{MAX_CALC} \times \left(I_{PPK_VMIN}^2 + \frac{\Delta i_{P_VMIN}^2}{3} - I_{PPK_VMIN} \times \Delta i_{P_VMIN} \right)} \quad \text{EQ 4.31}$$

$$I_{P_RMS_VMIN} = \sqrt{0.62 \times \left(3.19 \text{ A}^2 + \frac{1.86 \text{ A}^2}{3} - 3.19 \text{ A} \times 1.86 \text{ A} \right)} = 1.83 \text{ A} \quad \text{EQ 4.32}$$

Recall that the case size and power rating of the primary current sense resistor were left to be determined earlier in this section. Now that the maximum RMS current through this resistor is known, these details can be finalized.

Power dissipation is calculated by $1.83 \text{ A}^2 \times 100 \text{ m}\Omega = 0.33 \text{ W}$. A single 0.5 W, 1206-sized thick-film resistor will be used. However, a second, blank, 1206 footprint is added in parallel. This extra footprint can be very useful for other, high-power applications.

For engineers who want to build their own magnetics or want to provide more detailed specifications to their magnetics design partners, the following will cover core selection and the number of windings for the primary and secondary. To begin, the maximum permissible magnetic flux density must be defined. 0.3 T is a common choice for general-purpose power supplies and provides a balance between core utilization, size, and cost.

- Selected magnetic flux density limit for core: $B_{MAX} = 0.3 \text{ T}$.

The effective core cross-sectional area is the next parameter needed, but this requires a core to be selected first. The number of magnetic core shapes, sizes, and materials can be overwhelming at first, so for less experienced designers, one suggested starting point is to look at existing, off-the-shelf designs. Core volume is proportional to output power, so after a few designs a range of core shape and size combinations can be drawn from experience.

For example, the Würth 7491195212 uses an EP13 core with an effective cross-sectional area of 20 mm². A survey of global ferrite core manufacturers that use the EP13 shape yields two materials that would be good candidates: 3C96 from Yageo-Ferroxcube and N87 from TDK-Epcos. Note that the main parameters evaluated when selecting these two materials are power loss versus flux density and power loss versus frequency.

- Selected magnetic core: EP13
- Selected core's effective cross-sectional area: $A_E = 20 \text{ mm}^2$
- Selected core material: 3C96, N87, or equivalent.

The minimum number of turns can now be selected, starting with either the primary or the secondary. Here, peak primary current has been carefully set and adjusted for comparator delays so the design will be more accurate with calculating the primary turns:

$$N_{P_MIN} = \frac{L_P \times I_{PPK_VMAX}}{B_{MAX} \times A_E} = \frac{21 \mu\text{H} \times 3.31 \text{ A}}{0.3 \text{ T} \times 20 \text{ mm}^2} = 11.6$$

EQ 4.33

When the turns ratio N_{PS_TGT} is greater than "1", it is often simpler to divide the result of EQ.32 by N_{PS_TGT} to find the minimum secondary turns, and then select the next whole number greater than that value. This helps generate results with whole numbers of turns, as fractional numbers of turns are very difficult to build in practice.

$$N_{S_MIN} = \frac{N_{P_MIN}}{N_{PS_TGT}} = \frac{11.6}{1.33} = 9$$

EQ 4.34

The next highest whole number is nine itself, so the selected number of secondary turns is set to nine. This yields a whole number of primary turns.

- Selected number of secondary turns: $N_S = 9$.

$$N_P = N_S \times n_{PS} = 9 \times 1.33 = 12$$

EQ 4.35

- Selected number of primary turns: $N_P = 12$.

In most flyback designs, significant effort is required to identify and calculate the worst-case, highest peak current in order to make sure the transformer core won't saturate under those conditions. Here, the worst-case peak current is already well-defined thanks to the control type and EQ.6.27, I_{PPK_VMAX} . This value is then used to check the peak flux density in the core:

$$B_{PK} = \frac{L_P \times I_{PPK_VMAX}}{N_P \times A_E} = \frac{21 \mu\text{H} \times 3.31 \text{ A}}{12 \times 20 \text{ mm}^2} = 0.29 \text{ T}$$

EQ 4.36

This is below the limit of 0.3 T, implying that this transformer is being slightly under-utilized. On the positive side, there is no danger of saturation at maximum load. Also, some margin exists for higher output power or lower minimum input voltage if needed. On the negative side, the transformer itself could be made smaller or cheaper. Overall, these are the trade-offs that must be considered when deciding whether to use off-the-shelf vs. custom magnetics.

To complete the specifications for this flyback transformer, the secondary inductance and currents are now evaluated. Secondary inductance is calculated by:

$$L_S = \frac{L_P}{N_{PS}^2} = \frac{21 \mu\text{H}}{1.33^2} = 11.8 \mu\text{H}$$

EQ 4.37

Figure 6 shows a capture of the secondary current as a visual aid:

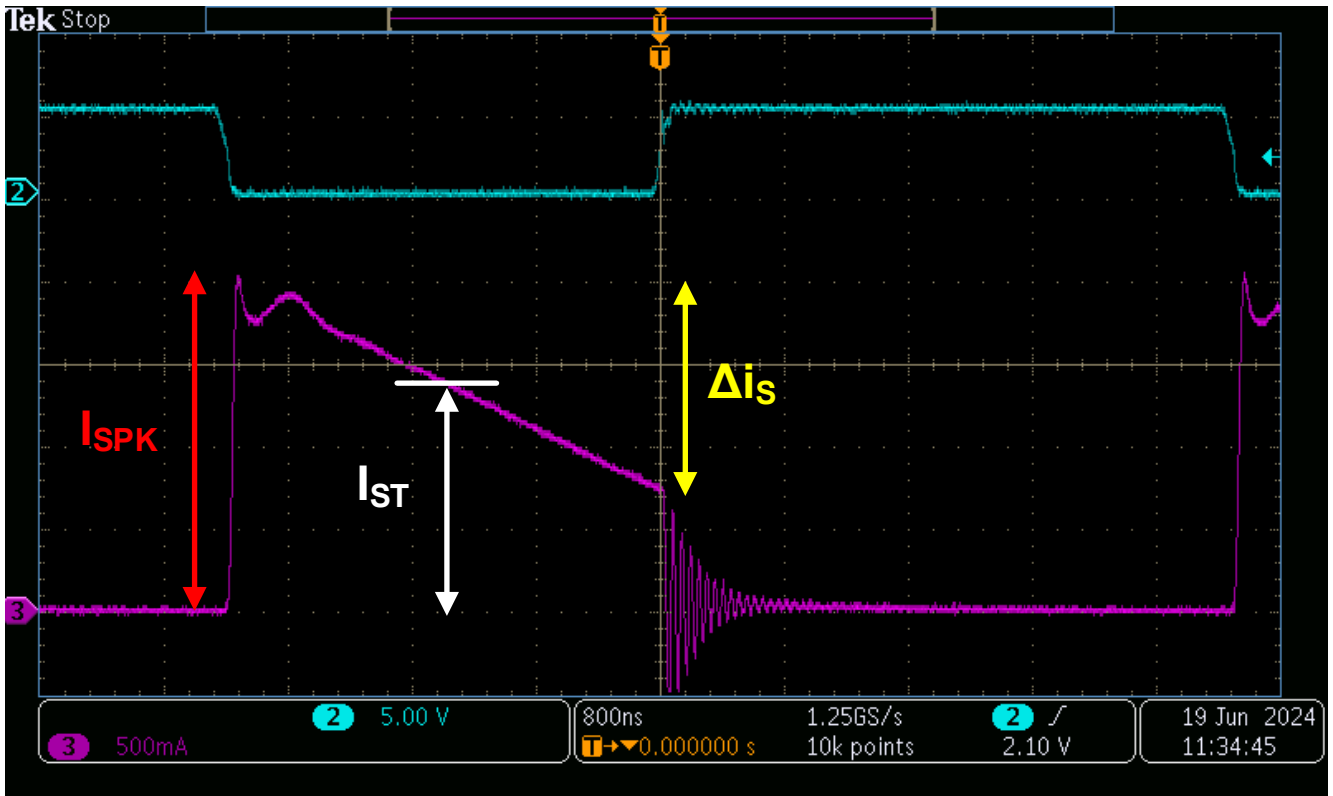


Figure 6. Secondary current with key aspects labeled. Ch.2 is the Gate of Q1

To begin, the peak secondary currents are calculated:

$$I_{SPK_VMIN} = I_{PPK_VMIN} \times N_{PS} = 3.19 \text{ A} \times 1.33 = 4.25 \text{ A} \tag{EQ 4.38}$$

$$I_{SPK_VNOM} = I_{PPK_VNOM} \times N_{PS} = 3.25 \text{ A} \times 1.33 = 4.34 \text{ A} \tag{EQ 4.39}$$

$$I_{SPK_VMAX} = I_{PPK_VMAX} \times N_{PS} = 3.31 \text{ A} \times 1.33 = 4.42 \text{ A} \tag{EQ 4.40}$$

As with the primary current, the average of the trapezoid wave's pedestals is next:

$$I_{ST_VMIN} = \frac{I_{O_MAX}}{1 - D_{MAX_CALC}} = \frac{1 \text{ A}}{1 - 0.62} = 2.66 \text{ A} \tag{EQ 4.41}$$

$$I_{ST_VNOM} = \frac{I_{O_MAX}}{1 - D_{NOM_CALC}} = \frac{1 \text{ A}}{1 - 0.58} = 2.39 \text{ A} \tag{EQ 4.42}$$

$$I_{ST_VMAX} = \frac{I_{O_MAX}}{1 - D_{MIN_CALC}} = \frac{1 \text{ A}}{1 - 0.54} = 2.19 \text{ A} \tag{EQ 4.43}$$

Then the peak-to-peak ripple currents:

$$\Delta i_{SV_MIN} = 2 \times (I_{SPK_VMIN} - I_{ST_VMIN}) = 2 \times (4.25 \text{ A} - 2.66 \text{ A}) = 3.18 \text{ A} \tag{EQ 4.44}$$

$$\Delta i_{SV_NOM} = 2 \times (I_{SPK_VNOM} - I_{ST_VNOM}) = 2 \times (4.34 \text{ A} - 2.39 \text{ A}) = 3.90 \text{ A} \tag{EQ 4.45}$$

$$\Delta i_{SV_MAX} = 2 \times (I_{SPK_VMAX} - I_{ST_VMAX}) = 2 \times (4.42 A - 2.19 A) = 4.46 A$$

EQ 4.46

Only the worst-case, maximum calculation of secondary RMS current is needed. In a custom transformer, it is used to select the wire type and gauge for the secondary. Here, it is used to predict the losses in the output diode and used in part of the calculation of the AC ripple current in the output capacitor(s). In peak current hysteretic control, the highest secondary RMS current occurs at the maximum input voltage:

$$I_{S_RMS_MAX} = \sqrt{(1 - D_{MIN_CALC}) \times \left(I_{SPK_VMAX}^2 + \frac{\Delta i_{SV_MAX}^2}{3} - I_{SPK_VMAX} \times \Delta i_{SV_MAX} \right)}$$

EQ 4.47

$$I_{S_RMS_MAX} = \sqrt{(1 - 0.54) \times \left(4.42 A^2 + \frac{4.46 A^2}{3} - 4.42 A \times 4.46 A \right)} = 1.72 A$$

EQ 4.48

In summary, the following specifications have been calculated for the flyback transformer:

- Core shape and size: EP13
- Core material: 3C96, N87, or equivalent
- Primary magnetizing inductance: $L_P = 21 \mu H$, $\pm 10\%$
- Primary-to-secondary turns ratio: $N_{PS} = 1.33:1$
- Selected number of primary turns: $N_P = 12$
- Selected number of secondary turns: $N_S = 9$
- Peak primary current: 3.31 A
- Maximum RMS primary current: 1.83 A
- Peak secondary current: 4.42 A
- Maximum RMS secondary current: 1.72 A.

4.3 Timing, Duty Cycles, and Switching Frequency

With all the transformer currents and inductances calculated, the on-times (when Q1 conducts) and off-times (when D1 conducts) can be re-evaluated with better precision. This in turns leads to more accurate duty cycle and switching frequency predictions. To begin, for the on-times:

$$t_{ON_MIN} = \frac{L_P \times \Delta i_{P_VMIN}}{V_{IN_MIN}} = \frac{21 \mu H \times 1.86 A}{10 V} = 3.92 \mu s$$

EQ 4.49

$$t_{ON_NOM} = \frac{L_P \times \Delta i_{P_VNOM}}{V_{IN_NOM}} = \frac{21 \mu H \times 2.46 A}{12 V} = 4.3 \mu s$$

EQ 4.50

$$t_{ON_MAX} = \frac{L_P \times \Delta i_{P_VMAX}}{V_{IN_MAX}} = \frac{21 \mu H \times 2.92 A}{14 V} = 4.38 \mu s$$

EQ 4.51

The off-times are calculated in similar fashion:

$$t_{OFF_MIN} = \frac{L_S \times \Delta i_{S_VMIN}}{V_{OUT}} = \frac{11.8 \mu H \times 3.18 A}{12 V} = 3.13 \mu s$$

EQ 4.52

$$t_{OFF_NOM} = \frac{L_S \times \Delta i_{S_VNOM}}{V_{OUT}} = \frac{11.8 \mu H \times 3.9 A}{12 V} = 3.84 \mu s$$

EQ 4.53

$$t_{OFF_MAX} = \frac{L_S \times \Delta i_{S_VMAX}}{V_{OUT}} = \frac{11.8 \mu H \times 4.46 A}{12 V} = 4.39 \mu s$$

EQ 4.54

Now, both switching frequency and duty cycle can be calculated:

$$D_{VMIN} = \frac{t_{ON_MIN}}{t_{ON_MIN} + t_{OFF_MIN}} = \frac{3.92 \mu s}{3.92 \mu s + 3.13 \mu s} = 0.56$$

EQ 4.55

$$D_{VNOM} = \frac{t_{ON_NOM}}{t_{ON_NOM} + t_{OFF_NOM}} = \frac{4.3 \mu s}{4.3 \mu s + 3.84 \mu s} = 0.53$$

EQ 4.56

$$D_{VMAX} = \frac{t_{ON_MAX}}{t_{ON_MAX} + t_{OFF_MAX}} = \frac{4.38 \mu s}{4.38 \mu s + 4.39 \mu s} = 0.5$$

EQ 4.57

$$f_{SW_VMIN} = \frac{1}{t_{ON_MIN} + t_{OFF_MIN}} = \frac{1}{3.92 \mu s + 3.13 \mu s} = 142 \text{ kHz}$$

EQ 4.58

$$f_{SW_VNOM} = \frac{1}{t_{ON_NOM} + t_{OFF_NOM}} = \frac{1}{4.3 \mu s + 3.84 \mu s} = 123 \text{ kHz}$$

EQ 4.59

$$f_{SW_VMAX} = \frac{1}{t_{ON_MAX} + t_{OFF_MAX}} = \frac{1}{4.38 \mu s + 4.39 \mu s} = 114 \text{ kHz}$$

EQ 4.60

Recall that the initial target frequency at nominal input voltage was 150 kHz. The combination of selecting a higher primary magnetizing inductance than the calculated value and the delay from the SLG47115's current comparator induces significant error. At this point, the designer can either choose to change the transformer or continue and accept the lower frequency. Variable frequency is a fact of life in hysteretic converters, so for this design the lower frequency is determined to be acceptable, and the design process continues. Note also that [EQ 4.58](#), [EQ 4.59](#) and [EQ 4.60](#) predict the actual switching frequency at max load with good accuracy, as shown in [Figure 18](#) of section 5

Typical Performance.

4.4 Input Capacitors

The input capacitors to a flyback converter must be able endure high AC ripple current due to the pulsed, trapezoid-wave currents they must supply. Figure 4 shows this waveshape, and the input capacitor's AC ripple current has the exact same waveshape except it is centered around zero. The following calculations provide a minimum total input capacitance and maximum total ESR, but in almost all cases the key specification is the AC ripple current rating of the combined input capacitor bank. Whenever capacitor types with an electrolyte that evaporates over time are used, their lifetime is directly affected by the self heating from the AC ripple current and their ESR. Maximum AC ripple current occurs when V_{IN} is at the minimum:

$$I_{CIN_RMS} = \sqrt{I_{P_RMS_VMIN}^2 - I_{IN_MAX}^2} = \sqrt{1.83 A^2 - 1.41 A^2} = 1.17 A$$

EQ 4.61

Any aluminum or polymer capacitor(s) selected should have a total RMS current rating of greater than 1.1 A at 100 kHz or higher. Using two or more capacitors in parallel splits the ripple current and is often less expensive and/or uses less total volume than one large capacitor.

The maximum allowable input voltage ripple to a switching converter is not usually defined as clearly as the output voltage ripple. However, input voltage ripple affects the conducted EMI directly and the radiated EMI indirectly so some limit to the input voltage ripple is necessary. If no other specification is available then 3 % peak-peak of the minimum input voltage can be used. This is low enough to prevent the ripple voltage itself from affecting all the previous calculations that assume this input voltage is constant during a complete switching cycle.

- Target input voltage ripple: $\% \Delta v_{IN_TGT} = 3\%$ of minimum V_{IN} , peak-peak.

$$\Delta v_{IN_MAX} = \% \Delta v_{IN_TGT} \times V_{IN_MIN} = 0.03 \times 10 V = 300 mV_{PP}$$

EQ 4.62

Minimum input capacitance and maximum ESR can be calculated based on Δv_{IN_MAX} . The factors of "2" in the following two expressions have been added based upon Renesas Applications Engineering evaluation. These factors assume that half of the input voltage ripple will come from the discharging of the input capacitors and the other half will come from the peak primary current flowing through their ESR.

$$C_{IN_MIN} = \frac{2 \times I_{IN_MAX} \times D_{VMIN}}{\Delta v_{IN_MAX} \times f_{SW_VMIN}} = \frac{2 \times 1.41 A \times 0.56}{0.3 V \times 142 kHz} = 37 \mu F$$

EQ 4.63

$$ESR_{CIN_MAX} = \frac{\Delta v_{IN_MAX}}{2 \times I_{PPK_VMIN}} = \frac{0.3 V}{2 \times 3.08 A} = 49 m\Omega$$

EQ 4.64

The next highest standard E6 value for capacitance is 33 μF , but a survey of available aluminum capacitors available from global distributors with a rating of 33 μF at either 25 V or 35 V reveals very few that meet the ESR requirement and none that come anywhere close to meeting the ripple current requirement. ESR drops and ripple current rating rises as the physical size of the aluminum capacitors increases, and with larger size/volume comes higher capacitance. As a result, the actual input capacitance will be greater than necessary (as predicted by EQ 4.63 so that the ESR and ripple current ratings can be met.

Nearly all switching power supplies benefit from a mix of capacitor types at their power inputs and outputs. In addition to using a larger value aluminum electrolytic capacitor rated at 330 μF , 35 V, ESR of 60 m Ω , and a rating of 1.19 A_{RMS} at 100 kHz, the input to this circuit will also have one nominal 10 μF , 25 V, 1206, X7R and one nominal 100 nF, 50 V, 0603, X7R MLC capacitor in parallel. All three of these capacitors combine to keep the input impedance low over a broad range of frequencies. The 10 μF MLC capacitor will also absorb some of the RMS ripple current and extend the operational lifetime of the aluminum capacitor while lowering the total ESR of the combined input capacitor bank.

A first-order estimation of the input voltage ripple can be calculated by first determining the impedance of the aluminum input capacitor and then multiplying it by the peak primary current. Real lab results will diverge due to factors such as ESL and the loss of capacitance as the frequency increases – lab testing is absolutely essential.

$$Z_{CIN} = \sqrt{ESR_{CIN}^2 - \left(\frac{1}{8 \times C_{IN} \times f_{SW_VMIN}}\right)^2} = \sqrt{60 \text{ m}\Omega^2 - \left(\frac{1}{8 \times 330 \text{ }\mu\text{F} \times 188 \text{ kHz}}\right)^2} = 60 \text{ m}\Omega$$

EQ 4.65

$$\Delta v_{IN} = I_{PPK_VMIN} \times Z_{CIN} = 3.19 \text{ A} \times 60 \text{ m}\Omega = 193 \text{ mV}$$

EQ 4.66

Figure 44 in section 5

Typical Performance shows that the actual input voltage ripple under the worst-case conditions of minimum input voltage and maximum load is right around 200 mV_{P-P}.

4.5 Output Capacitors

The output capacitors in a flyback converter also contend with heavy RMS ripple currents from the trapezoidal secondary current. As with the input capacitor current (see Figure 6) this same waveshape passes through the output capacitors but is offset so that its average value is zero. The RMS value of the output capacitor ripple current is far from zero however:

$$I_{CO_RMS} = \sqrt{I_{S_RMS}^2 - I_{O_MAX}^2} = \sqrt{1.63 A^2 - 1.0 A^2} = 1.29 A$$

EQ 4.67

For this circuit, the target peak-peak output voltage ripple is 2 % of V_{OUT}:

- Target output voltage ripple: %Δ_{O_TGT} = 2 % of minimum V_{OUT}, peak-to-peak.

$$\Delta v_{O_MAX} = \% \Delta v_{O_TGT} \times V_{OUT} = 0.02 \times 12 V = 240 mV_{PP}$$

EQ 4.68

Minimum output capacitance and maximum ESR are calculated in a nearly identical fashion to the input capacitance. The same factors of “2” are included based on the same assumption that half of the output voltage ripple comes from the peak secondary current passing through the ESR and the other half of the ripple comes from discharging of the capacitor(s) themselves.

$$C_{O_MIN} = \frac{2 \times I_{O_MAX} \times t_{ON_MAX}}{\Delta v_{O_MAX}} = \frac{2 \times 1.0 A \times 4.38 \mu s}{0.24 V} = 37 \mu F$$

EQ 4.69

$$ESR_{CO_MAX} = \frac{\Delta v_{O_MAX}}{2 \times I_{SPK_VMX}} = \frac{0.24 V}{2 \times 4.42 A} = 27 m\Omega$$

EQ 4.70

In practice, SMPS cost is always a factor, and one good way to control cost is to keep the BOM as simple as possible. To this end, the same aluminum electrolytic capacitor used for the input will be used again at the output. However, because of the heavier ripple current and lower maximum ESR, two of these 330 μF parts are used in parallel.

- Total output capacitance: C_{OUT} = 660 μF
- Total ESR: ESR_{CO} = 30 mΩ

In this design one 10 μF, 25 V, X7R, 1206-sized and one 100 nF, 50 V, X7R, 0603-sized MLC output capacitor will be placed in parallel. With their small size and low ESL, their main job will be to filter high frequency parasitic oscillations and transients. The contribution to output ripple voltage at the switching frequency from these MLCCs will be negligible, and they will reduce high frequency switching noise significantly.

To finish, the output voltage ripple can be estimated with the same method as the input voltage ripple by estimating the impedance of the output capacitor bank and multiplying that by the peak secondary current:

$$Z_{CO} = \sqrt{ESR_{CO}^2 - \left(\frac{1}{8 \times C_{OUT} \times f_{SW_VMIN}} \right)^2} = \sqrt{30 m\Omega^2 - \left(\frac{1}{8 \times 660 \mu F \times 143 kHz} \right)^2} = 30 m\Omega$$

EQ 4.71

$$\Delta v_O = I_{SPK_VMIN} \times Z_{CO} = 4.25 A \times 30 m\Omega = 128 mV$$

EQ 4.72

The predicted ripple looks much lower than the limit on paper, but early lab testing without the 10 μF MLCC, C16, exhibited higher ripple due to parasitic capacitances and inductances in real components and from a real PCB. This is shown in Figure 7.

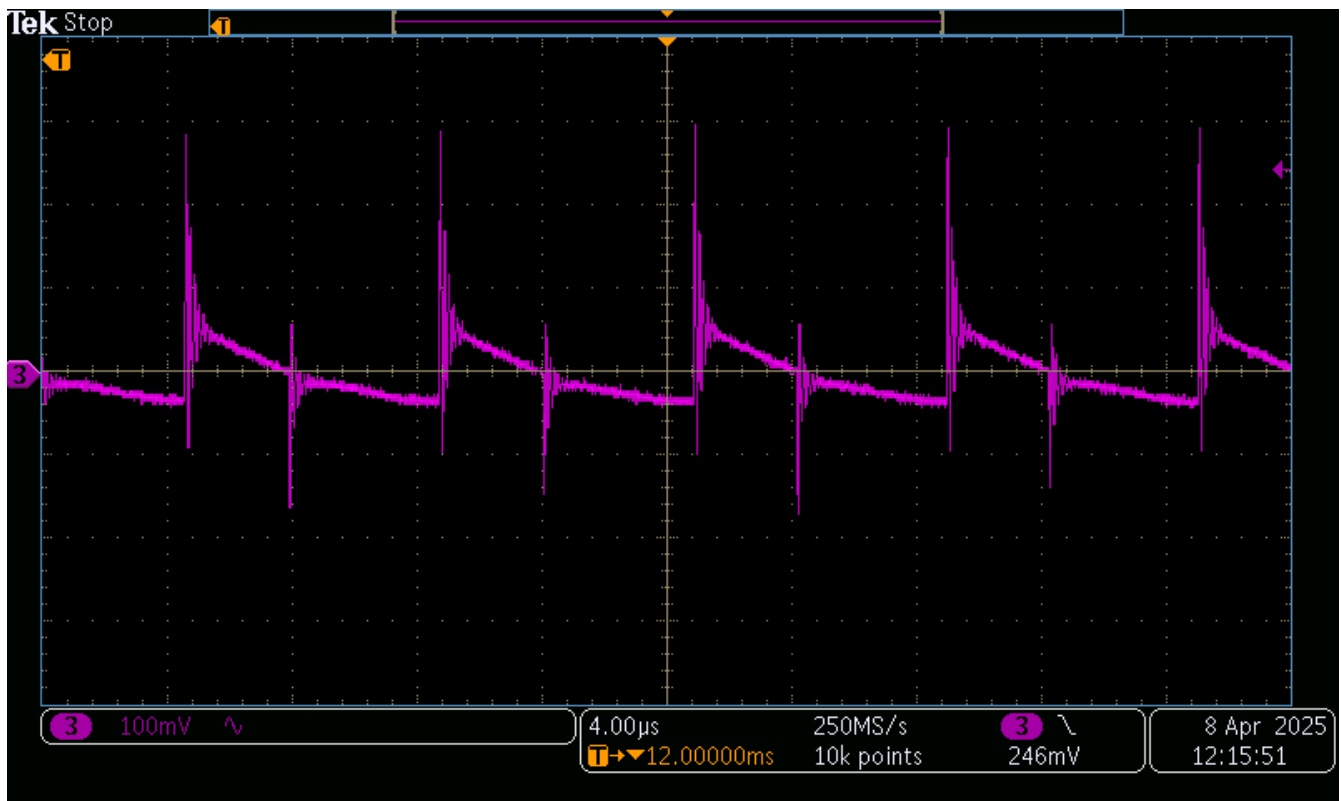


Figure 7. Steady State Output Voltage Ripple, $V_{IN} = 12\text{ V}$, 1A Load, without C16. Ch.3 = Δv_o AC-coupled

In contrast, [Figure 28](#), [Figure 30](#), and [Figure 32](#) show the lab tested results for output voltage ripple at a 1 A load with C16 in place for input voltages of 10 V, 12 V, and 14 V respectively. The ripple at the switching frequency is around 80 to 90 mV_{P-P} and the high frequency parasitic oscillations from [Figure 7](#) that increased the total ripple to nearly 500 mV_{P-P} are absent. In addition to adding MLC capacitors, additional solutions for reducing ripple include: implementing post filters using small inductors or ferrite beads and performing more aggressive snubbing of the noise at the switching edges of both the primary MOSFET and the secondary rectifier diode.

4.6 Selecting the Control MOSFET

Selecting the primary control MOSFET starts with deciding what level of gate-to-source drive voltage will be used. The SLG47115's VDD2 pins can accept up to 26.4 V – in theory even high voltage silicon carbide MOSFETs could be driven. In practice, using the same 5 V source that powers the VDD pins keeps the system simple. It also keeps the power dissipation inside the SLG47115 to a minimum. Once a gate drive voltage has been selected, it is especially important to never use any MOSFET that isn't specifically rated for that voltage. Parts rated for 6.0 V_{GS}, 10 V_{GS}, or higher provide no guarantees that they will be fully enhanced with only 5 V between their gates and sources.

Renesas offers over 50 N-MOSFETs that are rated for operation with a V_{GS} of 4.5 V or 5 V, and these have V_{DS} ratings of up to 100 V. A subset of 10 of these parts have V_{DS} ratings between 60 V to 100 V, which all use the popular, thermally-enhanced, and SO-8-compatible LFPACK package. From among these, the 80 V_{DS} RJK0852DPB is selected for its balance of switching losses and conduction losses. The following equations are available in the Excel design tool as first order estimations of the various loss terms. It is important to note that these calculations are generally correct when selecting relative losses between different MOSFETs, but they are not accurate for predicting actual losses. This is another area where lab testing is mandatory.

The following values must first be extracted from the datasheet of each candidate:

- Maximum on-resistance at 4.5 V_{GS} and at +25 °C ambient temperature, R_{DS(ON)}
- Typical output capacitance, C_{OSS}
- Typical reverse transfer capacitance, C_{RSS}
- Typical gate-to-drain charge, Q_{GD}

- Typical total gate charge, Q_G .

The gate drive voltage will come from the SLG47115's regulated 5.0 V V_{DD2} voltage. The second parameter needed from the SLG47115 is its peak gate drive sink and source currents. If one of the half-bridges is used then these are equal to 3 A for both sink and source. If both half-bridges are used, this increases to 6 A for sink and source. This design uses both half-bridges.

- $I_{SOURCE} = I_{SINK} = 6$ A

The drain-source rise and fall times can then be estimated by:

$$t_{RISE} = \frac{Q_{GD}}{I_{SINK}} \quad \text{EQ 4.73}$$

$$t_{FALL} = \frac{Q_{GD}}{I_{SOURCE}} \quad \text{EQ 4.74}$$

Conduction loss is the simplest term to calculate:

$$P_{COND} = I_{P_RMS_VMIN}^2 \times R_{DS(ON)} \quad \text{EQ 4.75}$$

Switching loss during turn-on comes from the overlap of the falling drain-source voltage and rising drain current:

$$P_{SW_ON} = 0.5 \times t_{FALL} \times f_{SW_VMIN} \times (I_{PPK_VMIN} - \Delta i_{P_VMIN}) \times (V_{IN_MIN} + V_{OUT} \times N_{PS}) \quad \text{EQ 4.76}$$

Switching loss during turn-off comes from the overlap of the rising drain-source voltage and falling drain current:

$$P_{SW_OFF} = 0.5 \times t_{RISE} \times f_{SW_VMIN} \times I_{PPK_VMIN} \times (V_{IN_MIN} + V_{OUT} \times N_{PS} + V_{CLAMP_TGT}) \quad \text{EQ 4.77}$$

Loss from charging and discharging the MOSFET's output capacitance is calculated as follows:

$$P_{COSS} = 0.5 \times V_{IN_MIN}^2 \times f_{SW_VMIN} \times C_{OSS} \quad \text{EQ 4.78}$$

Next comes the loss from the charging and discharging of the reverse transfer capacitance:

$$P_{CRSS} = 2 \times V_{IN_MIN}^2 \times I_{O_MAX} \times f_{SW_VMIN} \times C_{RSS} \quad \text{EQ 4.79}$$

The final loss term comes from charging and discharging the gate of Q1. This is the only loss that occurs in the driver itself, the SLG47115 IC:

$$P_{GATE} = V_{DD2} \times f_{SW_VMIN} \times Q_G \quad \text{EQ 4.80}$$

4.7 Output Diode

Schottky diodes are preferred for output rectification in almost every flyback as long as they are able handle the reverse voltage. Recall from [EQ 4.6](#) that the maximum reverse voltage plus the 10 % derating was calculated to be 54 V, making 60 V a good choice for the reverse blocking voltage. The estimated power dissipation for a flyback's output rectifier is a straightforward calculation:

$$P_{D1} = V_{F1} \times I_{O_MAX} = 0.5 \text{ V} \times 1.0 \text{ A} = 0.5 \text{ W} \quad \text{EQ 4.81}$$

Many choices for 60 V Schottky diodes are available. The most important factors in choosing which diode to use are the package and its thermal resistance. Among surface mount packages, the TO-277A has proven itself a good option thanks to its large thermal tab. Selecting a diode with a continuous forward current rating which is at least equal to the peak forward current usually gives excellent results. The peak forward current for the output

diode is equal to the peak secondary current, I_{SPK_VMAX} , which is 4.4 A. Figure 8 shows the secondary switch node at 1 A load and 10 V input voltage.

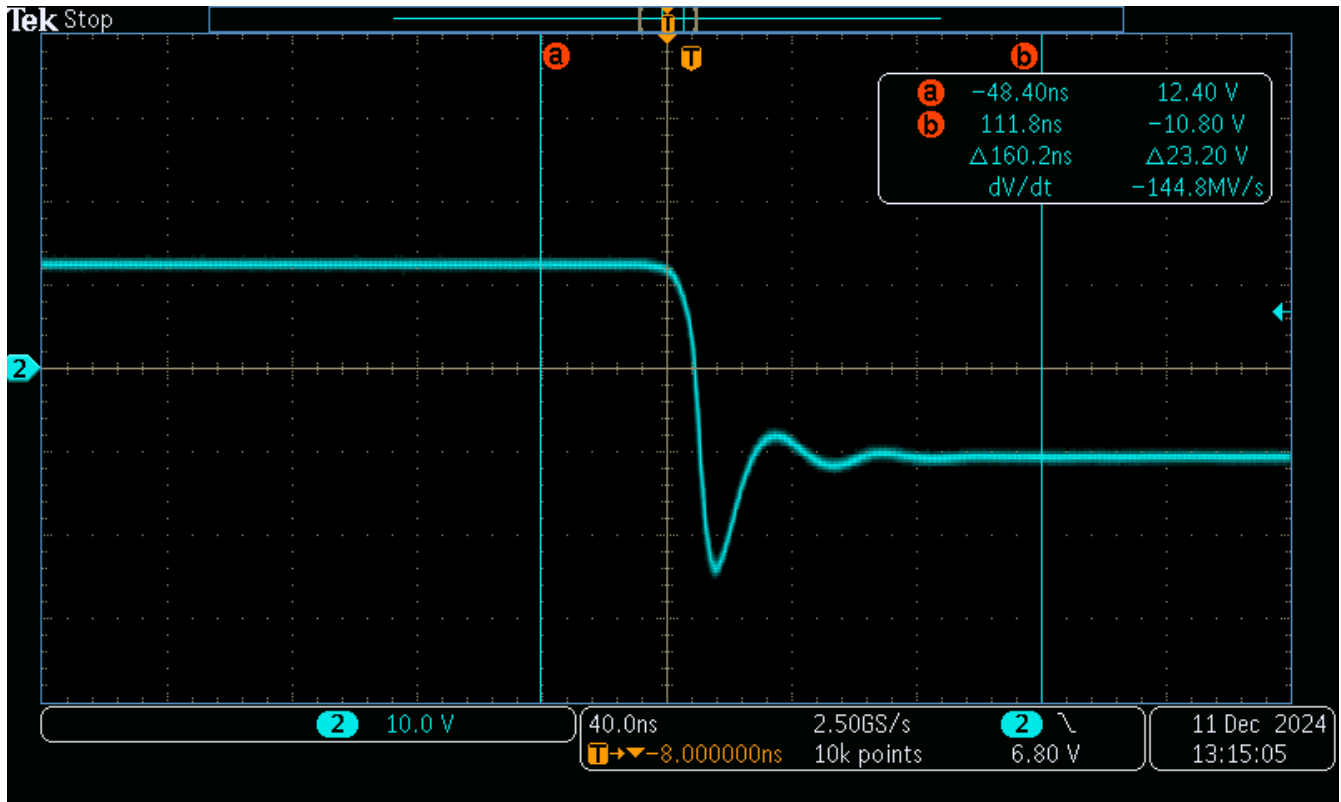


Figure 8. Secondary Switch Node

4.8 Primary Snubber

EQ 4.7 estimates the transient voltage spike generated by the flyback transformer’s leakage inductance, and EQ 4.11 estimates the peak drain-source voltage blocked by MOSFET Q1. The actual circuit used to clamp the leakage transient in low voltage, low power flybacks such as this one is most often the RCD clamp design (resistor, capacitor, and diode) as shown in Figure 9.

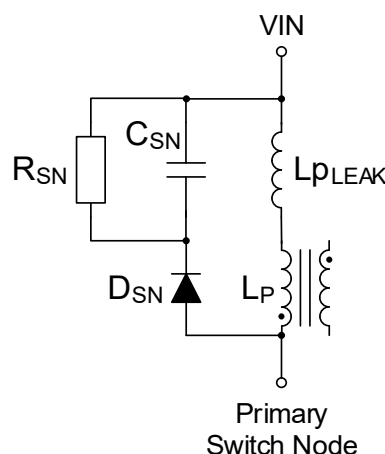


Figure 9. Primary Inductance with Leakage Inductance in Series and RCD Type Snubber

For this type of snubber, the diode should be a fast recovery type diode and also be rated to block at least as much reverse voltage as MOSFET Q1’s drain-source rating.

There are many methods to design RCD snubbers. The following procedure has worked well for Renesas Applications Engineering.

The first step is to measure the actual leakage inductance of the flyback transformer at the primary winding terminals. To make this measurement, short-circuit every other winding terminal together. If a network analyzer is available, a sweep of inductance versus frequency from ~100 Hz to beyond the maximum switching frequency of the flyback converter is recommended. If not, then using an LCR meter with programmable test frequency is the next best choice. For this converter, the primary leakage inductance from 100 kHz to 300 kHz needs to be known. Figure 10 shows a sweep of the primary leakage inductance with values noted at both 100 kHz and 300 kHz which are within specifications as with 7491195212's datasheet, which lists a maximum of 300 nH at 100 kHz.

- Maximum leakage inductance as the primary terminals, $L_{P_LEAK} = 300 \text{ nH}$.

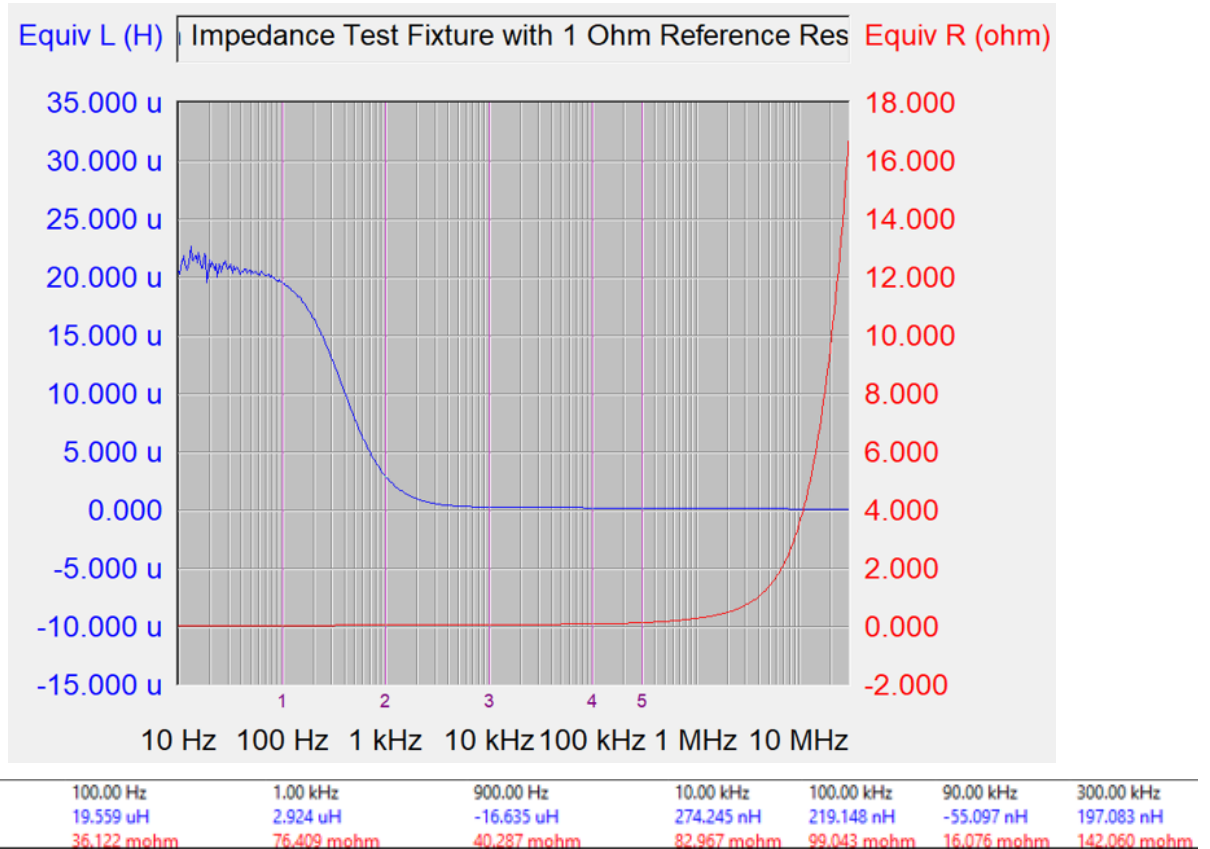


Figure 10. Sweep of Primary Leakage Inductance Versus Frequency for the 749119521 Transformer

The following two images show the various voltage levels of a flyback converter's primary switching node to illustrate the function of this circuit graphically. Note that these plots were taken from a different flyback converter whose larger transformer made it easier to insert series current probes:

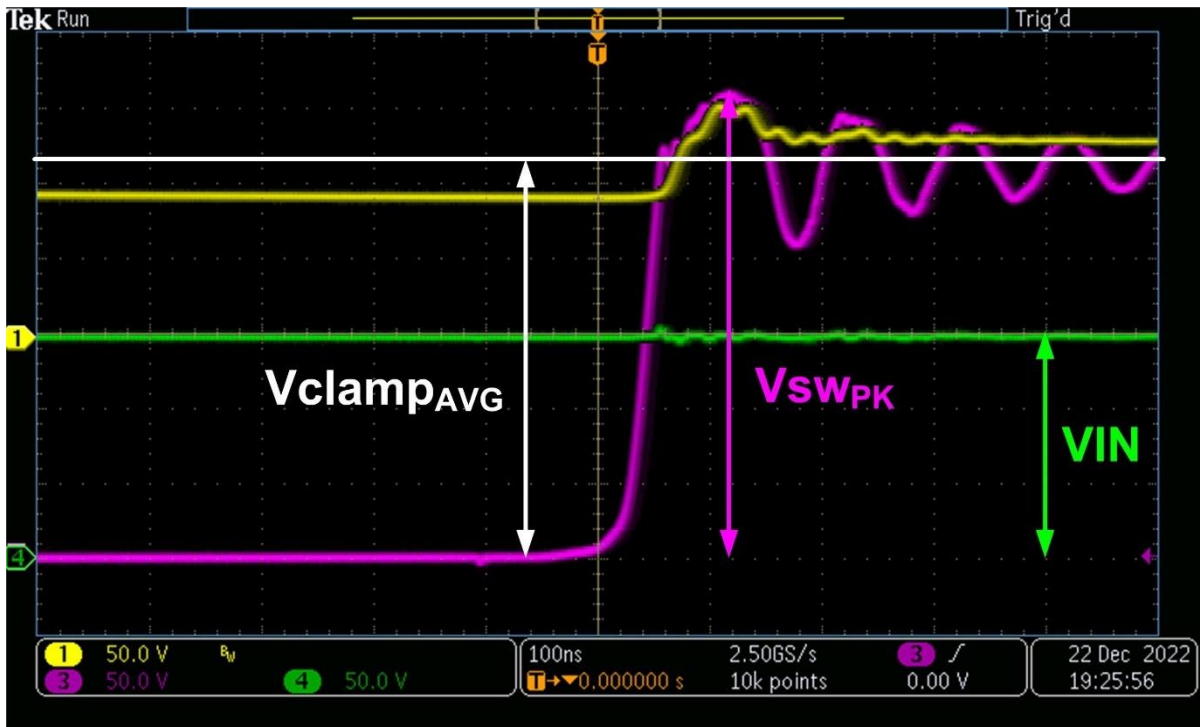


Figure 11. Detail of the Rising Primary Switch Node Voltage

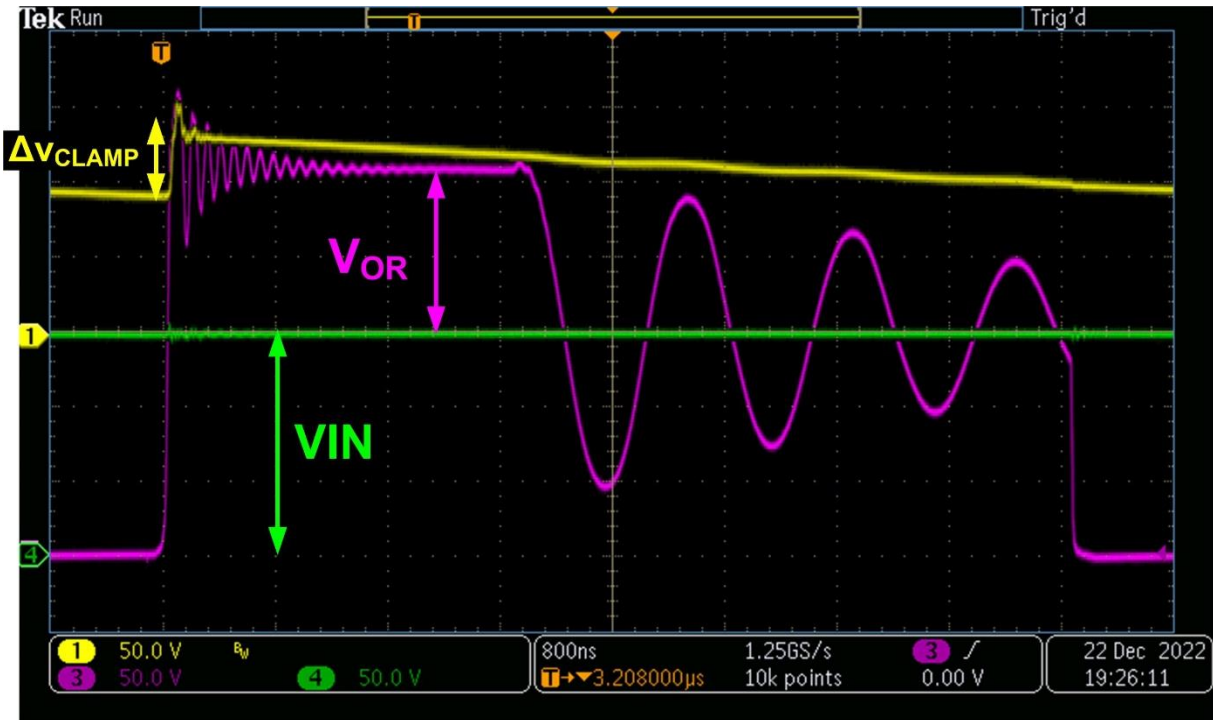


Figure 12. Longer Time Base Shows Clamp Ripple Voltage

The next step in designing this snubber begins by calculating the energy stored in the leakage inductance at the moment that Q1 is turned off. As the primary peak current is actively controlled, this energy calculation will be accurate. The worst case is always at maximum input voltage:

$$E_{P_LEAK} = 0.5 \times L_{P_LEAK} \times I_{PPK_VMAX}^2 = 0.5 \times 300 \text{ nH} \times 3.31 \text{ A}^2 = 1.6 \mu\text{J}$$

EQ 4.82

The maximum transient or spike voltage was calculated previously – this is the transient on top of the input voltage and the reflected output voltage. Now, a similar calculation will be carried out, but with respect to primary ground:

$$V_{CLAMP_MAX} = V_{DS_MAX} - V_{IN_MAX} = 72\text{ V} - 14\text{ V} = 58\text{ V}$$

EQ 4.83

Again, similar to the estimated voltage spike, a recommended clamp voltage with respect to PGND is calculated as follows, to ensure that the clamp does not engage at a value below the input voltage plus the reflected output voltage:

$$V_{CLAMP_REC} = \frac{V_{OR} + V_{CLAMP_MAX}}{2} = \frac{17\text{ V} + 58\text{ V}}{2} = 38\text{ V}$$

EQ 4.84

Experienced designers may set their target clamp voltage differently, but for this application the target will be set to exactly the same value as the recommended value:

- Target primary clamp voltage WRT primary ground, $V_{CLAMP_TGT} = 38\text{ V}$.

The purpose of the snubber capacitor is to absorb and store the energy in the leakage inductance, therefore the capacitance is inversely proportional to the clamp voltage:

$$C_{SN_MIN} = \frac{E_{P_LEAK}}{(V_{CLAMP_TGT}^2 - V_{OR}^2)} = \frac{1.6\ \mu\text{J}}{(38\text{ V}^2 - 17\text{ V}^2)} = 1423\text{ pF}$$

EQ 4.85

The two closest standard E6 values are 1.2 nF and 1.5 nF. Lower capacitance will save power but may allow too high of a clamping level, hence 1.2 nF will be used to start but tested carefully to see if 1.5 nF is necessary. For snubber circuits, a stable capacitance with respect to the applied voltage is critical. Neither the X5R nor X7R dielectrics are acceptable for this reason, and the design should use C0G/NP0.

Then, the next standard capacitor voltage rating beyond Q1's 80 V rating is 100 V. 5 % is the most common tolerance at these capacitance and voltage ratings. As for size, case sizes of 0603 and 0805 are widely available.

- Snubber capacitor, $C_{SN} = 1.2\text{ nF } 5\%, 100\text{ V}, 0805, \text{C0G}$.

The actual average clamp voltage can now be calculated:

$$V_{CLAMP_AVG} = \sqrt{\frac{E_{P_LEAK}}{C_{SN}} + V_{OR}^2} = \sqrt{\frac{1.6\ \mu\text{J}}{1.2\text{ nF}} + 17\text{ V}^2} = 41\text{ V}$$

EQ 4.86

The purpose of the resistor(s) in the snubber is to dissipate the energy in the capacitor during the rest of the switching cycle. The resulting waveform across the parallel network of R_{SN} and C_{SN} is a triangle/sawtooth wave that is shown in [Figure 11](#) and [Figure 12](#). Renesas Applications Engineering has found that dividing the target clamp voltage by a factor of 1.5 is a good starting point for calculating the target clamp ripple voltage:

$$\Delta V_{CLAMP_REC} = \frac{V_{CLAMP_TGT}}{1.5} = \frac{41\text{ V}}{1.5} = 25\text{ V}_{P_P}$$

EQ 4.87

- Target peak-to-peak clamp ripple voltage, $\Delta V_{CLAMP_TGT} = 25\text{ V}$.

The next step is selecting the maximum snubber resistance that will dissipate enough energy to keep the clamp ripple voltage at or below the target:

$$R_{CLAMP_MAX} = \frac{1}{f_{SW_VMAX} \times C_{SN} \times \ln\left(\frac{I_{PPK_VMAX}}{\Delta V_{CLAMP_TGT}} \times \sqrt{\frac{L_{P_LEAK}}{C_{SN}}}\right)^2}$$

EQ 4.88

$$R_{CLAMP_MAX} = \frac{1}{118 \text{ kHz} \times 1.2 \text{ nF} \times \ln\left(\frac{3.31 \text{ A}}{25 \text{ V}} \times \sqrt{\frac{300 \text{ nH}}{1.2 \text{ nF}}}\right)^2} = 4.8 \text{ k}\Omega$$

EQ 4.89

The power dissipation of the snubber resistor(s) will also be needed in order to select the actual resistance and to decide whether or not it is necessary to put multiple resistors in parallel to dissipate that power:

$$P_{RSN} = \frac{V_{CLAMP_AVG}^2}{R_{CLAMP_MAX}} = \frac{41 \text{ V}^2}{4.8 \text{ k}\Omega} = 350 \text{ mW}$$

EQ 4.90

Thick film resistors with 1206 case size and 250 mW power dissipation rating are among the most affordable options and can stand off up to 200 V. Three such devices in parallel should provide enough power dissipation capability and is proven by lab testing. In the first iteration of testing, three 10 kΩ resistors are selected. Pricing for 1 % versus 5 % tolerances is about the same, so 1 % parts are used.

- Three snubber resistors in parallel, $R_{SN} = 12 \text{ k}\Omega$ 1 %, 1206, thick-film, 100 ppm.

Starting with the minimum input voltage minimizes the risk of an over-voltage across Q1. From lab testing, [Figure 21](#) shows the peak voltage across Q1 reaches around 50 to 55 V, leaving a good margin of safety of 25 V to 30 V between the peak voltage and Q1's 80 V V_{DS_MAX} rating.

5. Typical Performance

The following graphs and scope captures were taken with ambient temperatures ranging from 15 °C to 25 °C.

$V_{IN} = V_{OUT} = 12\text{ V}$ unless otherwise noted.

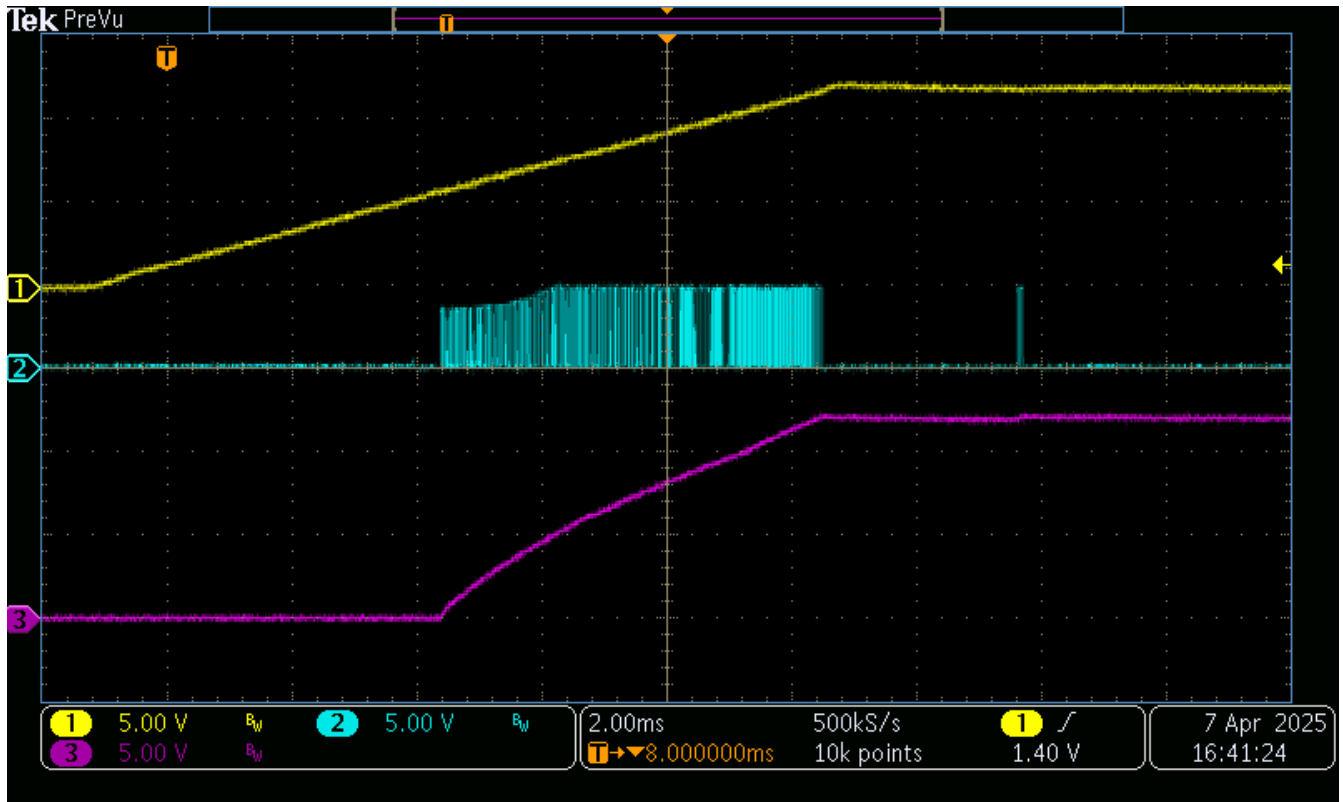


Figure 13. Startup, No Load, EN/SD* Pin Tied to +5V on J2. Ch.1 = V_{IN} , Ch.2 = Q1 V_{GS} , Ch.3 = V_{OUT}

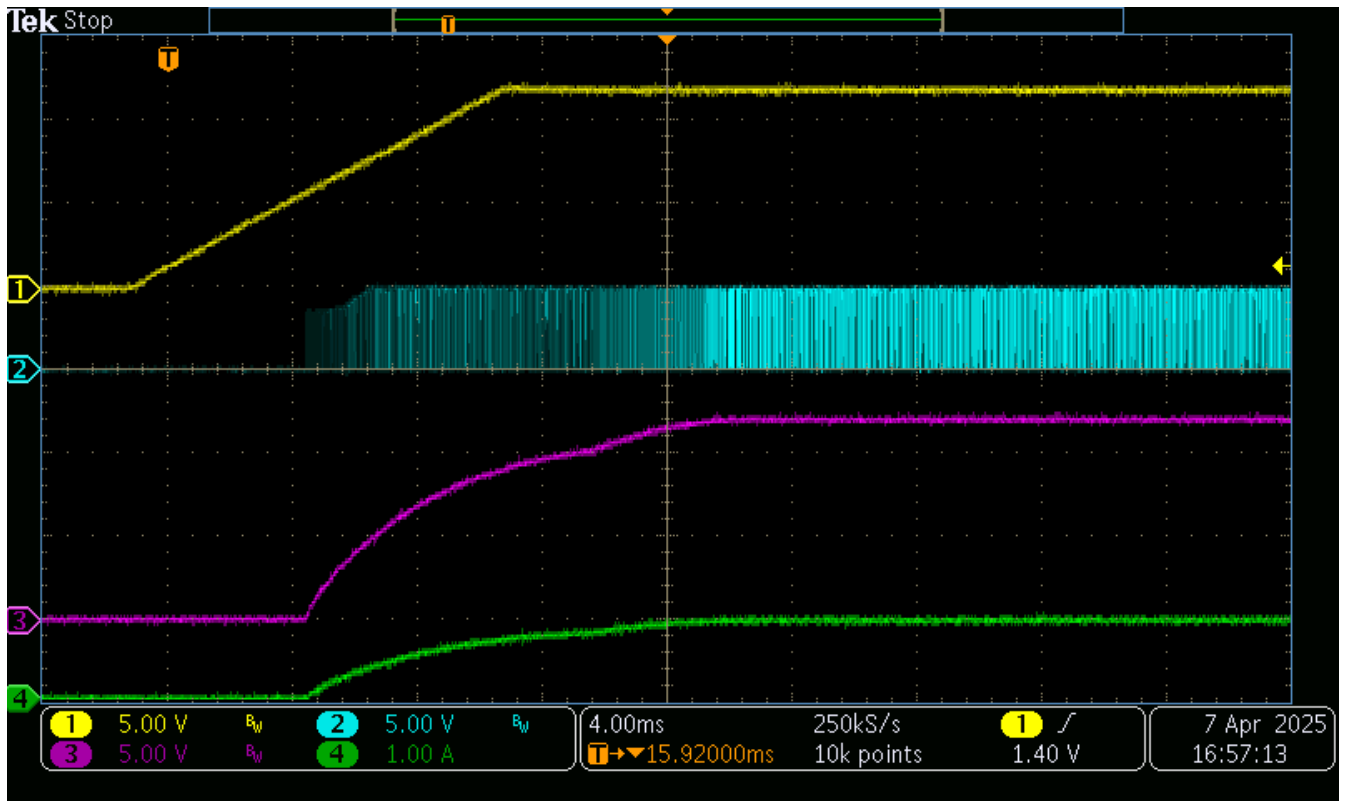


Figure 14. Startup, 13 Ω Load, EN/SD* Pin Tied to +5V on J2. Ch.1 = V_{IN}, Ch.2 = Q1 V_{GS}, Ch.3 = V_{OUT}, Ch.4 = I_o

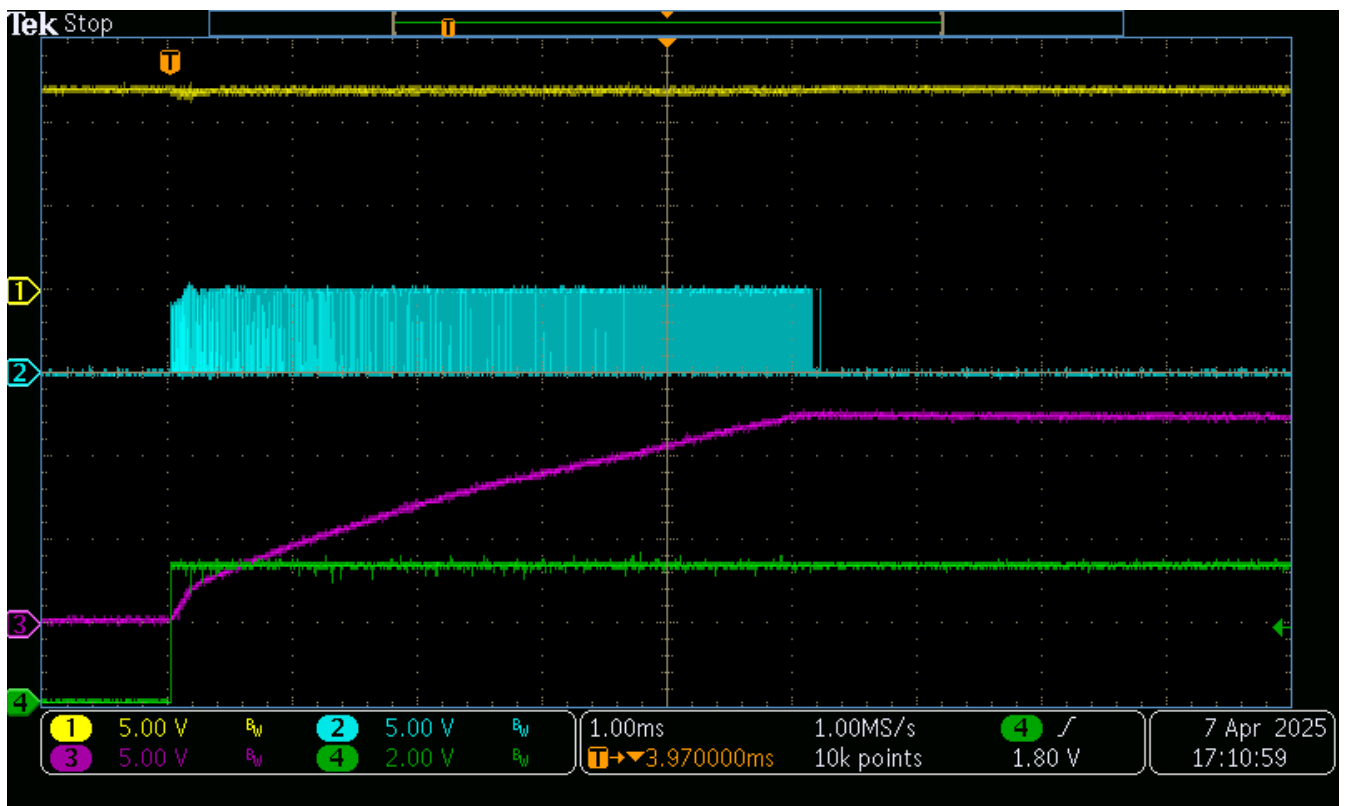


Figure 15. Enable Via EN/SD*, No Load. Ch.1 = V_{IN}, Ch.2 = Q1 V_{GS}, Ch.3 = V_{OUT}, Ch.4 = EN/SD*

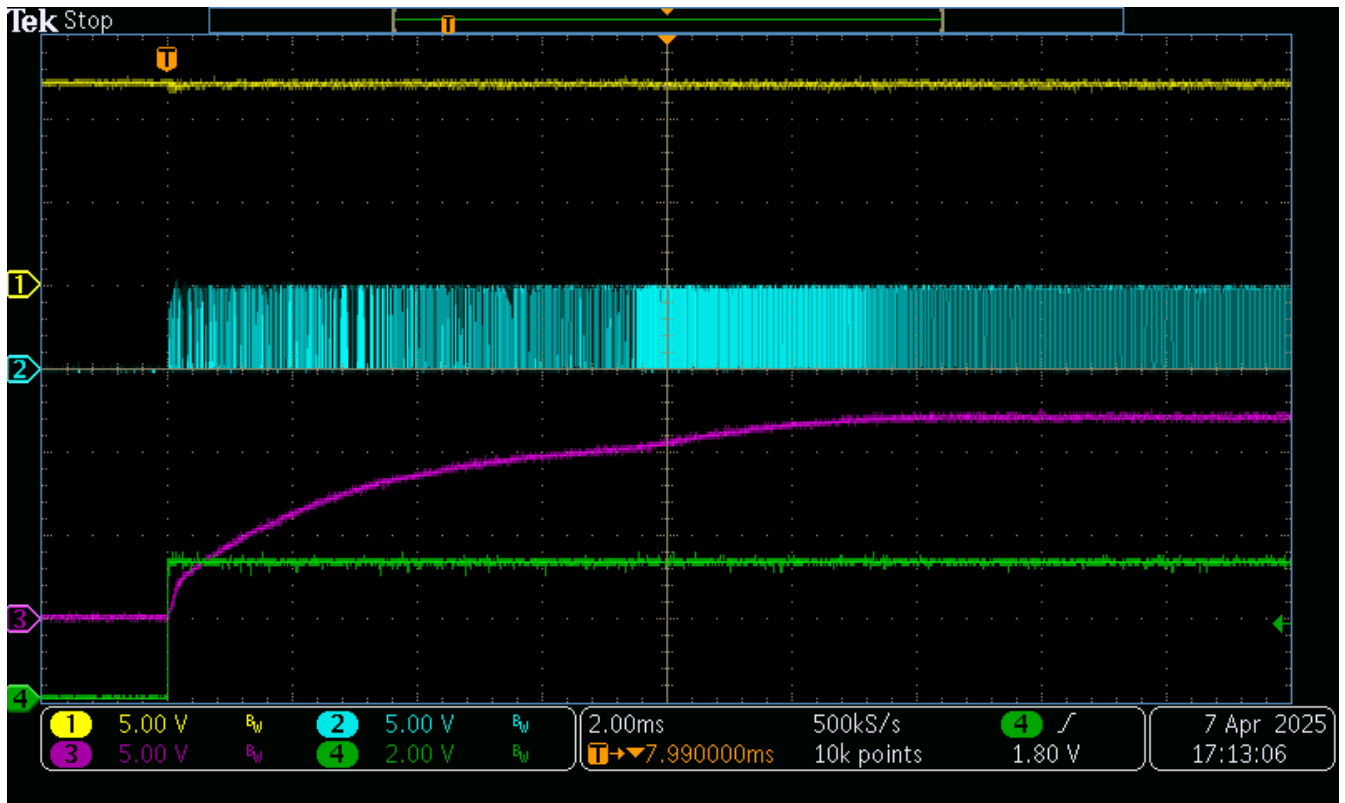


Figure 16. Enable Via EN/SD*, 13 Ω Load. Ch.1 = V_{IN} , Ch.2 = Q1 V_{GS} , Ch.3 = V_{OUT} , Ch.4 = EN/SD*

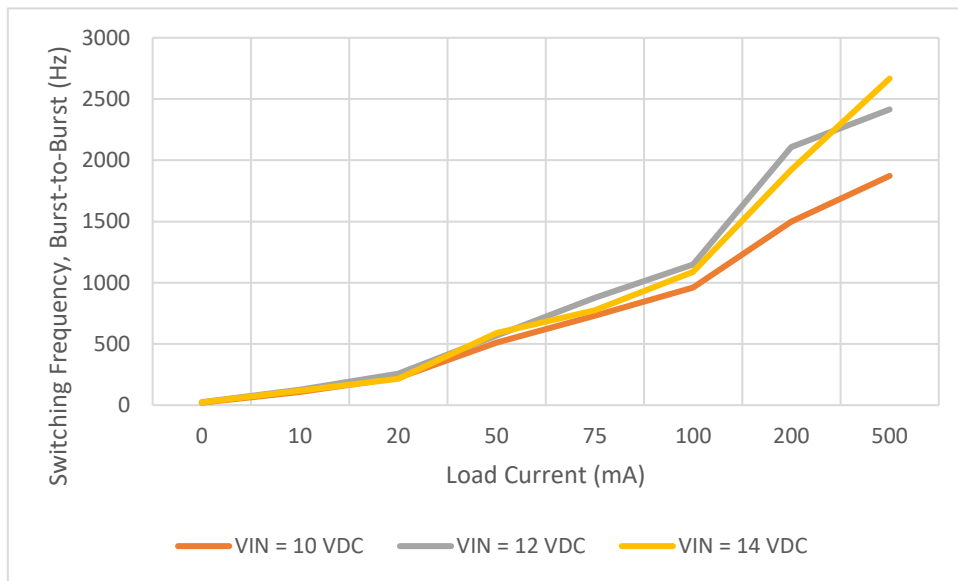


Figure 17. Burst Mode Frequency vs Input Voltage and Load

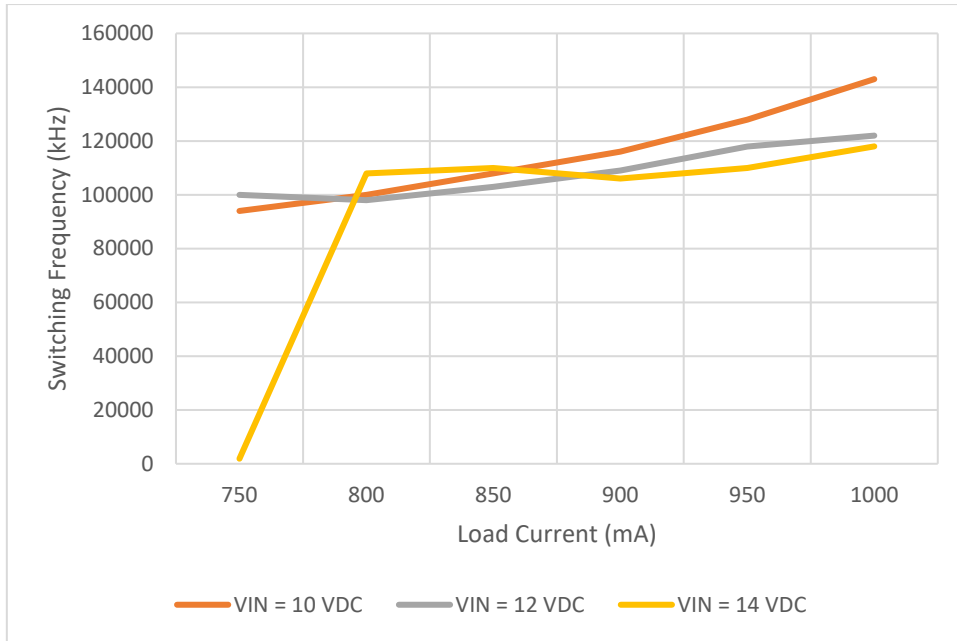


Figure 18. PWM Mode Frequency vs Input Voltage and Load

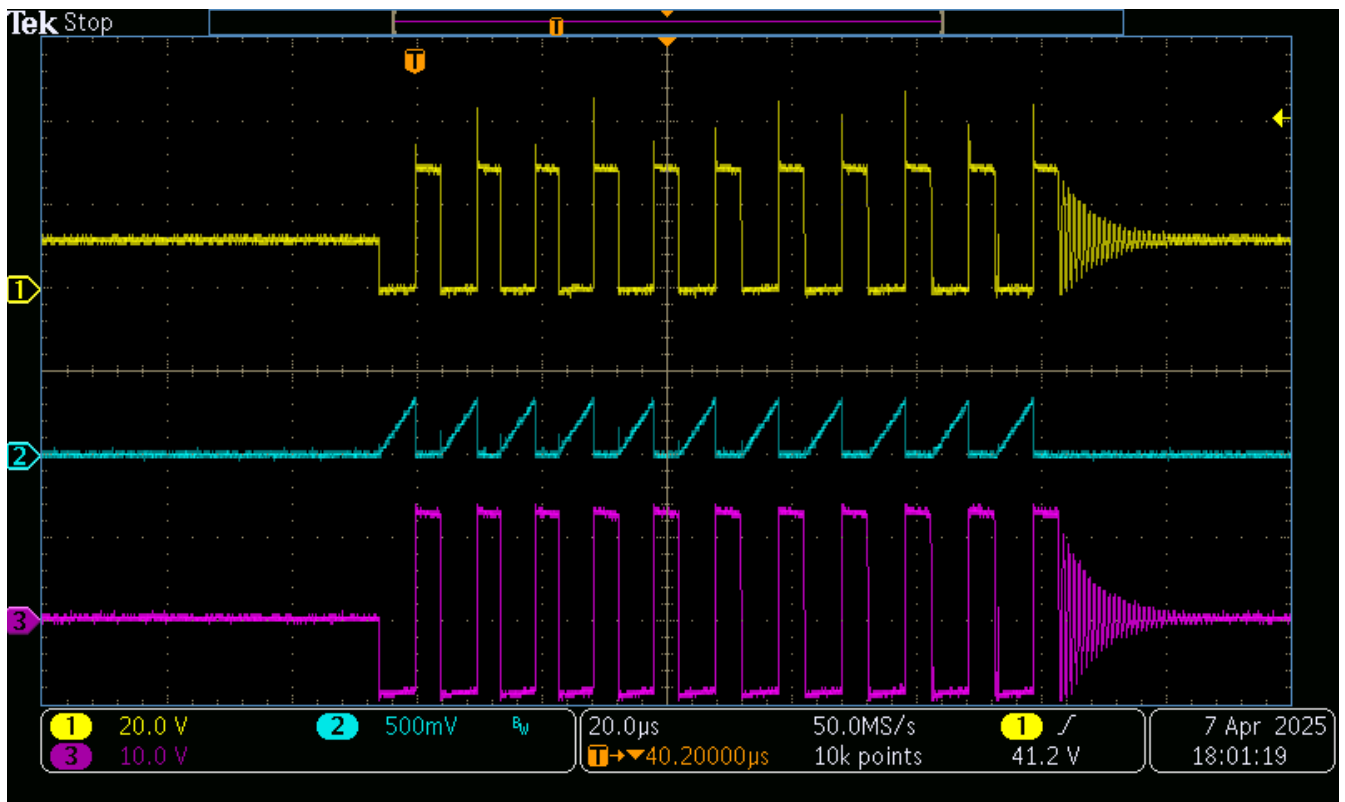


Figure 19. Steady State, V_{IN} = 12 VDC, 10 mA Load (Burst Mode). Ch.1 = Q1 V_{DS}, Ch.2 = V_{SNS}, Ch.3 = V_{SW_SEC}

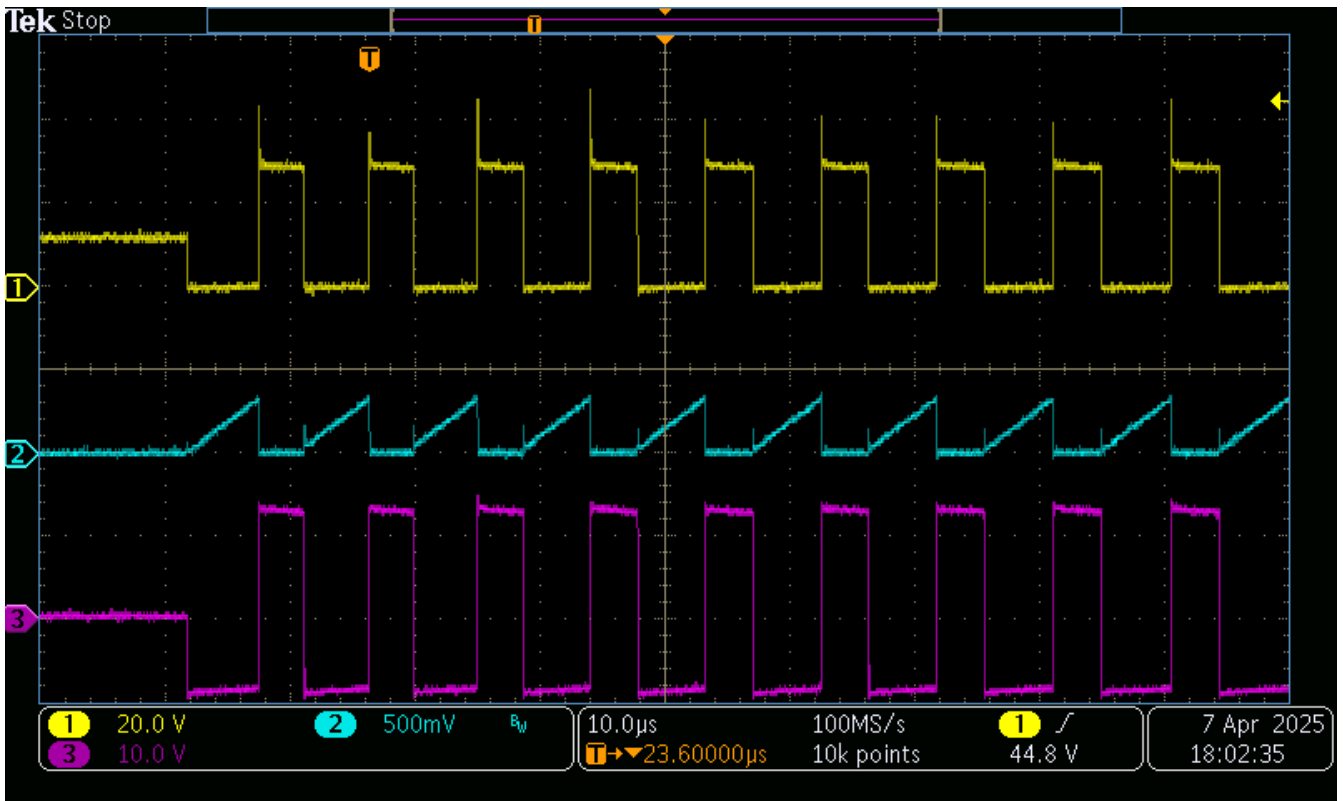


Figure 20. Steady State, V_{IN} = 12 VDC, 500 mA Load (Border Burst/PWM). Ch.1 = Q1 V_{DS}, Ch.2 = V_{SNS}, Ch.3 = V_{SW_SEC}

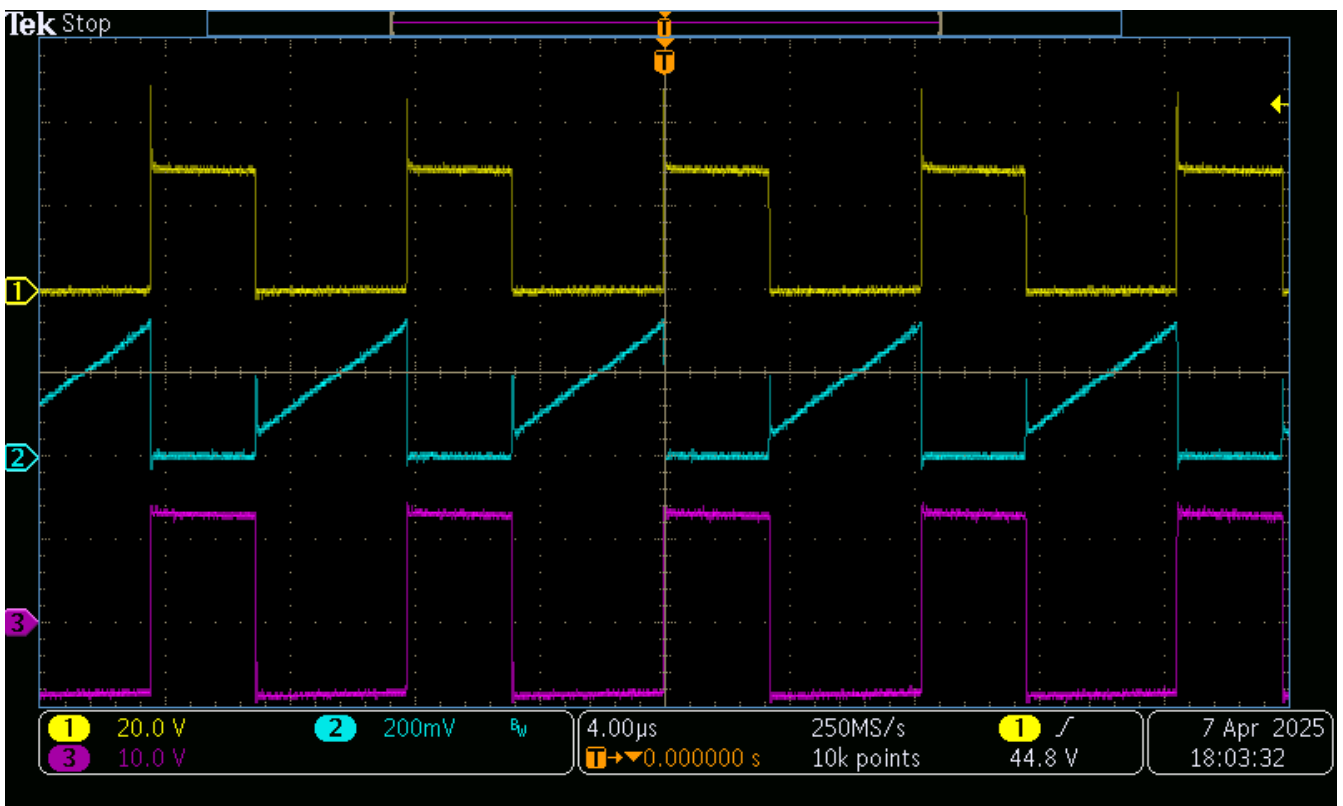


Figure 21. Steady State, V_{IN} = 12 VDC, 1 A Load (PWM Mode). Ch.1 = Q1 V_{DS}, Ch.2 = V_{SNS}, Ch.3 = V_{SW_SEC}

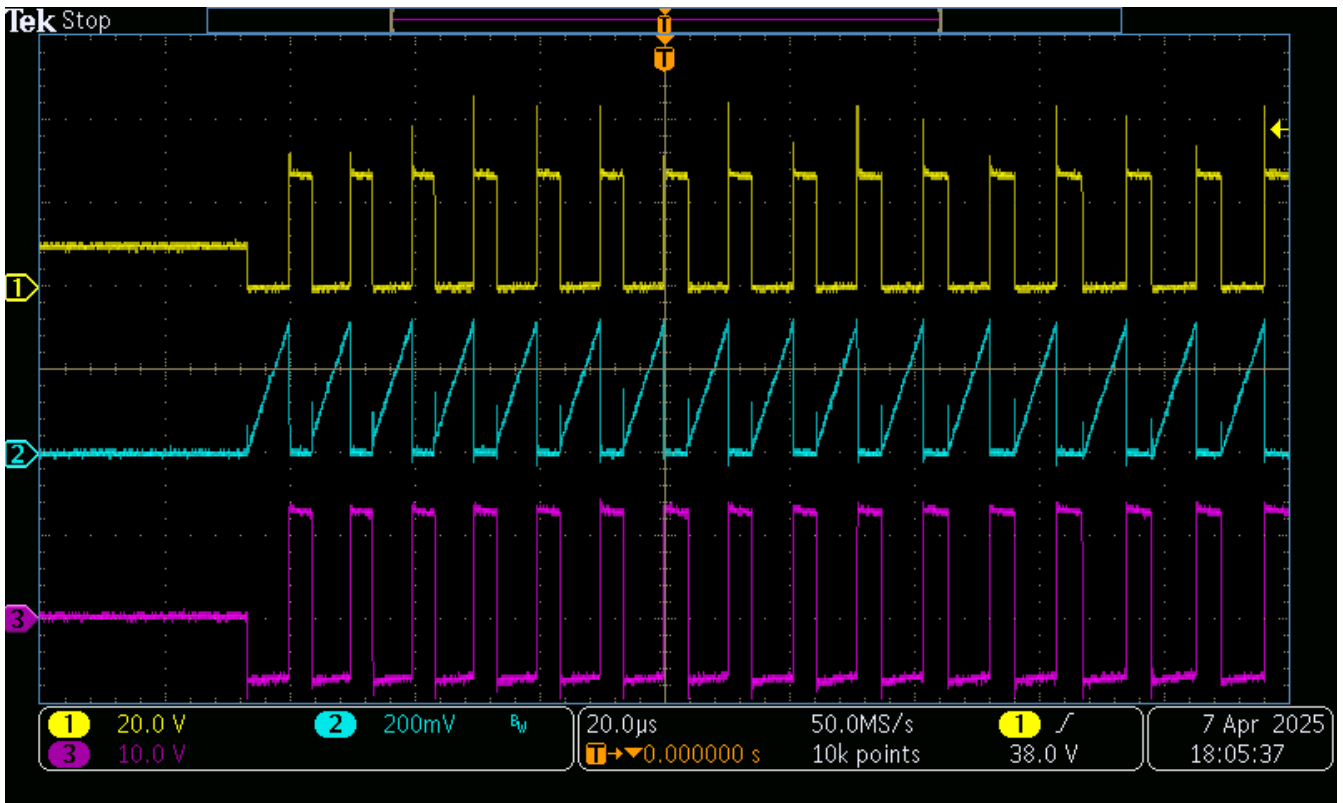


Figure 22. Steady State, $V_{IN} = 10\text{ VDC}$, 500 mA Load (Burst/PWM). Ch.1 = Q1 V_{DS} , Ch.2 = V_{SNS} , Ch.3 = V_{SW_SEC}

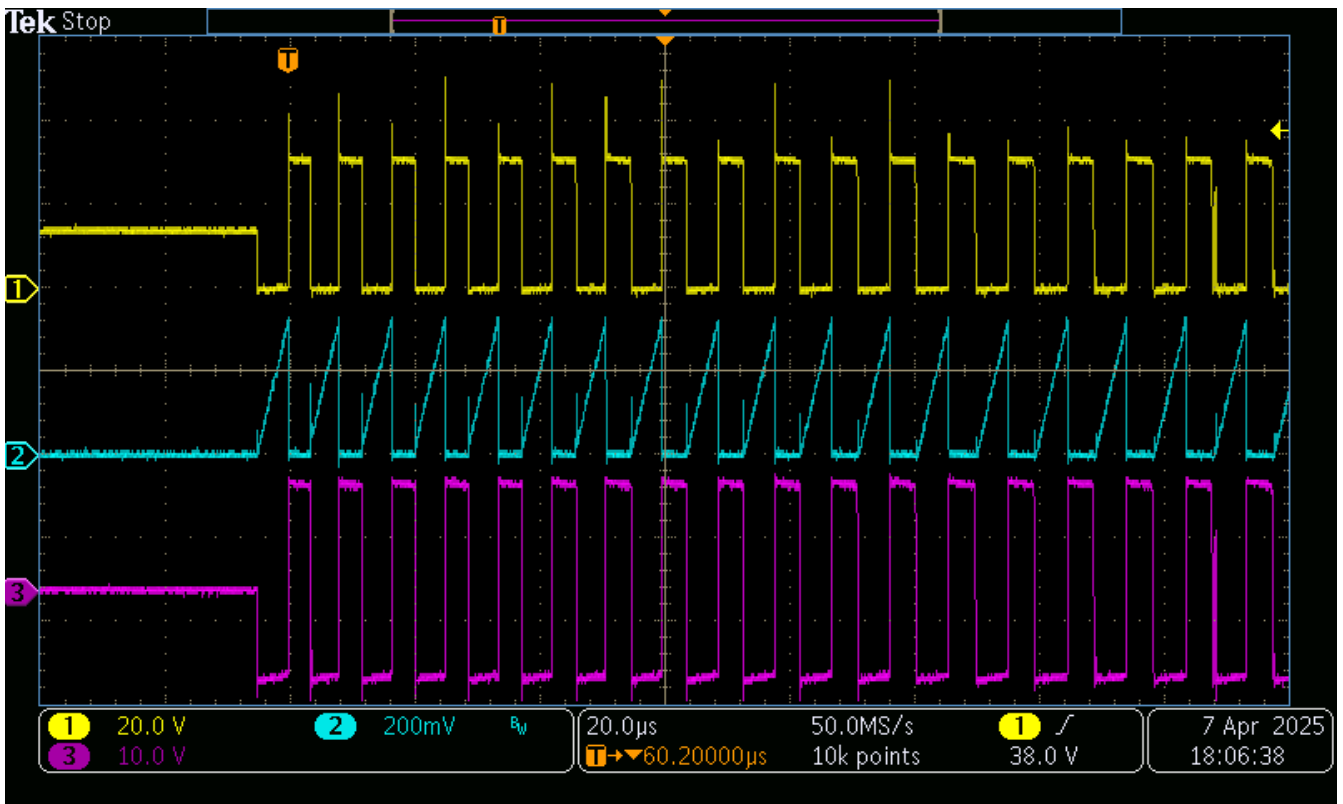


Figure 23. Steady State, $V_{IN} = 14\text{ V}$, 500 mA load (Burst/PWM). Ch.1 = Q1 V_{DS} , Ch.2 = V_{SNS} , Ch.3 = V_{SW_SEC}

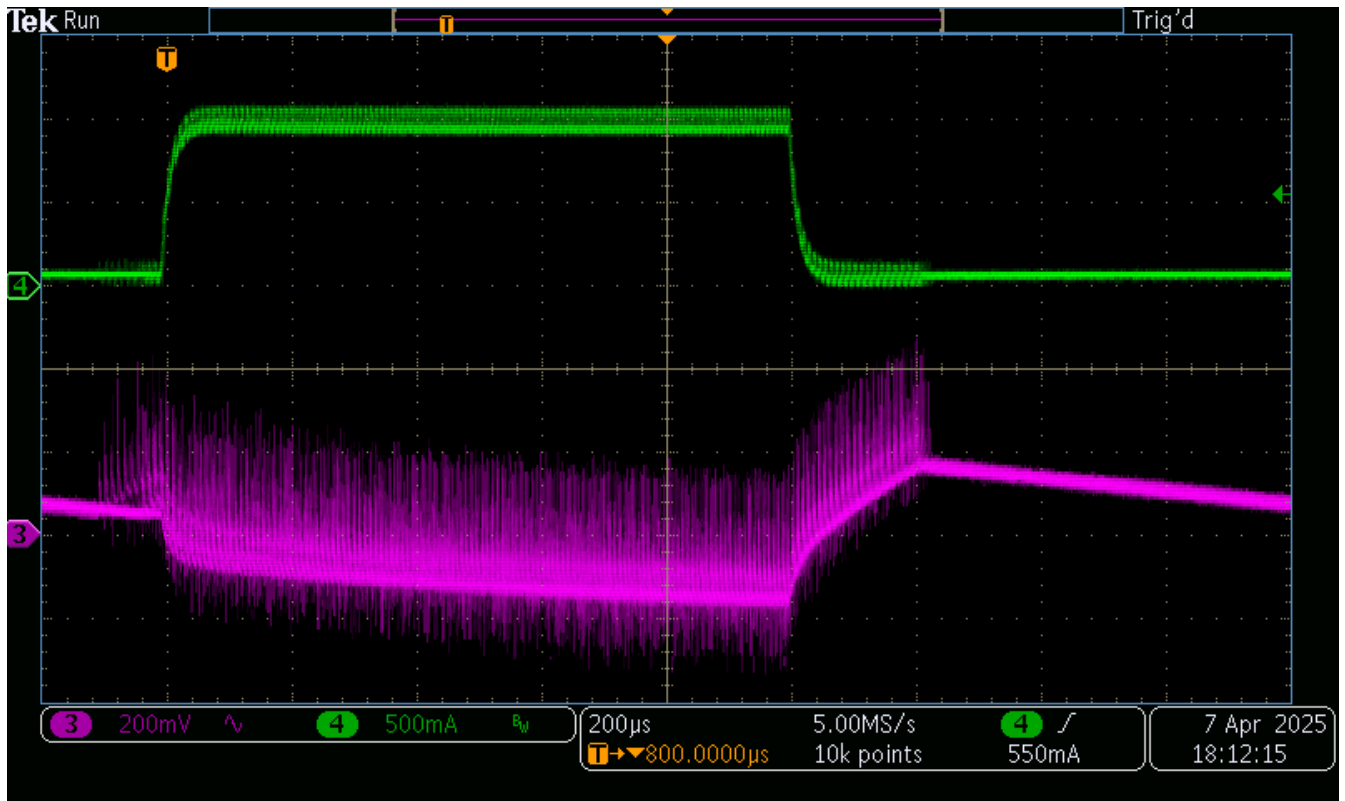


Figure 24. Load Transient, 0.1 to 1.0 A, $V_{IN} = 10$ V. Ch.3 = Δv_O AC-coupled, Ch.4 = I_O

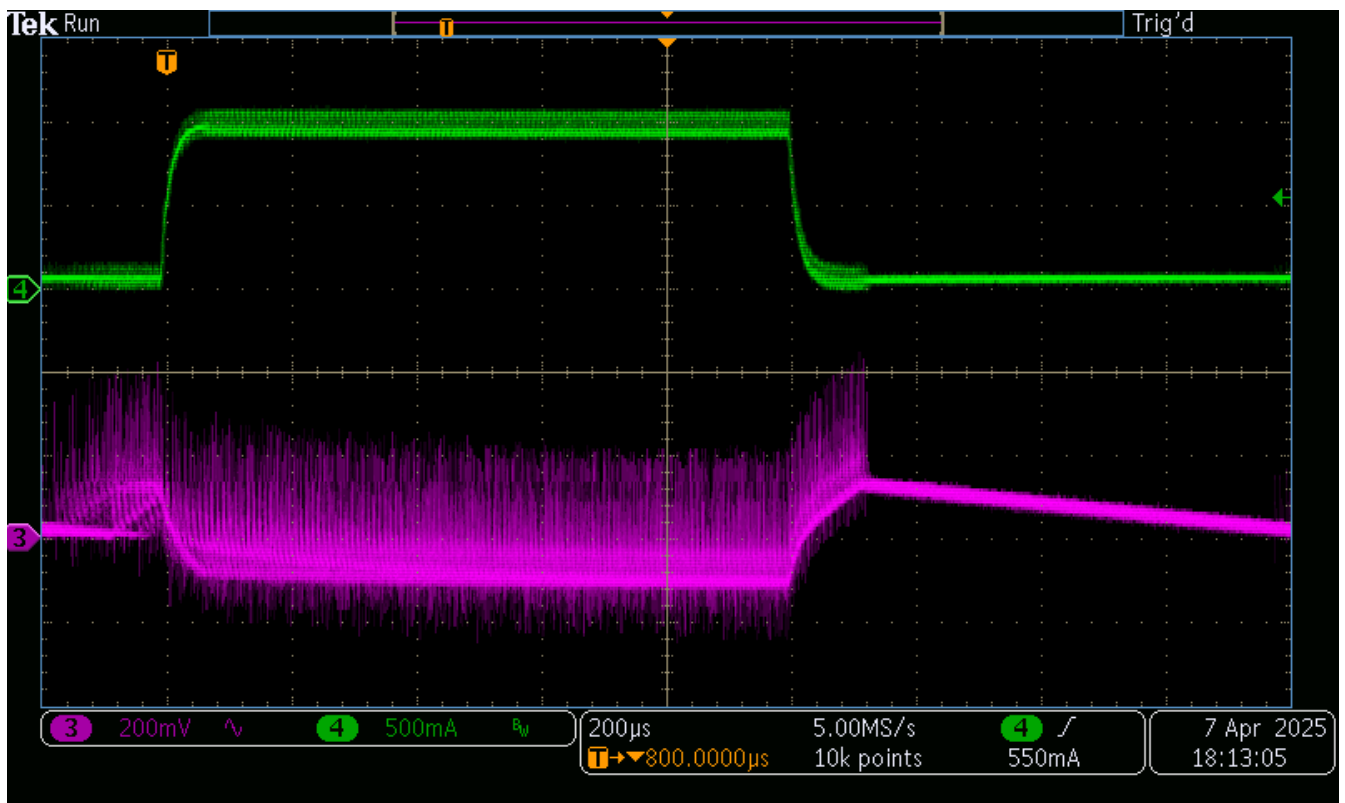


Figure 25. Load Transient, 0.1 to 1.0 A, $V_{IN} = 12$ V. Ch.3 = Δv_O AC-coupled, Ch.4 = I_O

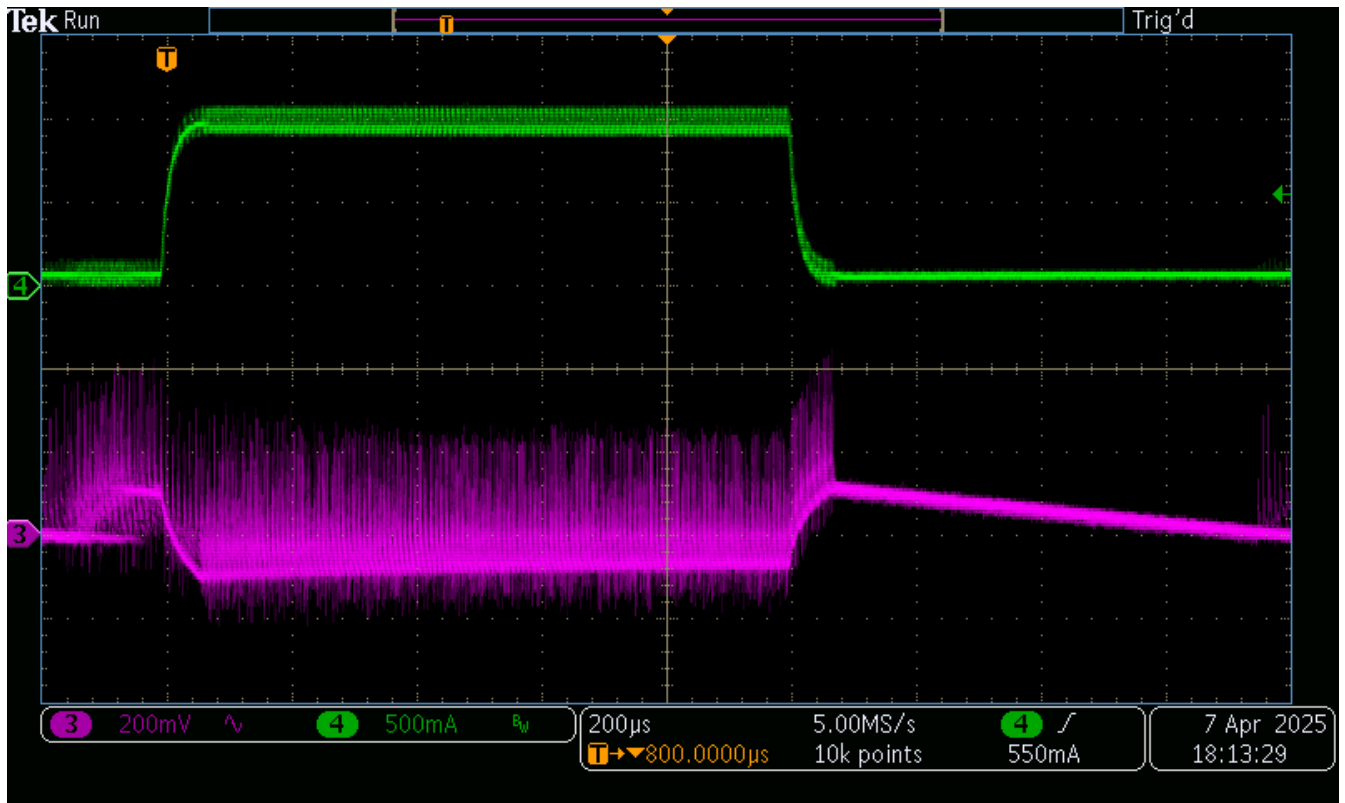


Figure 26. Load Transient, 0.1 to 1.0 A, $V_{IN} = 14$ V. Ch.3 = Δv_o AC-coupled, Ch.4 = I_o

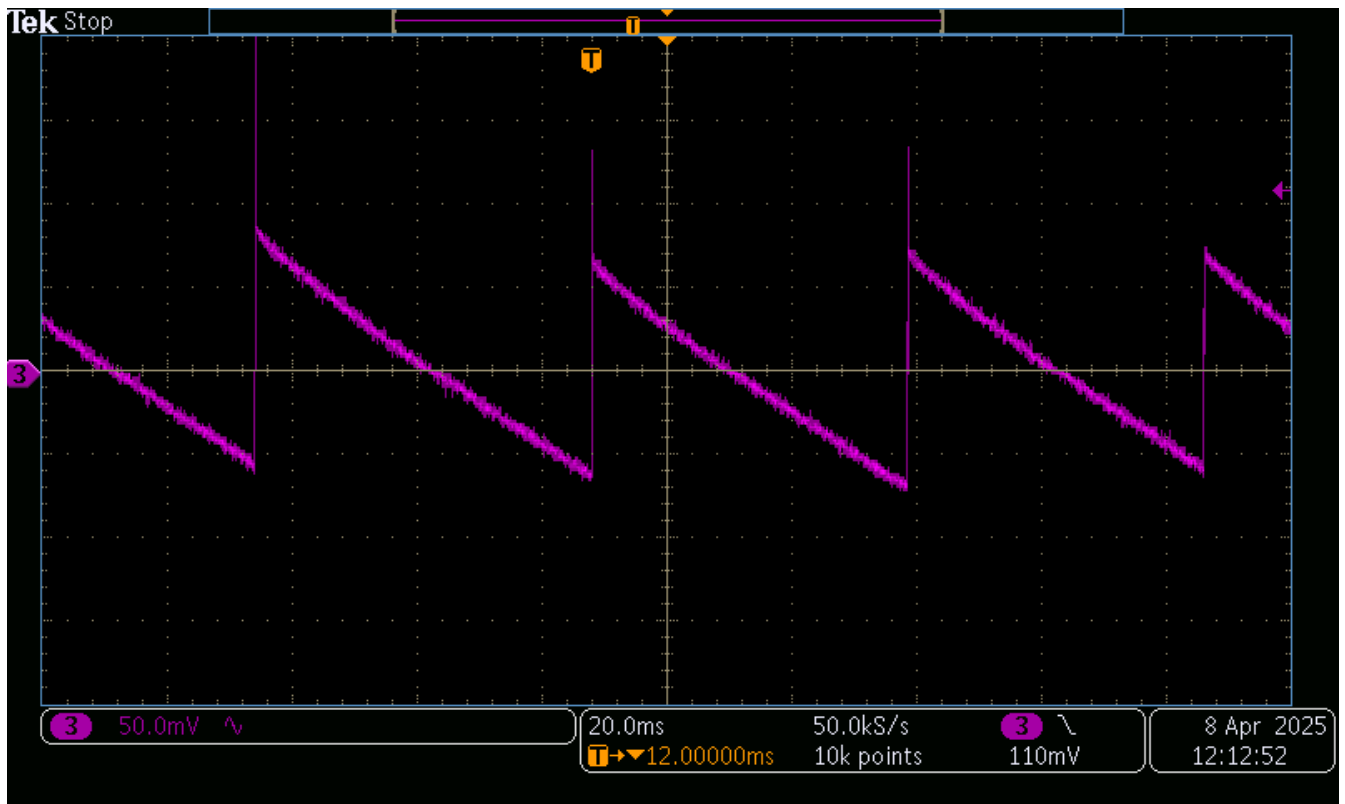


Figure 27. Steady State Output Voltage Ripple, $V_{IN} = 10$ V, No Load. Ch.3 = Δv_o AC-coupled

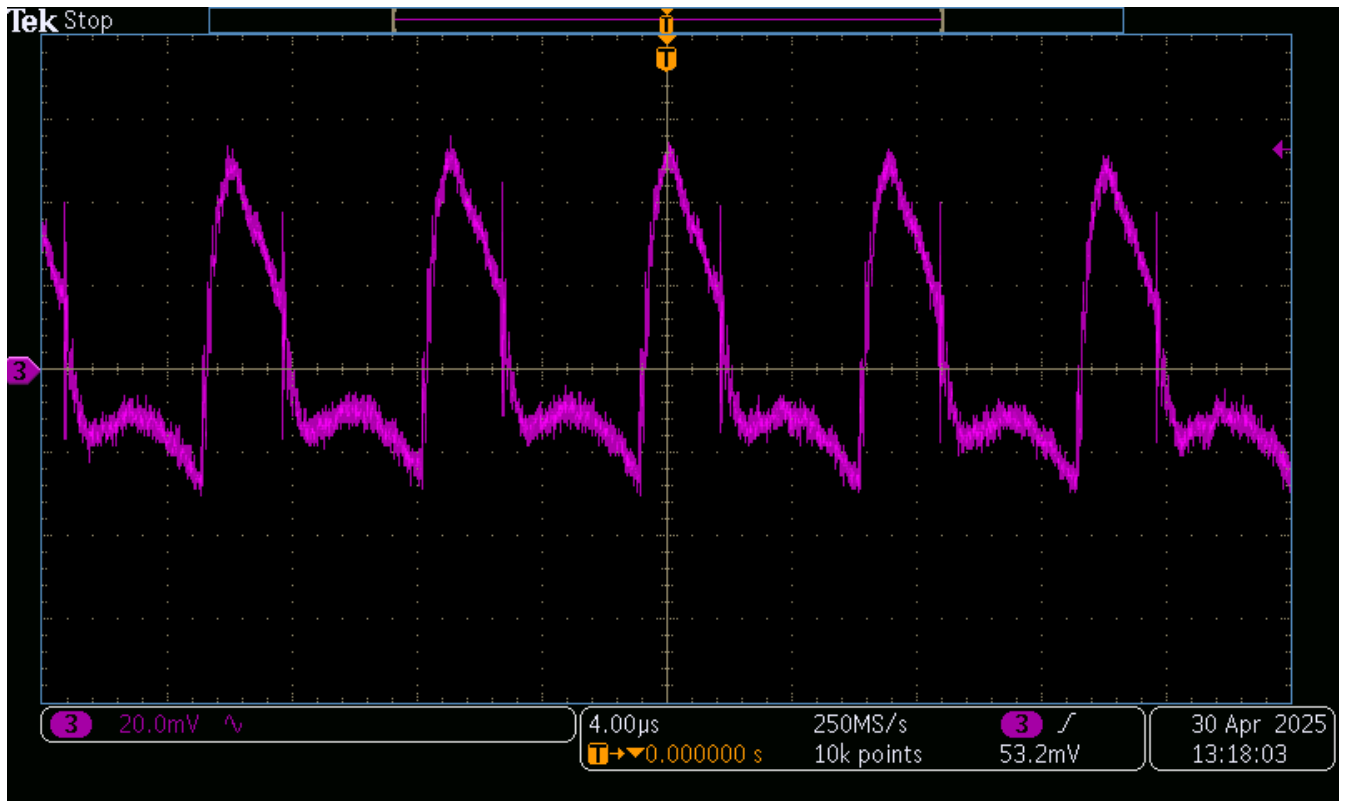


Figure 28. Steady State Output Voltage ripple, $V_{IN} = 10\text{ V}$, 1A Load. Ch.3 = Δv_o AC-coupled

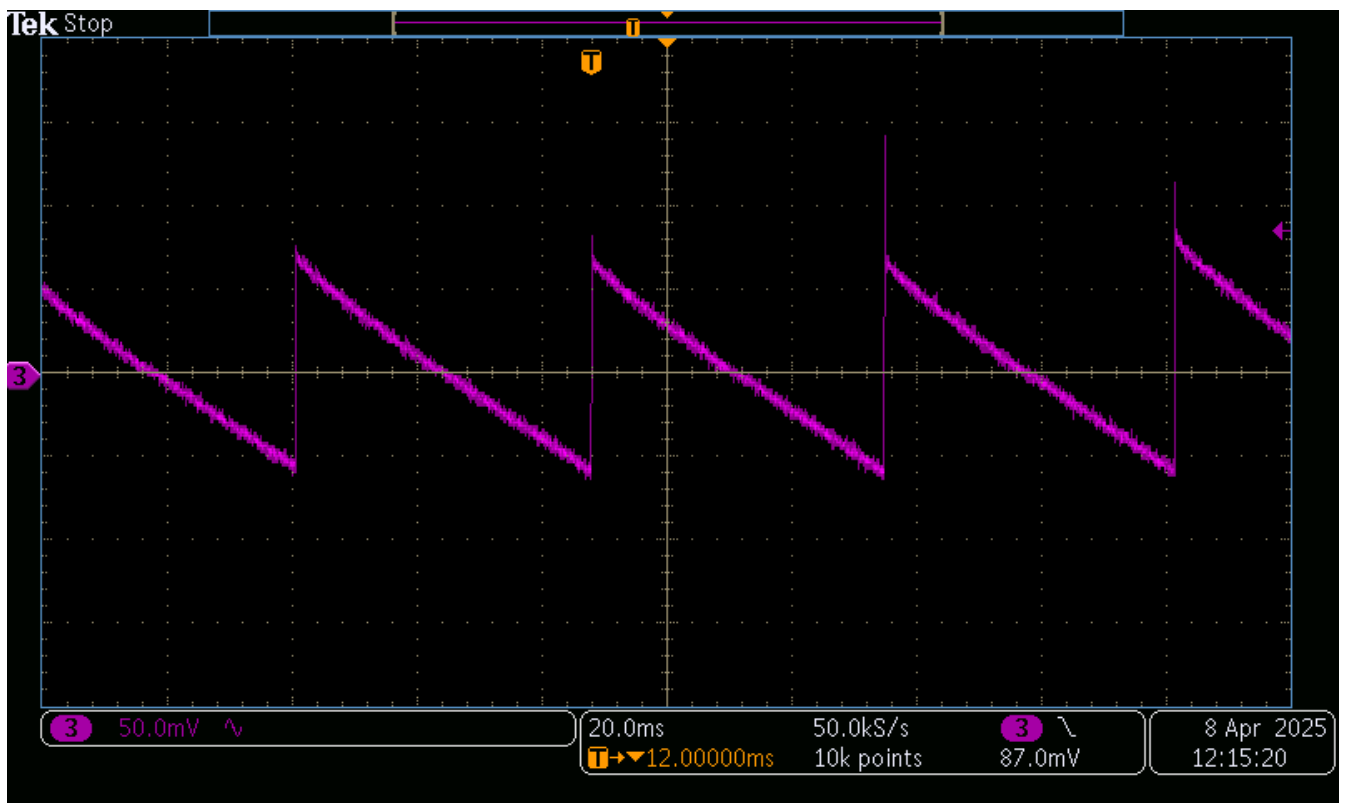


Figure 29. Steady State Output Voltage Ripple, $V_{IN} = 12\text{ V}$, No Load. Ch.3 = Δv_o AC-coupled

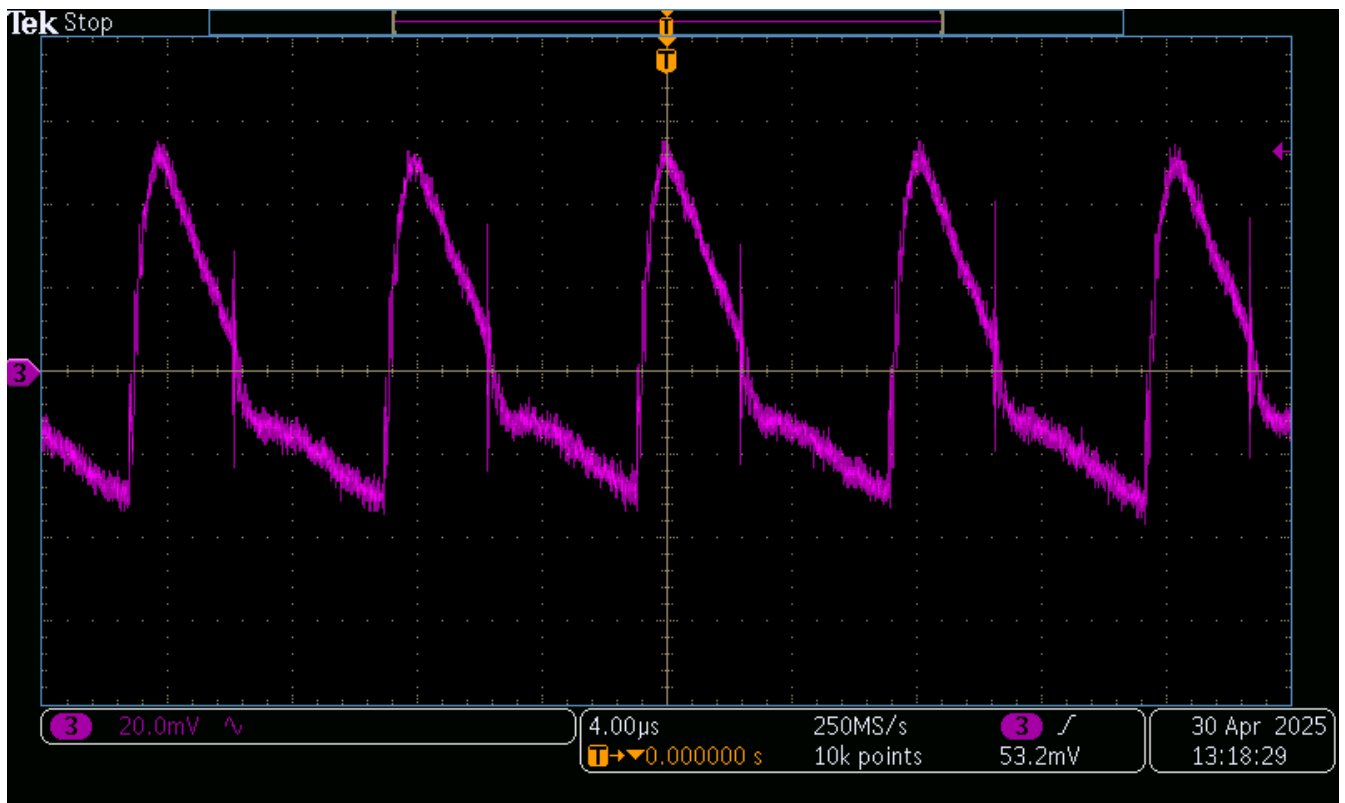


Figure 30. Steady State Output Voltage Ripple, $V_{IN} = 12\text{ V}$, 1A Load. Ch.3 = Δv_o AC-coupled

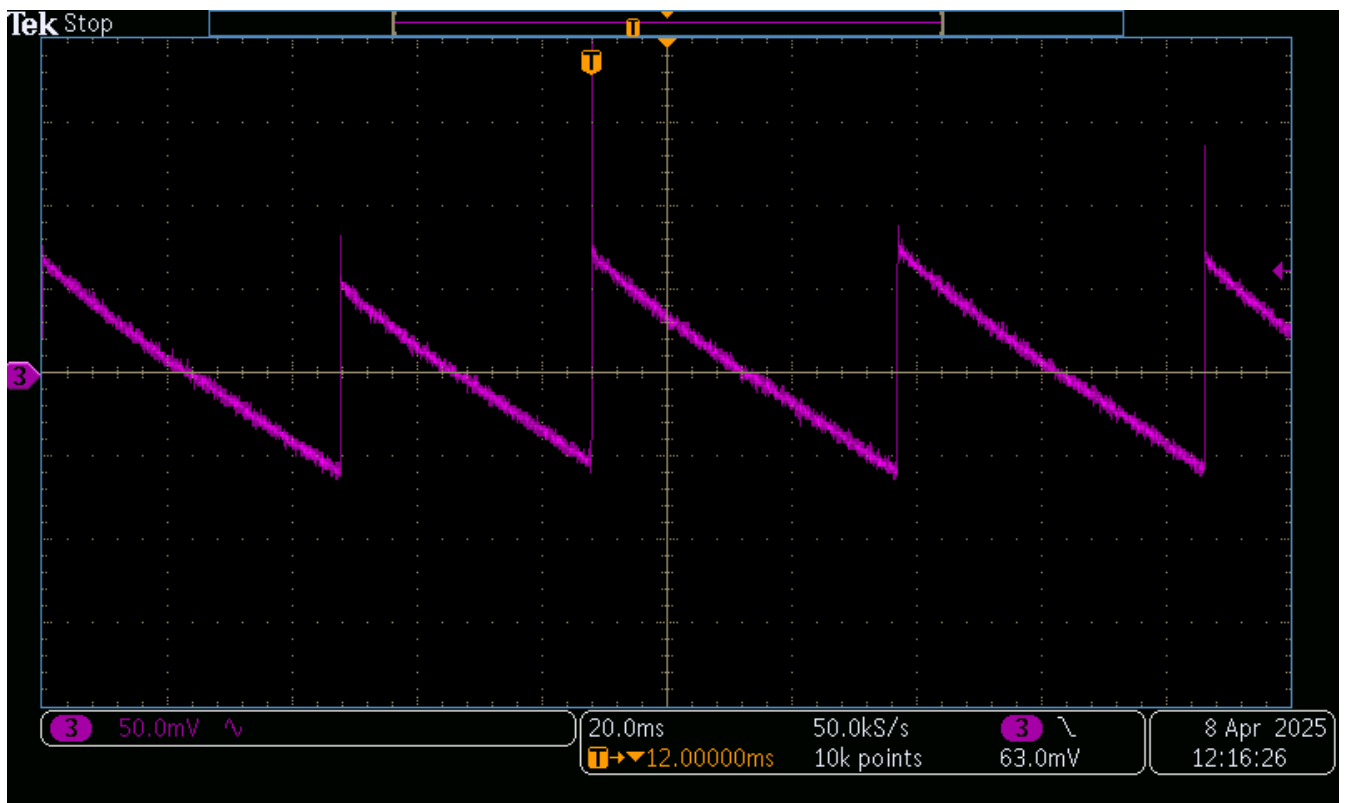


Figure 31. Steady State Output Voltage Ripple, $V_{IN} = 14\text{ V}$, No Load. Ch.3 = Δv_o AC-coupled

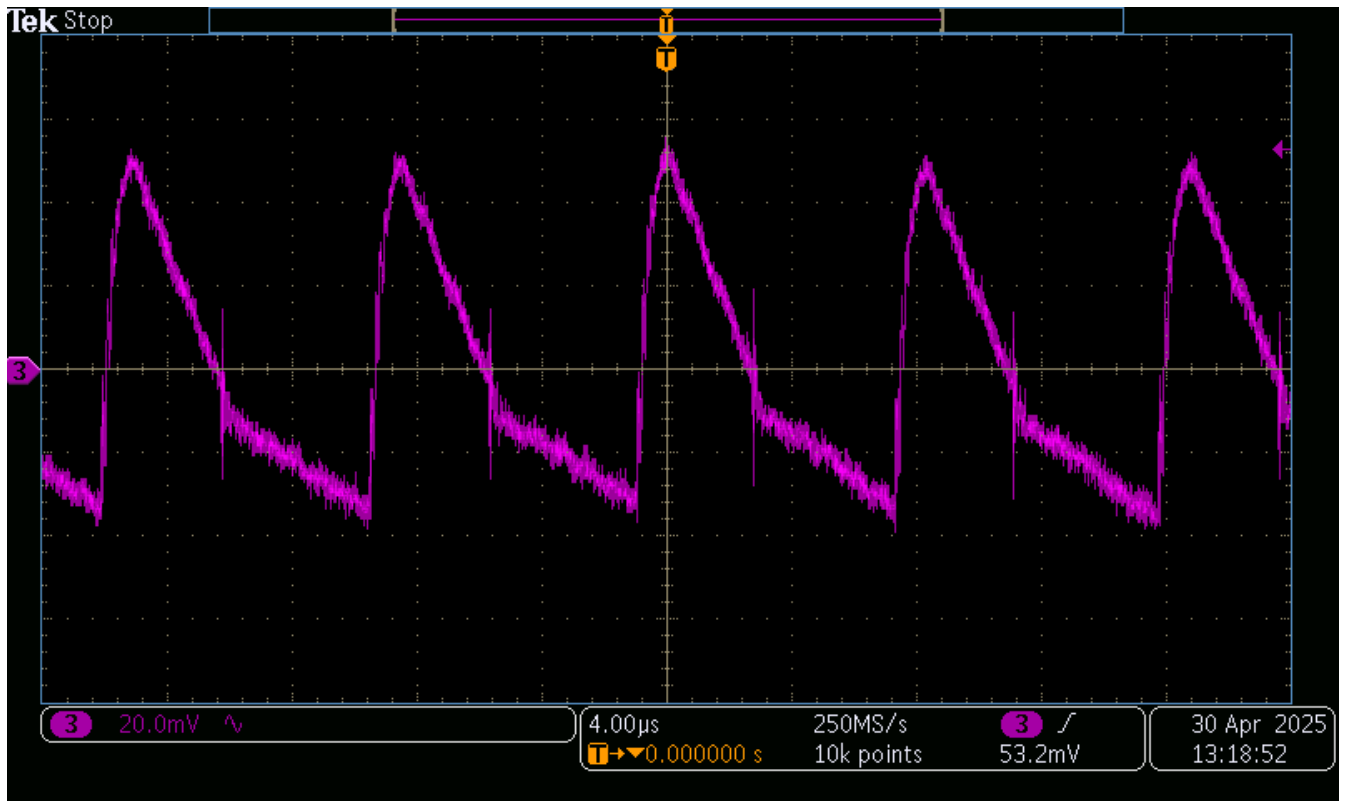


Figure 32. Steady State Output Voltage Ripple, $V_{IN} = 14\text{ V}$, 1A Load. Ch.3 = Δv_o AC-coupled



Figure 33. Shutdown via EN/SD*, 10 mA Load. Ch.1 = V_{IN} , Ch.2 = Q1 V_{GS} , Ch.3 = V_{OUT} , Ch.4 = EN/SD*

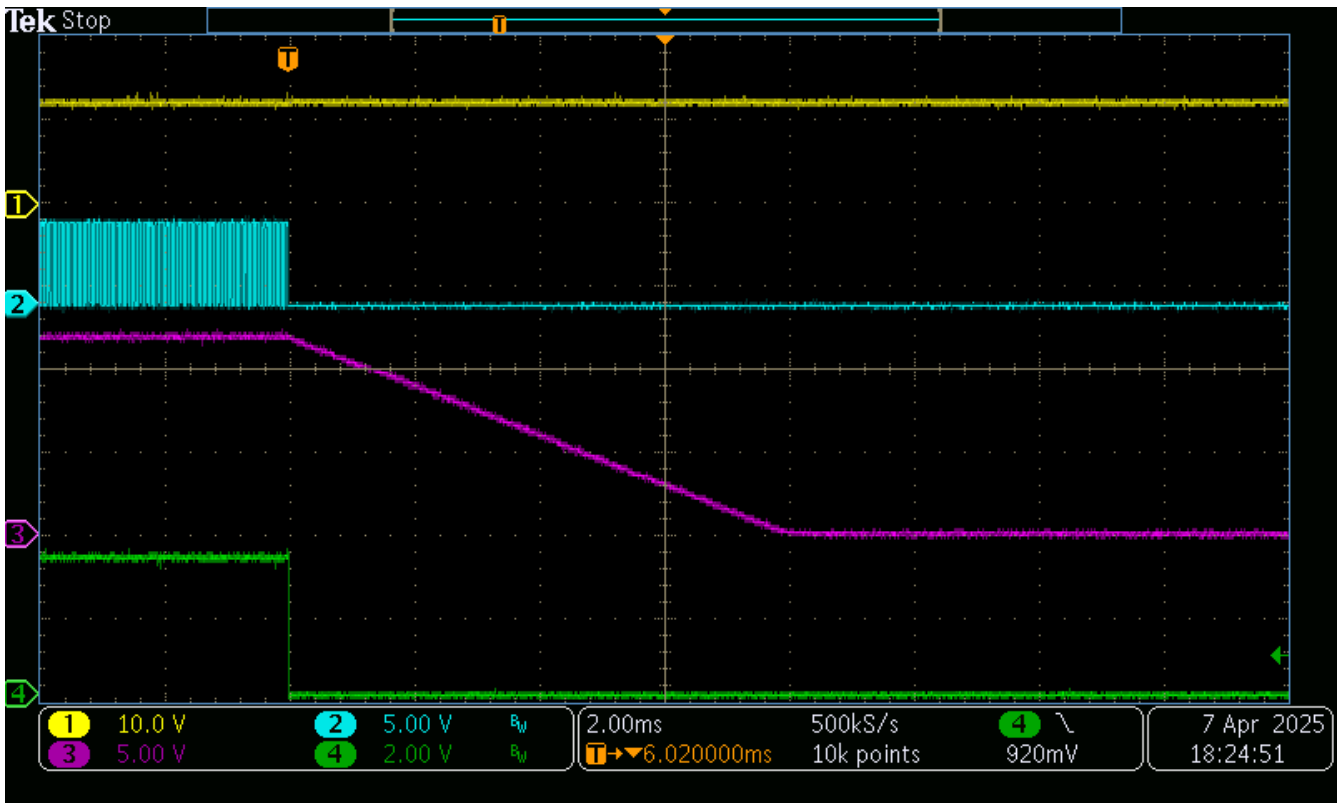


Figure 34. Shutdown via EN/SD*, 1 A Load. Ch.1 = V_{IN} , Ch.2 = $Q1 V_{GS}$, Ch.3 = V_{OUT} , Ch.4 = EN/SD*



Figure 35. Shutdown via Falling V_{IN} , 10 mA Load. Ch.1 = V_{IN} , Ch.2 = $Q1 V_{GS}$, Ch.3 = V_{OUT}



Figure 36. Shutdown via Falling V_{IN} , 1 A Load. Ch.1 = V_{IN} , Ch.2 = Q1 V_{GS} , Ch.3 = V_{OUT}

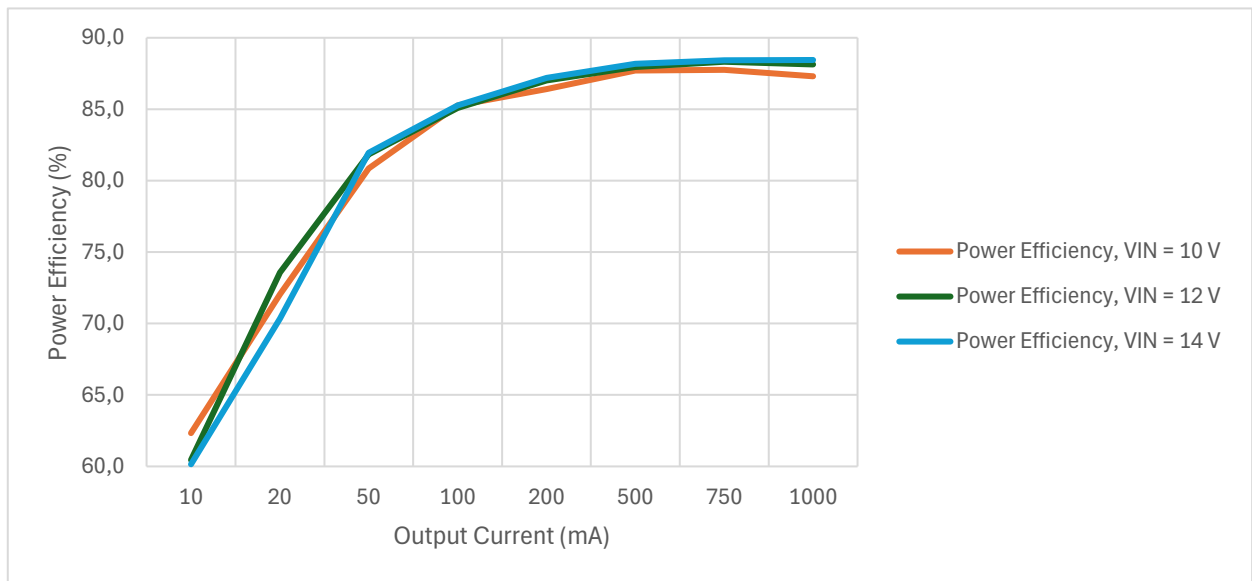


Figure 37. Power Efficiency vs Input Voltage and Load

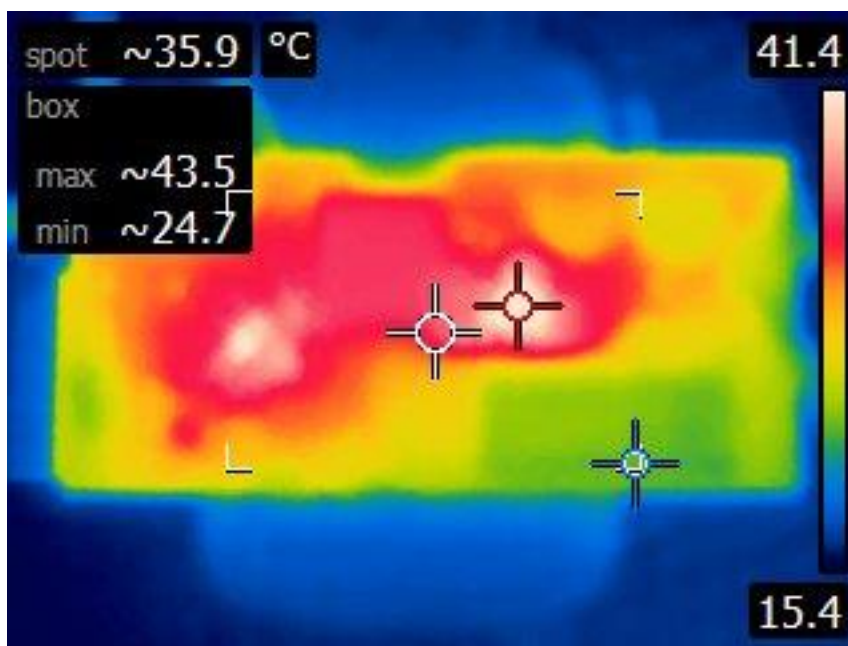


Figure 38. Thermal Image with Focus on Output Diode D6. $V_{IN} = 10\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.1\text{ }^\circ\text{C}$

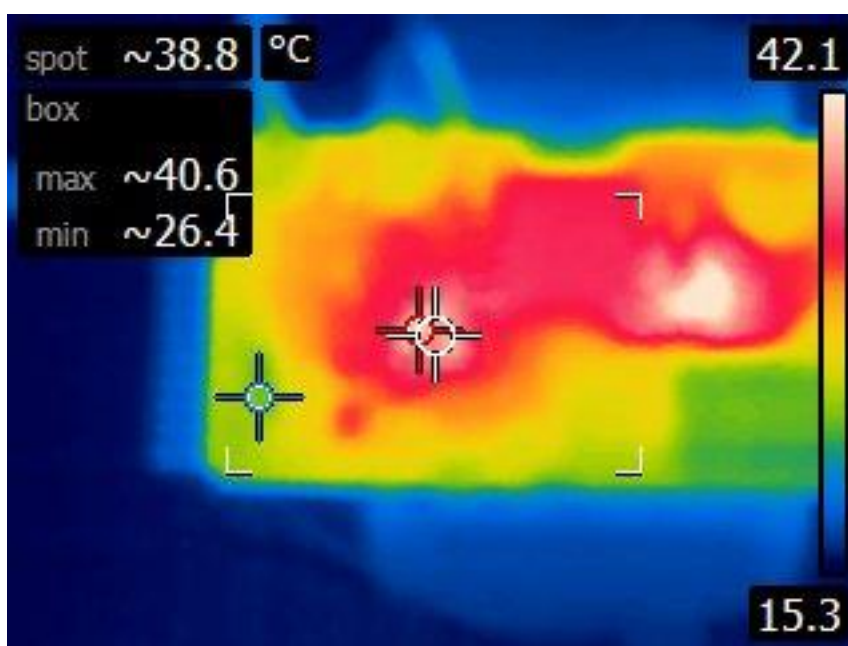


Figure 39. Thermal Image with Focus on Primary NFET Q1. $V_{IN} = 10\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.1\text{ }^\circ\text{C}$

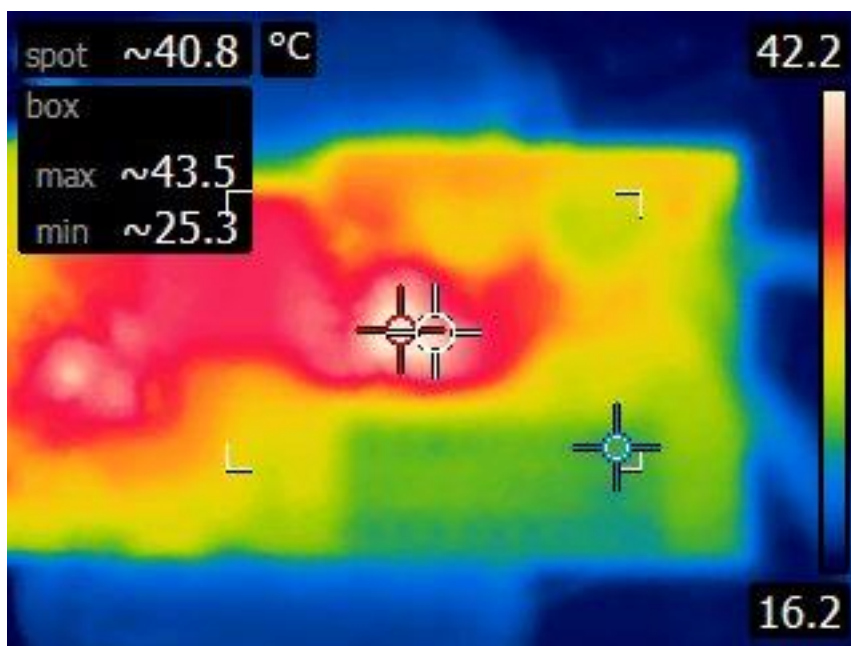


Figure 40. Thermal Image with Focus on Output Diode D6. $V_{IN} = 12\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.1\text{ °C}$

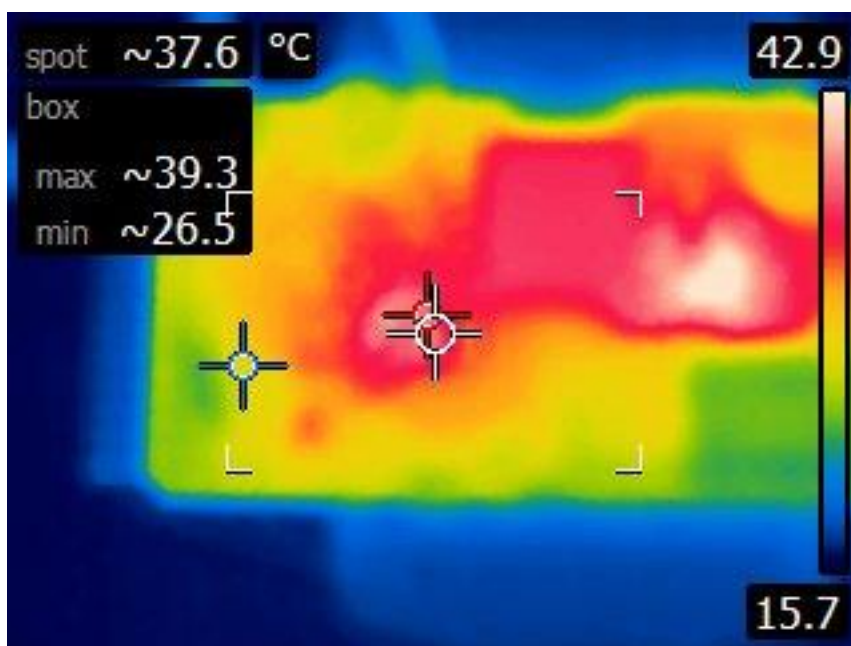


Figure 41. Thermal Image with Focus on Primary NFET Q1. $V_{IN} = 12\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.1\text{ °C}$

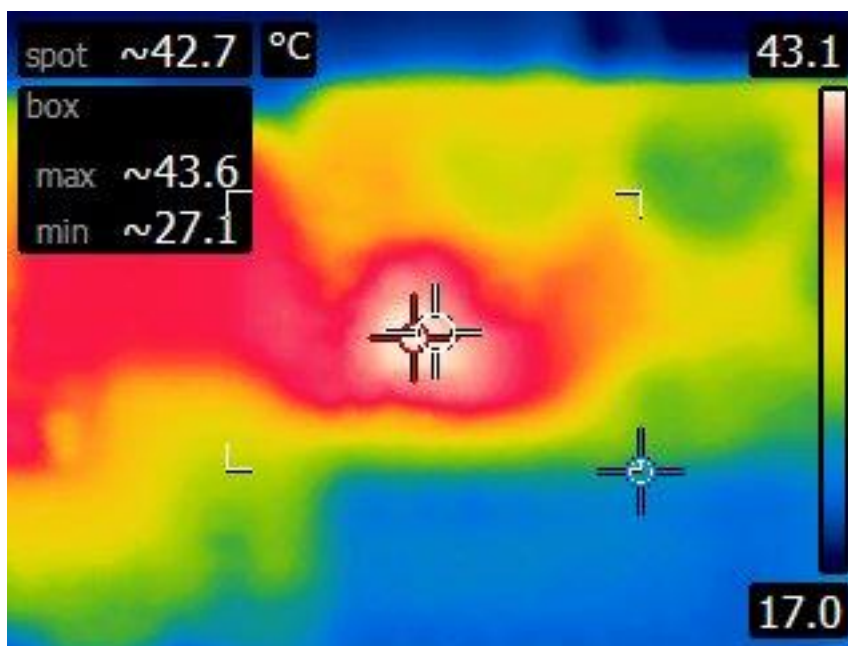


Figure 42. Thermal Image with Focus on Output Diode D6. $V_{IN} = 14\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.3\text{ °C}$

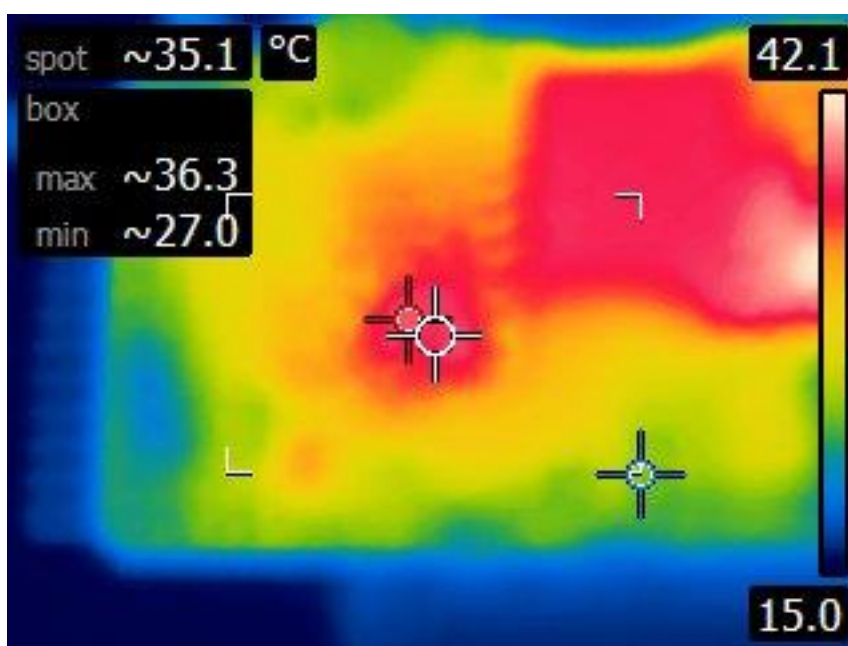


Figure 43. Thermal Image with Focus on Primary NFET Q1. $V_{IN} = 14\text{ V}$, $I_O = 1\text{ A}$, $T_A = 17.3\text{ °C}$

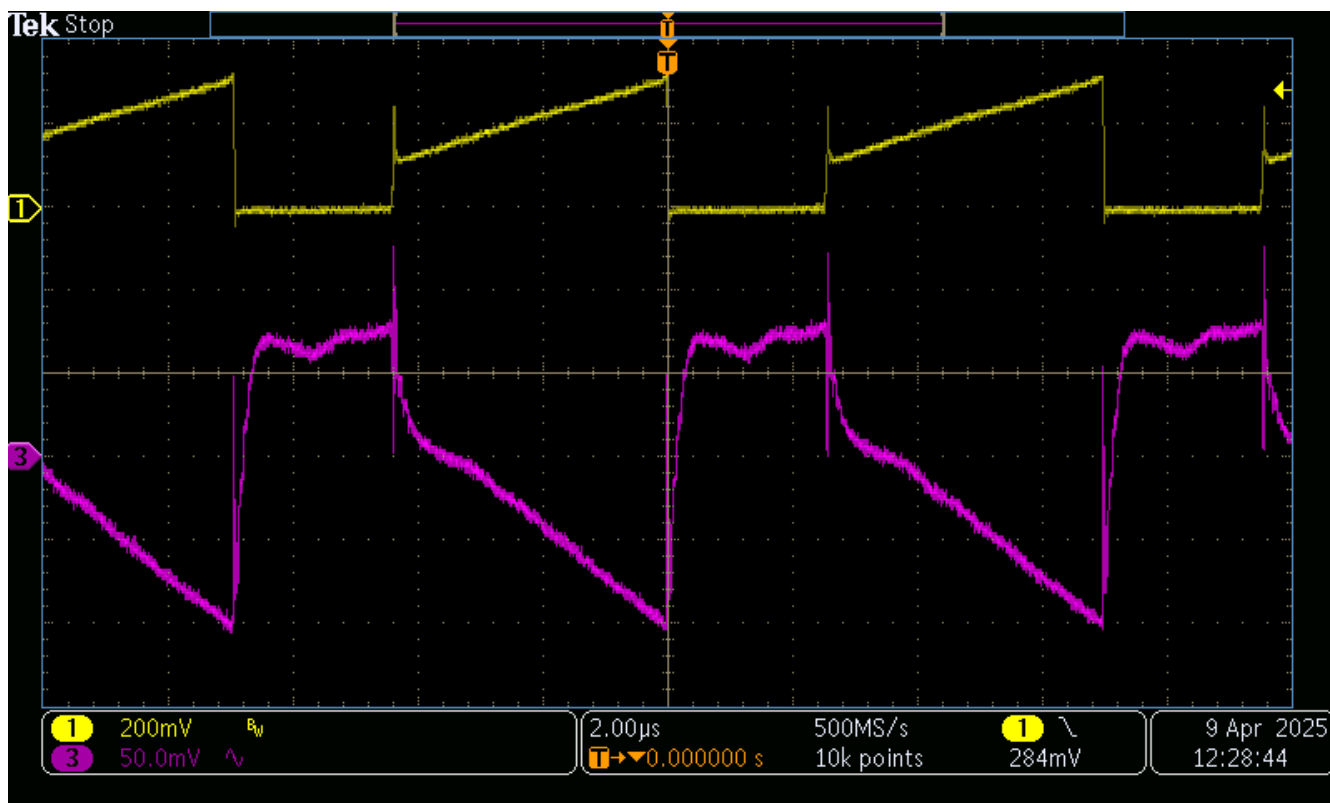


Figure 44. Steady State Input Voltage Ripple, $V_{IN} = 10\text{ V}$, 1 A Load. Ch.1 = V_{SNS} , Ch.3 = ΔV_{IN} AC-coupled

6. Complete Circuit Schematic

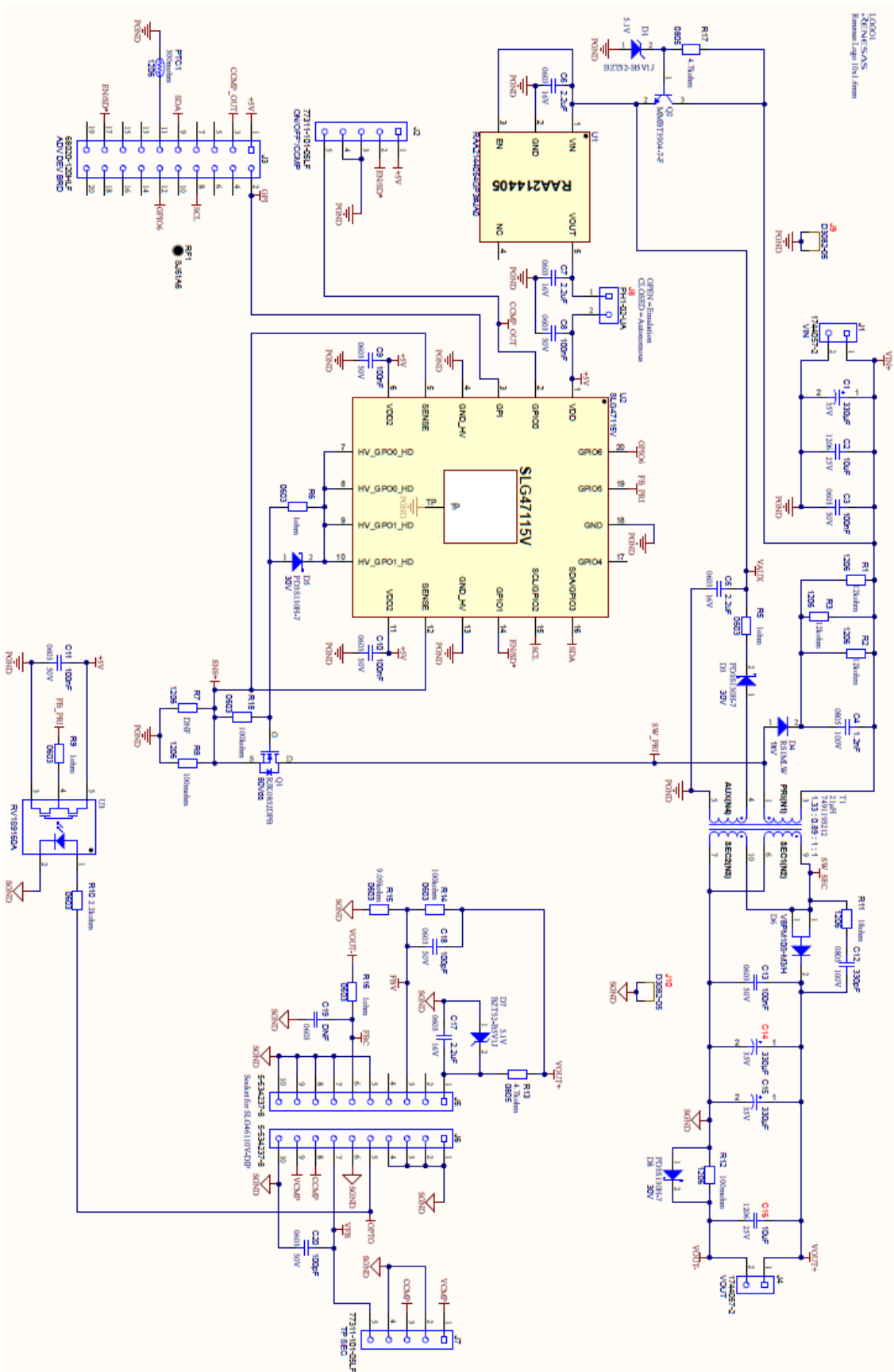


Figure 45. Complete Circuit Schematic

#	Name	Material	Type	Weight	Thickness
	Top Overlay		Overlay		
	Top Solder	Solder Resist	Solder Mask		0.01016mm
1	Top Layer		Signal	2oz	0.07mm
	Dielectric1	FR-4	Core		1.46mm
2	Bottom Layer		Signal	2oz	0.07mm
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm
	Bottom Overlay		Overlay		

Figure 48. PCB Layer Stackup

The SLG47115 and SLG46110 isolated flyback EVB uses two layers of 70 μm thick copper for improved power dissipation of its purely surface mount power components. The thermal images shown in Figure 38 to Figure 43 show that the most power is dissipated in Q1 and D6. Each has an array of thermal via to connect copper areas on the top and bottom layers to aid in spreading the heat. Each via has an outer diameter of 0.5 mm, a hole of 0.25 mm (prior to plating), and 1.0 mm of space between the center of each via to its neighbors' centers. This combination of via dimensions and spacing has led to good results for Renesas Applications Engineering, lowering thermal resistance without wicking away too much solder during assembly.

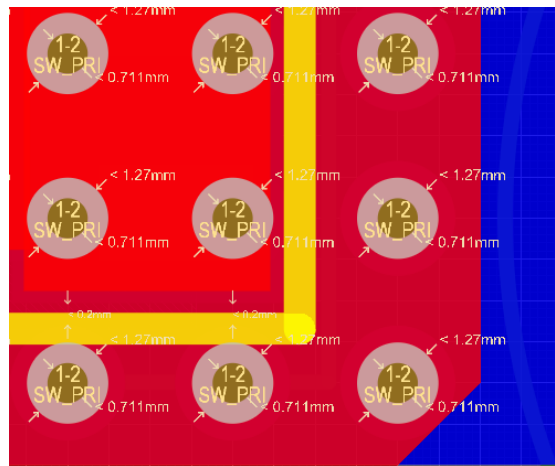


Figure 49. Thermal Via Array

7. Bill of Materials

Designator	Type	Value	Description	Manufacturer	Manufacturer Part Number	Case/Package	Quantity
C1, C14, C15	Aluminum Electrolytic Capacitor	330µF	Al-E Capacitor, 330uF, +-20%, 35V, -55 to 105°C, 2000h, SM, D10 H10.2	Panasonic	EEE-FP1V331AP	Can Radial	3
C2, C16	Multi-Layer Ceramic Capacitor	10uF	MLCC, 10µF +-10%, 25V, X7R, 1206 (3216 Metric)			1206	2
C3, C8, C9, C10, C11, C13	Multi-Layer Ceramic Capacitor	100nF	MLCC, 100nF, +- 10%, 50V, X7R, 0603 (1608 Metric)			0603	6
C4	Multi-Layer Ceramic Capacitor	1.2nF	MLCC, 1.2nF, +- 5%, 100V, VC0G, 0805 (2012 Metric)			0805	1
C5, C6, C7, C17	Multi-Layer Ceramic Capacitor	2.2uF	MLCC, 2.2uF, +-10%, 16V, X7R, 0603 (1608 Metric)			0603	4
C12	Multi-Layer Ceramic Capacitor	330pF	MLCC, 330pF +-5%, 100V, C0G, 0805 (2012 Metric)			0805	1
C18, C20	Multi-Layer Ceramic Capacitor	100pF	MLCC, 100pF, +- 5%, 50V, C0G, 0603 (1608 Metric)			0603	2
C19	Multi-Layer Ceramic Capacitor	DNF	Capacitor Place Holder, 0603 (1608 Metric)			0603	1
D1, D7	Zener Diode	5.1V	Zener Diode, 5.1V, +-2%, 590mW, SOD-123, Nexperia	Nexperia	BZT52-B5V1J	SOD-123	2
D3, D5, D8	Schottky Diode	PD3S130H-7	Schottky Diode, 30V, 1A, PowerDI-323, Diodes Inc	Diodes Inc	PD3S130H-7	SC-76 (SOD-323)	3
D4	PN Diode	RS1MLW	PN Diode, Fast, 1kV, 1A, SOD-123W, Taiwan Semi	Taiwan Semi	RS1MLW	SOD-123W	1
D6	Schottky Diode	V8PM10S-M3/H	Schottky Diode, 100V, 8A, TO-277A, Vishay	Vishay	V8PM10S-M3/H	TO-277A (SMPC)	1
J1, J4	Header	1744057-2	Male Header, Vert, 1x2, 3.96 mm, 1-Wall, TH, TE	TE	1744057-2	7.92x8.6x9.4mm	2
J2, J7	Board-to-Board	77311-101-05LF	Male Header, 1x5, 2.54mm, Vert, Straight, TH	Amphenol	77311-101-05LF	12.3x2.4x10.8mm	2
J3	Board-to-Board	68020-120HLF	Male Header, 2x10, 2.54mm, Vert, Right Angle, TH	Amphenol	68020-120HLF	25.4x12.7x4.83mm	1
J5, J6	Board-to-Board	5-534237-8	Female Socket, 1x10, 2.54mm, Vert, Straight, TH	TE Connectivity	5-534237-8	25.4x3.56x8.64mm	2
J8	Board-to-Board	PH1-02-UA	Male Header, 1x2, 2.54mm, Vert, Straight, TH	Adam Tech	PH1-02-UA	5.1x2.5x8.5mm	1
J9, J10	Shunt/Jumper	D3082-05	Shunt/Jumper, U-Bar, 10.16mm, 10A, Vert, TH, Harwin	Harwin	D3082-05	10.16x9mm D1.0	2
PTC1	PTC Resettable Fuse	300mohm	PTC Resettable Fuse, 350mA, 1206 (3216 Metric)	Bel Fuse	OZCJ0035AF2E	1206	1
Q1	Silicon NMOS	RJK0852DPB	NMOS, 80V, 30A, LFPK, Renesas	Renesas	RJK0852DPB-00#J5	LFPK	1
Q2	NPN BJT	MMBT3904-7-F	NPN, General Purpose, 40V, 0.2A, SOT23-3, Diodes Inc	Diodes Inc	MMBT3904-7-F	TO-236-3 (SOT23-3)	1
R1, R2, R3	Chip Resistor	12kohm	Chip Resistor, 1206, 12kohm +-1%, 0.25W, Thick Film, (3216 Metric)			1206	3
R5, R6, R9, R16	Chip Resistor	1ohm	Chip Resistor, 0603, 1ohm +-1%, 0.1W, Thick Film, (1608 Metric)			0603	4
R7	Chip Resistor	DNF	Resistor Place Holder, 1206 (3216 Metric)			1206	1
R8, R12	Current Sense Resistor	100mohm	Sense Resistor, 1206, 100mohm +-1%, 0.5W, ThickFilm, 3216 Metric	Vishay	RCWE1206R100FK EA	1206	2
R10	Chip Resistor	2.2kohm	Chip Resistor, 0603, 2.2kohm +-1%, 0.1W, Thick Film, (1608 Metric)			0603	1
R11	Chip Resistor	18ohm	Chip Resistor, 1206, 18ohm +-1%, 0.25W, Thick Film, (3216 Metric)			1206	1
R13, R17	Chip Resistor	4.7kohm	Chip Resistor, 0805, 4.7kohm +-1%, 0.125W, Thick Film, (2012 Metric)			0805	2
R14, R18	Chip Resistor	100kohm	Chip Resistor, 0603, 100kohm +-1%, 0.1W, Thick Film, (1608 Metric)			0603	2
R15	Chip Resistor	9.09kohm	Chip Resistor, 0603, 9.09kohm +-1%, 0.1W, Thick Film, (1608 Metric)			0603	1
RF1	Bumper	SJ61A6	Rubber Foot, Cylindrical, D7.92 H5.46, 3M	3M	SJ61A6	D7.92mm H5.46mm	1
T1	Transformer	7491195212	Flyback Xfmr, 24W, 1.33 : 1 : 1 : 0.89, 21uH, EP13, 1.5kVrms, SM, Würth	Würth	7491195212	17.6x14x14.5mm	1
U1	Linear Regulator	RAA214405	Low Dropout Regulator, 4.5-40VIN, 5Vout, 150mA, SOT23-5	Renesas	RAA2144054GP3# JA0	SOT23-5	1
U2	Programmable matrix	SLG47115V	GreenPAK Programmable Matrix, Quad Output, 24V, 6Apk, STQFN20-2x3	Renesas	SLG47115V	STQFN20-2x3	1
U3	Optocoupler	RV1S9160A	Optocoupler, Single, 15 Mbs, Push-Pull Output, 3750Vrms, 50kV/us, SOIC-5, Renesas	Renesas	RV1S9160ACCSP-100C#KC0	SOIC-5	1

8. Emulation of Different Configurations

Users can try different input voltages, output voltages, output powers, or switching frequencies by selecting their components using the equations described in this application note and accompanying Excel worksheet. Any of the parameters in the Flyback EVB's default Go Configure file can be modified and tested using the EVB connected to a development board and running it in Emulation Mode. It is important to first remove Jumper J8, which disconnects the onboard 5 V linear regulator U1 from the VDD and VDD2 pins of the SLG47115. The flyback evaluation board can then be plugged into an Advanced Development Board (part number SLG4DVKADV) or Development Board Lite (part number SLG4DVKLITE), both of which are available from renesas.com. Either board will then provide 5 V for the VDD and VDD2 nets. When used in Emulation Mode, either development board can overwrite the registers of the SLG47115 IC on the flyback evaluation board for as long as they are connected. Please keep in mind that as soon as Emulation ends and the Flyback EVB is removed, the SLG47115 IC will return to its default programming.

The parameters most commonly modified are:

- The inverting input threshold to the fast current comparator, CCMP
- The maximum on-time set by CNT/DLY1
- The minimum off-time set by CNT/DLY2
- The slew rate for the HV OUT CTRL block.

The following procedure should be followed:

1. Remove Jumper J8 from the PCBA.
2. Connect the Advanced Development Board or Development Board Lite to a PC with a USB cable.
3. Start the Go Configure software and load the Flyback EVB Go Configure file with the desired modifications.
4. Connect the Flyback EVB's output to a load via J4. If using an electronic load, leave it off or disabled.
5. Under Debug, select Emulation and the appropriate development board. In most cases an error message will pop up – this is because several pins of the Flyback EVB are unconnected.
6. Select “Skip and Proceed”.
7. Connect a lab supply to the VIN and PGND terminals of J1. Make sure it is rated for enough current to supply 150 % of the maximum output power of the flyback converter.
 - a. A program jumper can be used to short Pins 1 and 2 (+5 V and EN/SD*) of J2. When set, the Flyback EVB will begin operating as soon as input power is applied.
 - b. **IMPORTANT:** input power should NOT be applied before Go Configure has successfully begun Emulation.
8. If no jumper is fitted to Pin 1 and Pin 2 of J2, use a second lab supply or another logic signal to apply a voltage > 3.0 V to the EN/SD* pin on J2. This enables switching.

9. Non-isolated Flyback in Go Configure for Simulation

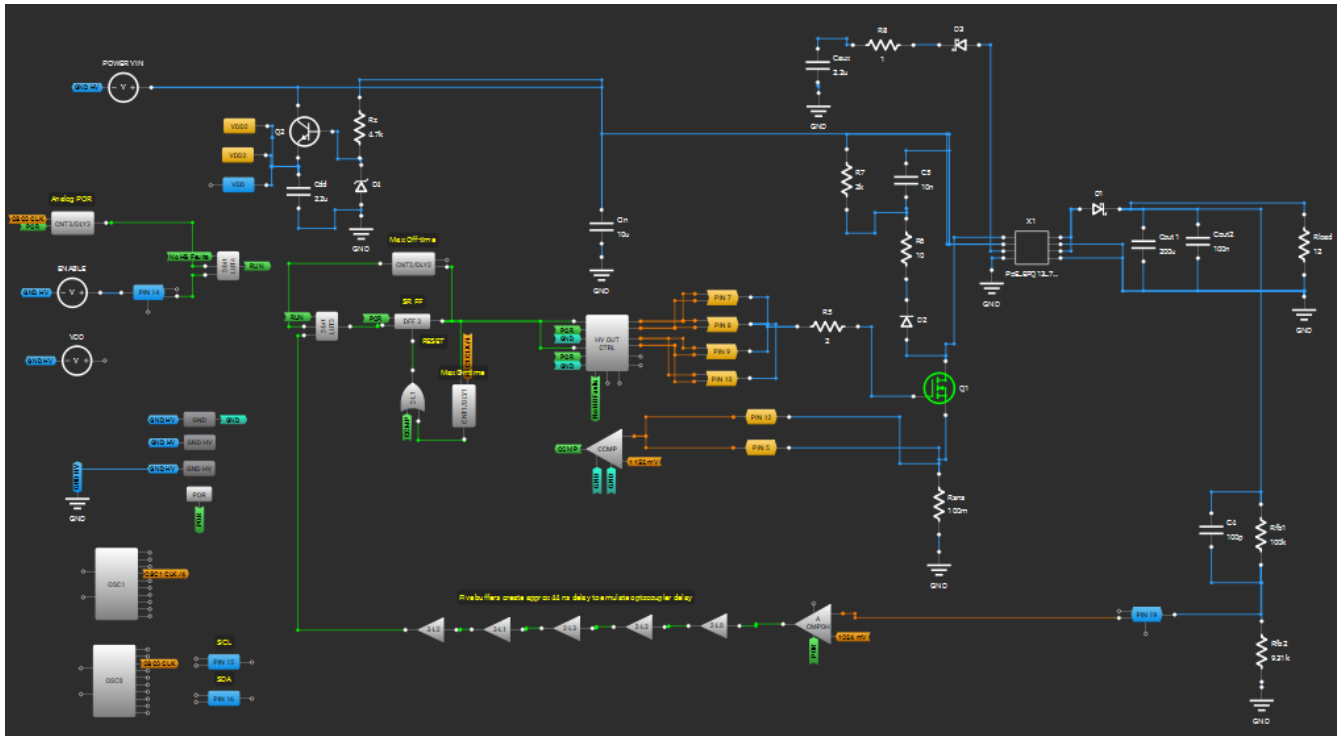


Figure 50. Non-isolated Flyback Go Configure File

Figure 50 shows the Go Configure design for a flyback regulator with the same operating conditions as the Flyback EVB, including an imported SPICE model for the transformer T1 and five buffers to emulate the propagation delay of the optocoupler. The SLG46110 is not needed as non-isolated feedback comes in to Pin 19 directly from the output voltage resistor divider. This circuit does not have the CC/CV dual control loop included in the actual Flyback EVB, but it can be used to simulate new designs using CV control before testing them with the development boards and the emulation feature.

10. Conclusion

Although the SLG47115 was designed with motor control applications in mind, its power half-bridge circuits and fast comparators allow it to control low-side switching regulators with a combination of hysteretic and peak current control. Besides the flyback, the SLG47115 can be used for boost regulators, SEPIC regulators and four-switch buck-boost regulators. Furthermore, a large selection of the GreenPAK mixed signal resources in the SLG47115 are not required to operate the flyback, including both analog comparators, the programmable delay, multiple combination function and multi-function macrocells and five GPIOs. The I²C interface could also be used to monitor and adjust flyback operation. On the secondary side, the SLG46110 still has five unused counter/delays, four lookup tables, an oscillator, a programmable filter/delay block and two spare GPIOs that could be employed in many different ways. Overall, the power converter presented in this application note is comparable in efficiency and power density to any other flyback regulator in the same frequency range and offers a host of mixed signal resources not found in any other switching regulator.

11. Revision History

Revision	Date	Description
1.00	Sep 9, 2025	Initial release