Binary Clock using SLG46533
SLG46533

This application note describes how to use the SLG46533 to implement a binary clock.

The application note comes complete with a design files that can be found in the Reference section.

Contents

1. Terms and Definitions

ACMP	Analog Comparator
CNT/DLY	Counter-Delay
DFF	D Flip-flop
GPO	General Purpose Output
IC	Integrated Circuit
I/O	Input / Output
LDR	Light-dependent resistor
LED	Light Emitting Diode
LUT	Look-up Table
MF	Multi-function Macrocell
OSC	Oscillator
PCB	Printed Circuit Board

2. References

For related documents and software, please visit:

GreenPAK Programmable Mixed-Signal Products | Renesas

Download our free GreenPAK Designer software [1] to open the .app files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Renesas Electronics

[2] AN-CM-419 Binary Clock using SLG46533, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

3. Introduction

A binary clock is a timekeeping device that displays the time of day in binary format.

Depending on the method of time representation, binary clocks are typically categorized into two types: Binary-Coded Decimal (BCD) Clocks and Binary-Coded Sexagesimal Clocks.

3.1 Binary-Coded Decimal Clocks

Most binary-coded decimal clocks use six columns of LEDs to represent binary digits (bits). Each column corresponds to a single decimal digit, following a format known as Binary-Coded Decimal (BCD). The bottom row in each column represents the least significant bit (value of 1 or 2^0), and each row above corresponds to higher powers of two, up to 2^3 (value of 8).

To read each individual digit of the time, the user sums the values of the illuminated LEDs in a column and then reads the resulting decimal digits from left to right. The first two columns represent the hour, the next two represent the minutes, and the last two represent the seconds.

3.2 Binary-Coded Sexagesimal Clocks

There are also binary clocks that represent time using a binary sexagesimal format. Instead of representing each decimal digit of conventional sexagesimal time separately, each component of the time (hours, minutes, seconds) is represented as a single binary number. This method may use up to 6 bits per time component, rather than the 4 bits that are used in BCD clock.

In 24-hour binary-coded sexagesimal clocks, the display typically includes either 11 or 17 LEDs: 5 LEDs for hours, 6 LEDs for minutes, and optionally another 6 LEDs for seconds (which are omitted in the 11-LED version).

There is also a format in which hours, minutes, and seconds are displayed as binary numbers arranged in three horizontal rows instead of vertical columns.

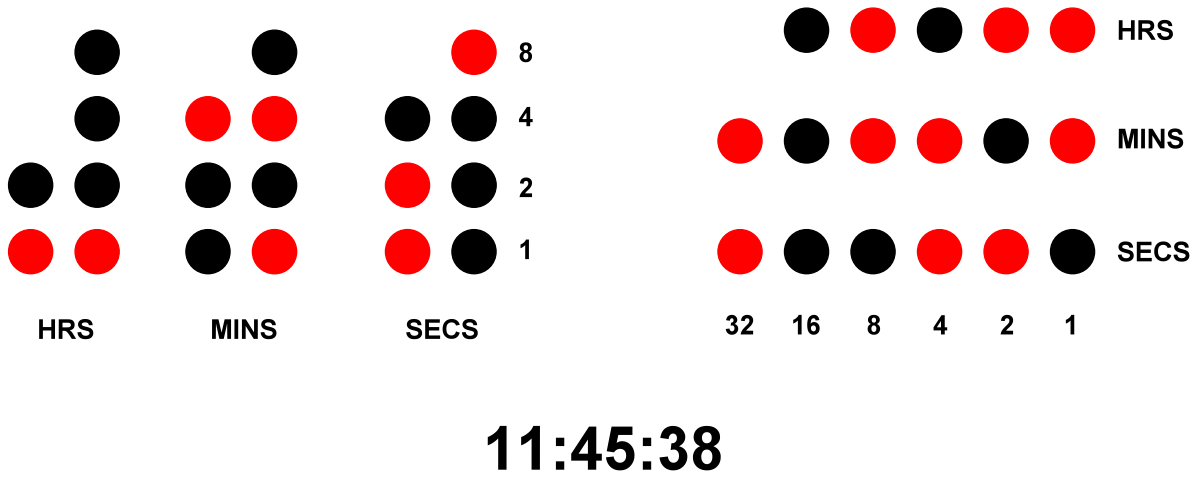

Figure 1. Examples of Time Representation on Binary-Coded Decimal Clocks (Left) and Binary-Coded Sexagesimal Clocks (Right)

This application note examines the implementation of each type of binary clock using GreenPAK SLG46533 chips. The SLG46533 is a suitable solution for a binary clock due to its integrated Crystal Oscillator module, twenty-six Combination Function Macrocells, and 17 GPIO / 1 GPI pins.

Any electronic clock consists of the following essential building blocks:

- A stabilized pulse generator (Crystal Oscillator)
- A divide-by-32768 circuit / seconds pulse generator
- A divide-by-60 circuit / “seconds” counter
- A divide-by-60 circuit / “minutes” counter
- A divide-by-24 circuit / “hours” counter
- Time setting and control circuitry

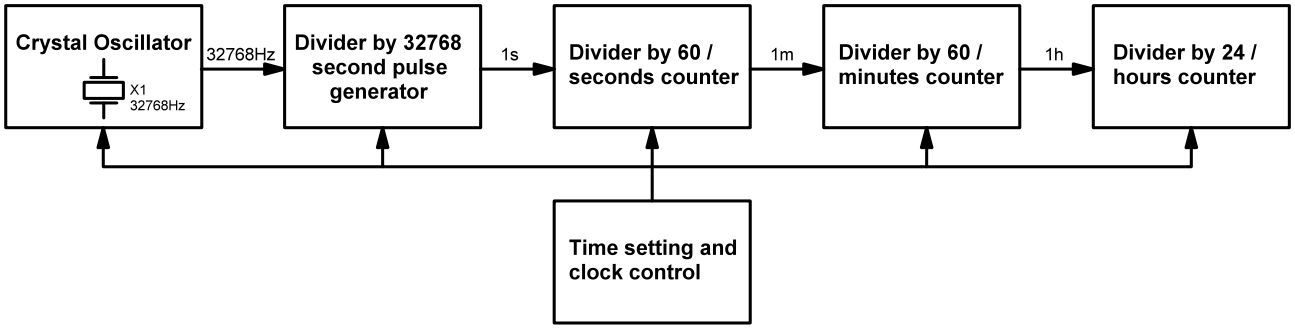

Figure 2. Simplified Block Diagram of an Electronic Clock

4. Binary-coded Decimal Clock Design

4.1 Circuit Design (Binary-coded decimal clock)

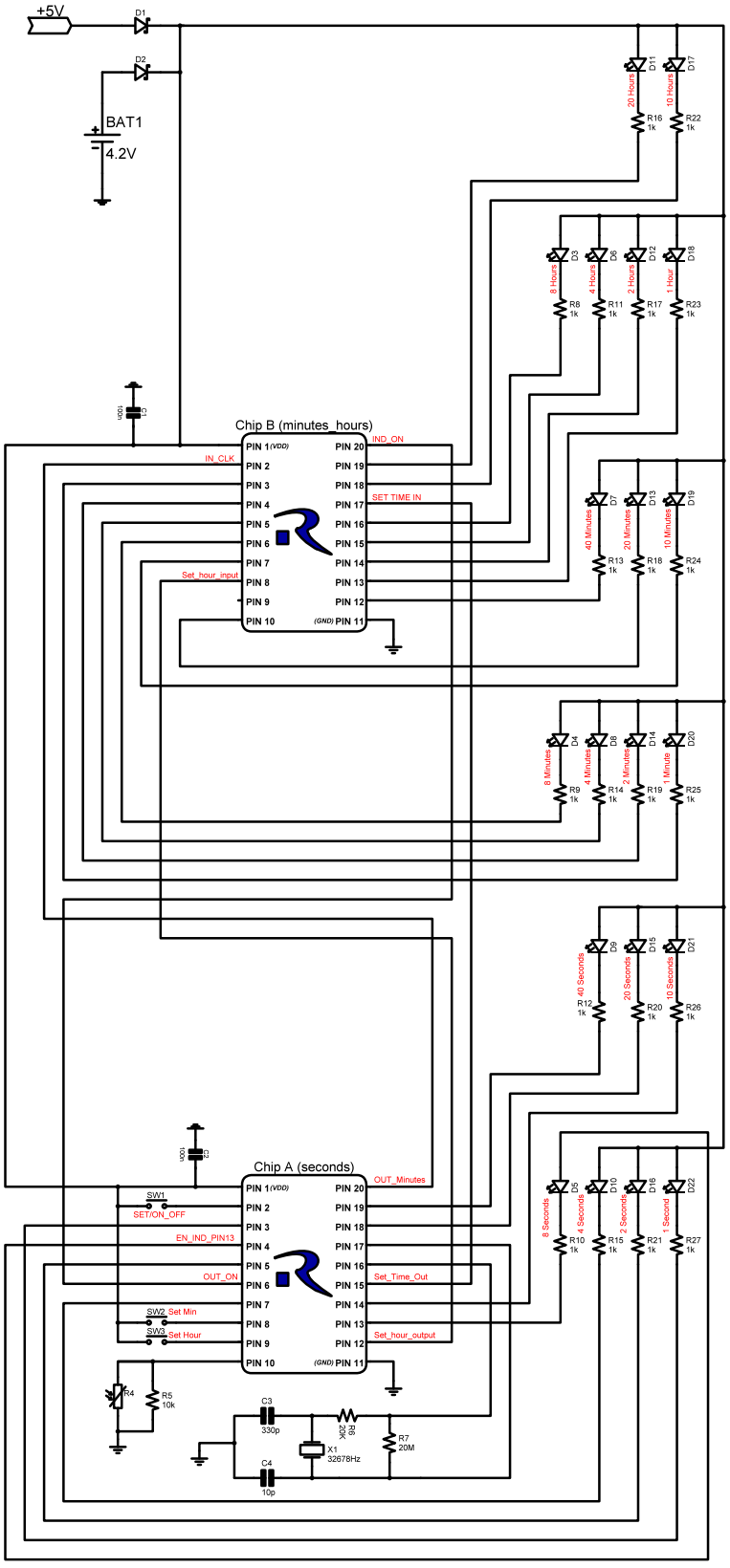

Figure 3. Electrical Schematic of a Binary-Coded Decimal Clock

This implementation of the Binary-Coded Decimal Clock is built using two SLG46533V chips.

The clock displays the time using 20 LEDs in a Binary-Coded Decimal (BCD) format. Time control and adjustment are performed using three buttons: SET/ON_OFF, Set Minutes, and Set Hours.

The clock can operate from a stationary 5 V power source or from a rechargeable battery (with a voltage range of 3.0 V to 4.2 V). When powered by a 5 V stationary supply, the time display remains continuously active. In battery-powered mode, the time display is activated for 1 minute by a short press of the SET/ON_OFF button to save energy.

The clock also features a "Night Mode", in which the brightness of the time display is reduced. This mode is automatically activated in low ambient light conditions. If the battery voltage drops below 3.4 V, the clock enters night mode to reduce power consumption, and the seconds segment begins to blink—indicating that the battery should be recharged soon. When the battery voltage falls below 3.0 V, the display is completely turned off while internal timekeeping continues uninterrupted.

To set the correct time, the SET/ON_OFF button must be held down for approximately 1 second. Entering the time-setting mode disables the internal one-second pulse generator and resets the seconds counter to zero.

The correct time is then set using the Set Minutes and Set Hours buttons. Time adjustments can only be made in the increasing direction. While in time-setting mode, the time display remains on regardless of the power source being used (battery or fixed). After setting the time, holding the SET/ON_OFF button for about 1 second switches the clock back to its normal operation mode.

Let us examine the design implementation of each of the chips in this version of binary clock:

Chip A:

- Crystal Oscillator
- Divide-by-32768/second pulse generator
- Divide-by-60 circuit / “seconds” counter
- Time setting and clock control

Chip B:

- Divide-by-60 circuit / “minutes” counter
- Divide-by-24 circuit / “hours” counter

4.2 GreenPAK Design of Chip A for Binary-Coded Decimal Clock

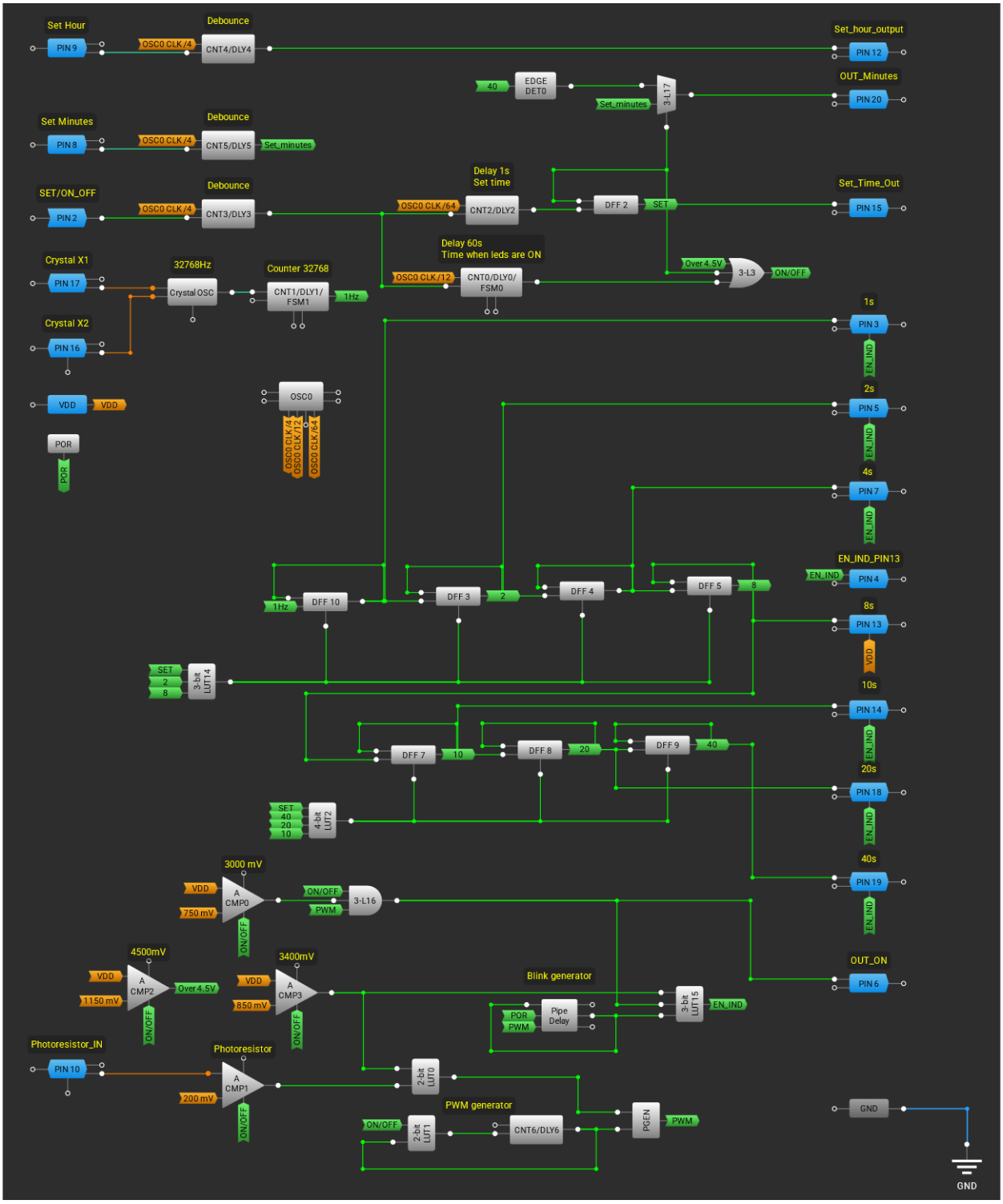

Figure 4. GreenPAK Design of Chip A for the Binary-Coded Decimal Clock

4.2.1. Crystal Oscillator

The stable pulse generator responsible for generating one-second timing pulses is built using the Crystal Oscillator module, which is specifically designed to operate with external quartz resonators.
Figure 5 shows the circuit configuration for connecting the quartz resonator. For this clock, we will use a standard quartz crystal resonator (typically used for watches) with a frequency of 32.768 kHz.

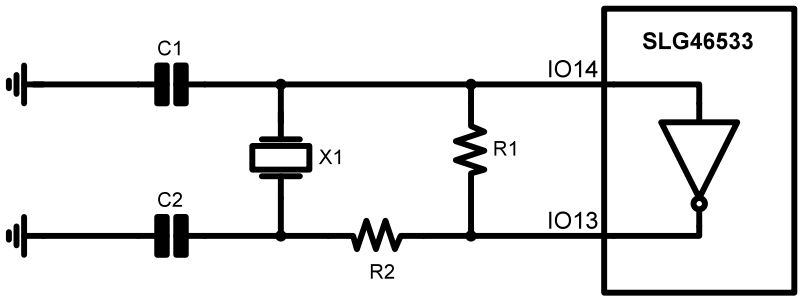

Figure 5. Circuit Diagram for connecting a standard Quartz Resonator

To obtain stable one-second intervals, the frequency of 32.768 kHz generated by the Crystal Oscillator needs to be divided by 32,768. A 16-bit CNT1/DLY1/FSM1 is used as the divider, configured as a counter (see Figure 6).

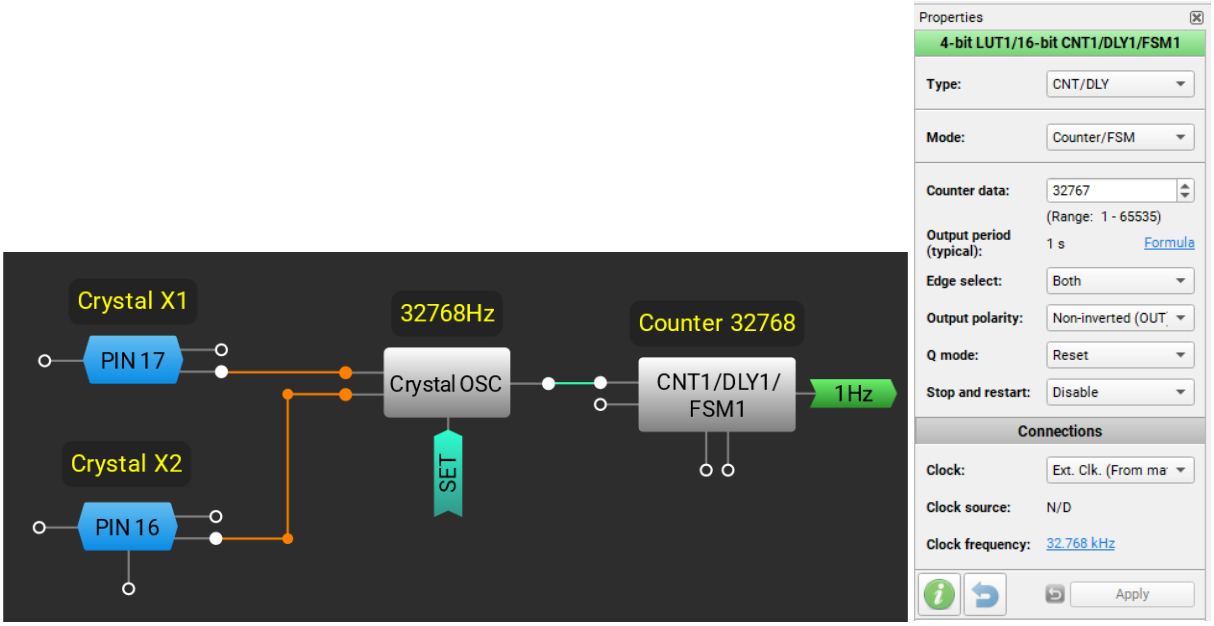

Figure 6. "Seconds" Pulse Generator and CNT1 Configuration

4.2.2. Divide by 60 / Seconds Counter

The Divide by 60 / "seconds" counter is responsible for converting the one-second pulses into one-minute pulses. This part of the design consists of two sections: the Divide by 10 counter and the Divide by 6 counter.

The Divide by 10 counter is based on a chain consisting of DFF10, DFF3, DFF4, DFF5, and 3-bit LUT14. Each DFF in this chain is configured as a divide-by-2 circuit. Thus, the entire chain performs a division operation on the frequency by 16. To limit the division to 10, 3-bit LUT14 is used to reset DFF10, DFF3, DFF4, and DFF5 to their initial state when a LOW signal appears on the outputs of DFF3 and DFF5.

The Divide by 6 counter follows a similar design using a chain consisting of DFF7, DFF8, DFF9, and 4-bit LUT2. The maximum division factor of this chain is 8. To achieve division by 6, 4-bit LUT2 is used to reset DFF7, FF8, and DFF9 to their initial state when the combination of HIGH, LOW, LOW signals appear at the outputs of DFF7, DFF8, and DFF9 respectively.

Together, these two dividers generate a frequency division by 60, resulting in pulses with a 1-minute period. The outputs of DFF10, DFF3, DFF4, DFF5, and DFF7, DFF8, DFF9 provide the signals to display the seconds on the clock. The active level for display is LOW. An oscilloscope waveform showing the operation of the Divide by 60 / "seconds" counter is shown in Figure 8.

Both 3-bit LUT14 and 4-bit LUT2 have SET inputs, where a HIGH level performs a reset of the entire Divide by 60 / “seconds” counter when entering the clock’s “Setting” mode.

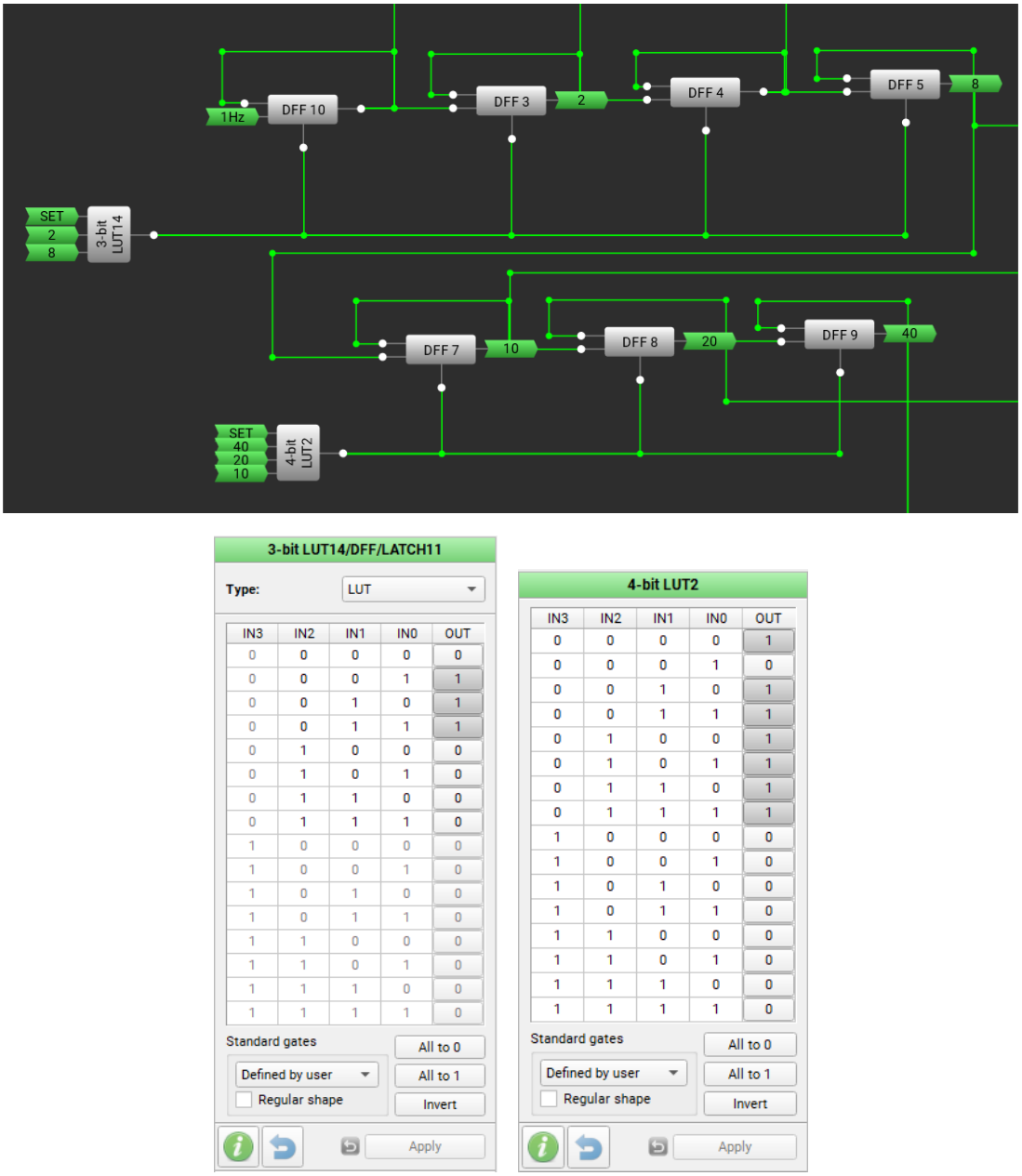

Figure 7. Divide by 60 / “seconds” counter and configuration settings for 3-bit LUT14 and 4-bit LUT2

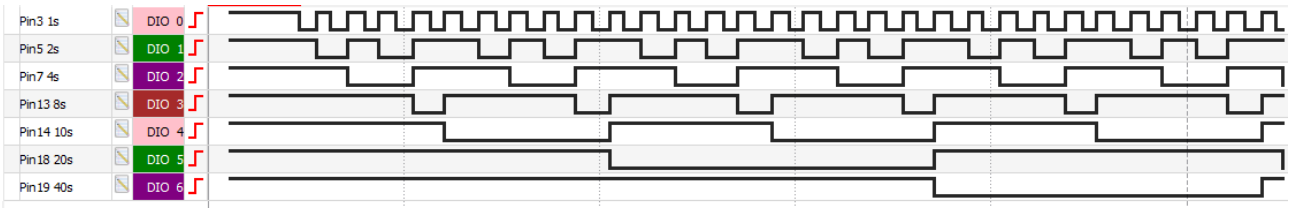

Figure 8. Divide by 60 / “seconds” Counter Operation Waveform

4.2.3. Time Setting and Clock Control

Time Setting and Clock Control involves processing the button signals, monitoring the power supply voltage, and controlling the brightness level of the clock.

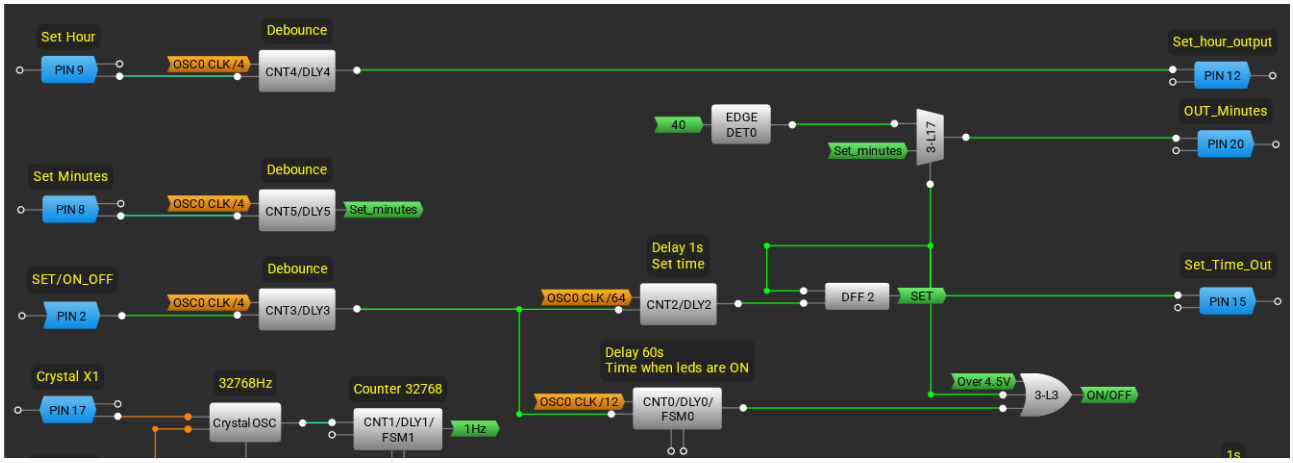

Figure 9. Button Press Handling Design Section

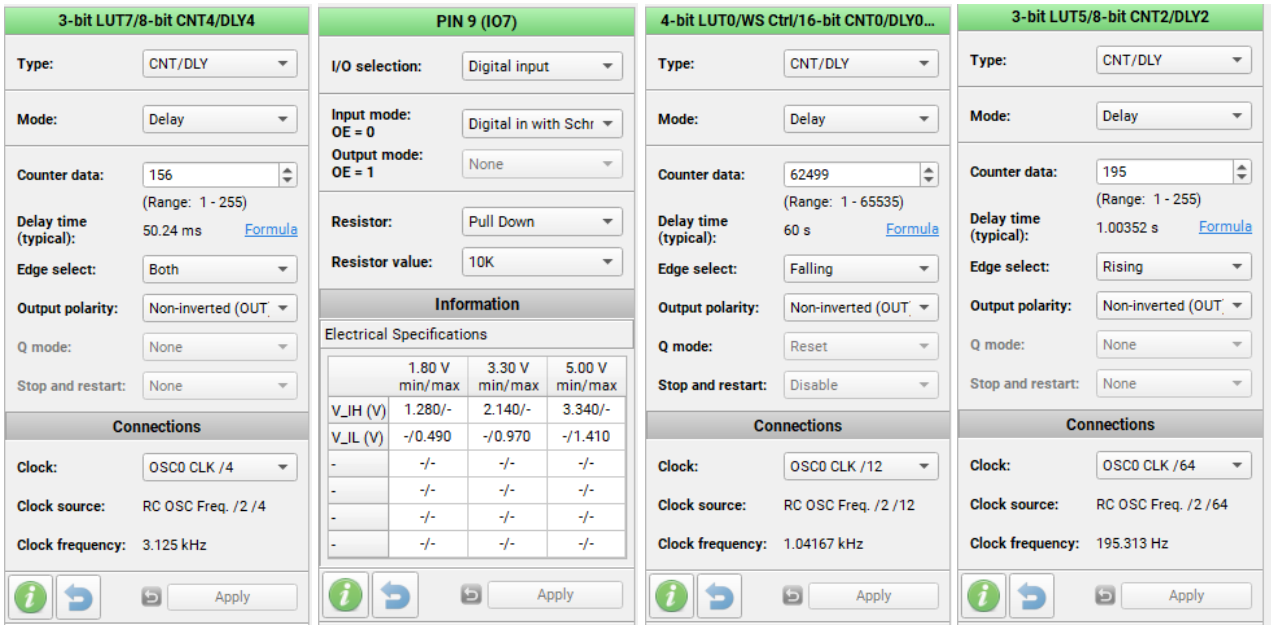

Figure 10. Configuration of Elements Responsible for Button Press Handling

To handle the button signals and prevent false triggers caused by contact bounce, CNT3/DLY3, CNT4/DLY4, and CNT5/DLY5 are used. The configuration of PINs 2, 8, and 9, which are connected to the buttons as digital inputs with Schmitt trigger, also help to reduce the negative effects of contact bounce. CNT3/DLY3, CNT4/DLY4, CNT5/DLY5, and PINs 2, 8, and 9 have identical configurations, which are illustrated in Figure 10.

Let's take a closer look at the operation of the "Set Hour" button, which is connected to PIN 9.

PIN 9 is configured as a digital input with Schmitt trigger and a pull-down resistor. CNT4/DLY4 is configured as a Delay with Both Edge Select. This configuration for PIN 9 and CNT4/DLY4 allows the filtering of chaotic switching (contact bounce) when the button is pressed and released and makes it possible for the button to be connected without additional external components. Figure 11 and Figure 12 show the oscilloscope waveforms for this part of the design. CNT4/DLY4 introduces a 50 ms delay and ignores any switching shorter than 50 ms.

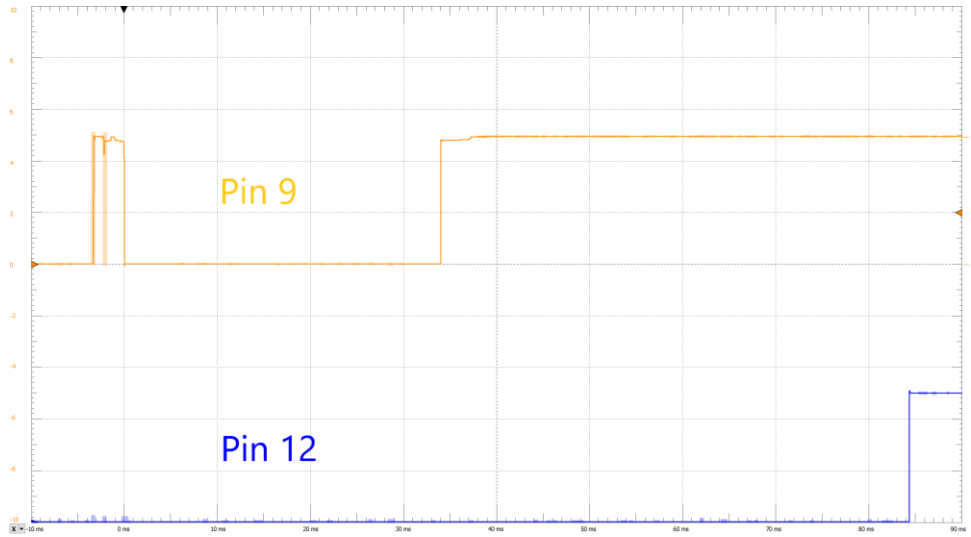

Figure 11. Example of the operation of a button contact bounce suppression circuit (rising edge).

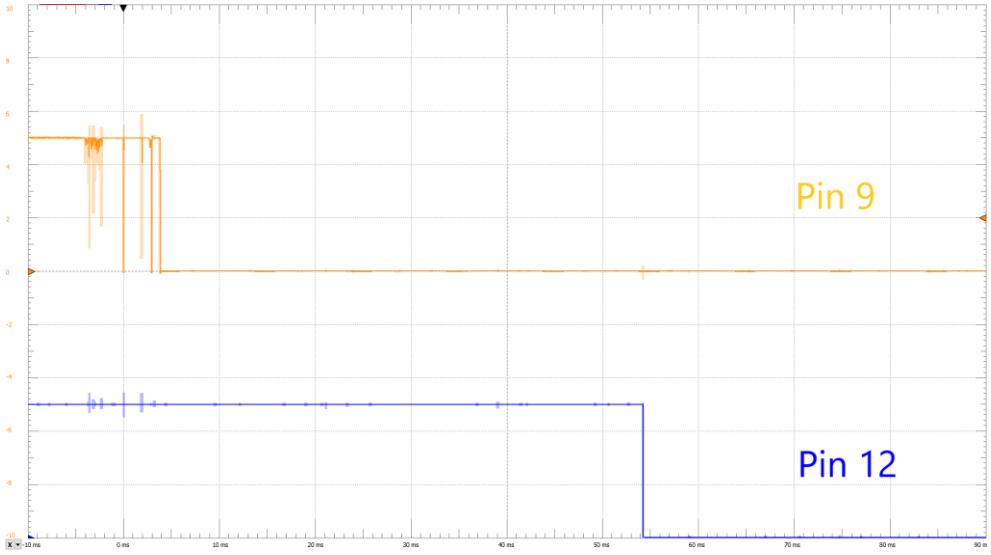

Figure 12. Example of the operation of a button contact bounce suppression circuit (falling edge).

The processed signal for setting the hours in configuration mode is output on PIN 12 of Chip B.

Contact bounce suppression works similarly for the Set Minutes button (PIN 8, CNT5/DLY5) and the SET/ON_OFF button (PIN 2, CNT3/DLY3).

CNT2/DLY2 is responsible for detecting long presses of the SET/ON_OFF button. By configuring CNT2/DLY2 as a Delay with Rising Edge Select (see Figure 10), a HIGH signal will appear at the output of CNT2/DLY2 only when the SET/ON_OFF button is held for more than 1 second. The rising edge of this signal changes the state of DFF2. DFF2 ensures that short presses of the SET/ON_OFF button will be ignored.

DFF2 generates the signal that switches the clock into configuration mode. To control Chip B, the SET signal from DFF2 is output to PIN 15. A HIGH level on DFF2 switches the clock to configuration mode, while a LOW level returns it to normal operating mode.

CNT0/DLY0 is responsible for keeping the clock display in the ON state. CNT0/DLY0 is configured as a Delay with Falling Edge Select (see Figure 9). Thus, the HIGH level input to CNT0/DLY0 from a short press of the SET/ON_OFF button keeps the display on for 60 seconds.

The *SET* signal from DFF2, the signal from CNT0/DLY0, and the *Over 4.5 V* signal are sent to 3-bit LUT3 to form the *ON/OFF* signal. This signal controls the power management circuit, the brightness of the display, and the time display activation.

3-bit LUT17 switches between the *Set_minutes* signal and the signal from the EDGE DET0 output. When a HIGH level is present at the S input of 3-bit LUT17, it transmits the *Set_minutes* signal to its output and to PIN 20. Conversely, when a LOW level is detected at the S input, it transmits the signal from the EDGE DET0 output. The *OUT_Minutes* signal at PIN 20, configured as an output, is used as the source of the minute pulses for Chip B.

EDGE DET0 with Rising Edge Detector eliminates false triggering of the Divide by 60 / “minutes” counter when transitioning from the clock's setting mode to its operational mode, in case the output of DFF9 is at a HIGH level.

ACMP2 controls the power supply voltage level (settings are shown in Figure 14) and outputs a HIGH level when Vdd is above 4.45 V. A HIGH level at the ACMP2 output keeps the clock's time display active until the supply voltage drops below 4.35 V, in other words, as long as the clock is connected to a fixed power supply.

ACMP0 also controls the power supply voltage level (settings are shown in Figure 14) and outputs a HIGH level when Vdd is above 3.05 V. ACMP0 monitors the minimum supply voltage and when the voltage level drops below 2.95 V, disables the clock's time display.

ACMP3 monitors the power supply voltage level and warns when the voltage level drops below 3.35 V. A LOW level at the ACMP3 output triggers the PWM signal generator to reduce the brightness of the clock’s time display and activates the Blink generator, which toggles the “seconds” display to turn on and off approximately every 500 ms.

The PWM generator is built on 2-bit LUT1, CNT6/DLY6, and PGEN. 2-bit LUT1 and CNT6/DLY6 form a clock pulse generator with a period of around 1 ms. These pulses clock the PGEN (settings are shown in Figure 13), which generates the pattern stored within. Changing the pattern can adjust the pulse width generated.

The Blink generator is built on Pipe Delay. Pipe Delay is configured and used as a frequency divider (divide by 32). The PWM signal with a period of about 16 ms is fed to the CLK input of the Pipe Delay, which then pulses with a period of approximately 500 ms at the nOUT1 output.

3-bit LUT15 and 3-bit LUT16 combine the control signals and generate the signal to control the “seconds” display on the clock. The signal from the 3-bit LUT16 output controls both the “minutes” and the “hours” displays for Chip B, and this signal is output via PIN 6, which is configured as an output.

ACMP1 is used for controlling the display brightness to switch the clock to night mode when low ambient lighting conditions are detected. ACMP1 has a built-in constant current generator of 100 µA, allowing the external lighting control circuit to be built using only a photoresistor.

Under bright lighting, the resistance of the photoresistor decreases, and the 100 µA current creates a voltage drop (about 100 mV) lower than the set threshold, resulting in a low level at the ACMP1 output. This does not trigger the PWM generator and does not reduce the clock's display brightness.

When the lighting detected by the photoresistor decreases, its resistance increases, causing the voltage at the ACMP1 input (PIN 10) to rise. When it exceeds the set threshold, ACMP1 outputs a HIGH level and triggers the PWM generator which reduces the clock's display brightness.

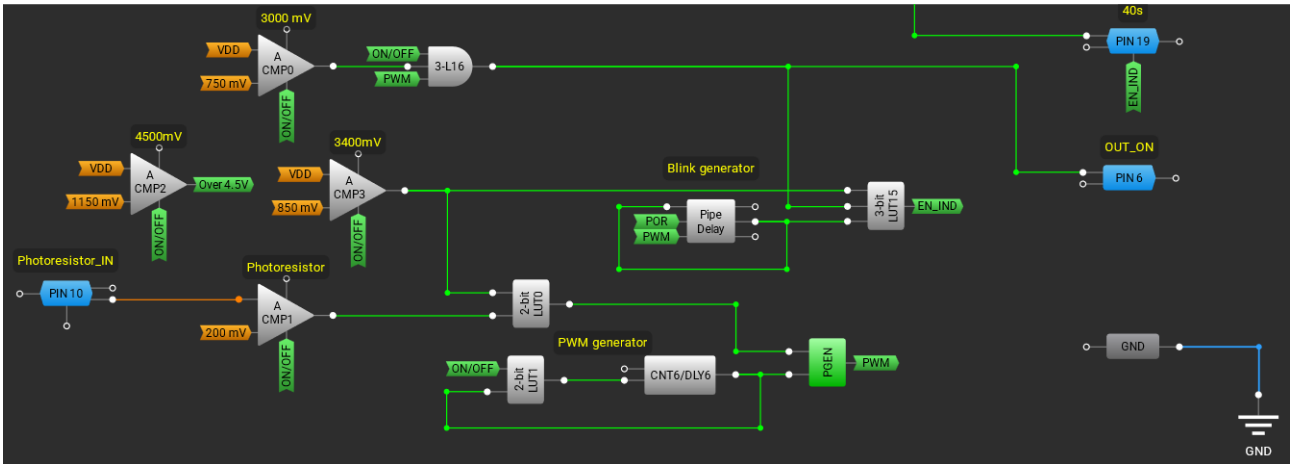

Figure 13. Showing the part of the design responsible for controlling the power supply voltage level and controlling the lighting level.

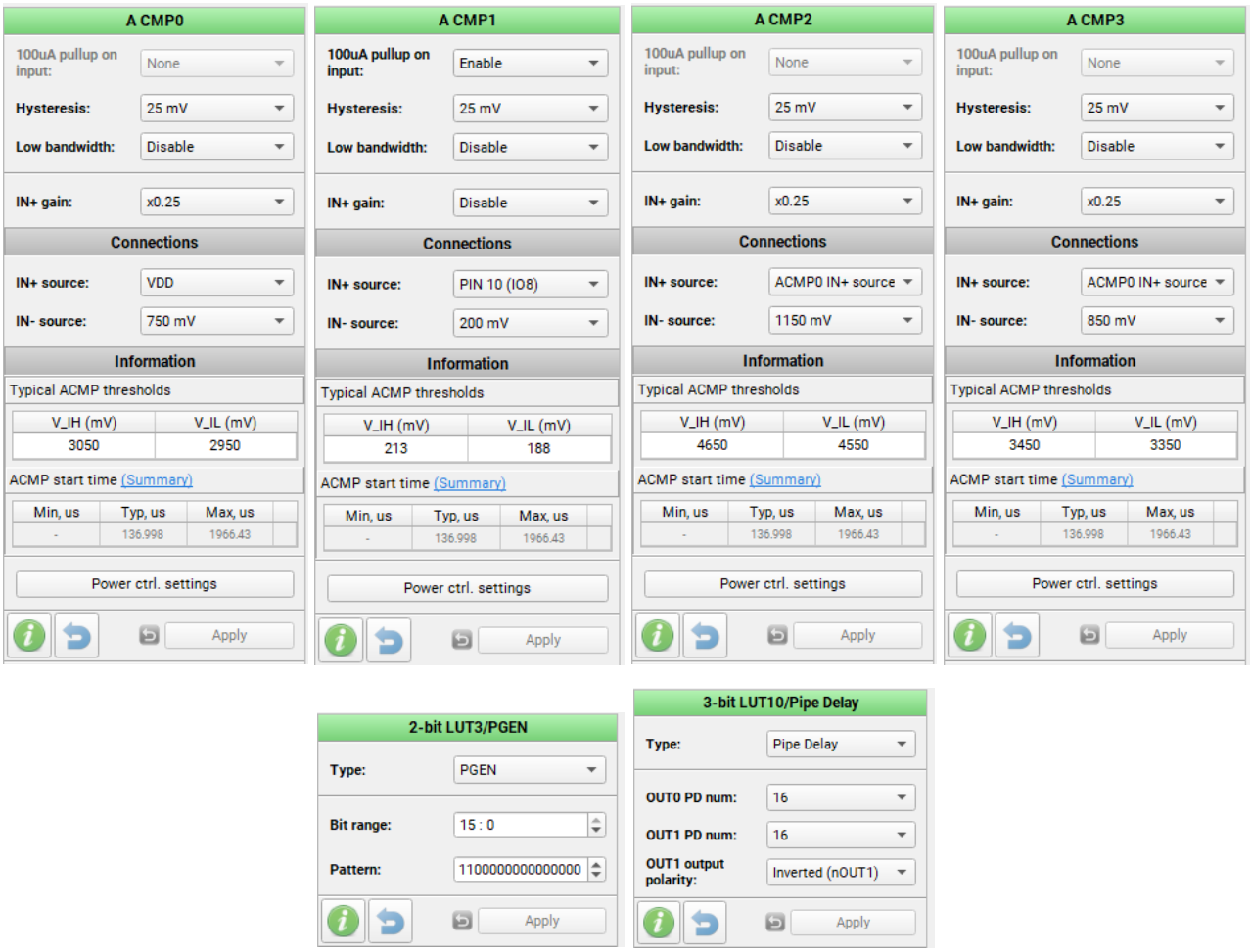

Figure 14. Configuration for elements responsible for controlling the power supply voltage level and controlling the lighting level.

Figure 15 and Figure 16 show the oscilloscope diagrams of the power supply voltage and lighting level control circuits in operation.

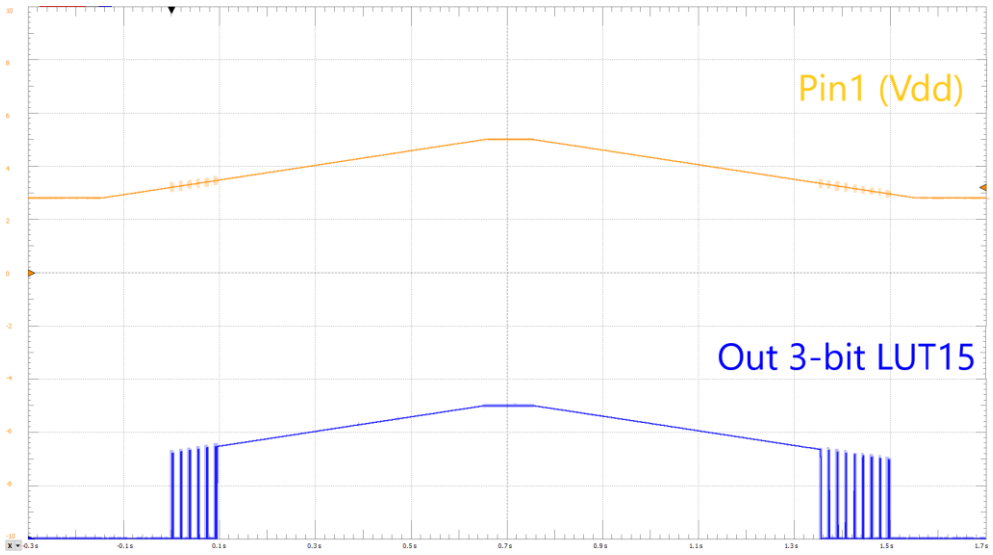

Figure 15. Operation of the power supply voltage and lighting level control circuit (lighting level above the threshold value).

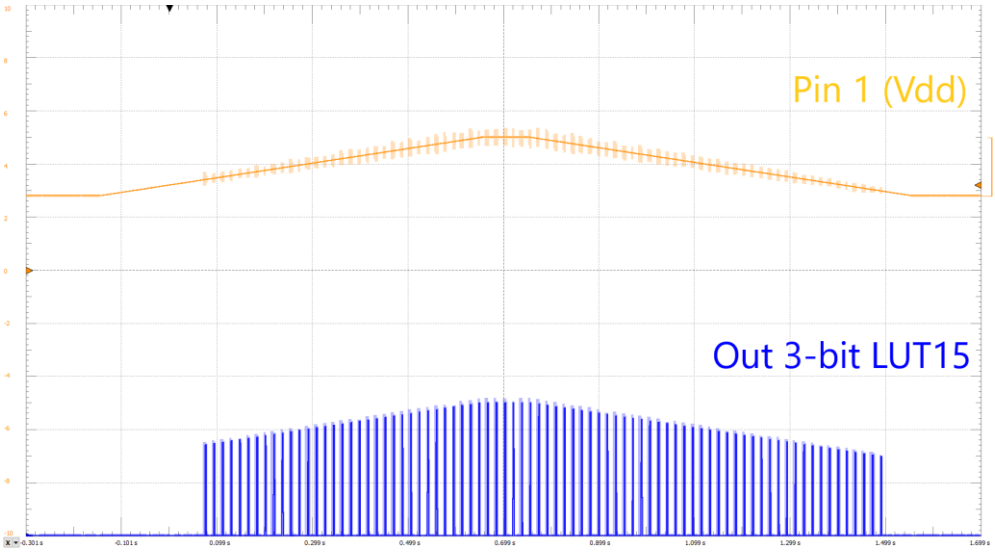

Figure 16. Operation of the power supply voltage and lighting level control circuit (lighting level below the threshold value).

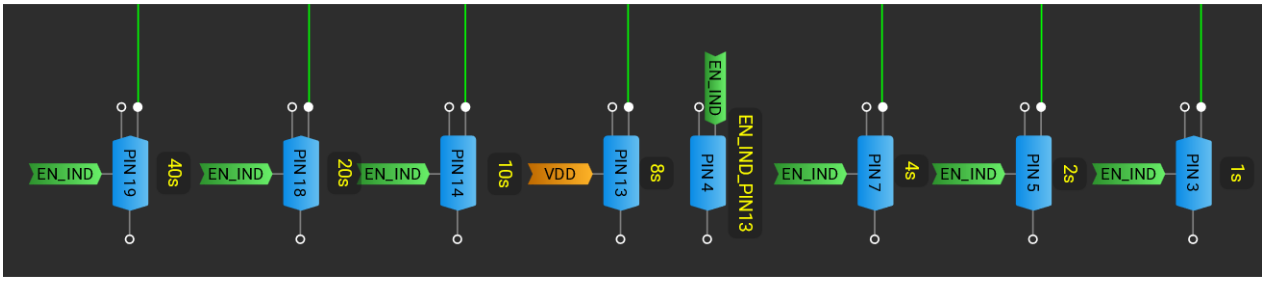

Figure 17. Output PINs for the Binary clock, Chip A indication.

A HIGH-level signal on the output of 3-bit LUT15 enables the “seconds” display using PIN 3, PIN 5, PIN 7, PIN 13, PIN 14, PIN 18, and PIN 19. Control of PIN 3, PIN 5, PIN 7, PIN 14, PIN 18, and PIN 19 is managed through the OE inputs of these pins by adjusting their settings. PIN 4 is used for controlling the display on PIN 13. Due to the characteristics of PIN 13’s internal circuit, this pin cannot be used as an OE input pin when the ACMP2 comparator is active.

4.3 Design of Chip B for the Binary-Coded Decimal Clock

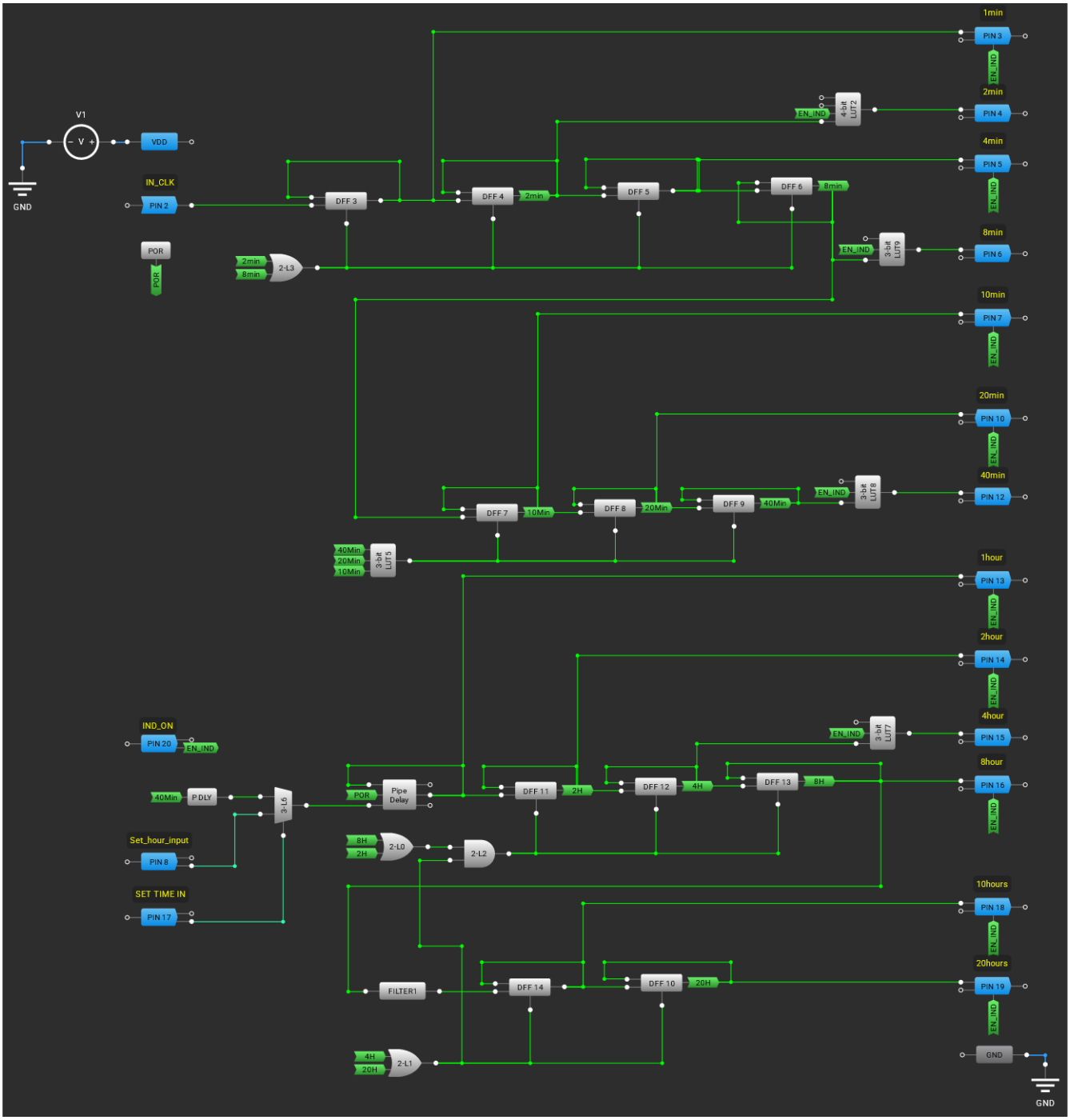

Figure 18. Design of Chip B for Binary-coded Decimal Clock

The design of Chip B performs the following basic functions:

- Counting the “minutes” pulses arriving at the PIN 2 (*IN_CLK*) input,
- Generating the “hours” pulses,
- Counting the “hours” pulses,
- Displaying the elapsed time based on the indication enable signal received at input PIN 20 (*IN_ON*),
- Setting the initial “hours” value in when in configuration mode using the signals coming to PIN 8 (*Set_hour_input*) and PIN 17 (*SET TIME IN*).

4.3.1. Divide by 60 / “minutes” counter

Counting the number of “minutes” pulses and generating the “hours” pulses is achieved by chaining together DFF3–DFF9, following a similar scheme to the Divide by 60 / “seconds” counter used in Chip A. This chain consists of a Divide by 10 counter (DFF3–DFF6, 2-bit LUT3) and a Divide by 6 counter (DFF7–DFF9, 3-bit LUT2) connected sequentially. As a result, we get a binary representation of the counted number of minutes at the outputs of DFF3–DFF9, and the hour pulses are generated at the output of DFF9. The oscilloscope waveform for this part of the design is shown in Figure 19.

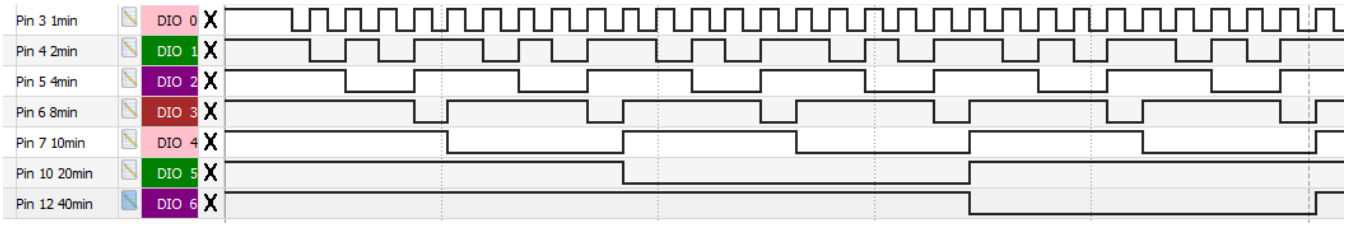

Figure 19. Divide by 60 / “minutes” counter waveform

4.3.2. Divide by 24 / “hours” counter

To count the number of hour pulses, a chain consisting of Pipe Delay and DFF10–DFF14 is used. Pipe Delay, DFF11–DFF13, 2-bit LUT0, and 2-bit LUT2 are used to perform the Divide by 10 counter function, counting the number of hours and forming the tens digit of the “hours” signal. DFF10, DFF14, 2-bit LUT1, and 2-bit LUT2 are used to perform the Divide by 2 counter function. Together, they count the hours from 0 to 23. The oscilloscope waveform for this part of the design is shown in Figure 20.

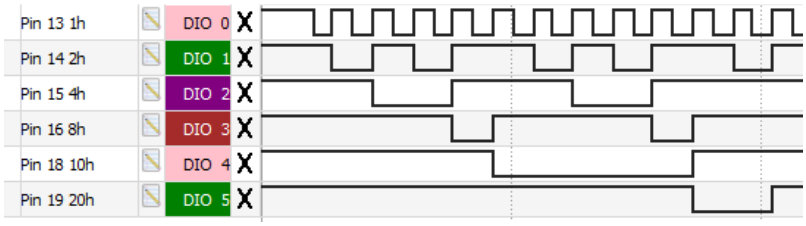

Figure 20. Divide by 24 / “hours” counter waveform

4.3.3. Time setting and clock control

The 3-bit LUT6 multiplexer switches the signal from the Set Hours button (PIN 8) and the internal signal from the output of DFF9 (hour pulses) depending on the control signal *SET TIME IN* (PIN 17). When the *SET TIME IN* signal is HIGH (PIN 17), the signal from PIN 8 is passed to the multiplexer output. When *SET TIME IN* is LOW, the internal signal from the output of DFF9 is passed through. P DLY with the Rising Edge Detector is configured to avoid false triggering of the hours counter when transitioning from time-setting mode to operational mode, particularly when the output of DFF9 is HIGH.

A HIGH level signal on *IND_ON* enables the display of minutes and hours using PINs 3–7, PIN 10, PINs 12–16, and PINs 18–19. The control of PINs 3, 5, 7, 10, 13, 14, 16, 18, and 19 is managed through their OE (Output Enable) inputs by adjusting their settings. For controlling the indication on PINs 4, 6, 12, and 15 (which do not have OE inputs) 3-bit LUT7, 3-bit LUT8, 3-bit LUT10, and 4-bit LUT2 are used, respectively.

5. Binary-coded Sexagesimal Clock Design

5.1 Circuit Design

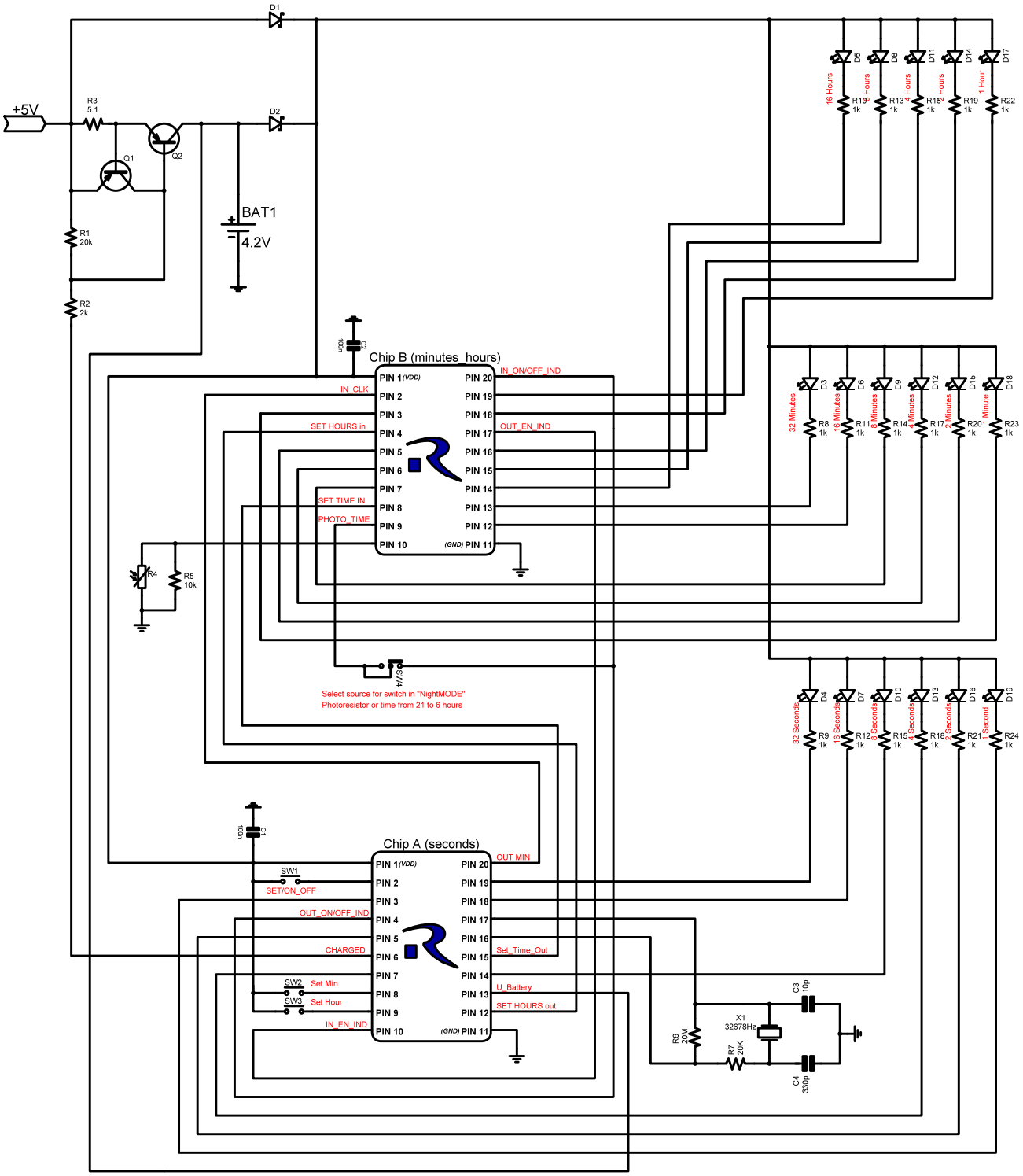

Figure 21. Electrical schematic of the Binary-coded Sexagesimal Clock

This version of the Binary Clock (Binary-coded sexagesimal Clock) is also built based on two SLG46533V chips. The clock functions in this design are very similar to the Binary-coded decimal clock.

In this version, six bits each are sufficient to display both the “seconds” (6 LEDs, 26 = 64) and “minutes” (6 LEDs, 26 = 64) while five bits are needed to display the “hours” (5 LEDs, 25 = 32). Therefore, a total of 17 LEDs are required to display time in the Binary-coded sexagesimal format.

Control and settings are done similarly (to the binary coded decimal clock) with three buttons: SET/ON_OFF, Set Minutes, Set Hours.

The clock can operate from a 5 V fixed power source or from a battery with a voltage ranging from 3.0 V - 4.2 V. When using a 5 V fixed power source, the time display continuously remains on, whereas when using a battery as the power source, the display turns on for only 1 minute with a short press of the SET/ON_OFF button to save power.

The clock also features a "Night Mode", in which the brightness of the time display is reduced. This mode is automatically activated in low ambient light conditions or activated according to a pre-determined schedule (from 21:00 to 6:00). If the battery voltage drops below 3.4 V, the clock enters night mode to reduce power consumption, and the “seconds” indicator begins to blink—indicating that the battery should be recharged soon.

When the battery voltage falls below 3.0 V, the display is completely turned off while internal timekeeping continues uninterrupted.

The clock circuit also monitors the maximum charging voltage and disables charging when the battery voltage reaches 4.2 V.

To set the correct time, the SET/ON_OFF button must be held down for approximately 1 second. Entering the time-setting mode disables the internal one-second pulse generator and resets the “seconds” counter to zero.

The correct time is then set using the Set Minutes and Set Hours buttons. Time adjustments can only be made in the increasing direction. While in time-setting mode, the time display remains on regardless of the power source being used (battery or fixed). After setting the time, holding the SET/ON_OFF button for about 1 second switches the clock back to its normal operation mode.

Let's look at the designs implemented in this version of the clock:

Chip A

- Crystal Oscillator
- Divide-by-32768/second pulse generator
- Divide-by-60 circuit / “seconds” counter
- Time setting and clock control

Chip B:

- Divide-by-60 circuit / “minutes” counter
- Divide-by-24 circuit / “hours” counter
- Clock Control for Night Mode

5.2 GreenPAK Design for Chip A for the Binary-coded Sexagesimal Clock

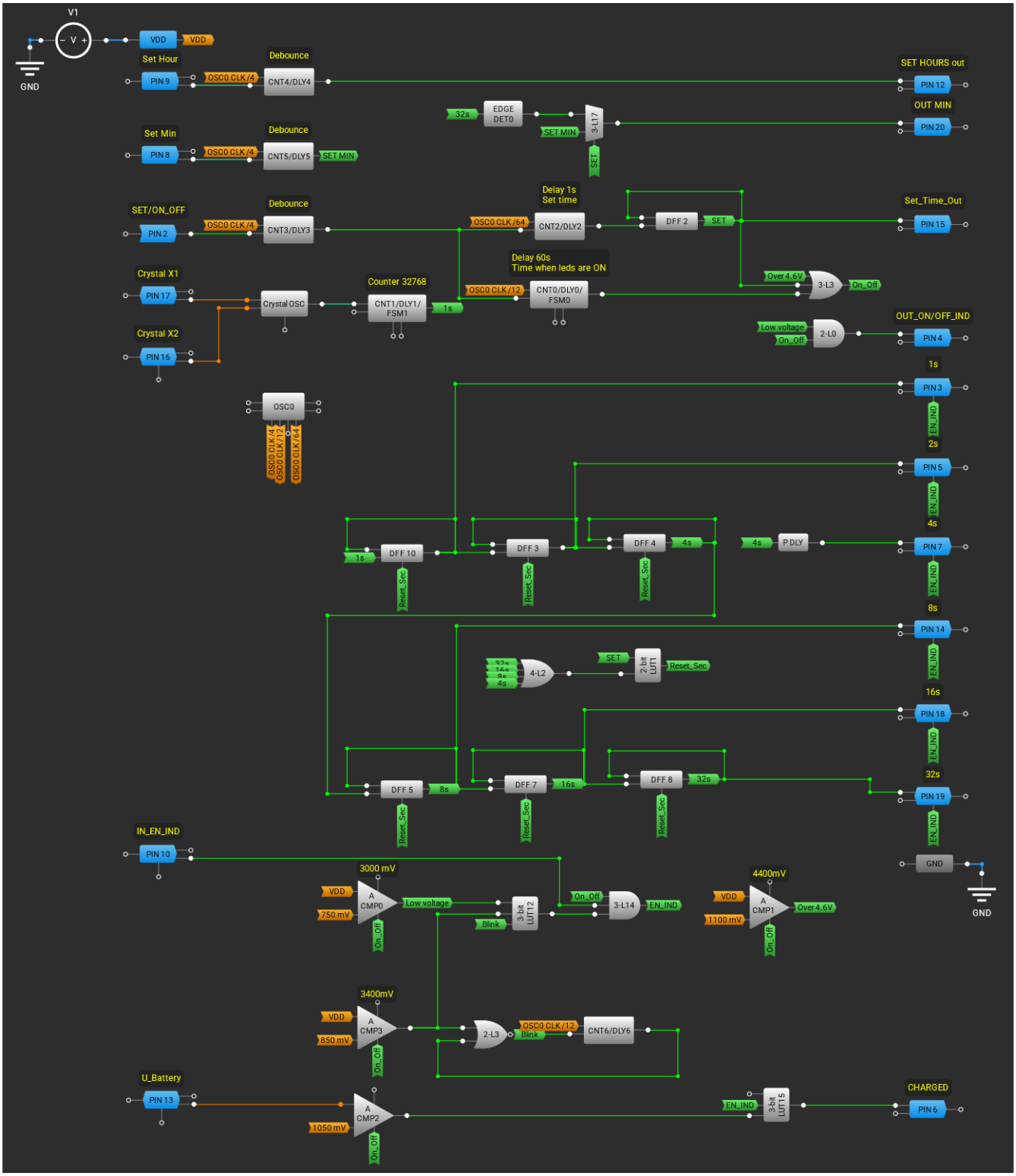

Figure 22. GreenPAK Design for Chip A of Binary-coded Sexagesimal Clock

5.2.1. Crystal Oscillator

Just like the binary-coded decimal clock design, a stable generator that provides “seconds” pulses is built using the Crystal Oscillator module. For this clock, we will use a standard quartz resonator with a frequency of 32768 Hz.

To obtain stable “seconds” intervals, the 32768 Hz frequency generated by the Crystal Oscillator needs to be divided by 32,768. The 16-bit CNT1/DLY1/FSM1 module, configured as a counter, is used as the divider.

5.2.2. Divide by 60 / “Seconds” Counter

The next part of the design responsible for displaying seconds and converting second pulses into minute pulses is the Divide by 60 / Seconds Counter.

The Divide by 60 / Seconds Counter is constructed by chaining DFF10, DFF3, DFF4, DFF5, DFF7, DFF8, 4-bit LUT2, and 2-bit LUT1. Each DFF in this chain is in divide by 2 configuration. Thus, the entire chain divides the frequency by 64.

To limit the division to 60, 4-bit LUT2 and 2-bit LUT1 are used. These logic blocks reset DFF10, DFF3, DFF4, DFF5, DFF7, and DFF8 to their initial state when a HIGH signal appears at the outputs of DFF4, DFF5, DFF7, and DFF8.

This results in a frequency division of 1 Hz by 60, producing pulses with a 1-minute period. Additionally, at the outputs of DFF10, DFF3, DFF4, DFF5, DFF7, and DFF8, we get signals to display the seconds on the clock. The active level for the display is LOW.

The oscilloscope diagram for the operation of the Divide by 60 / Seconds Counter is shown in Figure 23.

2-bit LUT1 has a SET input, where a HIGH level will reset the entire Divide by 60 / Seconds Counter when entering into clock setting mode.

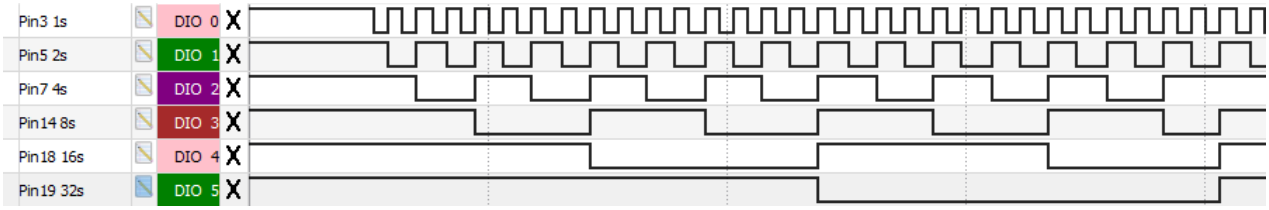

Figure 23. Divide by 60 / “Seconds” Counter Operation Waveform

5.2.3. Time Setting and Clock Control

The Time Setting and Clock Control processes involve handling button signals and monitoring the supply voltage level.

For button signal processing and protection against false triggers (due to contact bounce), CNT3/DLY3, CNT4/DLY4, CNT5/DLY5 are used. The configuration of PINs 2, 8, and 9, to which the buttons are connected as digital inputs with Schmitt trigger, also assist in reducing the negative effects of contact bounce.

This part of the design is the same as the design in the Binary-coded decimal clock version.

- ACMP1 monitors the supply voltage level. If Vdd exceeds 4.45 V, it outputs a HIGH level, which keeps the clock's time display on until the supply voltage drops below 4.35 V. This ensures the clock stays powered as long as it stays connected to a fixed power source.
- ACMP0 monitors the supply voltage level and when Vdd is greater than 3.05 V, outputs a HIGH level. ACMP0 ensures that the clock display is turned on only when the voltage level remains above 2.95 V. If the voltage falls below this threshold, the time display will turn off.
- ACMP3 monitors the supply voltage level and triggers a warning when the voltage level drops below 3.35 V. A LOW level at the ACMP3 output activates the Blink generator, which turns the “seconds” display on and off approximately every 500 ms.
- ACMP2 and 3-bit LUT15 form a circuit that monitors the battery voltage and ends charging operation once the voltage level reaches 4.2 V.

This circuit ensures efficient voltage management and provides warnings when the supply or battery voltage reaches critical levels.

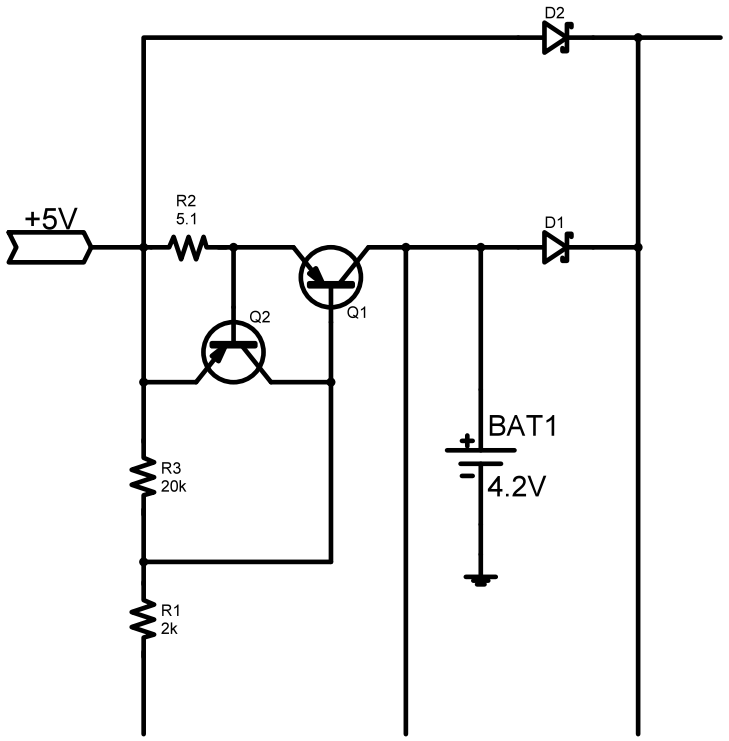

Figure 24. Part of the circuit responsible for battery charging control

A current stabilizer for charging the battery is created on transistors Q1 and Q2. The current stabilizer is turned on or off by a LOW level or HIGH level detected on PIN 6 (CHARGED), respectively. Diodes D1 and D2 are used to switch the power sources for the circuit.

5.3 GreenPAK Design for Chip B for the Binary-coded Sexagesimal Clock

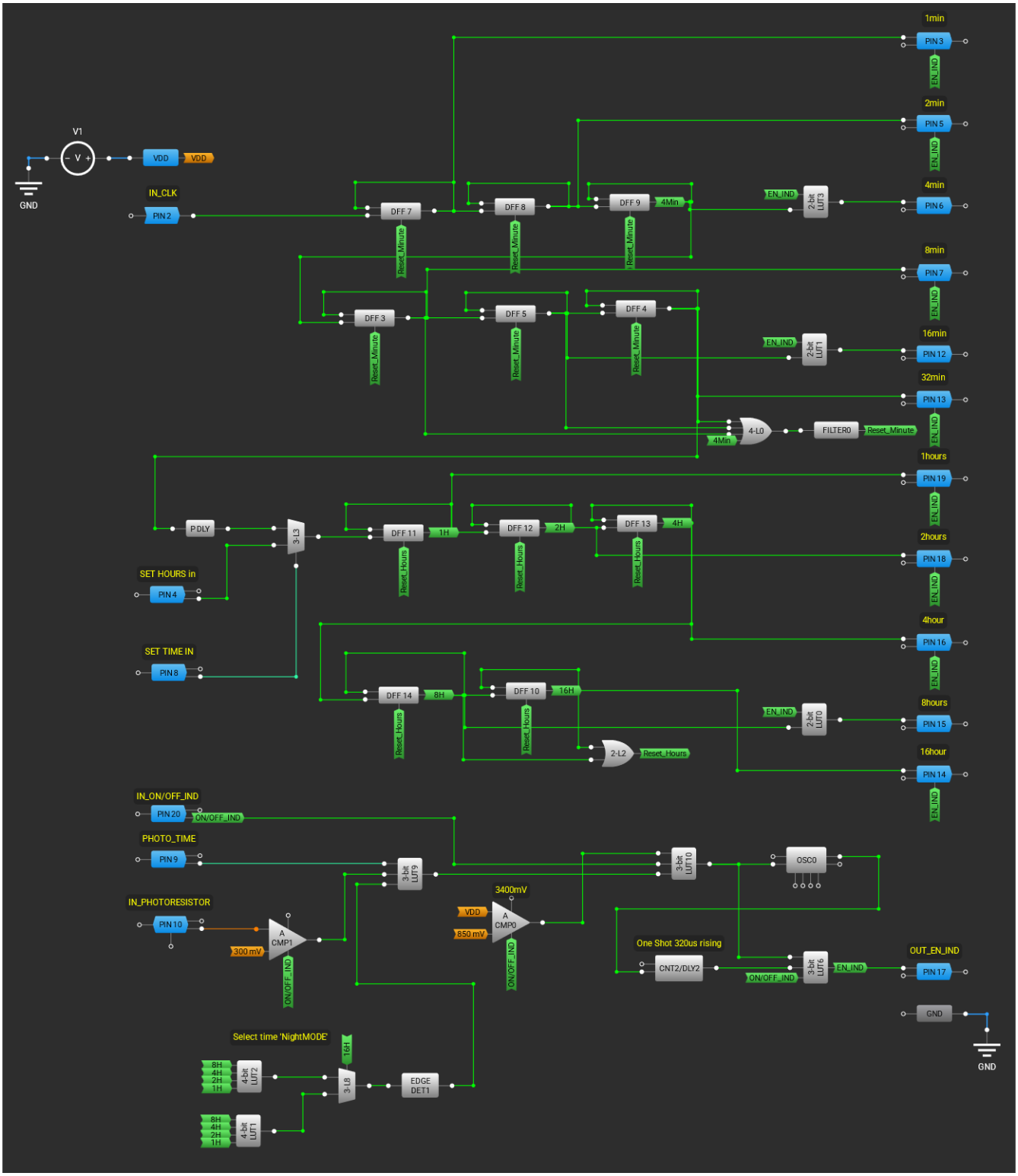

Figure 25. GreenPAK Design for Chip B of the Binary-coded Sexagesimal Clock

This design performs the following basic functions:

- Counting the “minutes” pulses arriving at input PIN 2 (IN_CLK).
- Generating “hours” pulses.
- Counting “hours” pulses.
- Displaying the elapsed time depending on the indication enable signal, which comes through input PIN 20 (IN_ON/OFF_IND).
- Setting the initial ”hours” value during setup mode through signals received at PIN 4 (SET HOURS IN) and PIN 8 (SET TIME IN).
- Controlling the light level and generating control signals for “Night Mode” operation.

5.3.1. Divide by 60 / Minutes Counter

Counting “minutes” pulses and generating “hours” pulses is done by chaining DFF7, DFF8, DFF9, DFF3, DFF5, DFF4, 4-bit LUT0, and FILTER0, following a similar scheme to the Divide by 60 / “Seconds” Counter used in Chip A. This results in the binary code of counted minutes at the outputs of DFF4-DFF9 and “hours” pulses at the output of DFF4. The oscilloscope waveform for this part of the design is shown in Figure 26.

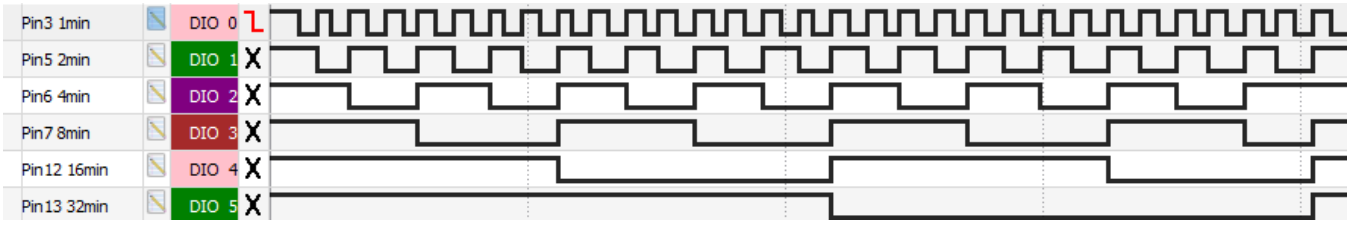

Figure 26. Divide by 60 / minutes counter waveform

5.3.2. Divide by 24 / Hours Counter

Counting “hours” pulses is done by chaining DFF10, DFF11, DFF12, DFF13, DFF14, and 2-bit LUT2. 2-bit LUT2 limits the overall division ratio of this chain to 24 (out of a possible 32). DFF10 to DFF14 are used to count the hours from 0 to 23. The oscilloscope waveform for this part of the design is shown in Figure 27.

Figure 27. Divide by 24 / hours counter waveform

5.3.3. Time Setting and Clock Control

Depending on the control signal *SET TIME IN* (PIN 8), a 3-bit LUT3 multiplexer switches between the signal from the SET HOURS IN button (PIN 4) and the internal signal from the DFF4 output (“hours” pulses). When the *SET TIME IN* signal (PIN 8) is at a HIGH level, the multiplexer outputs the signal from PIN 4. When the *SET TIME IN* signal is at a LOW level, it outputs the internal signal from DFF4.

The P DLY configured with rising edge detection ensures that there is no false triggering of the “hours” counter when switching between time setting mode to operating mode, especially when the DFF4 output is at a HIGH level. The HIGH level signal *IN_ON/OFF_IND* is used to generate the enable signal for the display of minutes and hours.

5.3.4. Controlling the lighting level and generating control signals for "Night Mode"

The circuit on ACMP1 is responsible for controlling the external lighting to trigger the clock's transition to Night Mode. ACMP1 includes an integrated 100 µA constant current generator, which enables the construction of an external lighting control circuit using only a light-dependent resistor (LDR).

Night Mode can also be enabled on a schedule which is done using 4-bit LUT1, 4-bit LUT2, and 3-bit LUT8. These components allow for tracking and setting the operational time for Night Mode.

A 3-bit LUT9 multiplexer is controlled by the *PHOTO_TIME* signal from PIN 9, which is responsible for selecting the source for the Night Mode activation.

3-bit LUT10, 3-bit LUT6, OSC0, and CNT2/DLY2 act as a controlled PWM signal generator to reduce the brightness of the clock display in Night Mode.

ACMP0 monitors the power supply voltage and raises an alert when the voltage drops below 3.35 V. A LOW level on the output of ACMP0 activates the PWM signal generator to dim the clock's time display for energy conservation.

The control of pins PIN 3, PIN 5, PIN 7, PIN 13, PIN 14, PIN 16, PIN 18 and PIN 19 is managed through the OE inputs of each of these pins, which adjust the pin settings. For controlling the display on pins PIN 4, PIN 6, PIN 12, and PIN 15, which do not have OE inputs, 3-bit LUT0, 3-bit LUT1, and 3-bit LUT3 are used respectively

6. PCB Design

For testing purposes, a PCB was designed, see Figure 28 and Figure 29.

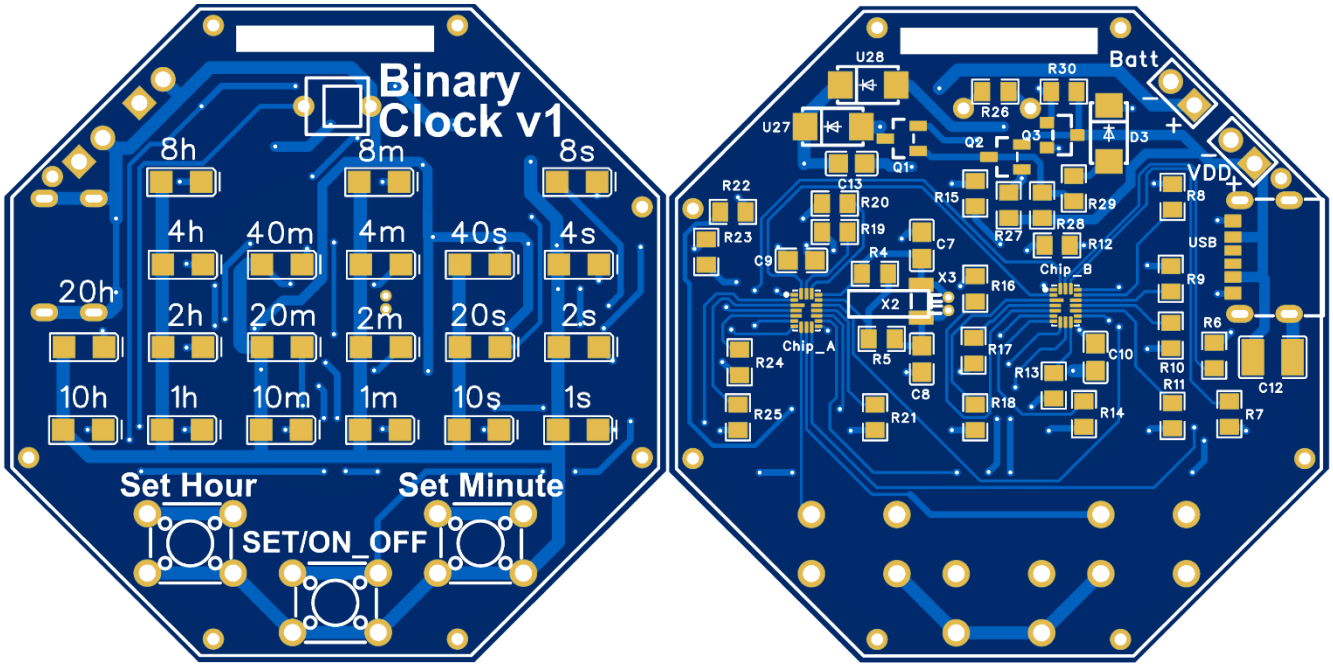

Figure 28. Top and bottom side of PCB for Binary Clock (Binary-coded decimal version)

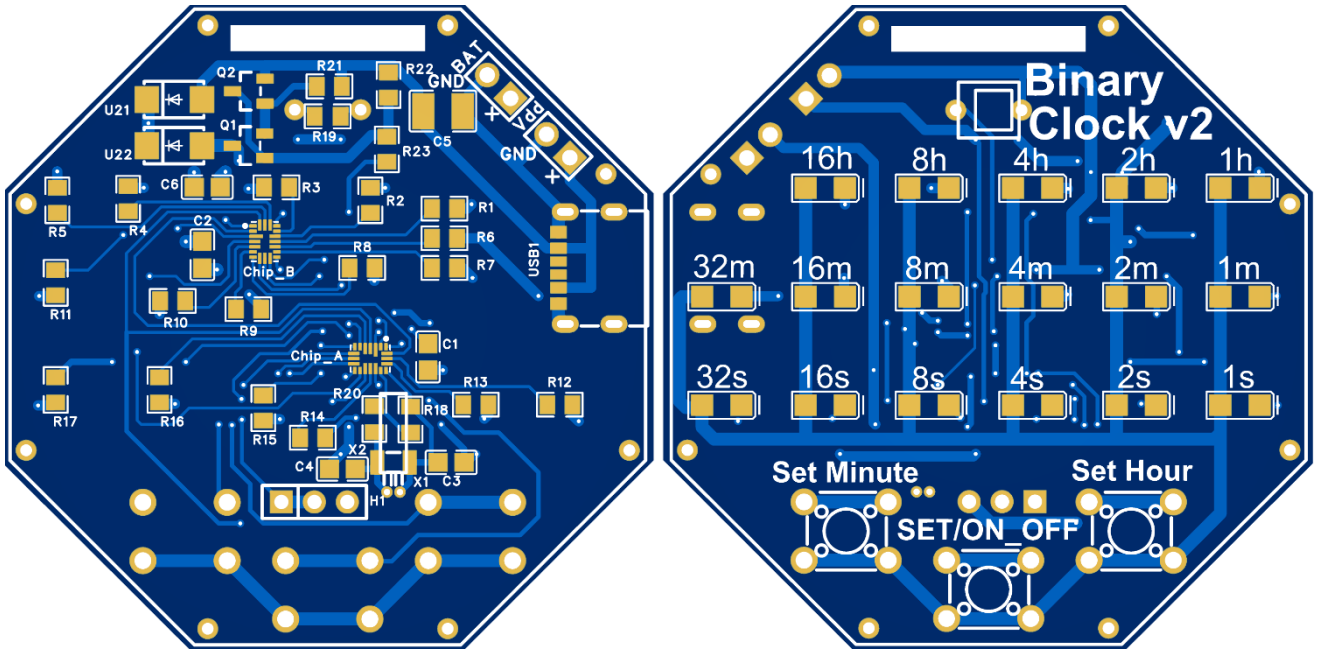

Figure 29. Top and bottom side of PCB for Binary Clock (Binary-coded sexagesimal version)

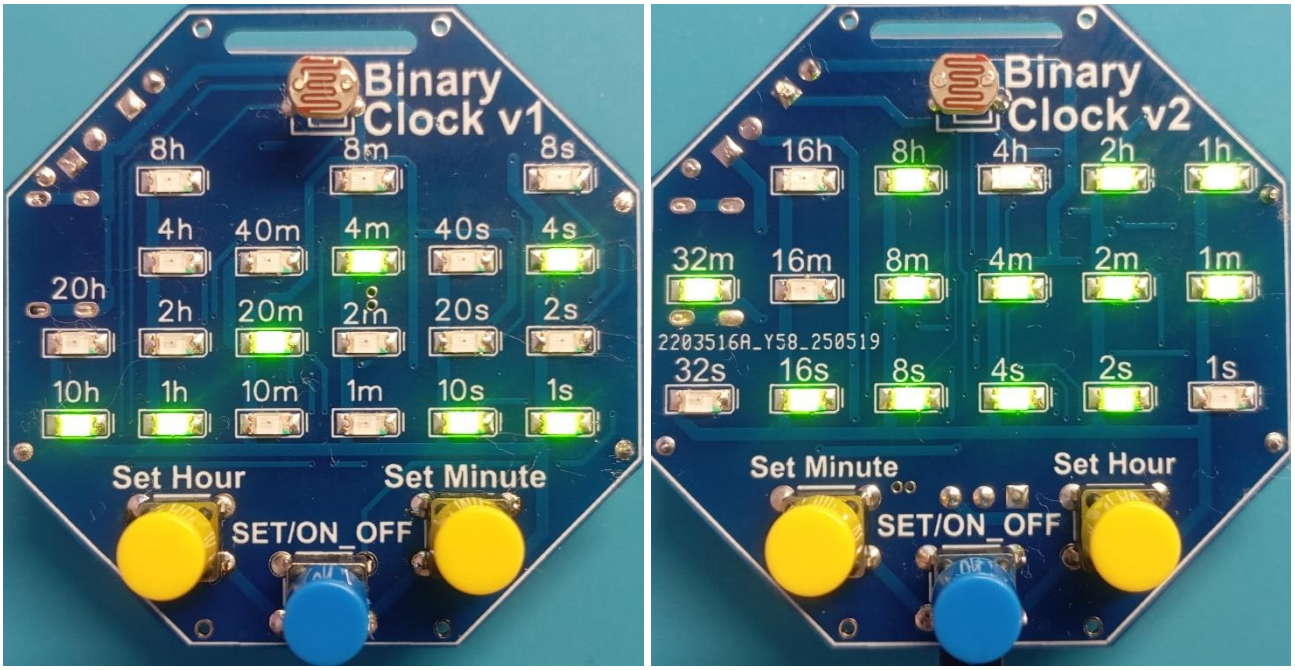

Figure 30. Assembled Binary Clocks
(Binary-coded decimal version shown on the left, Binary-coded sexagesimal version shown on the right)

The binary-coded decimal version of the clock shown in Figure 30 (left) displays the time: 11 hours 24 minutes 15 seconds. The binary-coded sexagesimal version of the clock in Figure 30 (right) displays the time: 11 hours 47 minutes 30 seconds.

7. Conclusion

Using only two SLG46533 chips, two versions of fully functional binary clocks were created.

These designs demonstrate the capabilities of both the digital and analog parts of the SLG46533 chips. The digital portion of the device contain everything needed to create an electronic clock as well as display the time using LED indicators. The analog portion makes it possible to control the clock's power supply and adjust the brightness of the LED indicators.

8. Revision History

Revision	Date	Description
1.00	Sep 8, 2025	Initial release.

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