HART Modem
SLG47011

This application note describes how the Renesas SLG47011 can be used in the implementation of a HART modem. This application note comes complete with design files which can be found in the References section.

Contents

References

For related documents and software, please visit:

AnalogPAK | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics
[2] AN-CM-407 HART Modem.aap, GreenPAK Design File, Renesas Electronics
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics
[5] SLG47011V HART Modem Demo Board, User manual, Renesas Electronics

Terms and Definitions

FSK	Frequency-Shift Keying
HART	Highway Addressable Remote Transducer
OCD	Output Carrier Detect
OSI	Open Systems Interconnection
RTS	Request-to-send
UART	Universal Asynchronous Receiver-Transmitter

Originally published here: https://www.embedded.com/hart-modem-design-implementation

1. Introduction

The basis of industrial automation relies on proper and reliable communication between machinery, control, and measuring instruments. It is often necessary to transmit signals over relatively long distances, which can result in significant voltage drops on the wires. The presence of environmental interference can also affect the signal negatively. To address these issues, the 4-20 mA current loop standard is typically used for transmitting information.

In current loop systems, a transmitter is connected to a transducer monitoring a process variable such as temperature, pressure, or flow. The transmitter is wired in series with a DC power supply and is responsible for converting the transducer output into a current that ranges from 4 mA to 20 mA. 4-20 mA instrumentation and controls typically support alarm signaling for conditions slightly below 4 mA and above 20 mA. For transmitters, current values below 4 mA and above 20 mA are used to signal a fault. The NE43 recommendation was created to standardize how transmitters indicate failures and how control systems should interpret these signals, thus facilitating improved analog integration. NE43 defines 3.8 mA to 20.5 mA as valid measurement values, with 3.8 mA to 4 mA and 20 mA to 20.5 mA indicating saturation.

Thanks to the use of the 4-20 mA current loop standard, even if the voltage drops significantly due to long wires or if the loop voltage fluctuates because a large motor started up elsewhere in the factory, it doesn't matter – the transmitter will maintain a constant current for a given process variable (see Figure 1). Another feature of this standard is that the device can also be powered from the current loop. In this case, the current consumption of the entire device must have a maximum of 3.5 mA.

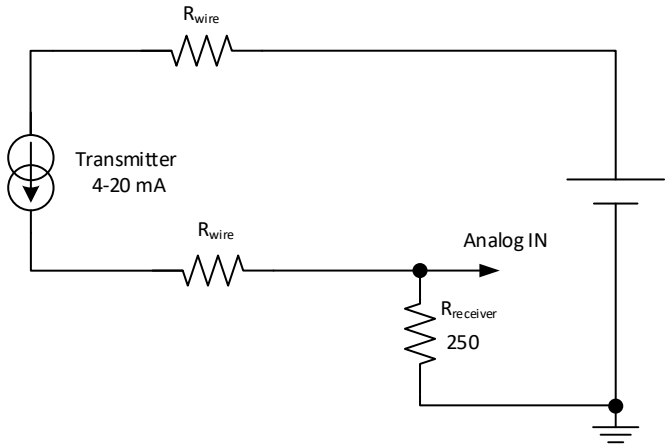

Figure 1. 4-20 mA Current Loop

Among several communication protocols in plant automation, the HART (Highway Addressable Remote Transducer) protocol stands out as the best overall solution for obtaining value-added device and diagnostic information in digital form while retaining compatibility with legacy 4-20 mA automation architectures. The standard HART transmission is frequency shift keyed (FSK). The FSK standard protocol frequencies are 1200 Hz (for binary 1) and 2200 Hz (for binary 0), and the communication speed is 1200 bits per second. An alternative to the standard FSK signal is a coherent 8-way phase-shift keyed (C8PSK) signal. In this project, the standard FSK protocol is used.

The other protocol versions add support for pure sinusoidal or trapezoidal signaling. The former signal type is more common, and the latter one is mostly used when very high data speed is required. In this project, the modem only works with a sinusoidal signal. The resulting transmitted HART signal must be DC balanced and must not interfere with analog signaling at all.

The HART protocol follows the seven-layer Open Systems Interconnection (OSI) protocol model. The OSI model describes seven layers that computer systems use to communicate over a network. A HART modem operates at the physical level (Level 1).

Designed for industrial process measurement and control applications, HART is considered a hybrid protocol due to its combination of analog and digital communication. It can convey a single variable using a 4-20 mA

analog signal while also transmitting additional information on a digital signal. Figure 2 shows the basic schematic of a HART System.

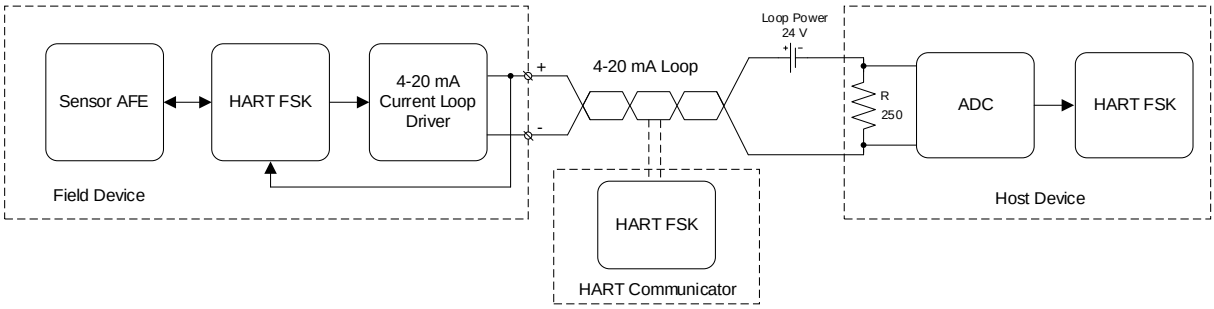

Figure 2. Typical HART System Example

The digital information signal is carried by low-level modulation superimposed on the standard 4-20 mA current loop. More importantly, the digital signal does not impact the analog reading as it is separated from the analog signal using standard filtering techniques.

The Renesas SLG47011 is a perfect fit for use as a HART modem. Figure 3 shows the general schematic of the modem based on the SLG47011. With minor circuit modifications, it can function as both a host (control or monitoring system) and as a field device (sensor). It should also be noted that in addition to providing basic functionality for the HART modem, the SLG47011 (like other GreenPAK ICs) features many other logic blocks which can be used to implement additional customer-defined circuits (such as watchdog, etc.).

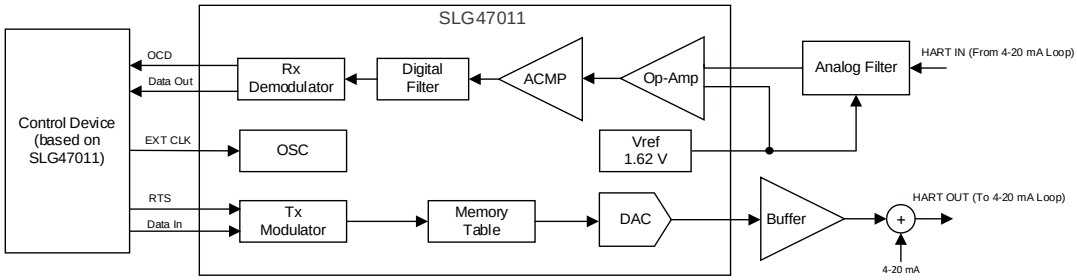

Figure 3. General Schematic of a HART Modem Based on SLG47011

The modem receives signals with a duration of 833 µs via a 4-20 mA line, and after filtering, converts them into bits using the UART protocol. The modem similarly sends signals, and the UART code converts it to a sine wave and sends it to the 4-20 mA line. Figure 4 shows an example of the HART protocol signal.

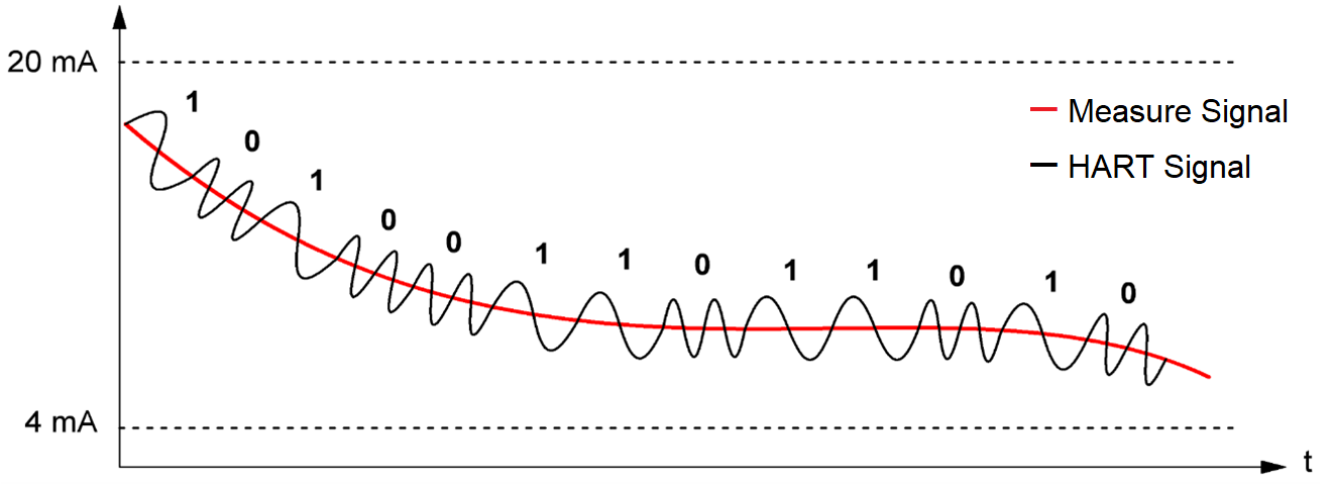

Figure 4. Example of HART Protocol Signal

2. External Analog Component Details of the HART Modem

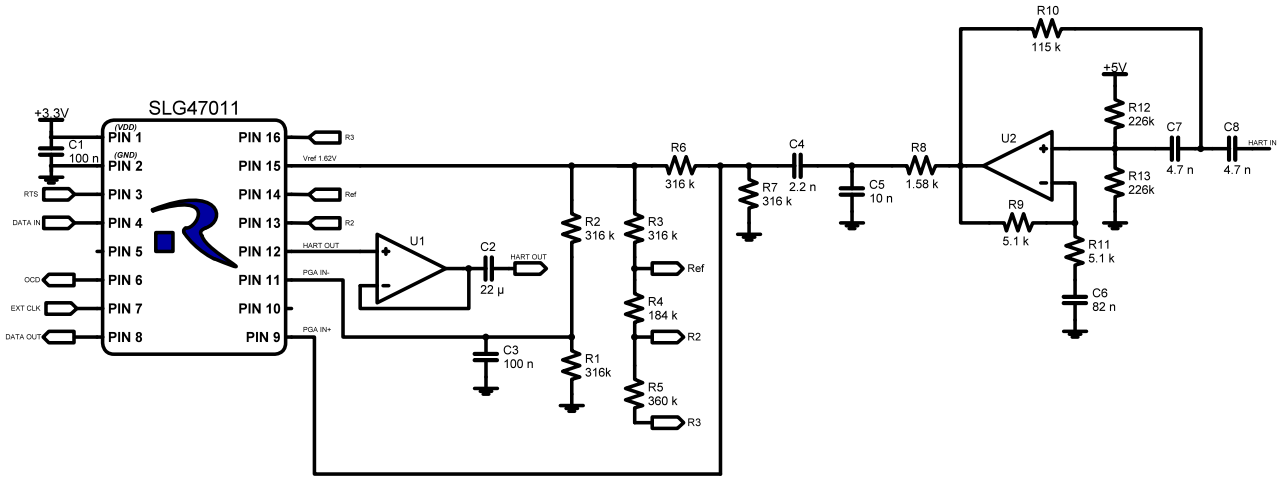

Figure 5. Schematic of External Analog Part of HART Modem

For correct operation and compliance with the standard official HART specification, the circuit includes an active filter that attenuates signals outside of the 1200 - 2200 Hz range. This prevents noise in the current loop from affecting the correct demodulation of packets. The op-amp U2 is configured as an active band-pass filter using the Sallen-Key topology, ensuring that only the relevant modulated signal is sent to the HART modem for further processing.

The circuit also features hysteresis to adjust the receive/reject threshold, which is controlled by resistors R3, R4, and R5. The values of the hysteresis are calculated to meet HART specification requirements. Buffer U1 is connected to the SLG47011 DAC output, which prevents it from being affected by the load. R1, R2, and C3 form the offset for the op-amp U2. R6, R7, and C4 are used to function as a high-pass filter, while R8 and C5 form a low-pass filter.

In this project, a 4 MHz external clock is used to meet the specification requirements. However, due to the flexibility of the SLG47011, a different clock frequency can be used with minor design changes. Additionally, this example is designed to operate the modem with a sine wave output with an amplitude of 500 mV peak-to-peak. Since this value is not standardized in the specification, it is possible to easily adjust the amplitude to suit the needs of any particular project.

Any low-cost amplifier with a bandwidth of at least 10 kHz and an output current of more than 1 mA can be used as an external op-amp. The value of the input offset voltage is not critical.

3. GreenPAK Design

The HART modem based on the SLG47011 combines both current loop signal modulation and demodulation. Figure 6 shows an internal design of the modem in the Go Configure Software Hub.

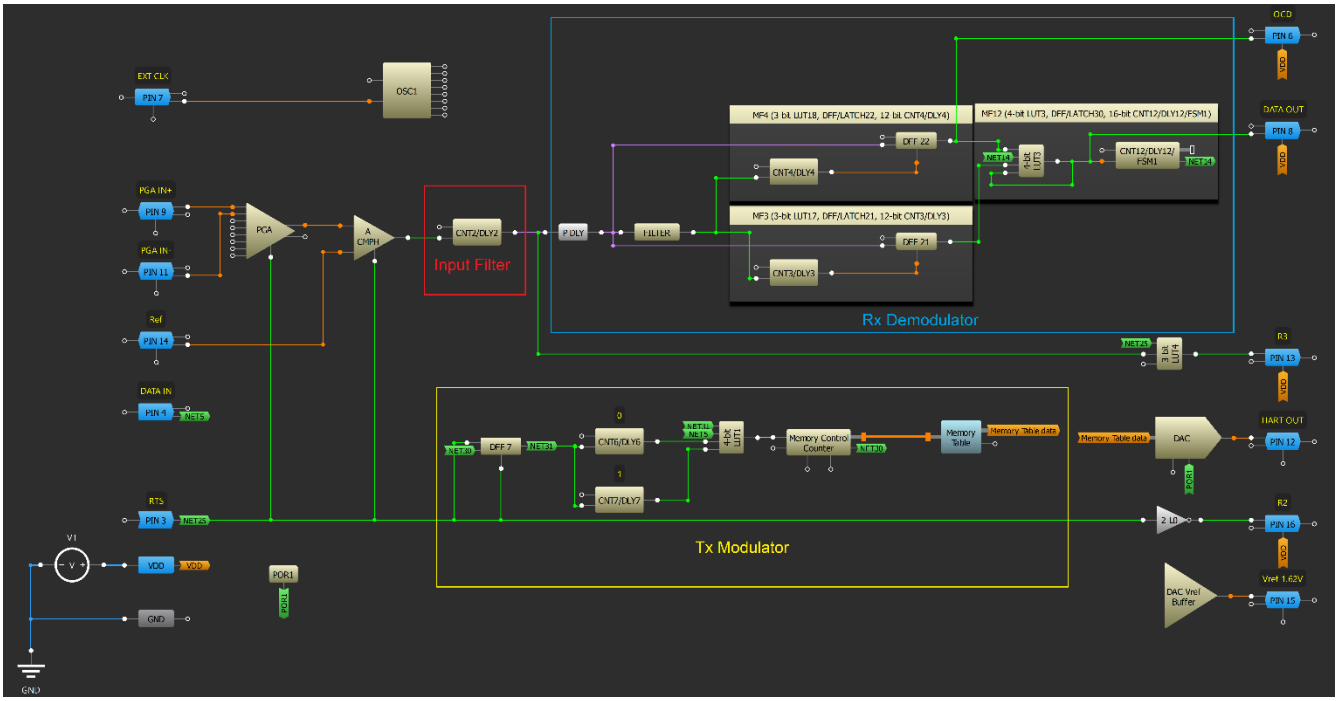

Figure 6. Go Configure Schematic of HART Modem

3.1 Modulator

The HART protocol uses frequency-shift keying to encode and transfer data, specifically a 1200 Hz signal for a binary “one” and 2200 Hz for a binary “zero”. Firstly, the host issues an active-low request-to-send (RTS) signal, activating the modulation mode. CNT7/DLY7 and CNT6/DLY6 are initiated upon this signal.

If a logical zero is transmitted to Pin 4, the 4-bit LUT1 outputs a 222 kHz signal from CNT7/DLY7. In the presence of a logical one on the pin, it instead outputs a 121 kHz signal from CNT6/DLY6. The Memory Control Counter counts from 0 to 100, corresponding to 101 samples of a sinusoidal waveform, providing the required frequencies required by the HART protocol.

The ROM table stores values to generate the sine wave, and the DAC converts this ROM digital data into a sine wave signal (without phase shift). This signal is then summed with the current loop signal through a buffer.

To change the clock frequency of the modulator, it is necessary to recalculate the number of samples into which the generated sine wave will be divided. Accordingly, the new memory table values must be calculated for the revised data. In addition, for the new number of samples, new counter data values must be selected for CNT/DLY6 and CNT/DLY7.

Figure 7 shows waveforms for sending modulated data.

Channel 1 (yellow/top line) – HART OUT.

Channel 2 (light blue/2nd line) – PIN 4 (DATA IN).

Channel 3 (magenta/3rd line) – PIN 3 (RTS).

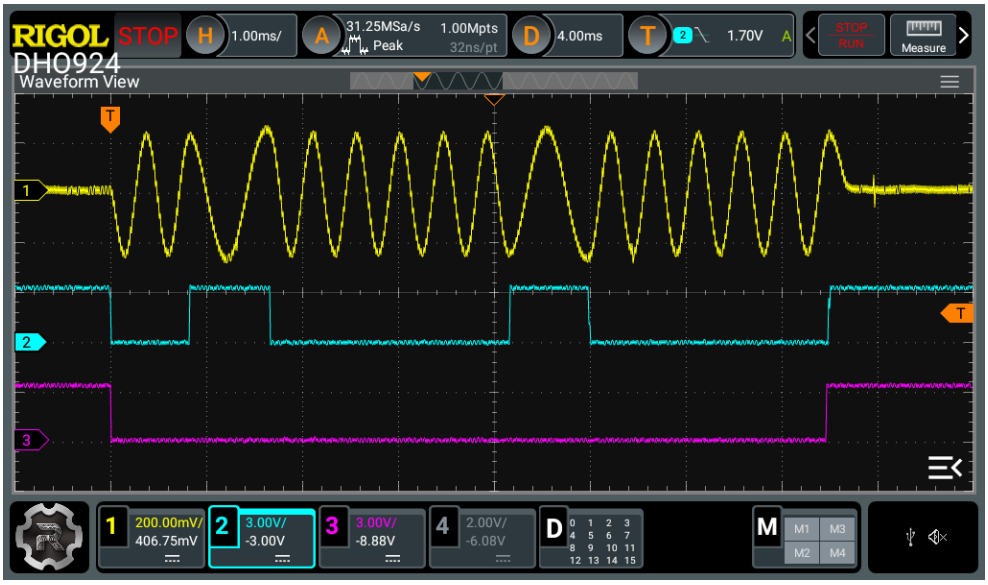

Figure 7. Sending Data to the Current Loop (Data is 0x11)

3.2 Demodulator

In this mode, the host's RTS signal is HIGH, powering up the demodulator's analog blocks (PGA and ACMP). The filtered signal from the current loop is fed to the differential input of the Programmable Gain Amplifier (PGA), amplifying the signal by 4b Subsequently, the Analog Comparator (ACMP) compares this signal with the reference voltage formed by an external divider. Demodulation starts as soon as the SLG47011 detects a 1200/2200 Hz signal with V_{IN} > 120 mV peak-to-peak on the line (in turn, a sine signal with amplitude V_{IN} < 80 mV peak-to-peak will be ignored). These amplitude values are taken in accordance with the HART specification requirements, and the solution based on the SLG47011 meets this specification.

The CNT2/DLY2 delay eliminates noise from the comparator output, while P DLY functions as a Both Edge Detector. Delay CNT3/DLY3 and DFF21 determine which of the two known frequencies is at the input; specifically, a logical zero at the DFF output indicates an input frequency of 2200 Hz, and a logical one indicates 1200 Hz. Delay CNT4/DLY4 and DFF22 determine whether there is a sinusoidal signal at the input at all. A logical one at the DFF output indicates the presence of an input signal, while a logical zero indicates its absence. Simultaneously, the OCD (Output Carrier Detect) signal at the output of Pin 6 informs the host that the carrier has been detected. One Shot (CNT12/DLY12) forms an output signal with a duration of 820 µs, which is sent via Pin 8 to the host data input.

Pin 13 (controlled by 3-bit LUT4) and Pin 16 provide hysteresis for the ACMPH in demodulation mode. In modulation mode, the reference divider is disconnected from the power source to reduce power consumption.

Figure 8 shows the waveforms for receiving data.

Channel 1 (yellow/top line) – HART IN.
Channel 2 (light blue/2nd line) – PIN 8 (DATA OUT).
Channel 3 (magenta/3rd line) – PIN 6 (OCD).

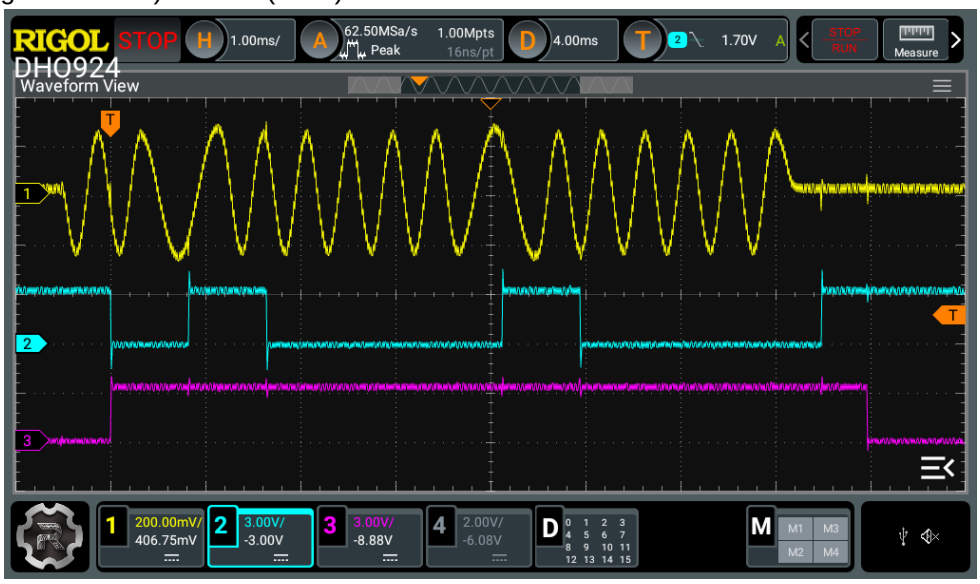

Figure 8. Receiving Data from the Current Loop

4. Conclusions

This application note demonstrates the SLG47011 integrated circuit's effectiveness in implementing a HART modem. The circuit successfully performs both the modulation and the demodulation of the HART signal. Since all HART devices must be certified, this GreenPAK circuit is tuned to meet HART's official test specification requirements. However, this design can be easily modified as needed to suit specific project requirements as well. The SLG47011's standout features, such as its low power consumption, flexibility, compact footprint, and robust performance, make it a compelling choice for engineers and developers interested in enhancing their HART-enabled applications.

Renesas also has a HART Modem Demo Board (with a PCB), which makes testing the modem operation very easy and accessible. See more details in the demo board User Manual [5].

5. Revision History

Revision	Date	Description
1.00	March 5, 2025	Initial release.

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