PIR (Passive Infrared) 2-Channel Sensor
SLG47011

Abstract

This application note describes the design for a Passive Infrared (PIR) Sensor application. The PIR component is categorized as an analog electronic sensor that measures infrared (IR) light radiating from objects in its field of view. Analog PIR sensors are commonly used in security systems and automatic lighting applications. Specifically, the rise in popularity of smart homes and Internet of Things (IoT) devices are a major driver for the digital PIR market's expansion. Digital PIR sensor systems (as opposed to analog) perform with higher accuracy, with adjustable sensitivity and timer control for motion detection. In this case, the SLG47011 is used to digitize the analog signal from a PIR senor to indicate the status of detected motion. This application note details this design which includes the use of PGA, ADC, Buffer, DCMP, DLY/CNT, and LUT blocks.

Contents

Terms and Definitions

ADC	Analog to Digital Converter
AFE	Analog Front-End
DCMP	Multichannel Digital Comparator
DLY/CNT	Delay/Counter
DFF	D Flip Flop
I2C	Inter-Integrated Circuit
LUT	Look Up Table
PIR	Passive Infrared
PGA	Programmable Gain Amplifier

References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the design file [2] and view the proposed circuit design. Use the AnalogPAK development tools to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-403 PIR (Passive Infrared) 2-Channel Sensor.aap, AnalogPAK Design File, Renesas Electronics

[3] AnalogPAK Development Tools, AnalogPAK Development Tools Webpage, Renesas Electronics

[4] Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

[5] PIR Click | Mikroe

[6] zilog.com/docs/zmotion/PS0402.pdf

1. Introduction

The SLG47011 provides diverse digital and analog marcocells for AFE applications. Figure 1 shows SLG47011 block diagram. One 14-bit SAR ADC and one 4-channel PGA will be used to capture the Analog Front-End signal. The PGA can operate in different configurations such as single-end mode and differential mode. Additionally, the Vref to the PGA and ADC can be configured with different sources and values. The ADC can support different resolutions ranging from 8 to 14 bits. Moreover, the SLG47011 offers 4 Buffer blocks in which average and over-sampling functions can be used to process the ADC data.

The multichannel DCMP marcocell is a configurable comparator for the independent ADC channels. Internal threshold and hysteresis for each individual ADC channel can be assigned with different sources or values as well. These features allow the AFE application to output multiple analog signals and to be implemented in various configurations.

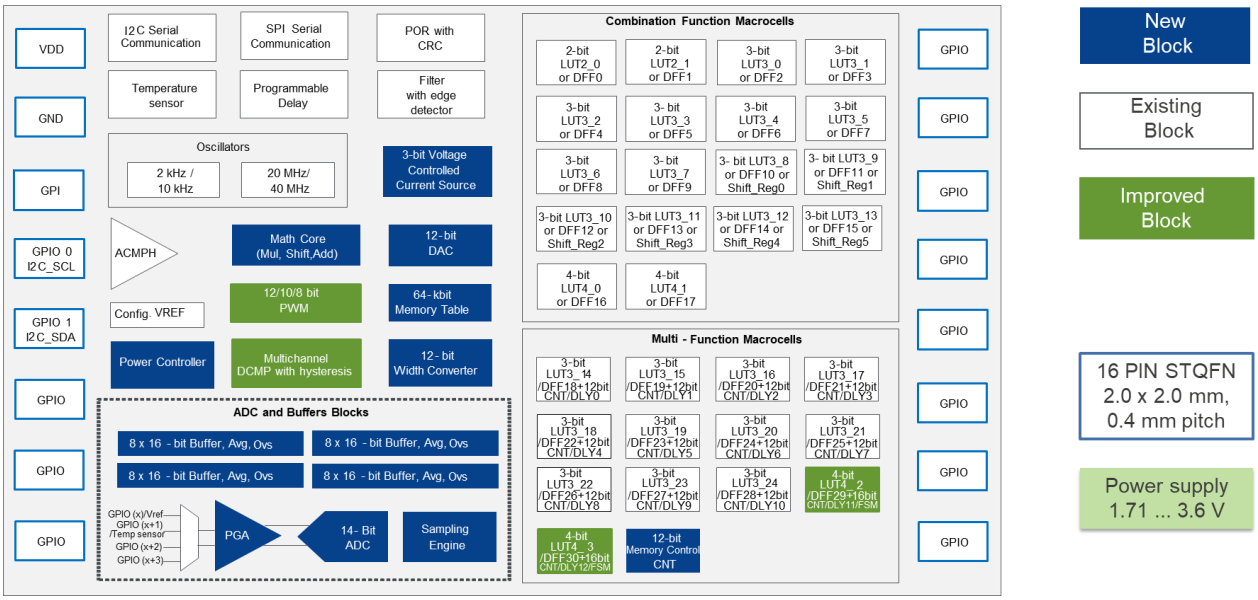

Figure 1. SLG47011 Block Diagram

2. Design Principle

Particularly in the security alarm industry, PIR sensors are utilized to detect the infrared radiation emitted by humans or animals. Infrared light emitting from any object can force PIR signal variation. This variation reflects how close the object is to the PIR sensor itself.

Figure 2 shows the system diagram for a dual PIR sensor application. Each PIR sensor interacts with two external low pass filters to synthesize a band-pass filter. The PGA is configured as an instrumentation amplifier with differential inputs for detecting the PIR signal. PIN 7 and PIN 11 are configured as a differential sensing-input pair to detect motion from PIR signal #1; PIN 8 and PIN 12 are configured as separate differential sensing-input pair to detect motion from PIR signal #2. PIN 15 and PIN 16 provide motion status detection as Motion_S1 and Motion_S2 respectively.

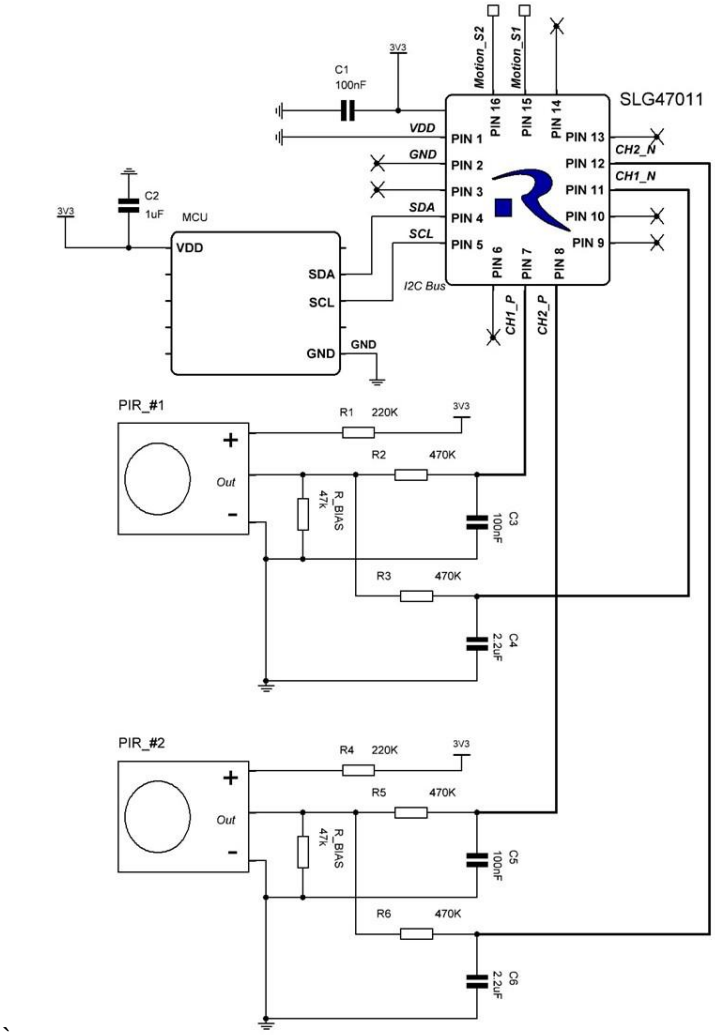

Figure 2. System Diagram

Figure 3 depicts the operation of this PIR application. The SLG47011 will capture a PIR signal and indicate the corresponding motion detection status. The internal Multichannel DCMP operates as window-comparator to set the voltage window. The delay macrocell which is used to provide blanking time, can be adjusted by its corresponding register.

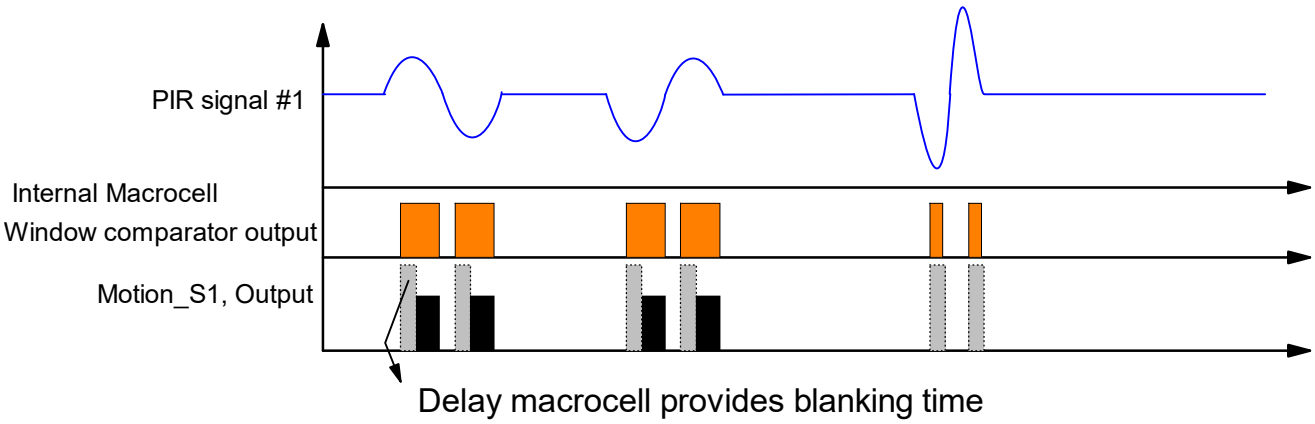

Figure 3. Operation Timing Diagram

3. Internal Block Configuration in the GreenPAK Designer

The GreenPAK Design is presented in Figure 4.

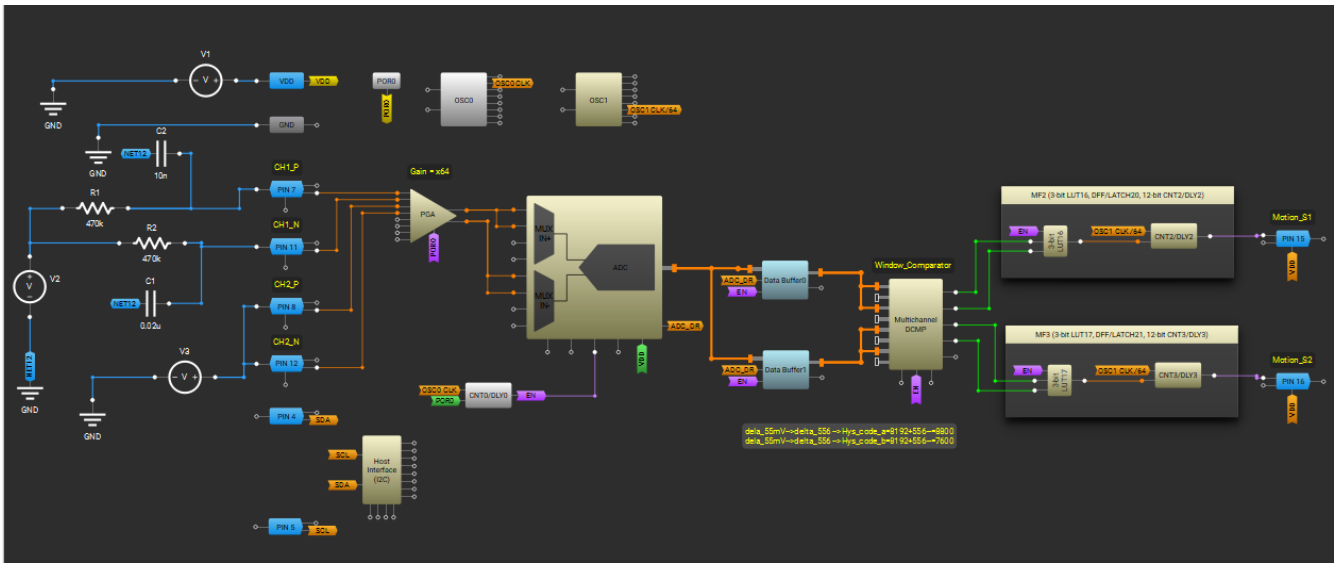

Figure 4. Block Diagram for PIR Design

The PGA is configured to act as an instrumentation amplifier in differential mode. To get the PIR signal effectively and to reduce signal error, the external low-pass RC filter pair is used as a bandpass filter. This allows the instrumentation amplifier to obtain the band-pass signal from the individual PIR signal. We can calculate the RC component parameters based on the following equation for cutoff frequencies fc1 and fc2.

$$fc = \frac{1}{2\pi \cdot R \cdot C}$$

- fc1 = 3.380 Hz; R2 = 470 kΩ; R5 = 470 kΩ; C3 = C5 = 100 nF
- fc2 = 0.154 Hz; R3 = 470 kΩ; R6 = 470 kΩ; C4 = C6 = 2.2 µF

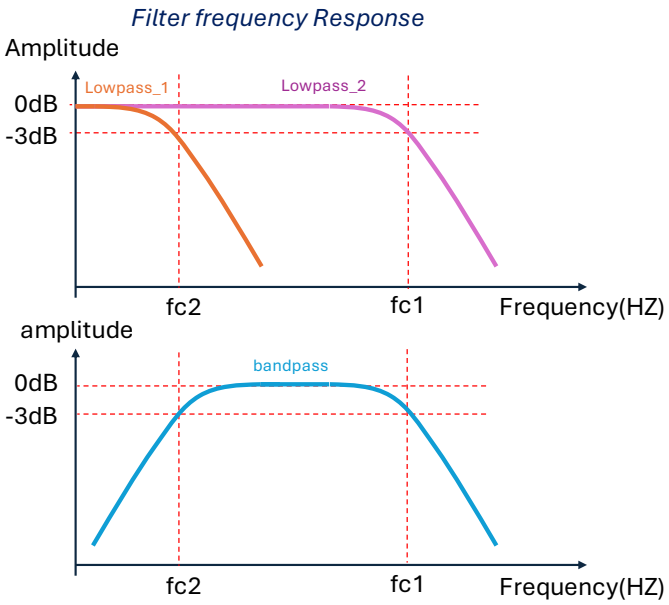

Figure 5. Filter frequency Response

Figure 6 shows the configuration windows for the PGA, ADC, and two Data Buffers. The PGA needs to operate with high input impedance to detect the PIR signal. The PGA gain is set to x64 to widen PIR variation. The ADC macrocell provides 14 bits of resolution and a lower sampling rate of 15.625 ksps in this design to monitor the PIR signal. Data Buffer0 and Data Buffer1 are configured to collect individual ADC channel data.

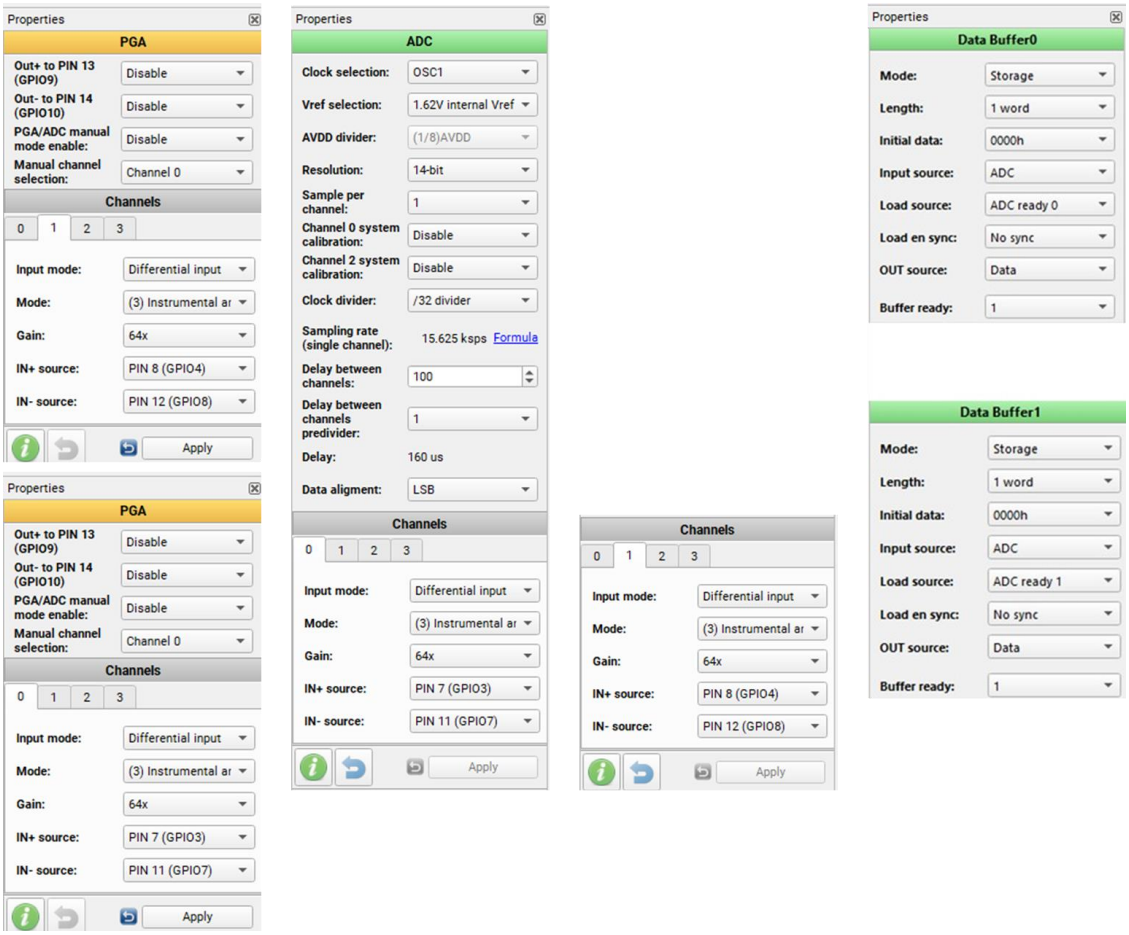

Figure 6. Configuration properties for PGA, ADC, Data Buffer1, and Data Buffer0

Since the PGA is configured as a differential instrumentation amplifier, ADC data will need to reflect a input difference. For example, CH1_P > CH1_N results in ADC data > 8192; otherwise, ADC data < 8192. The Multichannel DCMP macrocell operates as a 2-channel window-comparator to detect PIR motion. Each channel's window-comparator is comprised of two 14-bit (16383) digital comparators in parallel. Once the input difference (ΔV) of the PGA is greater than 10 mV, the DCMP will indicate the active motion status. The threshold of each individual digital comparator can be obtained by equation below:

$$\text{Static Threshold} = 8192 \pm 1.6383 \cdot \frac{\Delta V \cdot Gain\_PGA}{1.62V} \quad \text{(bits)}$$

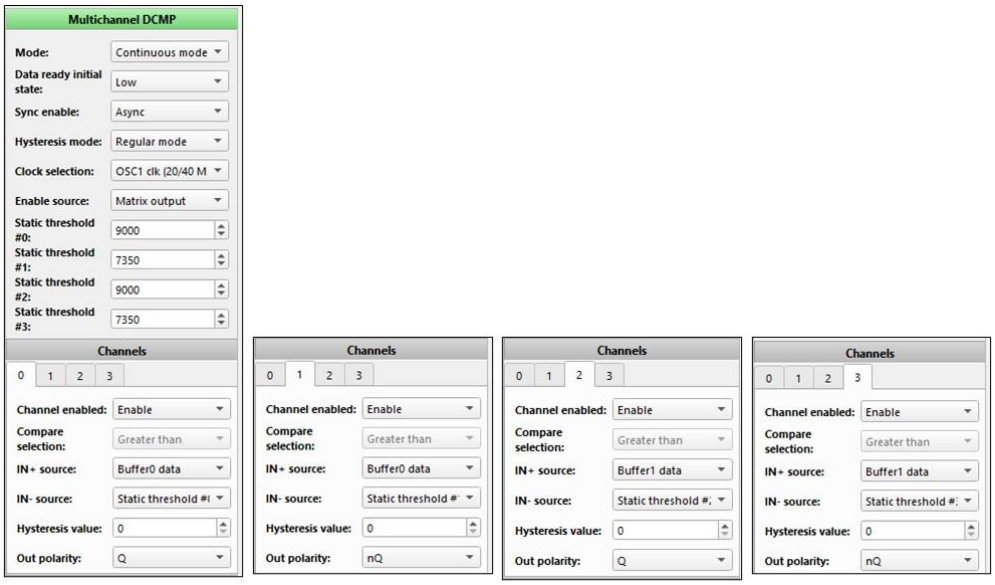

Figure 7. Configuration properties for the Multichannel DCMP

Since characteristic tolerances exist both in the components and in the chip itself, the related DCMP threshold needs to be adjustable. Table 1 and Table 2 show the DCMP and CNT/DLY registers used to set these thresholds

Table 1: DCMP static threshold Register

Address Byte	Register Bit	Block	Function
0x17C	<3047:3040>	DCMP_ST_THLD_0_MSB	Determine upper limit to Window-comparator 0
0x17D	<3055:3048>	DCMP_ST_THLD_0_LSB	
0x17E	<3063:3056>	DCMP_ST_THLD_1_MSB	Determine lower limit to Window-comparator 0
0x17F	<3071:3064>	DCMP_ST_THLD_1_LSB	
0x180	<3079:3072>	DCMP_ST_THLD_2_MSB	Determine upper limit to Window-comparator 1
0x181	<3087:3080>	DCMP_ST_THLD_2_LSB	
0x182	<3095:3088>	DCMP_ST_THLD_3_MSB	Determine lower limit to Window-comparator 1
0x183	<3103:3196>	DCMP_ST_THLD_3_LSB	

Table 2: CNT2/DLY2 and CNT3/DLY3 counter data Control Registers

Address Byte	Register Bit	Block	Function
0xEC	<1891:1888>	CNT2 / DLY2 clock source selection	//Based on design, don't change it
	<11895:1892>	CNT2 / DLY2 MSB of CNT Data	Adjust the sensitivity of PIR motion status, Motion_S1
0xED	<1903:1896>	CNT2 / DLY2 LSB of CNT Data	
0XF3	<1947:1944>	CNT3 / DLY3 clock source selection	//Based on design, don't change it
	<1951:1948>	CNT3 / DLY3 MSB of CNT Data	Adjust the sensitivity of PIR motion status, Motion_S2
0XF4	<1957:1952>	CNT3 / DLY3 clock source selection	

4. Design Simulation

The design simulation of the SLG47011 operating as a motion detector is shown in Figure 8.

The simulation assumes that the SLG47011 has just detected voltage variation on PIR#1.

The Buffer0 data is also changed according to the PIR#1 signal. The DCMP recognizes this as an object approaching PIR#1.

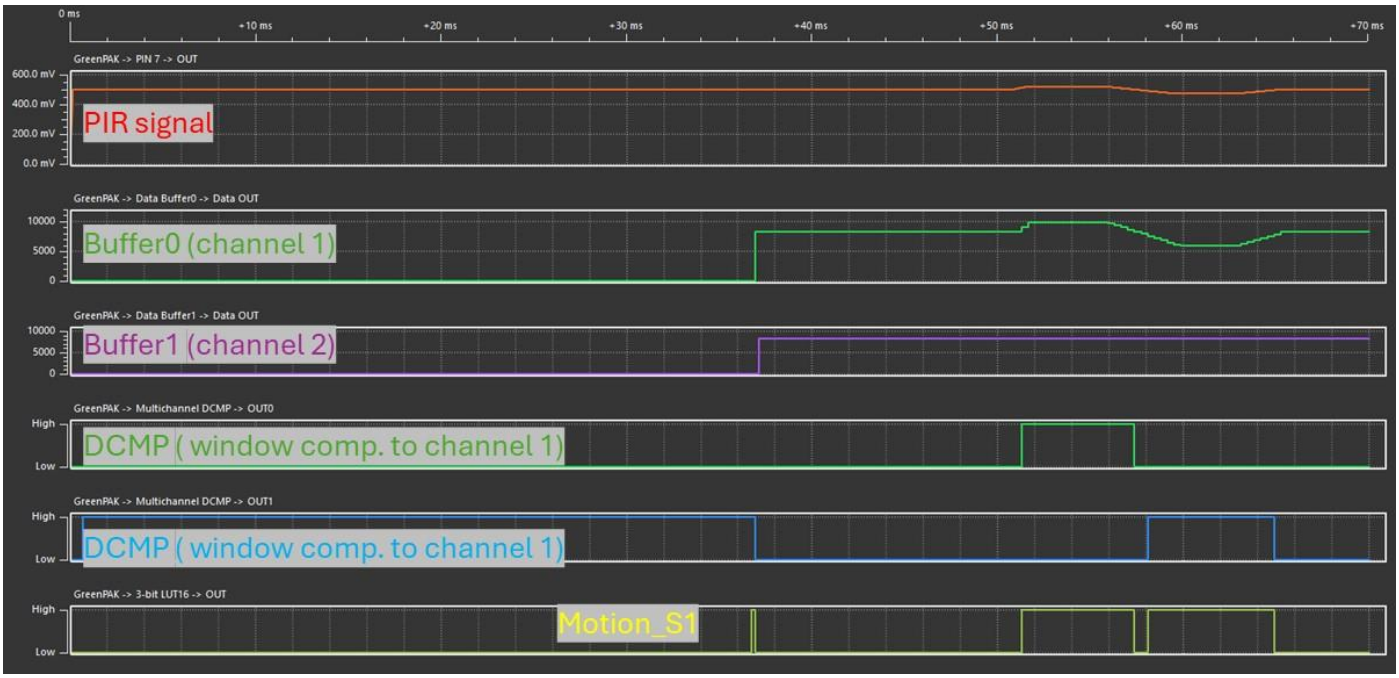

Figure 8. Simulation Result

5. Design Verification Using a Hardware Prototype

To detect a human approaching, we two PIR Click boards are used for validation. Each PIR click board is equipped with external band pass filters as a synthesised bandpass filter. When a human approaches an individual PIR sensor, the SLG47011 will detect PIR signal variation and reflect the motion status in real-time.

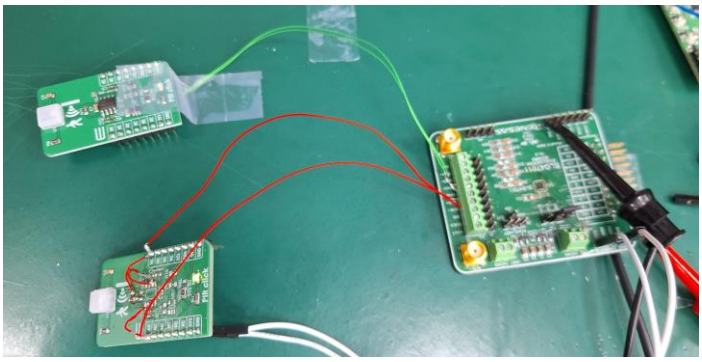

Figure 9. System Implementation

Channel 1 (yellow/top line) – PIN# 11 (CH1_N) → signal is filtered with low pass fc2 = 0.154 Hz
Channel 2 (light blue/2nd line) – PIN# 7 (CH1_P) → signal is filtered with low pass fc1 = 3.380 Hz
Math 1 (orange /bottom line) – Subtraction calculation: PIN# 7 - PIN# 11
D0 – PIN# 15 (Motion_S0) → output motion signal

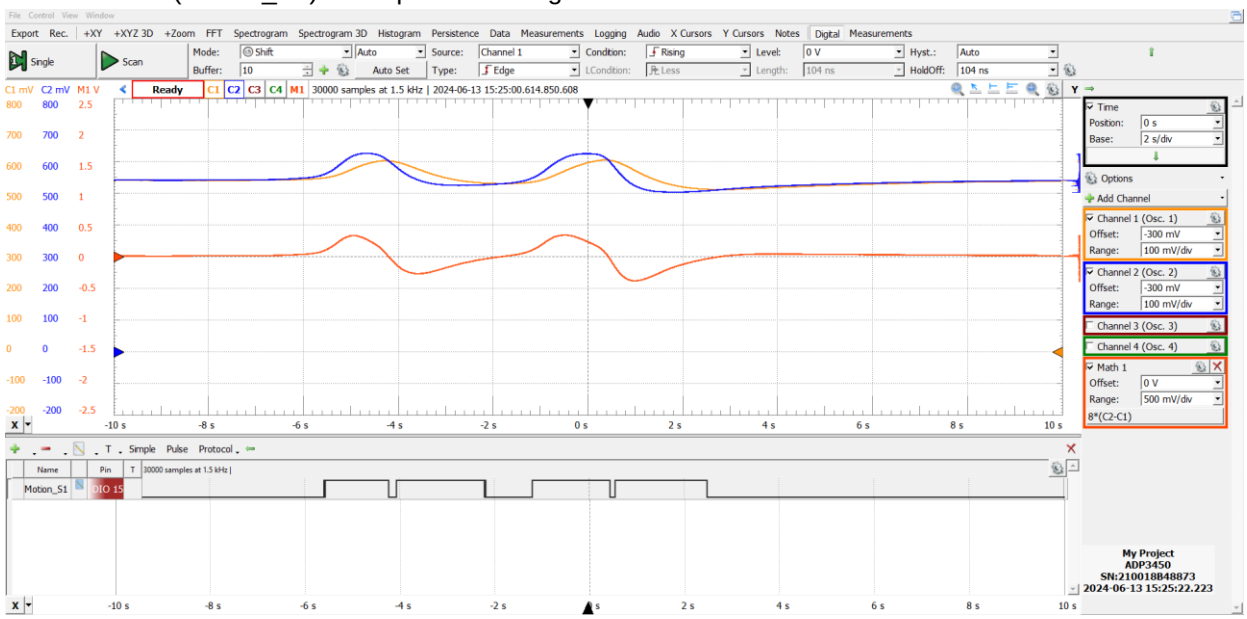

Figure 10. Measurement: Human approaching PIR sensor (Distance is 50 cm)

PIR sensor ZRE200GE [5] was also used for validation. This PIR sensor is designed to deliver high performance and excellent EMI immunity. The tester is far away (2 meters) from the PIR sensor. Once the tester starts to move, the PIR sensor reflects this change in pyroelectricity. The SLG47011 captures the PIR signal and provides the motion status.

Channel 1 (yellow/top line) – PIR signal
D0 – PIN# 15 (Motion_S0) → output motion signal

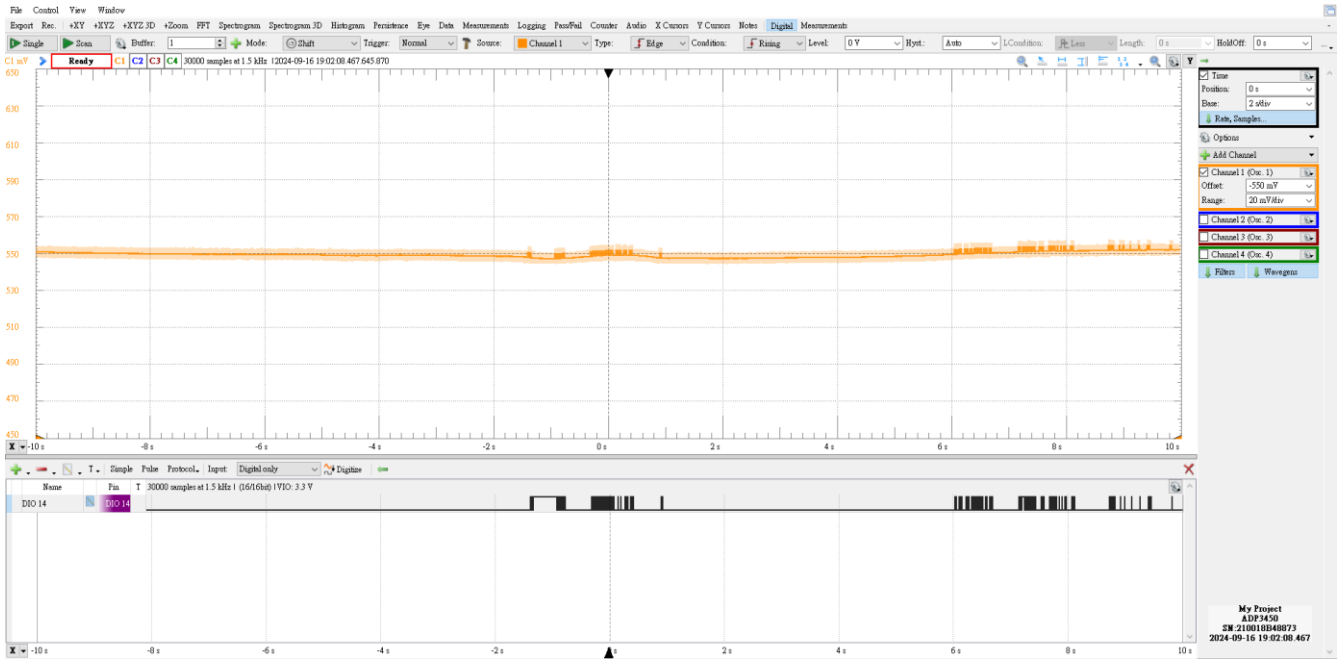

Figure 11. PIR signal measurement at 2 meters

Next, the tester is moved to a distance of 4 meters from the PIR sensor. Once the tester starts to move, the PIR sensor reflect the change in pyroelectricity. The SLG47011 captures the PIR signal and provides the motion status.

Channel 1 (yellow/top line) –PIR signal
D0 – PIN# 15 (Motion_S0) → output motion signal.

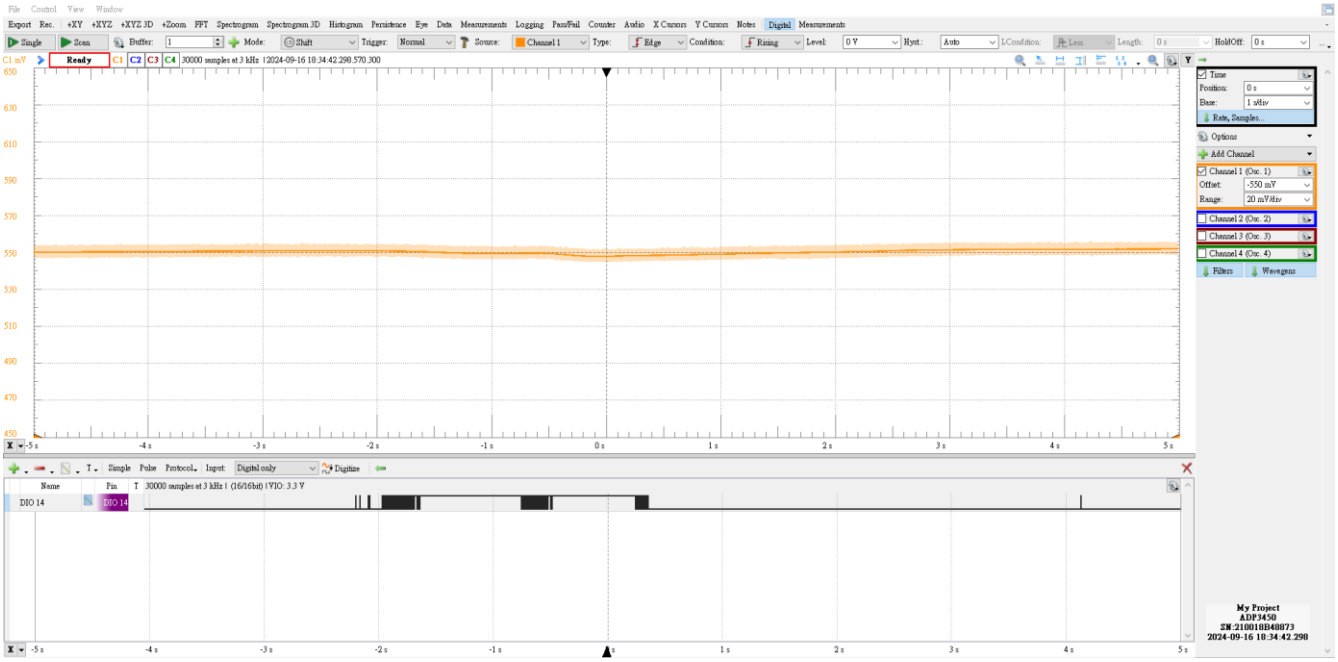

Figure 10. PIR signal measurement at 4 meters

6. Conclusion

The validation result verifies that the SLG47011 works well in PIR detection applications. The PIR analog signal needs an external bandpass filter to reduce noise. The internal window comparator can successfully differentiate the signal change.

7. Revision History

Revision	Date	Description
1.00	November 5, 2024	Initial release

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