Thermistor Linearization
SLG47011

Abstract

This application note describes how to use the SLG47011 to implement a design for a Thermistor Linearization application. Since the thermistor component is categorized as a negative-temperature-coefficient (NTC) resistor, the linearization process can convert rows of NTC data into linear data. The Memory Table macrocell in the SLG47011, which can contain a dataset of 4096 12-bit words, is the primary component used to process rows of NTC data to be linearized.

Contents

Abstract **1**

1. Terms and Definitions **2**

2. References **2**

3. Introduction **3**

4. Design Principle **4**

5. GreenPAK Design Internal Block Configuration **5**

6. Simulation Results **9**

7. Design Verification Using Hardware Prototype **9**

7.1 Thermistor results at 25 ˚C 9

7.2 Thermistor results at 65 ˚C 10

7.3 Thermistor results at 100 ˚C 10

8. Conclusion **10**

9. Revision History **11**

© 2024 Renesas Electronics

1. Terms and Definitions

ADC	Analog to Digital Converter
AFE	Analog Front-End
I2C	Inter-Integrated Circuit
LUT	Look Up Table
MEM	Memory
NTC	Negative Temperature Coefficient
PIR	Passive Infrared
PGA	Programmable Gain Amplifier

2. References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the design file [2] and view the proposed circuit design. Use the AnalogPAK development tools to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes [4] featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics
[2] AN-CM-401 Thermistor Linearization.aap, AnalogPAK Design File, Renesas Electronics
[3] AnalogPAK Development Tools, AnalogPAK Development Tools Webpage, Renesas Electronics
[4] Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

3. Introduction

The SLG47011 is comprised of a diverse collection of digital and analog marcocells for AFE applications. One 14-bit SAR ADC and one 4-channel PGA (shown in the Block Diagram of the SLG47011 in Figure 1) are used to perform Analog Front-End signal capturing. The PGA is capable of operating in different configurations such as single-ended mode and differential mode. Additionally, the reference voltages used by the PGA and ADC can be configured independently as needed. The ADC supports resolutions ranging from 8 bits to 14 bits. Moreover, the SLG47011 offers four Buffer blocks in which averaging and over-sampling functions are used to process ADC data.

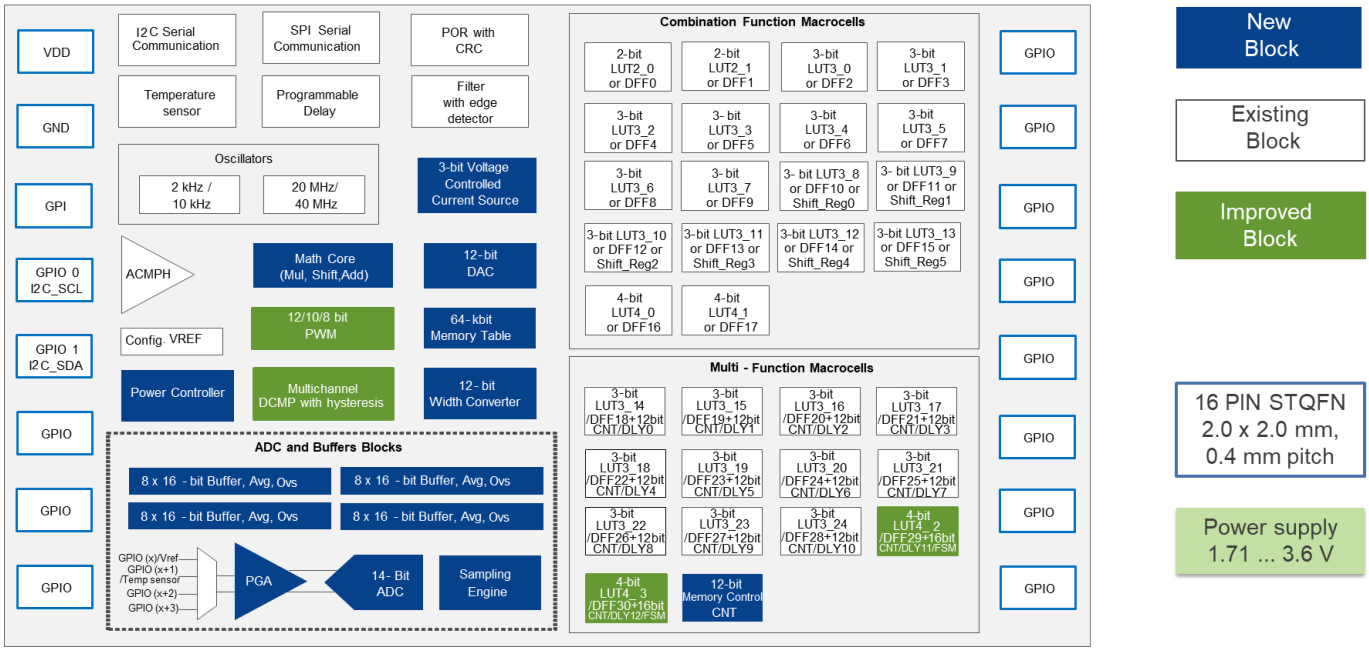

Figure 1. SLG47011 Block Diagram

Linearization is the process of taking the nonlinear data with respect to all variables and creating a linear representation for any point of data (see Figure 2). The SLG47011 accomplishes this by utilizing its internal Memory Table microcell as shown in figure below.

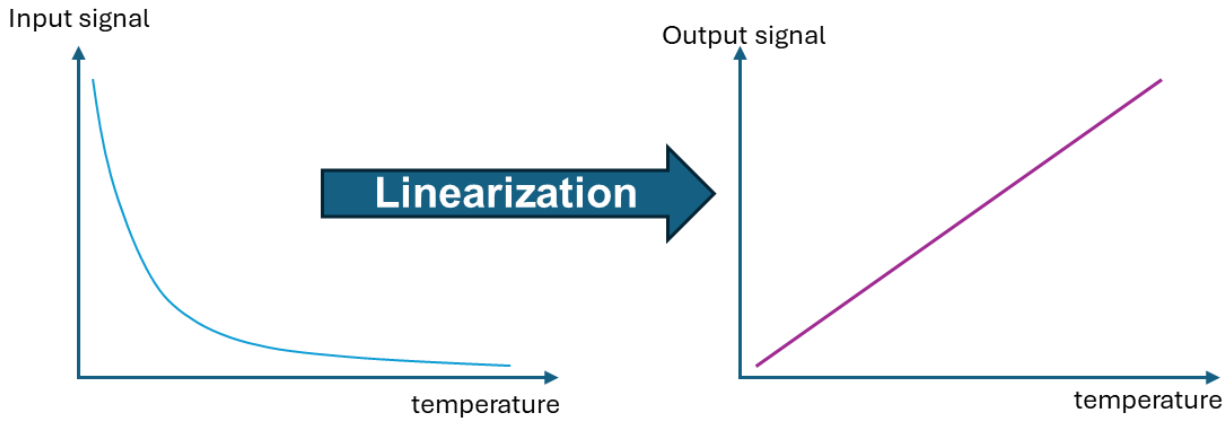

Figure 2. Conversion from Nonlinearity to Linearity

4. Design Principle

Figure 3 shows the system diagram of our Thermistor Linearization design. PIN 7 acts as the sensing input which captures the voltage drop across the thermistor. The resulting linear thermistor data from the DAC is output on PIN 12.

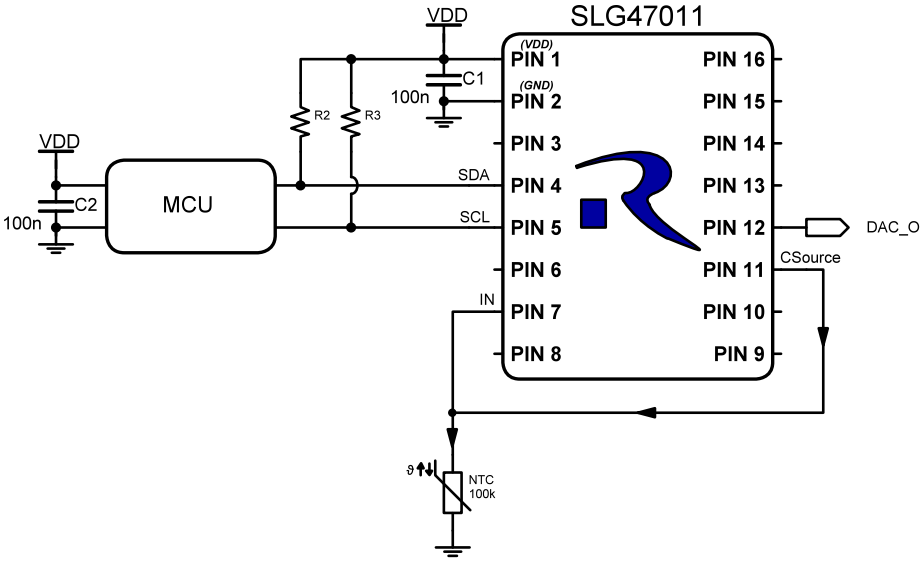

Figure 3. System Diagram

In general, the NTC characteristic of the thermistor component are non-linear, which can create challenges and errors in applications. To combat this, signal conversion is used to transform non-linear signals from the thermistor into linear signals. The SLG47011 can reshape the digital signal from the ADC and output an analog signal corresponding to the rate of temperature change.

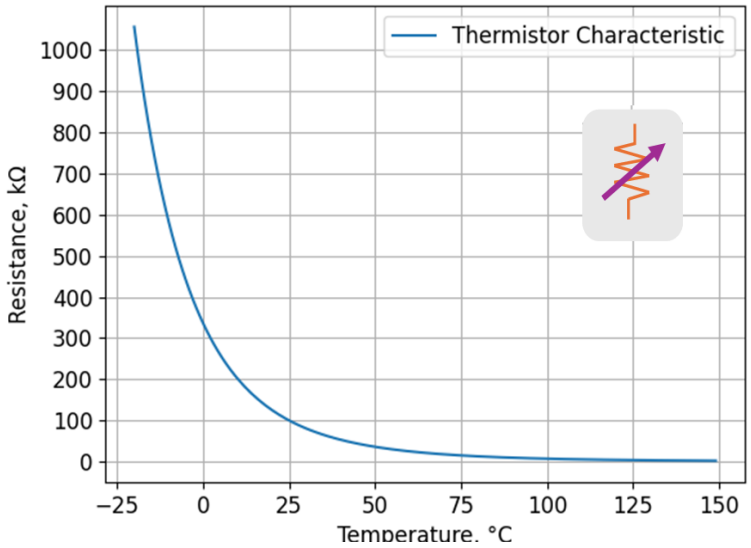

Figure 4. NTC thermistor characteristic. (R_{25C} = 100 KΩ; β = 3950)

5. GreenPAK Design Internal Block Configuration

The GreenPAK Design as shown in the GoConfigure software is presented in Figure 4.

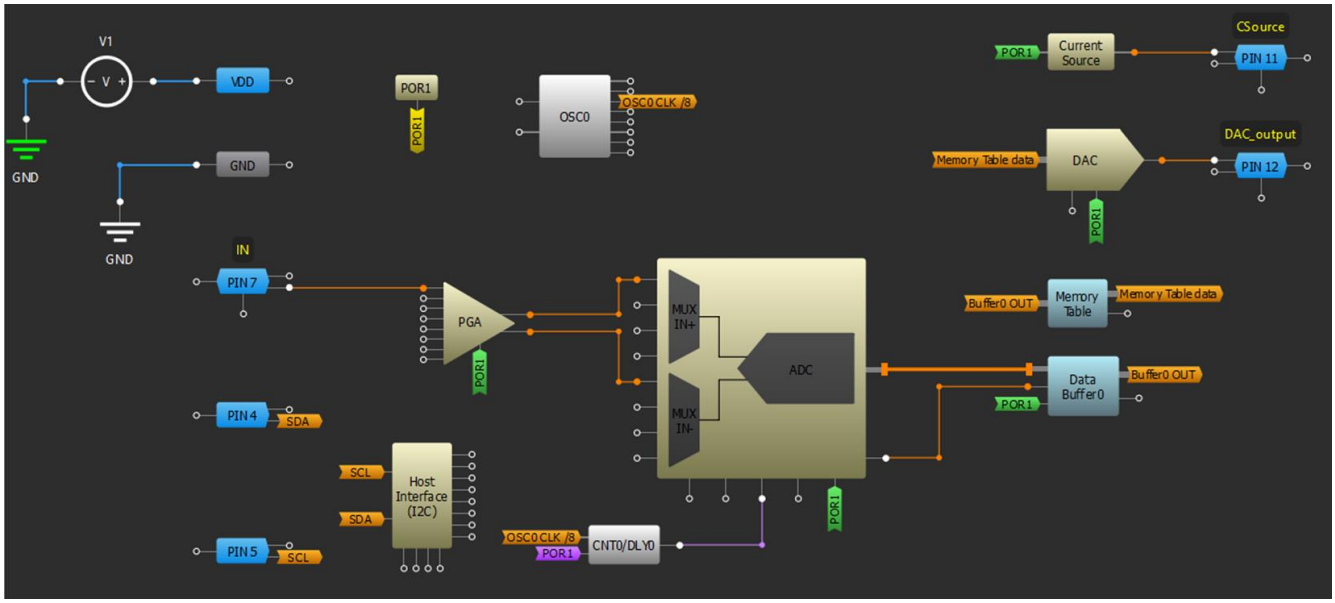

Figure 4. GreenPAK Designer Schematic

The current source is assigned to PIN11 and provides a configurable constant current through the external thermistor component. The PGA is configured as a single-ended buffer AFE channel. The 12-bit resolution ADC performs the conversion of the analog signals into a digital representation. Buffer0 is used to provide averaging to filter the ADC digital signals.

To accomplish linearization, the SLG47011 utilizes the Memory Table and DAC macrocells. The Memory Table and DAC offer a convenient way to convert the non-linear thermistor signal into a linear signal based on the digital data from Memory Table. The configuration settings for the design are shown in Figure 5.

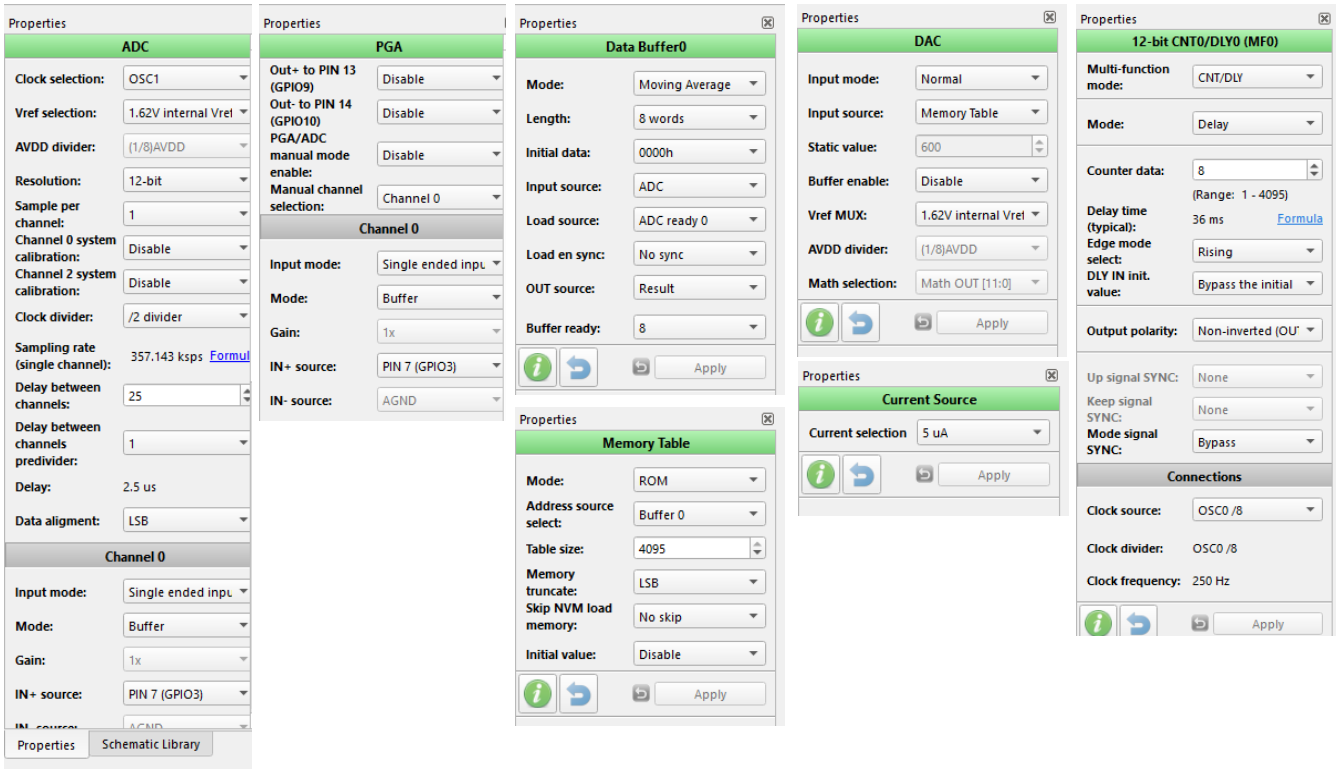

Figure 5. Design Configuration Settings

Thermistor Linearization

This SLG47011 thermistor linearization design supports a temperature range from 10 °C to 120 °C.

The NTC thermistor resistance is given by:

$$R_T = R_{25C} \cdot e^{\beta \cdot \{1/(\mathrm{T}+273)-1/298\}}$$

where:

R_{25C} = thermistor's resistance at 25 °C

T = temperature

β = material coefficient.

PIN 11 (CS source) produces a constant value Ics of current through the NTC thermistor.

$$\mathrm{Ics} = 5\ uA$$

The non-ideal signal of the NTC thermistor can be expressed as:

$$V_T = 100\mathrm{k}\Omega \cdot \mathrm{Ics} \cdot e^{3950 \cdot \{1/(\mathrm{T}+273)-1/298\}}$$

where:

R_{25C} = 100 kΩ

β = 3950

It is assumed that the DAC output provide linearization with 0.5 V ~ 1.2 V variation corresponding to a temperature range of 10 ˚C to 120 ˚C.

The Python script showing the calculation is shown in the code snippet below.

```
import numpy as np
import pandas as pd
import matplotlib.pyplot as plt

# setup temperature range for -20 C~120 C,
t = np.arange(10, 120+0.05, 0.005)
# set up constant current provided by PIN11 (CSource)
Is=5e-6
#func Define: Thermistor R equation
def Rth(x, Coefficient=3950):
    R_25c = 100000
    RT=R_25c*np.exp(Coefficient*(1/(x+273)-1/298))
    return RT
#func Define: PIN12 (DAC output) perform linearization
def Lin_r(x):
    V_start = 0.5  # T= 10C
    V_end = 1.2    # T= 120C
    slew=(V_end-V_start)/(120-10)
    out=slew*(x-10)+V_start
    return out
#Calculation
VT=Rth(t)*Is
#Calculation
DAC_out=Lin_r(t)
#plot
plt.figure(figsize=(12, 8))
plt.plot(t,VT, label="NTC Thermistor,  Coefficient=3950 ")
plt.plot(t,DAC_out, label="Linearization-->DAC output ")
#plt.plot(t,np.log(50)+3950*(1/(t+273)-1/298), label="Linearization-->DAC output ")
plt.legend(fontsize=18)
plt.xlabel("Temperature,  °C", fontsize=18)
plt.ylabel("Volage, V", fontsize=18)
plt.xticks(fontsize=18)
plt.yticks(fontsize=18)
plt.show()

# Next
```

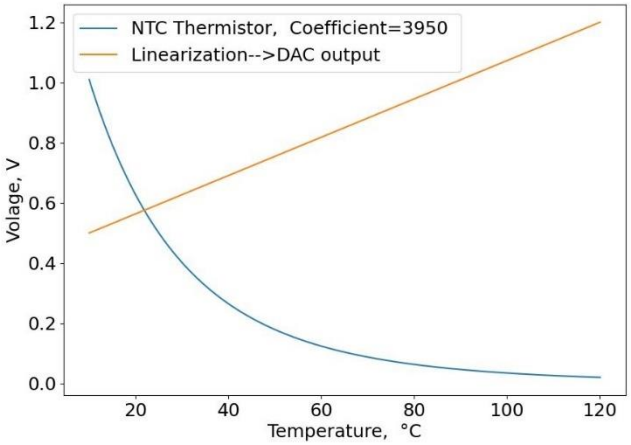

Figure 6. NTC Thermistor and DAC output corresponding to Temperature

The GoConfigure software provides an import tool for manipulating data sets to achieve the desired digital transfomation.

The Memory Table import tool accepts both .csv and/or .txt files (see Figure 7). The following python script completes preparation of the data sets.

```
df=pd.DataFrame({
                 "NTC(bit)": (VT/1.62*4095).astype(int),
                 "DACout(bit)": (DAC_out/1.62*4095).astype(int)
                 })
#
for i in range (df["NTC(bit)"].min(), df["NTC(bit)"].max()+1):
    try:
        df.loc[df["NTC(bit)"]==i,["DACout(bit)"]]=df.loc[df["NTC(bit)"]==i,["DACout(bit)"]].values.max()
    except:
        pass
#
df = df.drop_duplicates(subset='NTC(bit)', keep='first')
df = df.sort_values(['NTC(bit)'], ascending= True,ignore_index=True).copy()
#
get_min = df["NTC(bit)"].min()
get_max = df["NTC(bit)"].max()
#
new_data_2=np.concatenate((df["DACout(bit)"].max()*np.ones(get_min),df["DACout(bit)"],
                           df["DACout(bit)"].min()*np.ones(4095-get_max)))
#
df2=pd.DataFrame({"Memory Table data":  list(map(lambda x: f"0X{x:#0{6}x}"[2:], list(map(int, new_data_2))))})
#
df2.to_csv("MEM_Table_r001_1.csv", index= False)
```

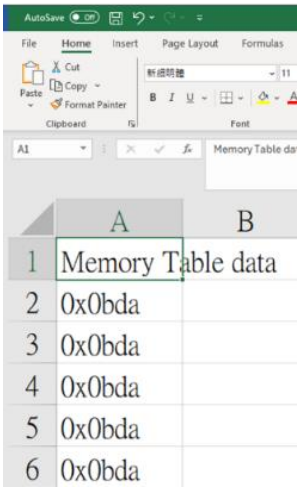

Figure 7. Importing the data set using .csv file

6. Simulation Results

The simulation results of the SLG47011 linearization is shown in Figure 8.

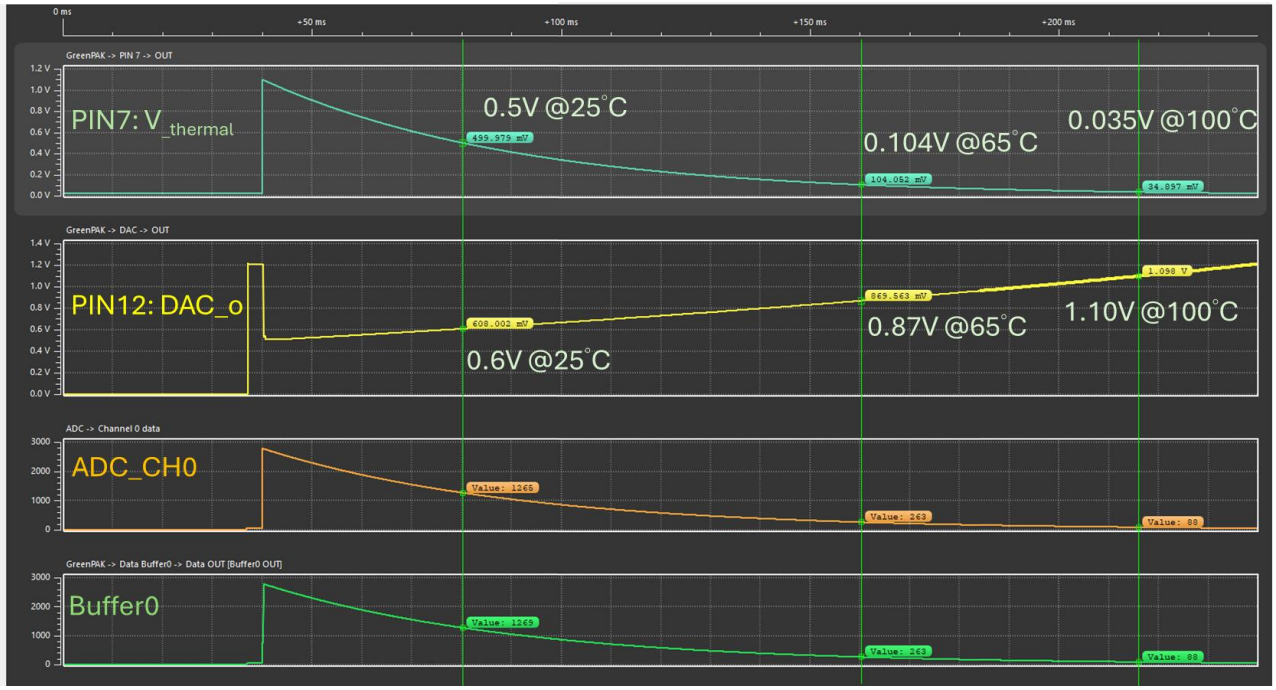

Figure 8. Simulation results

7. Design Verification Using Hardware Prototype

A hardware prototype used to verify the simulation results at varying temperatures shows that the SLG47011 can convert the non-linear thermistor signal to a linear signal properly.

7.1 Thermistor results at 25 ˚C

Channel 1 (yellow/top line) – PIN# 7 (IN) → Thermistor (NTC 10K/B3950 1%) signal.
Channel 2 (light blue/2nd line) – PIN# 12 (DAC_output) →DAC output

Calculation for operation at 25 ˚C, Thermistor signal = 0.500 V; DAC output = 0.595 V
Measured result shows DAC output = 0.594 V

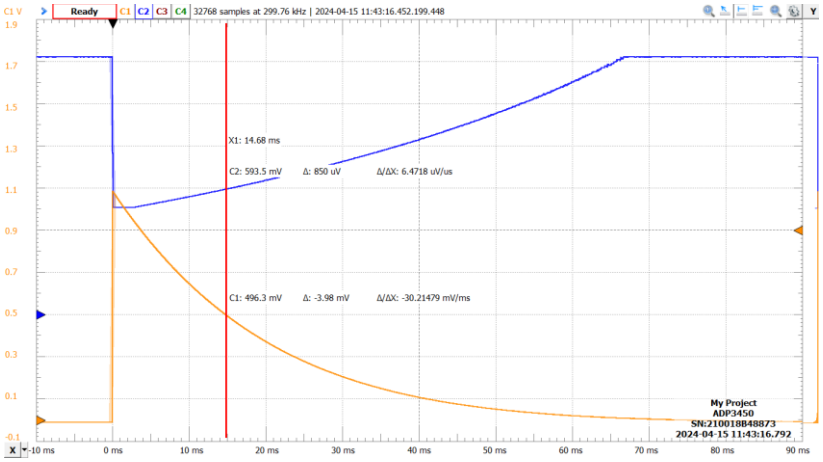

Figure 9. Thermistor results at 25 ˚C, cursor indication

7.2 Thermistor results at 65 ˚C

Channel 1 (yellow/top line) – PIN# 7 (IN) → Thermistor (NTC 10K/B3950 1%) signal.
Channel 2 (light blue/2nd line) – PIN# 12 (DAC_output) → DAC output

Calculation for operation 65 ˚C, Thermistor signal = 0.104 V; DAC output = 0.85 V
Measured result shows DAC output = 0.831 V

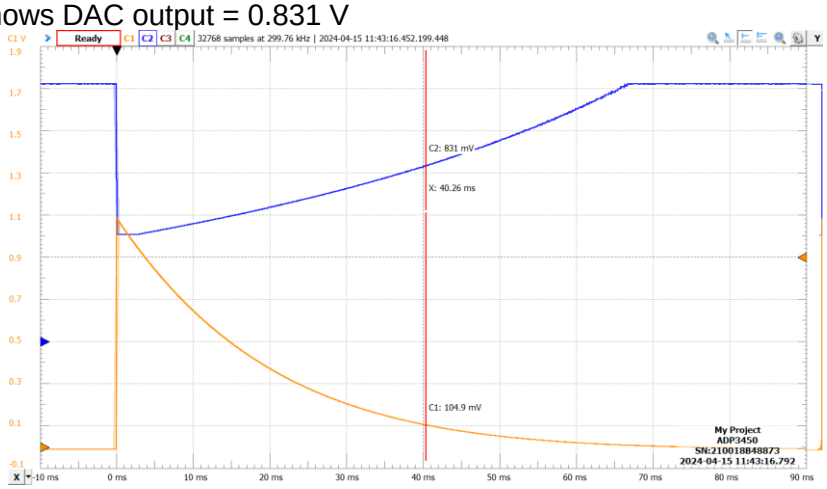

Figure 10. Thermistor results at 65 ˚C, cursor indication

7.3 Thermistor results at 100 ˚C

Channel 1 (yellow/top line) – PIN# 7 (IN) → Thermistor (NTC 10K/B3950 1%) signal.
Channel 2 (light blue/2nd line) – PIN# 12 (DAC_output) → DAC output

Calculation for operation 100 ˚C, Thermistor signal = 0.035 V; DAC output = 1.072 V
Measured result shows DAC output = 1.010 V

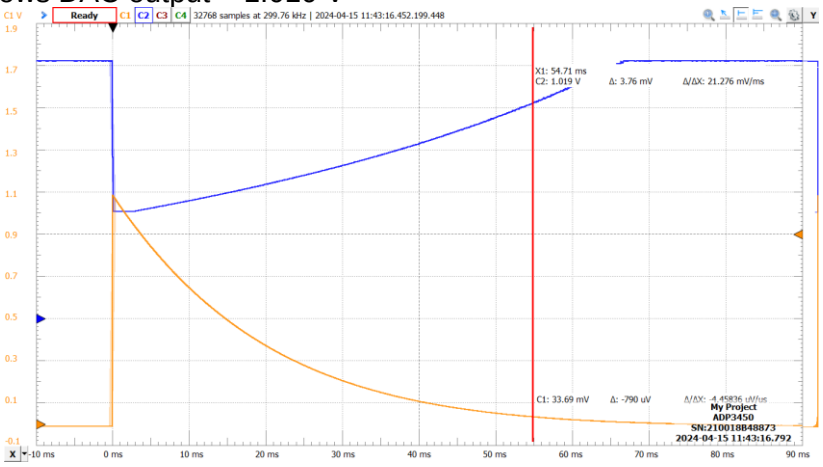

Figure 11. Thermistor results at 100 ˚C, cursor indication

8. Conclusion

The SLG47011 can be used to achieve thermistor linearization with proper design and configuration with the output verified between software simulation and hardware validation.

9. Revision History

Revision	Date	Description
1.00	November 5, 2024	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2025 Renesas Electronics Corporation. All rights reserved.