External Flash Interface
SLG47011

This application note describes the flash memory with the DataFlash interface, the features of the SLG47011 operation with this memory, and the expansion of the SLG47011 functionality due to multi-time programming. The application note is accompanied by design files, which can be found in the References section.

Contents

References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the .aap file [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas Electronics provides a complete library of application notes **Error! Reference source not found.** featuring design examples, as well as explanations of features and blocks within the Renesas IC.

[1] GreenPAK Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-395 External Flash Interface.aap, AnalogPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

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1. Introduction

One of the new members of the AnalogPAK family from Renesas is the SLG47011. It has a 14-bit four-channel ADC. The built-in calibration function performs PGA offset cancellation, and the Mathematical Core performs mathematical operations on measured signals. However, there are situations when it is necessary to trim certain parameters of individual SLG47011 blocks periodically. For this purpose, new values of the coefficients must be written. Since the SLG47011 is a one-time programmable IC, an external memory is needed to store these coefficients. The Renesas AT45DB081E ultra-low energy serial flash memory can be used as this external memory.

2. AT45DB081 Flash Memory Overview

The AT45DB081E uses the DataFlash interface – a low pin-count serial interface for flash memory, compatible with the SPI standard. This memory supports SPI modes 0 and 3. In mode 0: CPOL (clock polarity) = 0 and CPHA (clock phase) = 0; the clock default is low, with rising edge sampling and falling edge shifting out. In mode 3: CPOL = 1 and CPHA = 1; the clock default is high, with rising edge sampling and falling edge shifting out. The AT45DB081E contains two bidirectional buffers, accelerating the transferred data flow. These buffers act as an embedded pseudo-cache, allowing data to be accepted for writing during programming/erase operations.

Figure 1 shows a block diagram of the AT45DB081E.

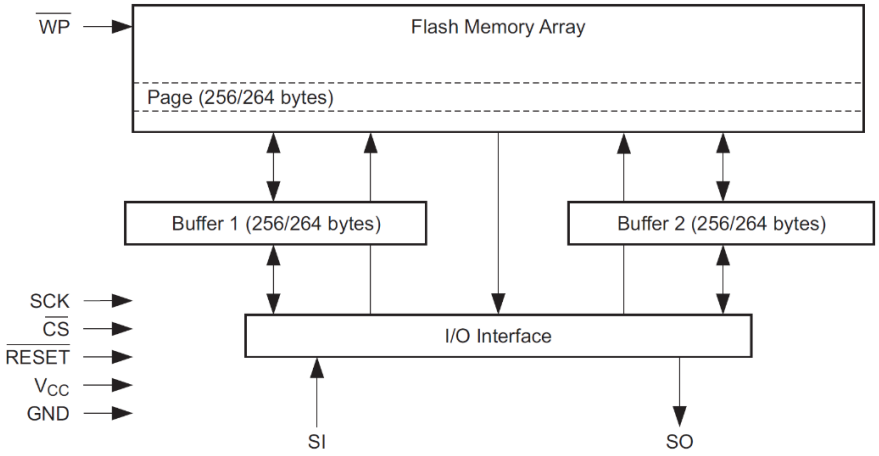


Figure 1. AT45DB081E Block Diagram

3. AnalogPAK Design

Thanks to the external flash memory, changing register data in the SLG47011 on the fly is possible. This allows, for example, to auto-trim parameters during operation. Figure 2 shows the general schematic of the external flash interface. This application note illustrates how to change a counter's data by loading values from external flash memory. This allows changing the frequency of the clock signal at the Pin 15 output.

Figure 3 shows the external flash interface design in the Go Configure Software Hub. By default, CNT11/DLY11 data equals 10000, and with a 10 MHz OSC1 signal at its CLK input, it outputs a 1 kHz clock signal to Pin 15. When the button is pressed for the first time, the new value of CNT11/DLY11 data is read from the external flash memory, and in this case, its data is set to 5000, and the frequency of the signal on Pin 15 is set to 2 kHz. Pressing the button a second time causes the next CNT11/DLY11 data value to be read from the next pages of the external flash memory. In this case, CNT11/DLY11 data changes to 2500, and the frequency of the signal on Pin 15 is set to 4 kHz.

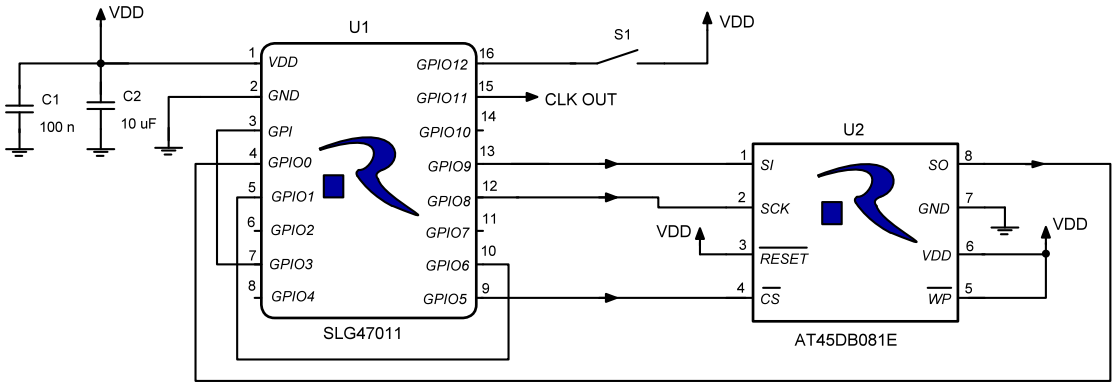


Figure 2. General Schematic of External Flash Interface

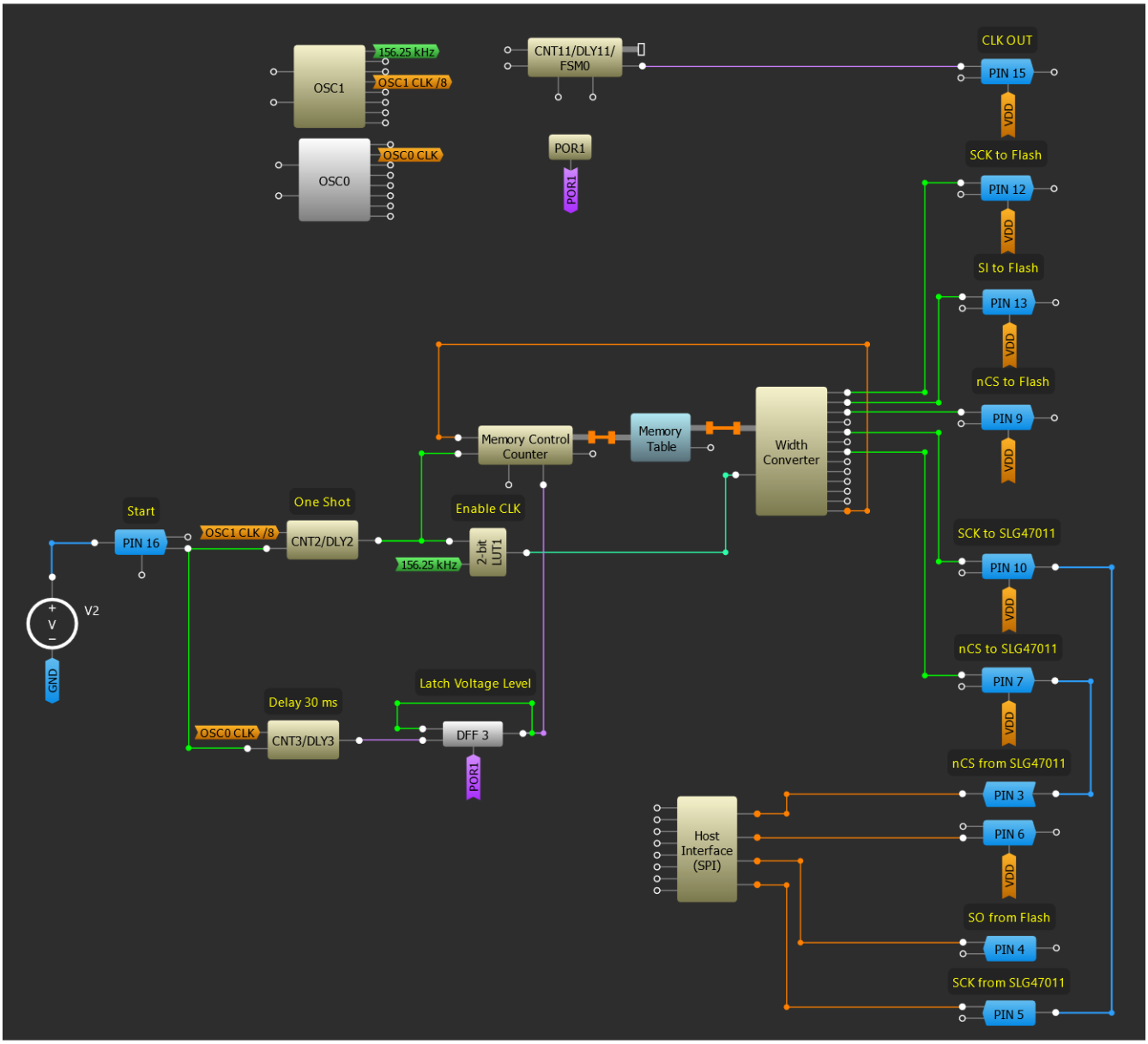


Figure 3. AnalogPAK Design Schematic for Reading from Flash and Rewriting CNT11/DLY11 Data

The SLG47011 Memory Table is set as the SPI master. The Memory Table has a feature to save and load data in XML, CSV, and .txt formats. In this project, data is stored in CSV format. To work with these files, it is

necessary to navigate to the Memory Table Editor and select the Manual Editor option. Subsequently, a window appears, allowing for the import and export of files (see Figure 4).

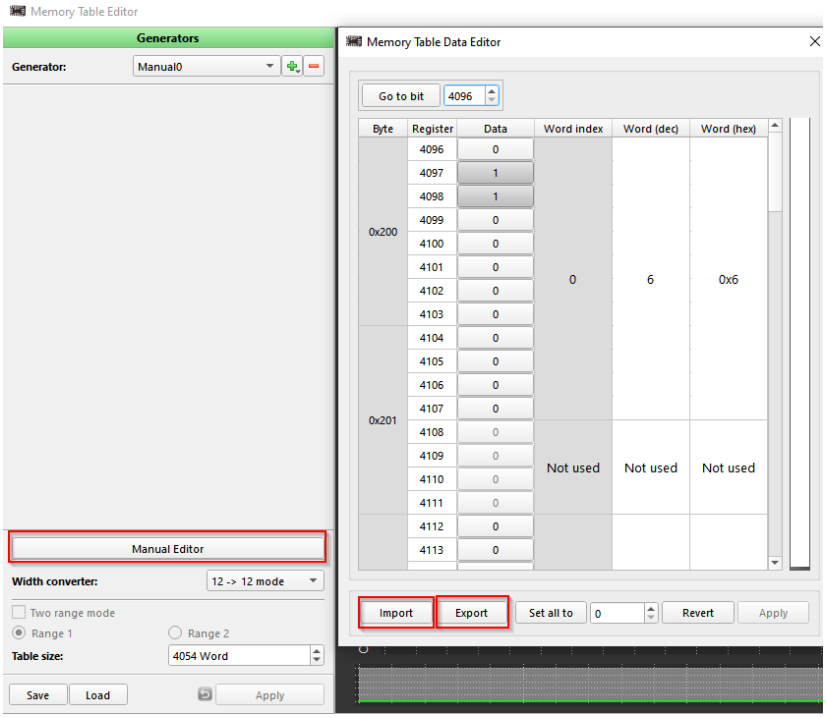


Figure 4. AnalogPAK Design Settings Windows to Import/Export Files

The Memory Control Counter controls the input address of the Memory Table. Width Converter provides data from the Memory Table macrocell to the connection matrix.

The register data rewriting process starts with a HIGH-level signal on Pin 16. CNT2/DLY2 operates as a One Shot and sets the necessary time to transfer 375 words from the Memory Table. This is the size of the data transmitted via the SPI protocol and is required to change the CNT11/DLY11 data. Since the Memory Control Counter frequency is 156.25 kHz, the One Shot data time is calculated as (1/156250) x 375 = 2.4 ms. 2-bit LUT1 enables the clock for the Width Converter at the HIGH level of the One Shot output. To eliminate switch bouncing, a Delay macrocell CNT3/DLY3 is used. DFF3 provides the ability to switch between two Memory Control Counter ranges by changing the signal level at its Range input. In this project, two ranges were used for convenient switching between the necessary data. This allows reading one of the two pre-recorded CNT11/DLY11 data values depending on whether the button was pressed an even or odd number of times.

3.1 Read Data from External Flash

Before starting to read from or write to the flash memory, it is important to determine which page size version the current flash memory uses. Since AT45DB memory ICs exist with binary page sizes and DataFlash standard page sizes, a data frame should be formed accordingly. The page size can be found by reading the status register. This project uses a memory IC with a page size of 256 bytes, which is a power of two.

To implement data reading using SPI, the SLG47011 Memory Table has a Generator tool that allows the configuration of SPI data transfer. For reading data from the flash, the SLG47011 SPI master is set to mode 0 with the following settings: CS polarity – idle HIGH, MOSI initial state – HIGH, and a pause of one CLK between transmitted bytes.

To read data from the flash Main Memory Page Read command is used. Figure 5 shows a timing diagram for this command. This command allows the user to read data directly from any of the 4096 pages in the main memory, bypassing both data buffers and leaving their contents unchanged.

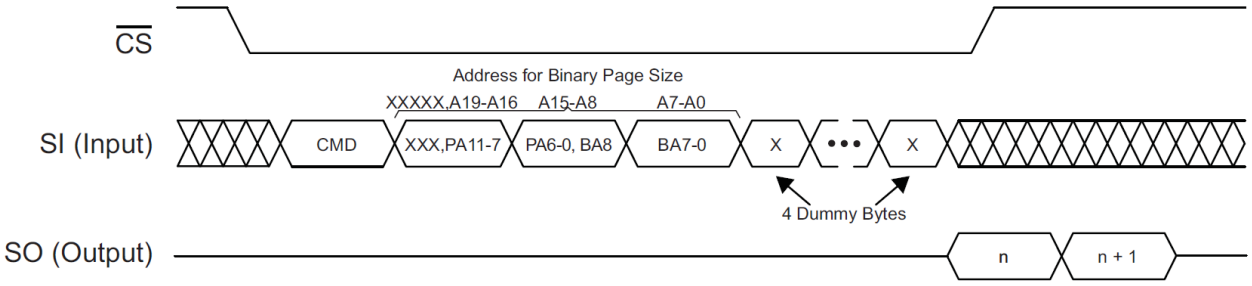


Figure 5. Main Memory Page Read. Timing Diagram

To start a page read from the binary page size (256 bytes), the opcode 0xD2 must be clocked into the device, followed by three address bytes and four “don’t care” bytes. The first 12 bits (A19 - A8) of the 20-bit sequence specify which page of the main memory array to read, and the last eight bits (A7 - A0) of the 20-bit address sequence specify the starting byte address within the page. The “don’t care” bytes that follow the address bytes are sent to initialize the read operation. Following the “don’t care” bytes, additional pulses on SCK (serial clock) result in data being output on the SO (serial output) pin. The nCS (chip select) pin must remain low during the loading of the opcode, the address bytes, the “don’t care” bytes, and the reading of data. A low-to-high transition on the CS pin terminates the read operation and tri-states the output pin (SO).

As CNT11/DLY11 is 16-bit and its counter data are located in two bytes, but the SLG47011 allows writing only one byte of data in one data frame, so LSB and MSB bytes should be sent separately. Figure 6 shows the timing diagram of reading the register address and register data for CNT11/DLY11 from flash to the CNT11/DLY11 data register.

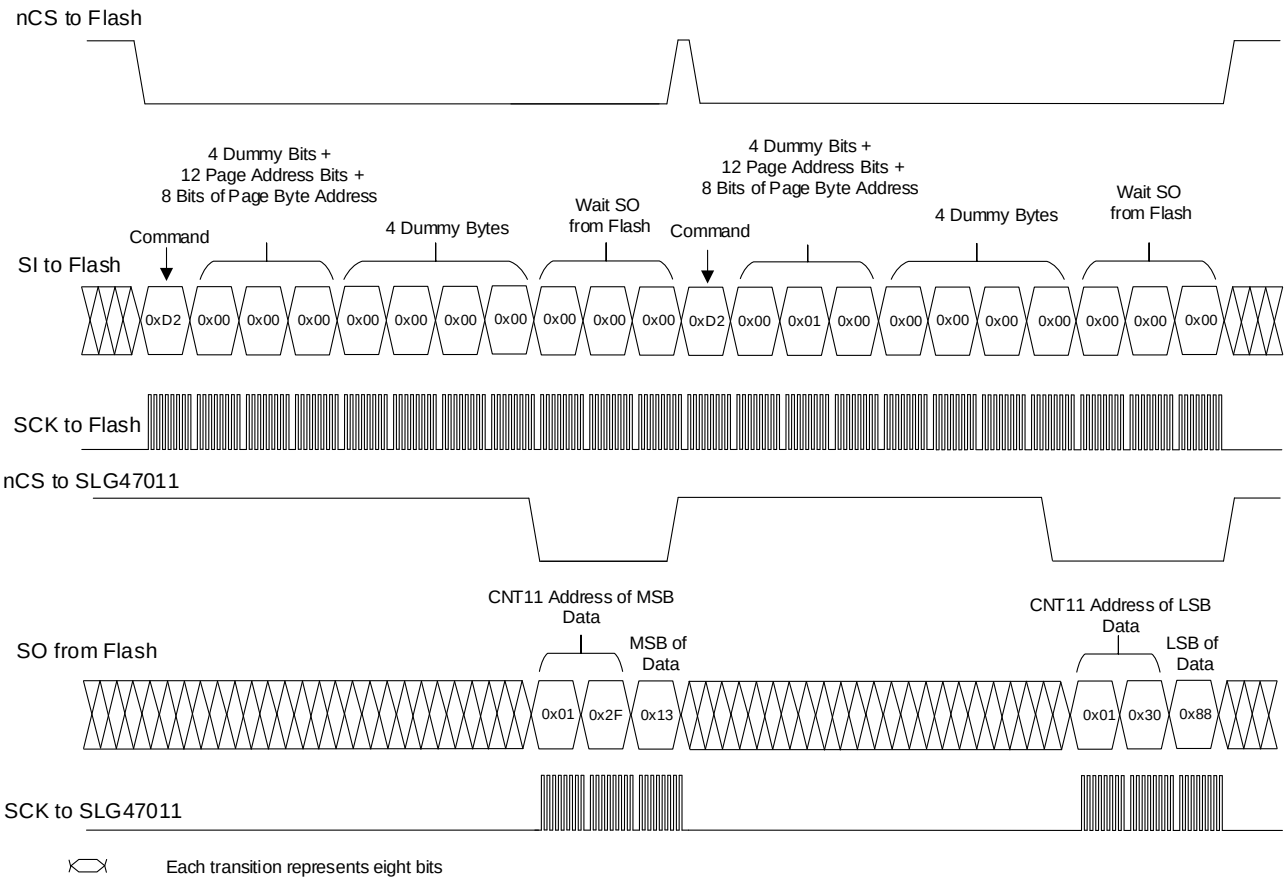


Figure 6. Timing Diagram for Reading Data from Flash and Rewriting CNT11/DLY11 Data for 2 kHz OUT

SLG47011 sends signals to read data on lines nCS, SCK, and SI to flash and simultaneously it controls lines SCK and nCS on its Host Interface. Thanks to this control, data from the memory is received via the line MOSI (on Pin 4) on the Host Interface. Since this data contains the CNT11/DLY11 counter register address and data intended for this register, the contents of the register are overwritten, and the CNT11/DLY11 outputs a clock signal with a frequency of 2 kHz.

Looking into the details, when the nCS signal goes LOW, a clock signal is sent to SCK and data to the SO output. Firstly, the read command 0xD2 is sent, followed by the address 0x00 for the zero page, and then four dummy bytes. After that, the SLG47011 doesn't send data but instead, the flash sends at first two bytes, which consist of the register's address of CNT11/DLY11 MSB data – 0x12F. Then, the memory sends the next byte – 0x13. This data is an MSB byte of CNT11/DLY11 data. The transmission ends with a HIGH level at the nCS output.

Next, the LSB of the CNT11/DLY11 data byte is read on the LOW signal on the nCS line. The same read command 0xD2 is sent, following the first page's address 0x01 and four dummy bytes. After that SLG47011 stops sending data but instead the flash sends two bytes which consist of the register address of CNT11/DLY11 LSB data – 0x130. Then it sends register data – 0x88.

For a 2 kHz clock output, CNT11/DLY11 data must be equal to 5000, which in the binary system is equal to 00010011 10001000. In hexadecimal, the MSB is 0x13 and the LSB is 0x88, as mentioned above.

When there is a need to switch to 4 kHz mode with the button, the reading process is similar, except that the data is read from pages two and three, and the content of these pages is different. Specifically, for a 4 kHz output, CNT11/DLY11 data must be equal to 2500, which in the binary system is equal to 00001001 11000100. In hexadecimal, the MSB is 0x09 and the LSB is 0xC4. Figure 7 shows the process of reading the register address and register data for CNT11/DLY11 from flash to the CNT11/DLY11 data register to achieve a 4 kHz CNT11/DLY11 output.

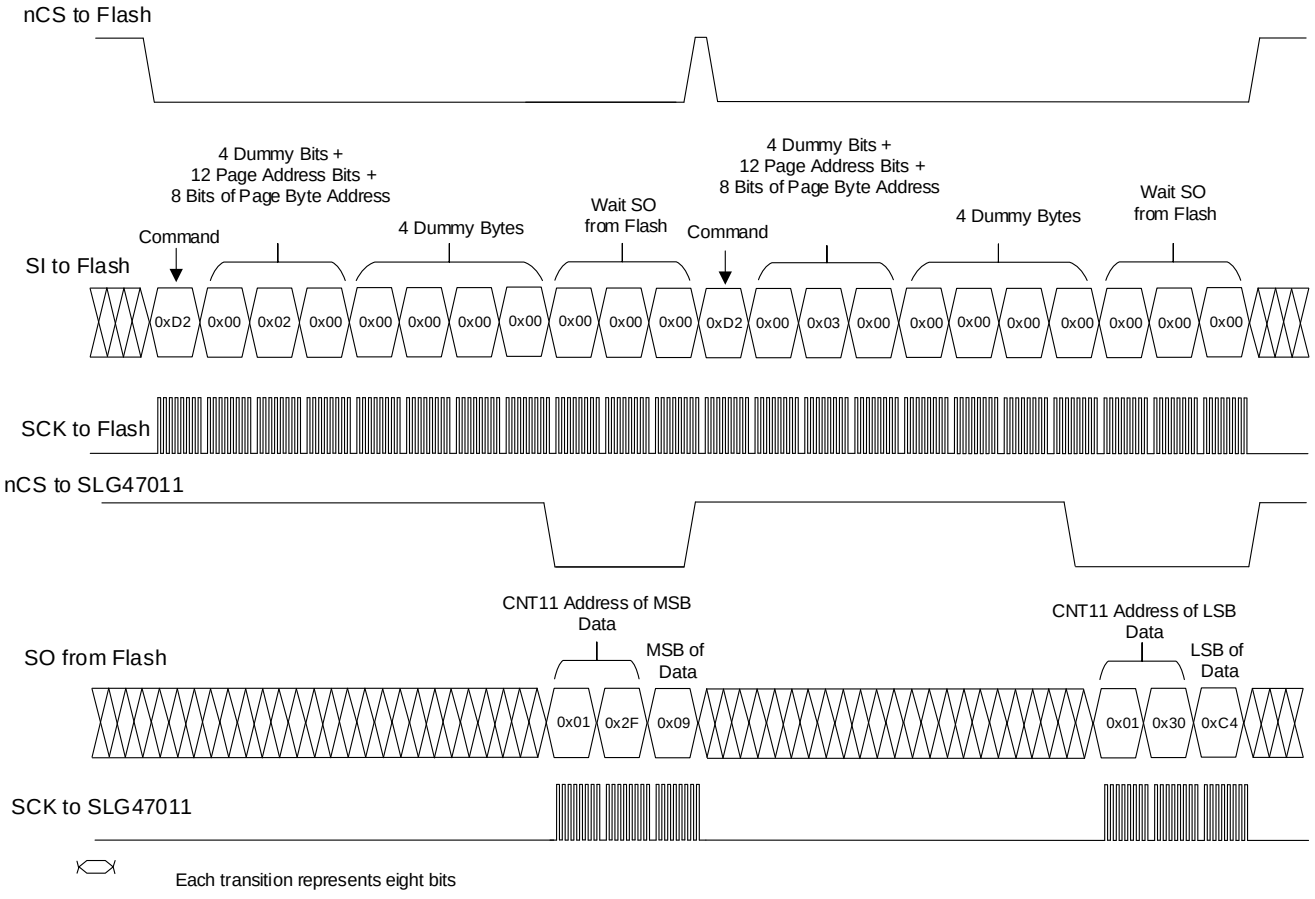


Figure 7. Timing Diagram for Reading Data from Flash and Rewriting CNT11/DLY11 Data for 4 kHz OOT

Figure 8 shows waveforms for reading data from flash memory and rewriting CNT11/DLY11 data.

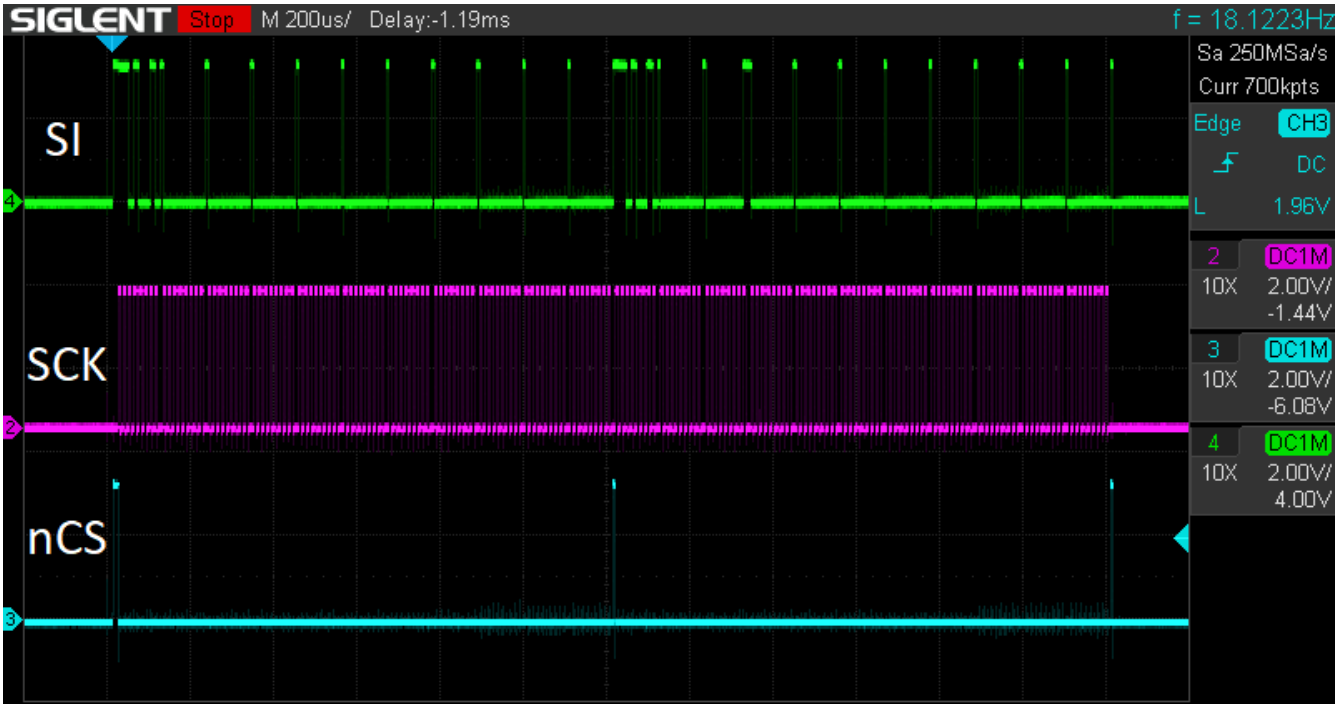
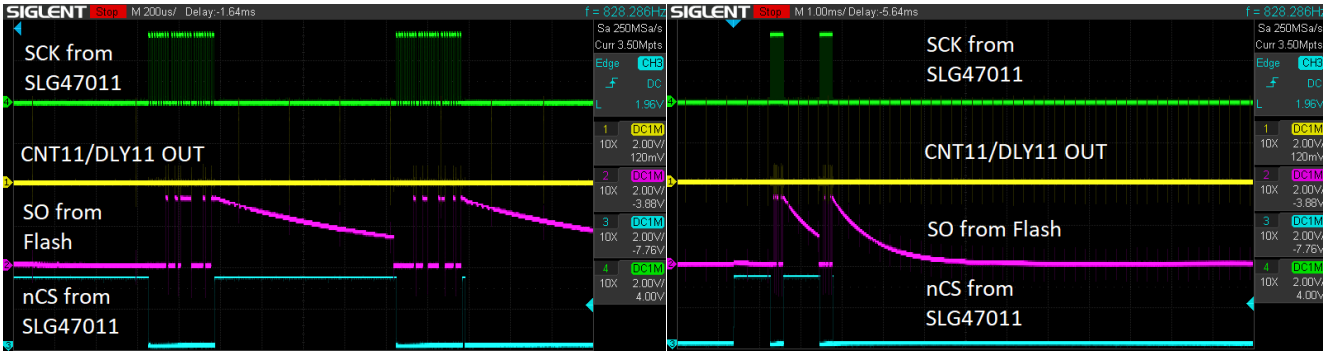


Figure 8. Waveforms for Reading Data from Flash and Rewriting CNT11/DLY11 Data for 2 kHz Output

Figure 9 shows waveforms for SLG47011 control signals, the SO signal from flash, and the CNT11/DLY11 output signal, which changes its frequency after receiving data from memory.



a) b)

Figure 9. Waveforms on SLG47011 Host Interface INs and CNT11/DLY11 OUT: a) Zoomed; b) not Zoomed

3.2 Program Flash with Trim Data

Initially, the SLG47011 should be used to write default coefficients to the flash. Later, at the adjustment stage, a customer could overwrite them.

DataFlash interface offers a couple of ways to program the flash memory. In this application note, a sequence of commands is used: Buffer Write and Buffer Main Memory Page Program with Built-In Erase (see Figure 10 and Figure 11).

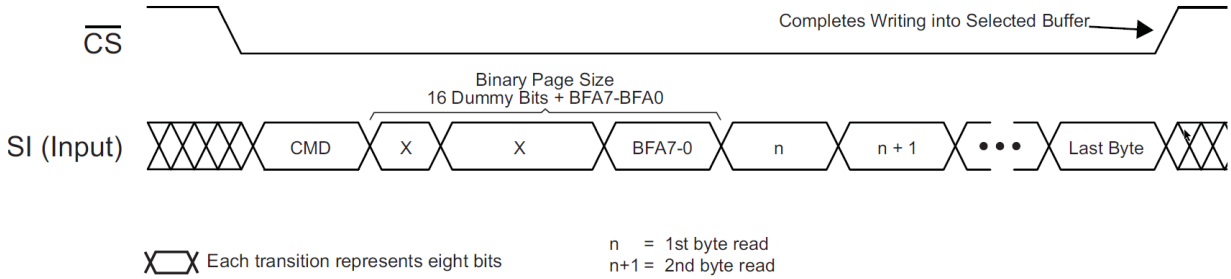


Figure 10. Buffer Write. Timing Diagram

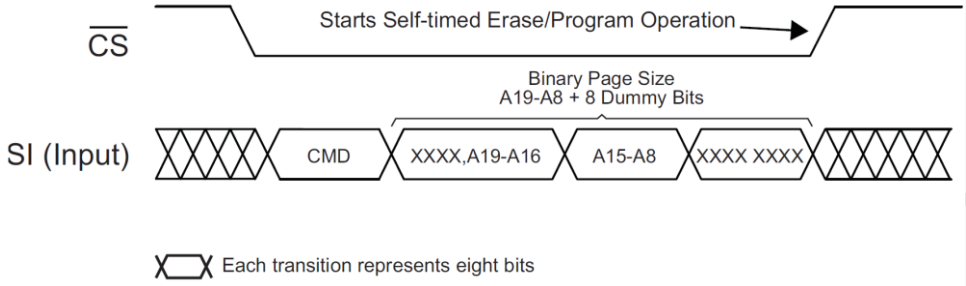


Figure 11. Buffer Main Memory Page Program with Built-In Erase. Timing Diagram

Figure 12 shows the AnalogPAK Design Schematic for writing from the SLG47011 to the flash.

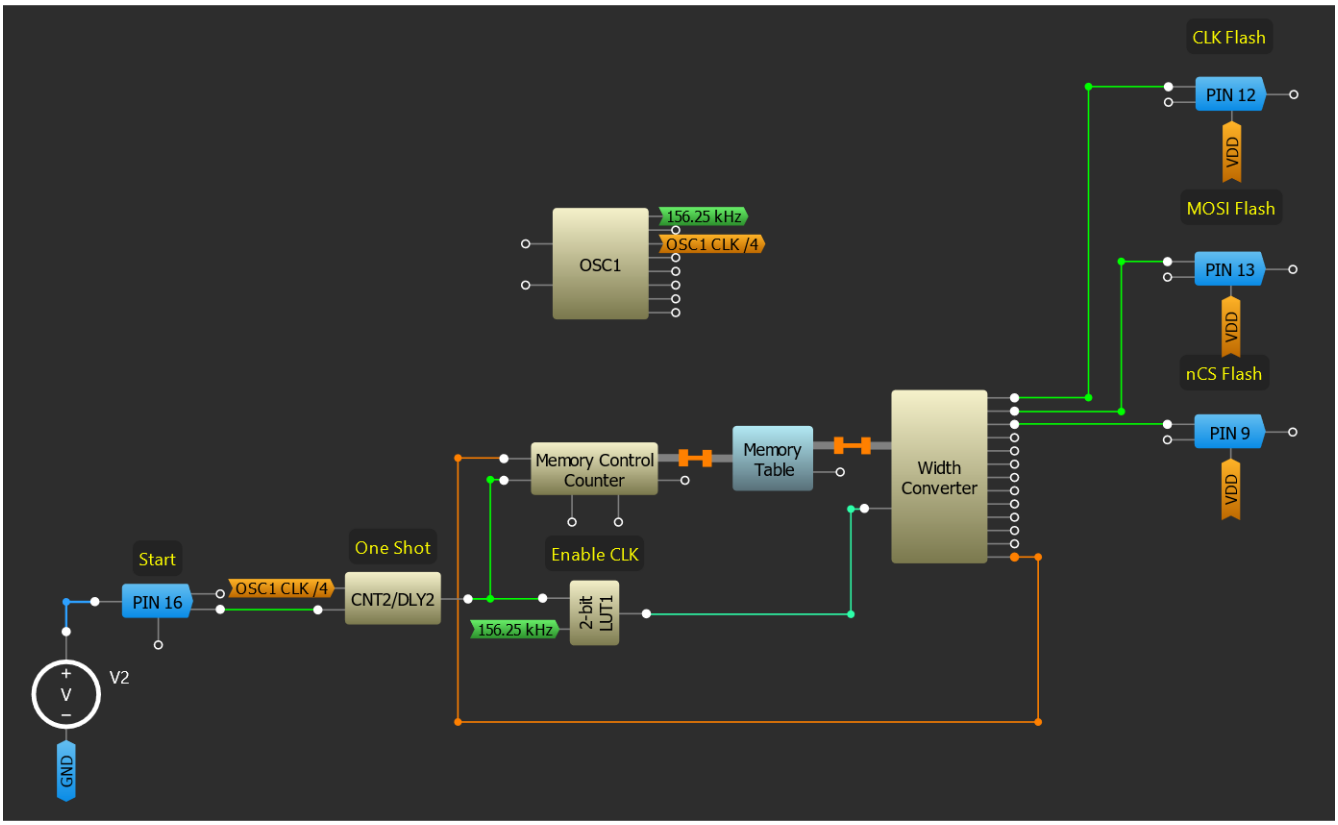


Figure 12. AnalogPAK Design Schematic for Programming Flash

The writing process starts with a HIGH-level signal on Pin 16. CNT2/DLY2 operates as a One Shot and sets the necessary time to transfer 4054 words of data from the Memory Table. 2-bit LUT1 enables the clock for the Width Converter at the HIGH level of the One Shot output.

The SLG47011 SPI Generator tool from Memory Table is used to implement writing data. In this case, the SLG47011 SPI master is set to mode 0 with the following settings: CS polarity – idle HIGH, MOSI initial state – HIGH, and pauses between transmitted bytes of one CLK are also applied.

As the data from the flash memory is intended to be written to the SLG47011, therefore it is necessary to write the data in a format suitable for SLG47011 registers beforehand. Figure 13 shows how to write configuration register 8-bit data to the SLG47011 via SPI. Since CNT11/DLY11 is 16-bit and its counter data are located in two bytes, but the SLG47011 allows writing only one byte of data in one data frame, so the LSB and MSB bytes should be sent separately.

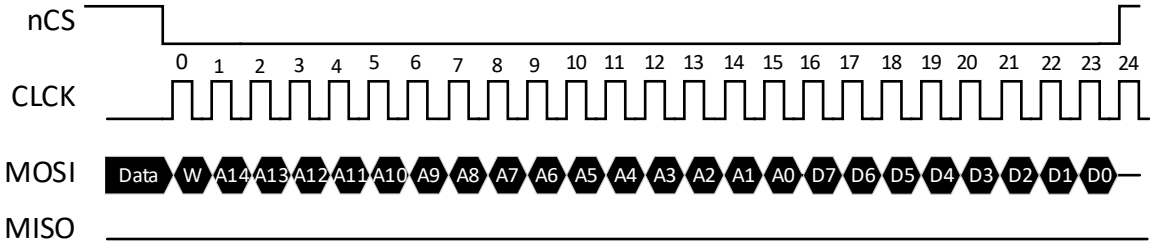


Figure 13. Timing Diagram for Writing Configuration Register 8-bit Data to SLG47011 via SPI

Since CNT11/DLY11 MSB and LSB bytes are transmitted separately, there is a need to add a delay between transfers because according to the flash memory datasheet, the erase and programming of the page should take place in a maximum of 50 ms. In this case, this delay was set to 96 ms. Figure 14 shows the general timing diagram for writing data to the flash memory and Figure 15 shows the waveforms to write CNT11/DLY11 register data into the flash memory.

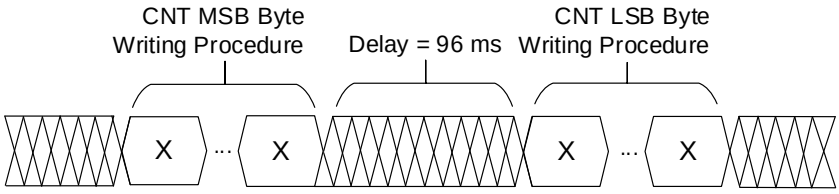


Figure 14. Basic Timing Diagram for Writing Counter Register Data into Flash Memory

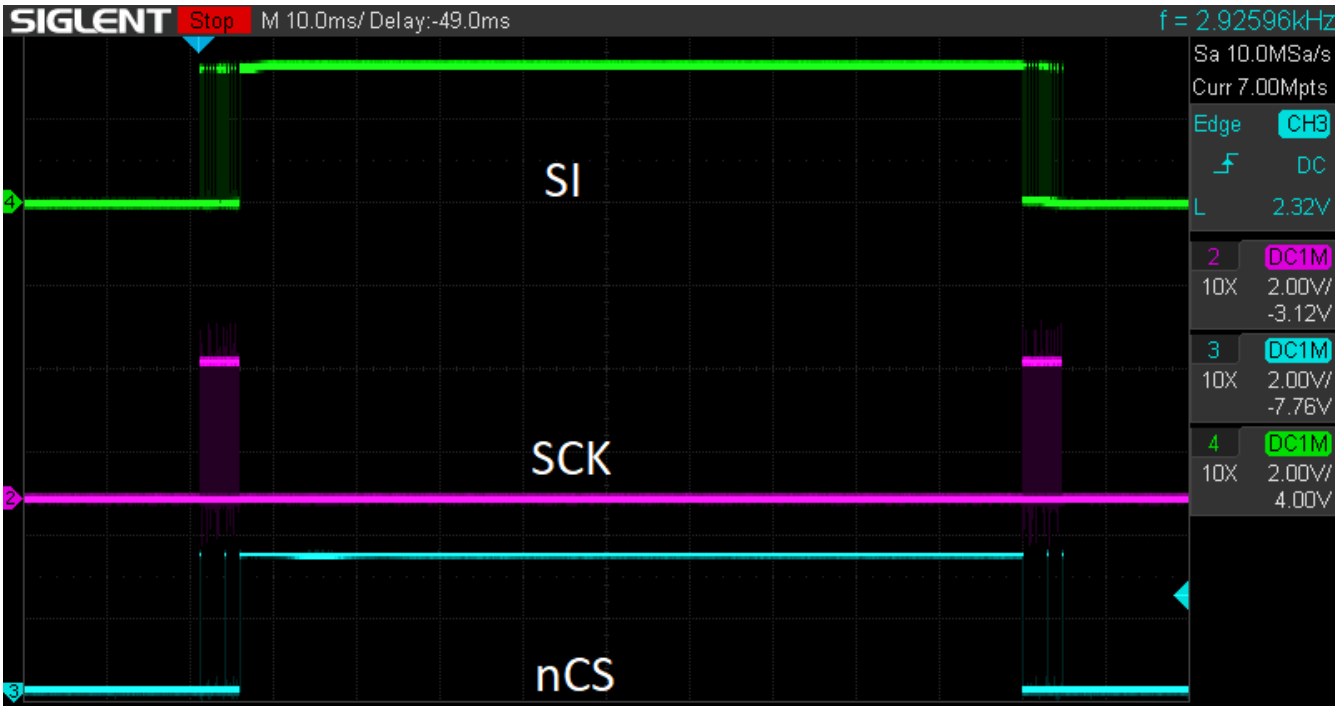


Figure 15. Waveforms for Writing CNT11/DLY11 Register Data into Flash Memory for 2 kHz OUT

According to Figure 10, to load data into a buffer, an opcode of 0x84 must be clocked into the device followed by 16 dummy bits and eight buffer address bits (in this case 0x00). After the last address byte has been clocked into the device, data can be clocked in on subsequent clock cycles. The first 16 bits of data contain the CNT11/DLY11 MSB data register address – 0x12F and the following 8-bit data itself – 0x13. Figure 16 shows the timing diagram to write the MSB byte of CNT11/DLY11.

To perform a buffer to main memory page program with built-in erase, an opcode of 0x83 must be clocked into the device followed by three address bytes comprised of four dummy bytes, 12 page's address bits that specify the page in the memory to be written, and eight dummy bits. When a low-to-high transition occurs on the nCS pin, the device first erases the selected page in the main memory and then programs the data stored in the appropriate buffer in that same page in the main memory. In this case, the data is written to the 0th page of the memory. Figure 17 shows the waveforms to write the CNT11/DLY11 register MSB data into flash memory.

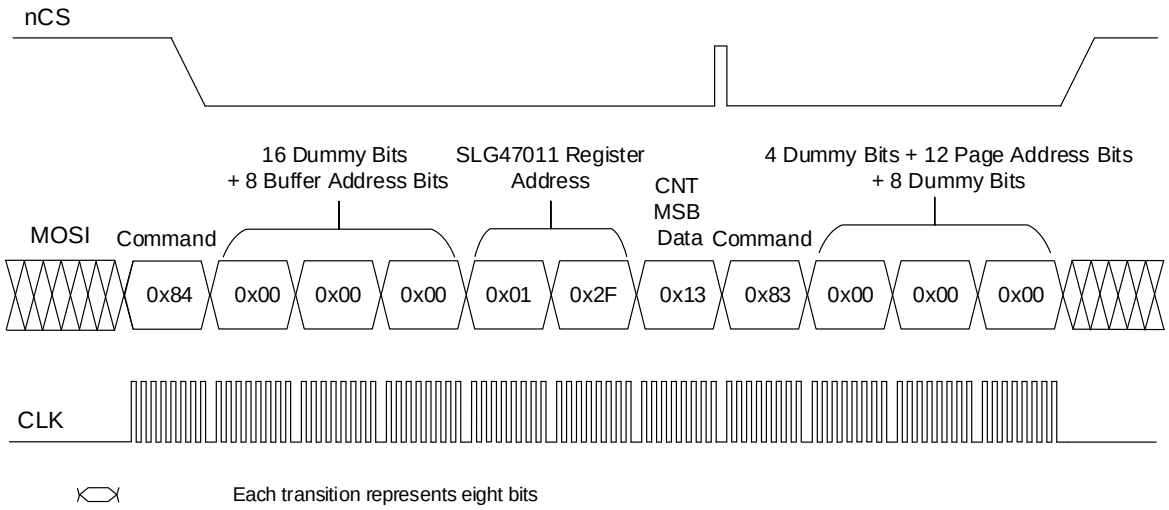


Figure 16. Timing Diagram for Writing CNT11/DLY11 Register MSB Data into Flash Memory for 2 kHz OUT

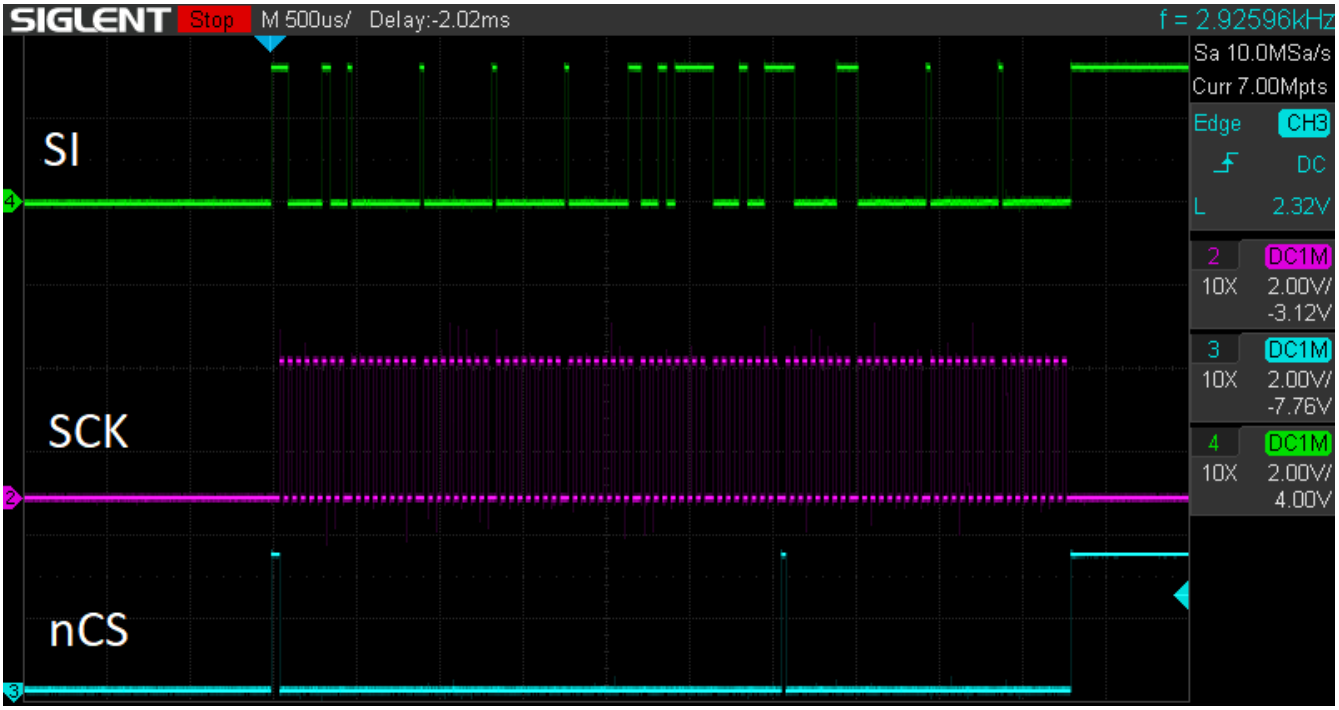


Figure 17. Waveforms for Writing CNT11/DLY11 Register MSB Data into Flash Memory for 2 kHz OUT

Writing the counter LSB byte is similar, except that the data is written to page one, and the first 16 bits of data contain the CNT11/DLY11 LSB data register address – 0x130, and 8-bit represents its data – 0x88. Figure 18 and Figure 19 show the timing diagram and waveform for writing the LSB byte of CNT11/DLY11 data.

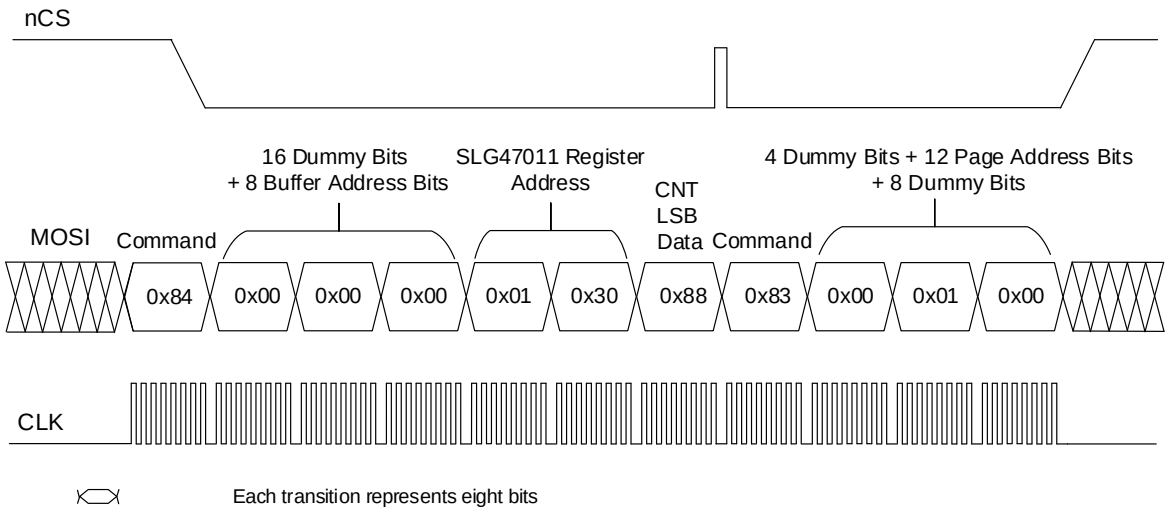


Figure 18. Timing Diagram for Writing CNT11/DLY11 Register LSB Data into Flash Memory for 2 kHz Output

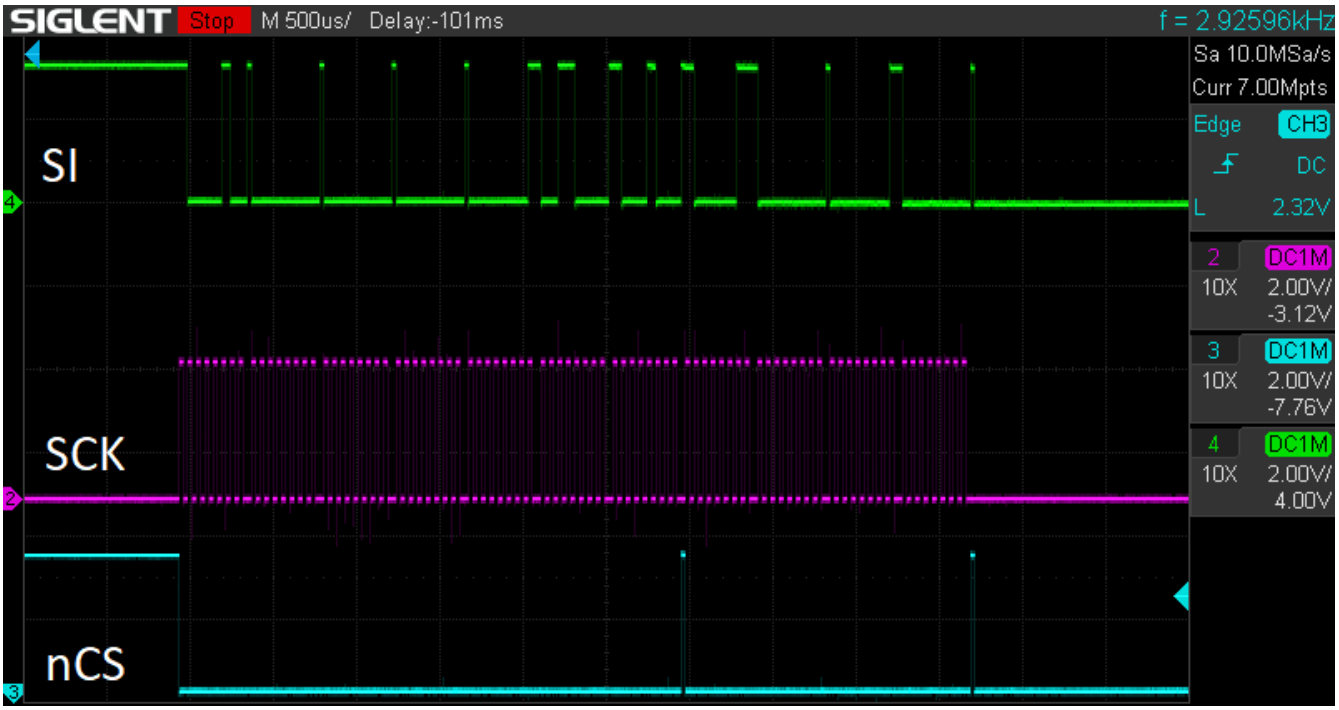


Figure 19. Waveforms for Writing CNT11/DLY11 Register LSB Data into Flash Memory for 2 kHz OUT

In order to have three modes of operation for the counter: default – 1 kHz, 2 kHz, and 4 kHz, there is a need to write additional data into the flash memory for the 4 kHz output mode. For this purpose, a separate CSV file was created in the Memory Table Generator, which is designed to write counter MSB and LSB data in the third and fourth memory pages, respectively. In this case, the written data is as follows: CNT11/DLY11 MSB data register address – 0x12F and its data – 0x09, CNT11/DLY11 LSB data register address – 0x130 and its data – 0xC4.

Figure 20 and Figure 21 show the timing diagram and waveforms for writing the MSB byte of CNT11/DLY11 data.

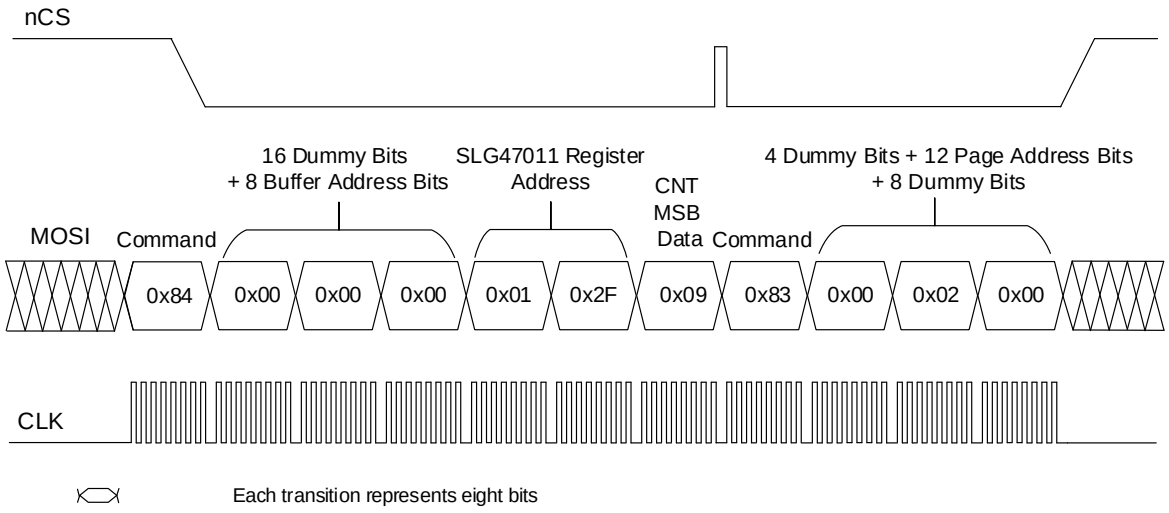


Figure 20. Timing Diagram for Writing CNT11/DLY11 Register MSB Data into Flash Memory for 4 kHz Output

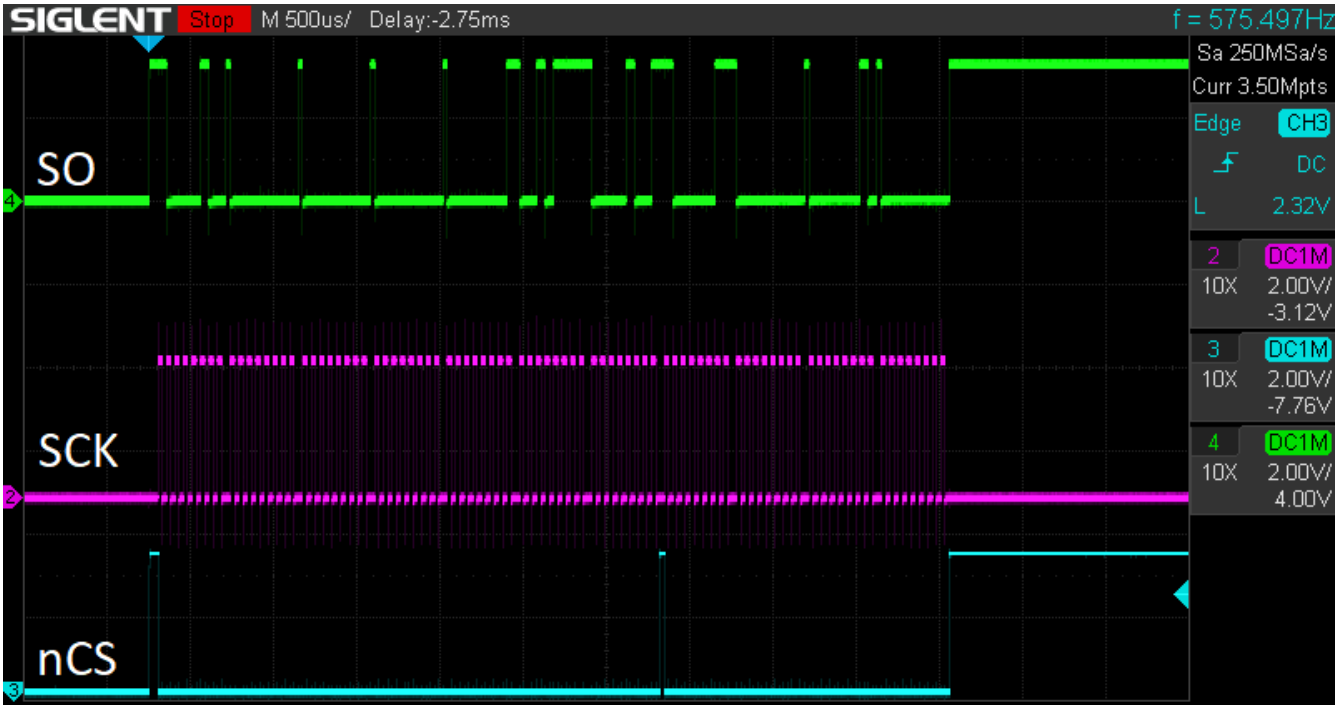


Figure 21. Waveforms for Writing CNT11/DLY11 Register MSB Data into Flash Memory for 4 kHz OUT

Figure 22 and Figure 23 show the timing diagram and waveforms to write the LSB byte of CNT11/DLY11 data.

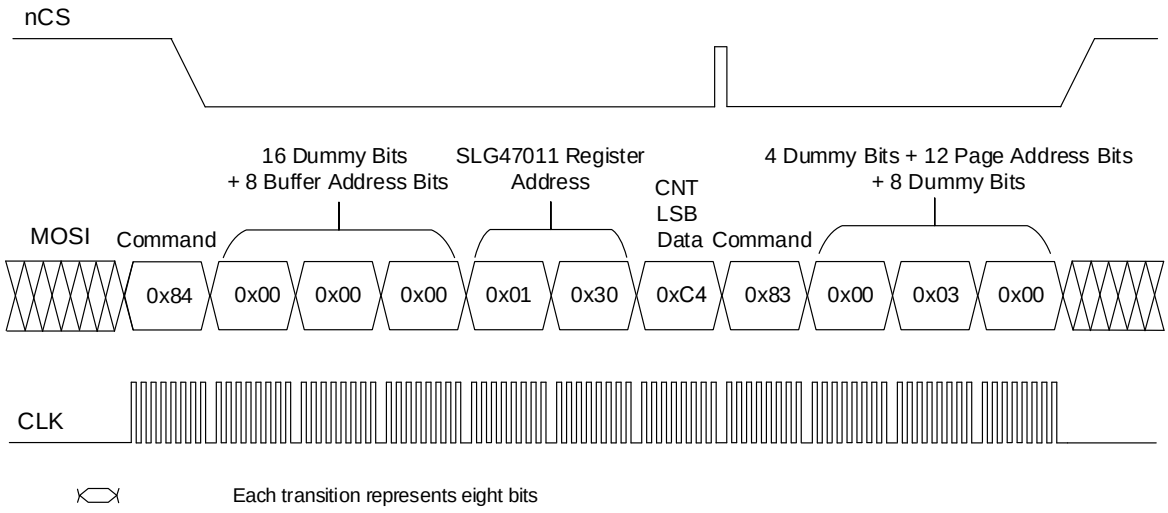


Figure 22. Timing Diagram for Writing CNT11/DLY11 Register LSB Data into Flash Memory for 4 kHz OUT

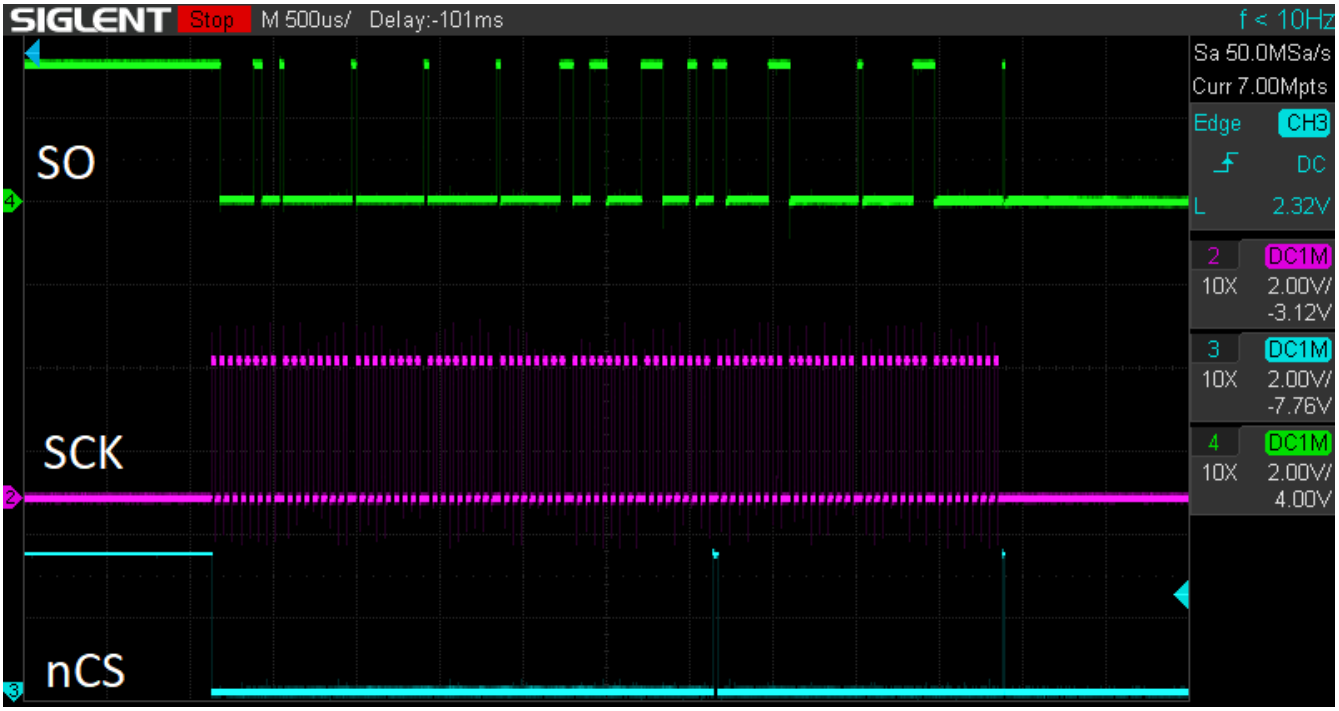


Figure 23. Waveforms for Writing CNT11/DLY11 Register LSB Data into Flash Memory for 4 kHz Output

4. Project Simulation

The GreenPAK Designer (Go Configure Software hub) has a built-in simulation tool that allows users to evaluate the design functionality even without a development board. Figure 24 shows the simulation waveforms for reading data from memory and rewriting CNT11/DLY11 data. Figure 25 shows simulation waveforms for writing the CNT11/DLY11 register data into the flash memory.

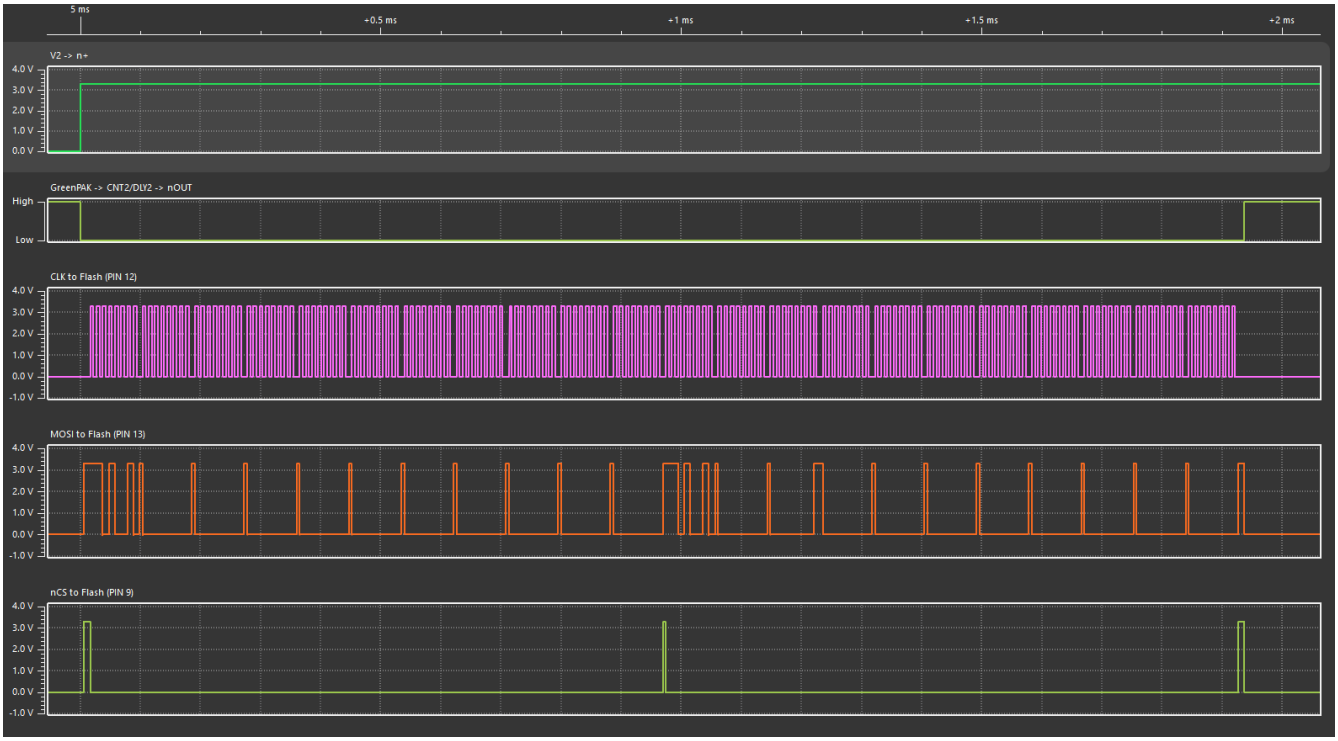


Figure 24. Simulation Waveform to Read Data from Flash and Rewrite CNT11/DLY11 Data for 2 kHz OUT

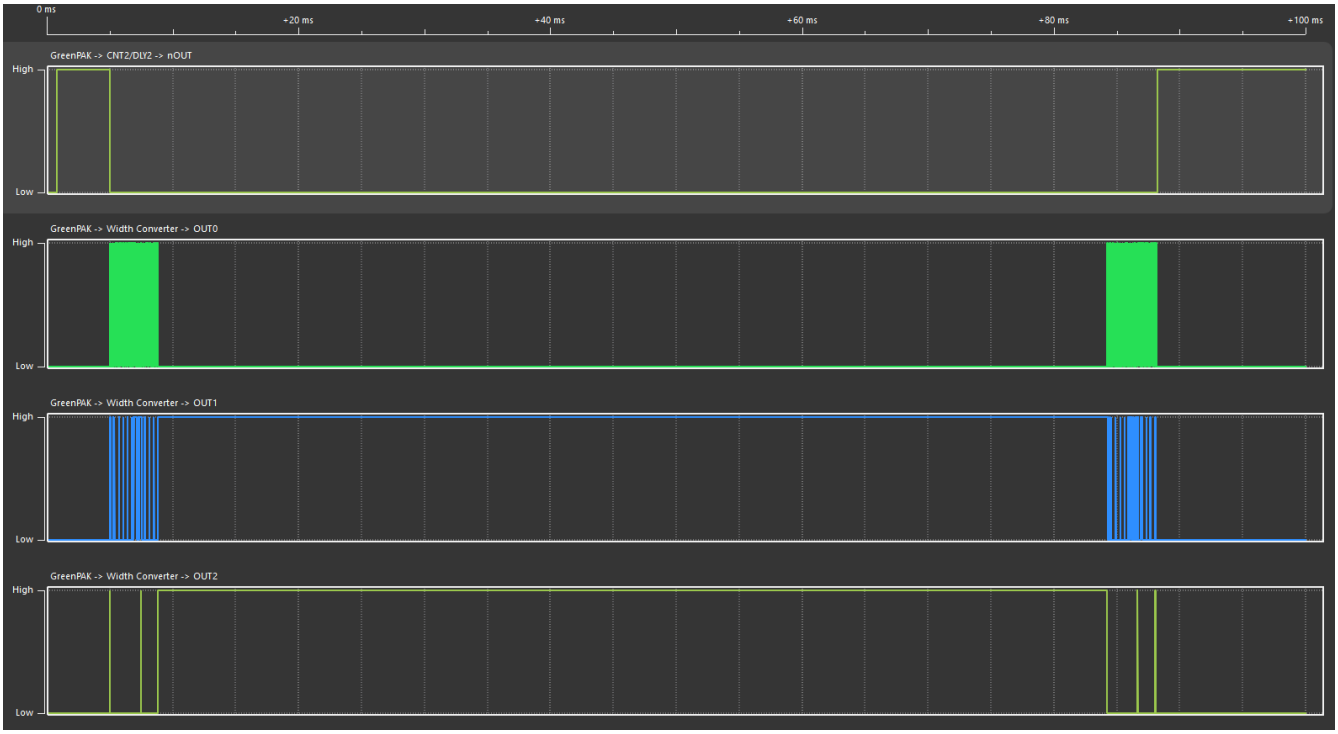


Figure 25. Simulation Waveform to Write CNT11/DLY11 Register Data into Flash Memory for 2 kHz OUT

5. Conclusions

This application note demonstrates using the SLG47011 to interface with external flash memory. The external memory expands the functionality of the SLG47011, transforming it from a one-time programmable to a multi-time programmable device. This functionality, in turn, enables the reprogramming of registers and the implementation of trimming specific parameters during the operation of the device. Furthermore, the SLG47011 is cost-effective and energy-efficient, featuring a compact package size of 2.0 mm x 2.0 mm.

6. Revision History

Revision	Date	Description
1.00	Sep 24, 2024	Initial release.

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