SLG47011 PGA Explained
SLG47011

This application note explains in depth how to use a Programmable Gain Amplifier (PGA) within the SLG47011 IC with real-life application examples.

The IC is equipped with the PGA, 14-bit ADC, analog Temp Sensor, Data Buffers, Memory Table, MathCore, and a huge amount of different macrocells (LUTs, DFFs, DLY/CNTs, etc). But in this document, only PGA and PGA-related macrocells will be described.

The application note comes complete with a design file that can be found in the References section.

Contents

1. Terms and Definitions

ADC	Analog-to-Digital Converter
CNT/DLY	Counter-Delay
DAC	Digital-to-Analog Converter
IC	Integrated Circuit
I2C	Inter-Integrated Circuit Protocol
MUX	Multiplexer
OSC	Oscillator
PGA	Programable Gain Amplifier

SAR	Successive-approximation-register
SCL	Signal Clock
SDA	Signal DataReferences

2. References

For related documents and software, please visit:

AnalogPAK™ | Renesas

Download our free Go Configure Software Hub [1] to open the *.aap files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Renesas provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC.

[1] Go Configure Software Hub, Software Download and User Guide, Renesas Electronics

[2] AN-CM-393 PGA Explained, GreenPAK Design File, Renesas Electronics

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Renesas Electronics

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Renesas Electronics

Author: Nazar Sliunchenko, Technical Documentation Manager, Renesas Electronics

3. Introduction

A Programmable Gain Amplifier is a component often used in conjunction with an Analog-to-Digital Converter (ADC) to adjust the input signal level before it is converted into a digital representation.

Key functions:

- **Signal Amplification**: The PGA can amplify the analog signal coming from the external source. This is useful when the input signal is weak and needs to be boosted before it can be accurately digitized by the ADC.
- **Signal Buffering**: In addition to amplification, the PGA can act as a buffer for the input signal. This means it can isolate the ADC from the source of the input signal, providing impedance matching and ensuring that the ADC sees a consistent and stable input voltage regardless of variations in the source impedance. By acting as a buffer, the PGA helps to minimize loading effects on the input signal, improving the overall accuracy and linearity of the ADC's performance. Additionally, it helps to prevent any potential interference or distortion caused by the ADC's input circuitry, ensuring that the digitized signal faithfully represents the original analog input.
- **Adjustable Gain**: One of the key features of a PGA is that it allows for adjustable gain. This means that the level of amplification can be controlled or programmed according to the requirements of the application. Different situations may call for different levels of amplification, and the PGA provides the flexibility to accommodate these variations.
- **Precision and Accuracy**: By using a PGA, you can maintain precision and accuracy in the digitization process. It allows you to tailor the amplification level to optimize the signal-to-noise ratio (SNR) and dynamic range, ensuring that the converted digital signal retains as much fidelity to the original analog signal as possible.
- **Dynamic Range Optimization**: The ability to adjust the gain also helps in optimizing the dynamic range of the ADC. Dynamic range refers to the range between the smallest and largest values of a signal that

can be accurately measured. By adjusting the gain dynamically, the PGA can help ensure that the entire range of the ADC is effectively utilized, maximizing the resolution and accuracy of the digitized signal.

In summary, a Programmable Gain Amplifier in an ADC system, see Figure 1, provides flexibility in adjusting the amplification level of the input signal before it undergoes analog-to-digital conversion. This helps in optimizing the accuracy, precision, and dynamic range of the digitized signal, making it a valuable component in many measurement and sensing applications.

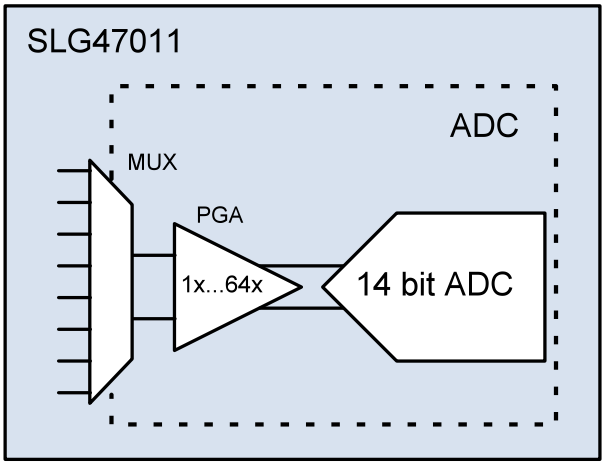


Figure 1: Simplified ADC System Structure

4. PGA Modes

Programmable Gain Amplifier macrocell of the SLG47011 allows to amplify small signals or to interface the load with a high output impedance. PGA has a 3-bit gain selection. Possible gain settings are: PGA bypass, 1x, 2x, 4x, 8x, 16x, 32x, 64x. It has rail-to-rail input and output. It is possible, although not recommended, to bypass the PGA and measure signals directly with ADC.

PGA has eight modes (see Table 1 and Figure 2), that share three input type categories:

- **Single-ended**: with IN- connected to the ground, $Vout = Gain \times V+$
- **Differential**: gain is applied to the difference between IN+ and IN- with an offset of $\frac{\text{ADC\_Vref}}{2}$. For example, output is $\frac{\text{ADC\_Vref}}{2}$ when input voltage difference is zero. IN+ can be above or below IN-. $Vout = Gain \times (V+ - V-) + \frac{\text{ADC\_Vref}}{2}$.
- **Pseudo-differential** (mode 4 only): gain is applied to the difference between IN+ and IN- with no offset. Output is 0 V when input difference is zero. The operating range assumes IN+ is always above IN-. $Vout = Gain \times (V+ - V-)$

Table 1. PGA/ADC Input/Output Modes

Mode	PGA In/Out Configuration		ADC in Configuration	Description
	Input	Output		
1a	Bypass	Bypass	Differential	ADC operates in differential mode
1b	Bypass	Bypass	Single-ended	ADC operates in single-ended mode
2	Single-ended	Single-ended	Single-ended	High input impedance non-inverting single-ended amplifier

3	Differential	Differential	Differential	Instrumentation amplifier with common mode voltage limits and high input impedance
4	Pseudo-Differential	Single-ended	Single-ended	Pseudo-differential amplifier with low input impedance and extended common mode voltage
5a	Differential	Single-ended	Single-ended	Differential amplifier with low input impedance and $\frac{\text{ADC\_Vref}}{2}$ reference voltage and single-ended output
5b	Differential	Differential	Differential	Differential amplifier with low input impedance and $\frac{\text{ADC\_Vref}}{2}$ reference voltage and differential output
6	Buffer	Buffer	Single-ended	ADC operates in single-ended mode

PGA can be used separately as a standalone amplifier with the single-ended or differential output connected to the PIN13 and PIN14. The output current of PGA is low. Thus a high-impedance load should be applied. When the PGA is powered down and its output is routed to external pins, the PGA output is in a Hi-Z state.

When the PGA power-up signal is LOW or the PGA is turned off by the register, bypass switches pass analog signal from input MUXs to the ADC, so the signal can be sampled without the need to power the PGA.

PGA has individual power-up signal that can be controlled either independently or along with ADC.

PGA output can be also connected to the analog comparator’s non-inverting input.

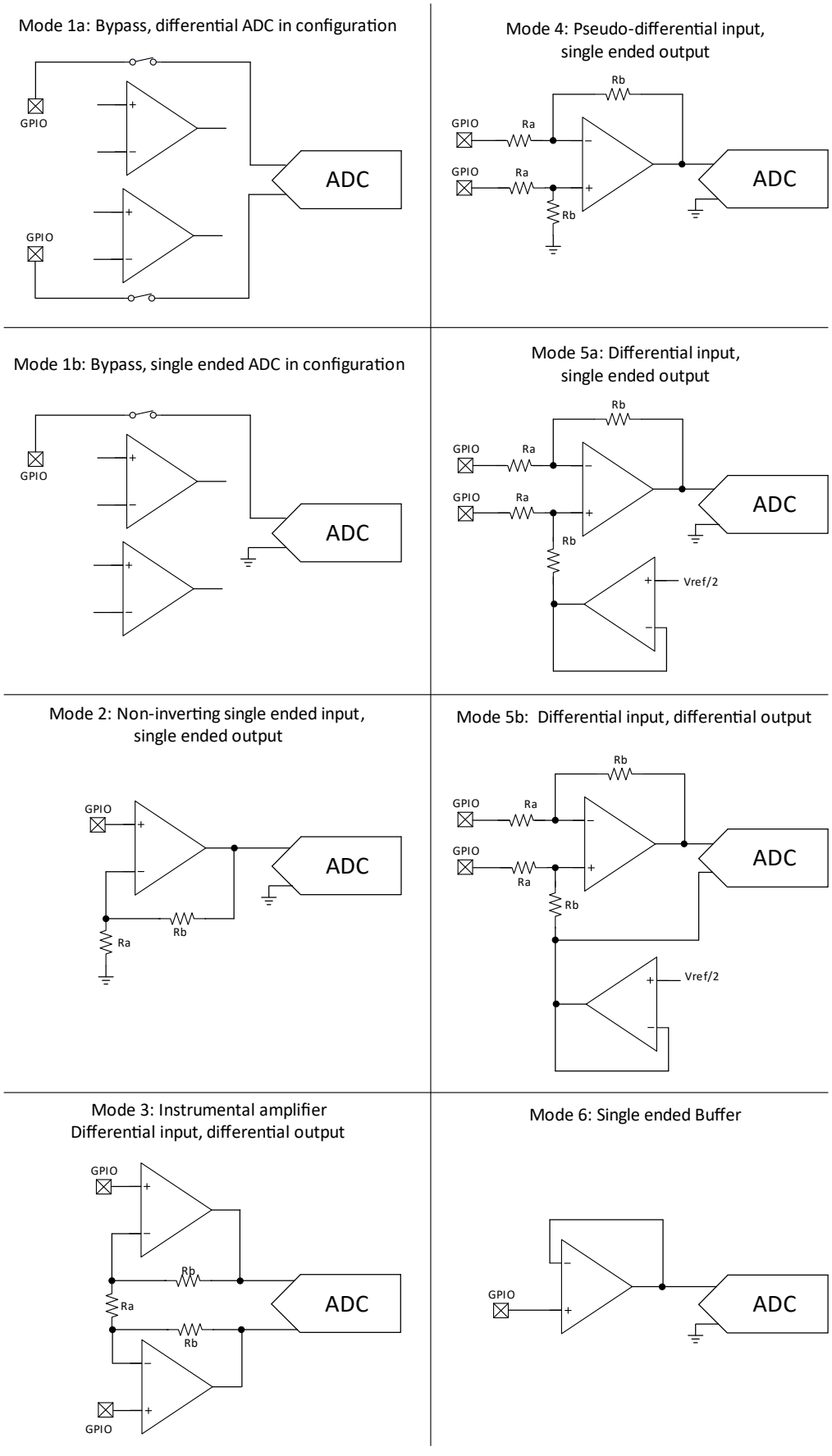


Figure 2: PGA Configuration Modes

5. PGA Settings

All PGA (or any other macrocell) settings are done using the Go Configure software.

Wright after starting, select by double click the SLG47011V part number. On the right panel (Components) find and tick on the PGA box in the Analog Components group. The PGA will appear and if the cursor is placed on it, all inputs/outputs will be shown, see Figure 3.

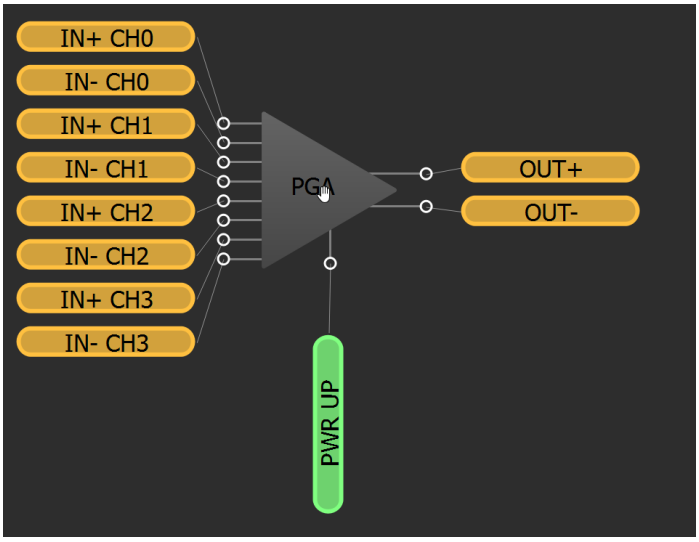


Figure 3: PGA, Go Configure Screenshot

The right-side panel (Properties) allows configuring the PGA. It is divided into five parts for general settings and settings for each channel individually, see Table 2, Table 3, and Figure 4.

Table 2. PGA General Configuration

Setting	
OUT+ to PIN13	Disable/Enable
OUT- to PIN14	Disable/Enable
PGA/ADC manual mode enable	Disable/Enable
Manual channel selection	• Cannel 0 • Cannel 1 • Cannel 2 • Cannel 3

Table 3. PGA Channels Configuration

Setting	Channel 0, 1, 2, 3		
Input mode	Disable	Differential input	Single-ended input
Mode	PGA bypass	• PGA bypass • Instrumental amp. • Differential amp. • Vref/2 biased diff amp, s/e	• Non-inverting amp • Buffer

		• Vref/2 biased diff amp, diff	
Gain	1x	1x, 2x, 4x, 8x, 16x, 32x, 64x	
IN+ source	• PIN7 (GPIO3) • PIN8 (GPIO4) • PIN9 (GPIO5) • PIN10 (GPIO6) • Vref ACMP • Temp Sensor • VDD (PIN1) • GND (PIN2)		
IN- source	• PIN11 (GPIO7) • PIN12 (GPIO8) • AGND		

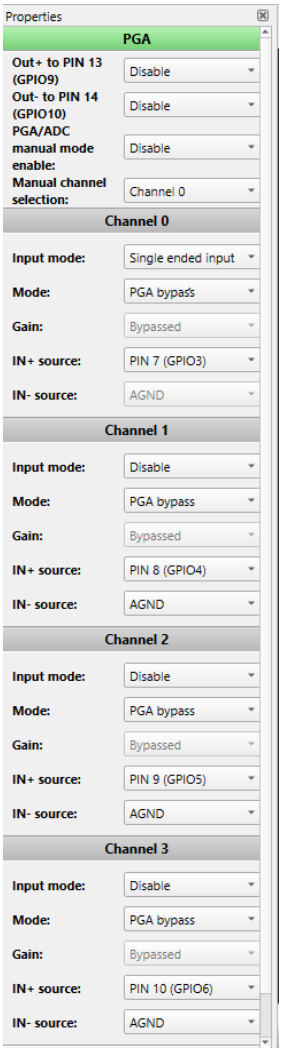


Figure 4: PGA Properties, Go Configure Screenshot

6. Design Example

Figure 5 shows a simple design of a four-channel ADC. It has two single-ended (gain 1x and 2x) inputs as well as two differential (gain 4x and 8x) including an instrumentation amplifier. Each ADC channel sends its data to

the corresponding Data Buffer set to Moving Average mode, where data is averaged and can be read via I2C or processed by other macrocells within the IC. It should be noted that like all analog macrocells PGA and ADC have a POWER UP input where logic 1 must be applied to power them up. Depending on the application, the power-up signal can be dynamically ON/OFF to save power, but in this case, a POR1 signal is used. It provides a logic 1 to the POWER UP inputs ensuring correct macrocell start up.

6.1 ADC settings

By left-clicking on the ADC, we can enter the ADC Properties side panel. It also includes settings for every channel the same as in the PGA side panel, see Figure 4, so no need to configure channels again. See Figure 6 for the ADC Properties side panel. Almost all settings can be left by default, but to increase ADC accuracy and overall performance, some changes should be made. Such as:

- Sample per channel – 8
- Delay between channels – 1000
- Delay between channels predivider – 8

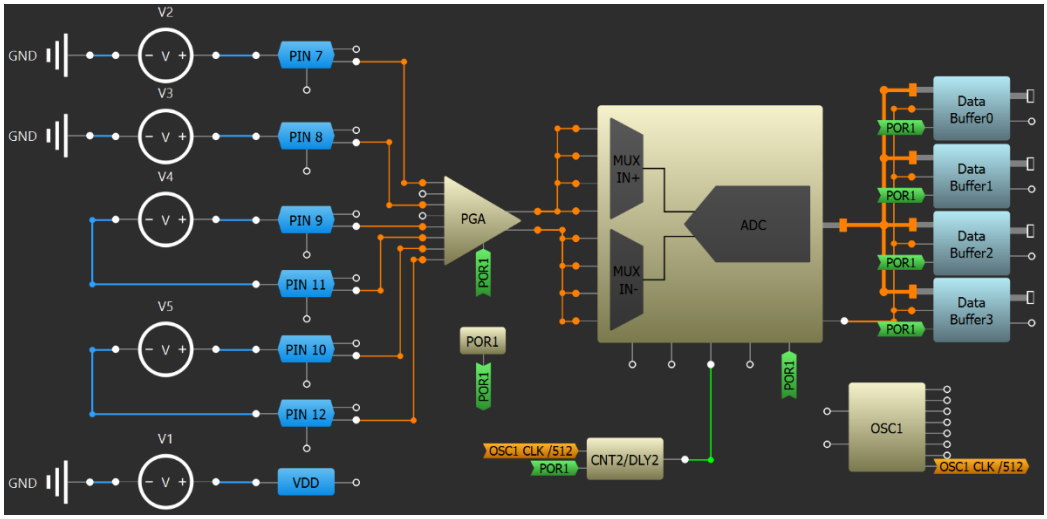


Figure 5: Design Example

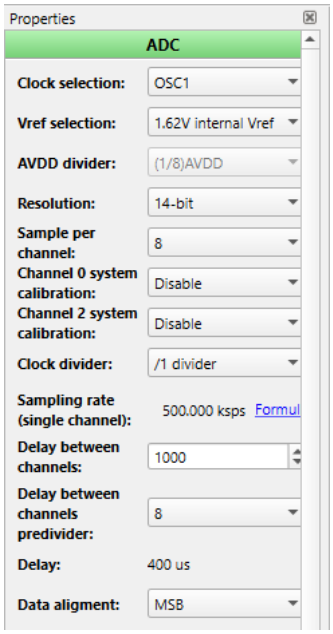


Figure 6: ADC Properties, Go Configure Screenshot

Also, in order for ADC proper start up, a delayed power on signal on the Conversion start input must be applied. For this purpose, CNT2/DLY2 is used. It is set to a Delay mode, counter data 390 (10 ms), Rising edge, Clock source – OSC1/512. Delay input connected to POR1.

6.2 Data Buffers Settings

All four data buffers are used to average the data coming from each ADC channel. The Go Configure software allows reading the data directly without an external I2C master device. Note that to start buffering a power-up signal must be applied to the Load EN input of every Data Buffer, in this case POR1. See Figure 6 for the settings of each Data Buffer.

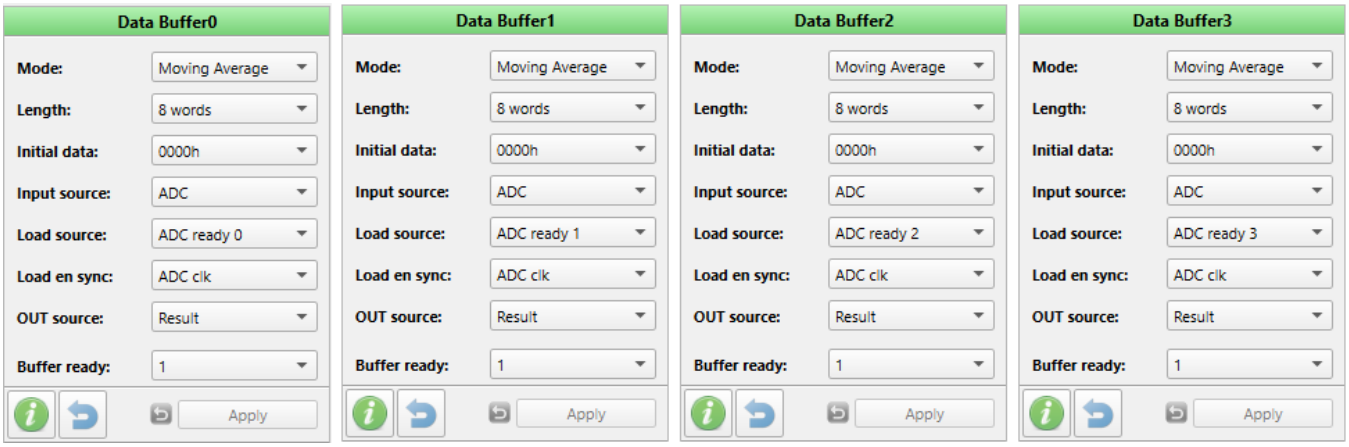


Figure 7: Data Buffers Properties, Go Configure Screenshot

6.3 Running Simulation

The Go Configure software, among other features, allows the simulation of the project. To do that, the virtual voltage sources V1 through V5 must be set to voltages as shown in Figure 8. Additionally, V1 must start with a at least 1 ms ramp.

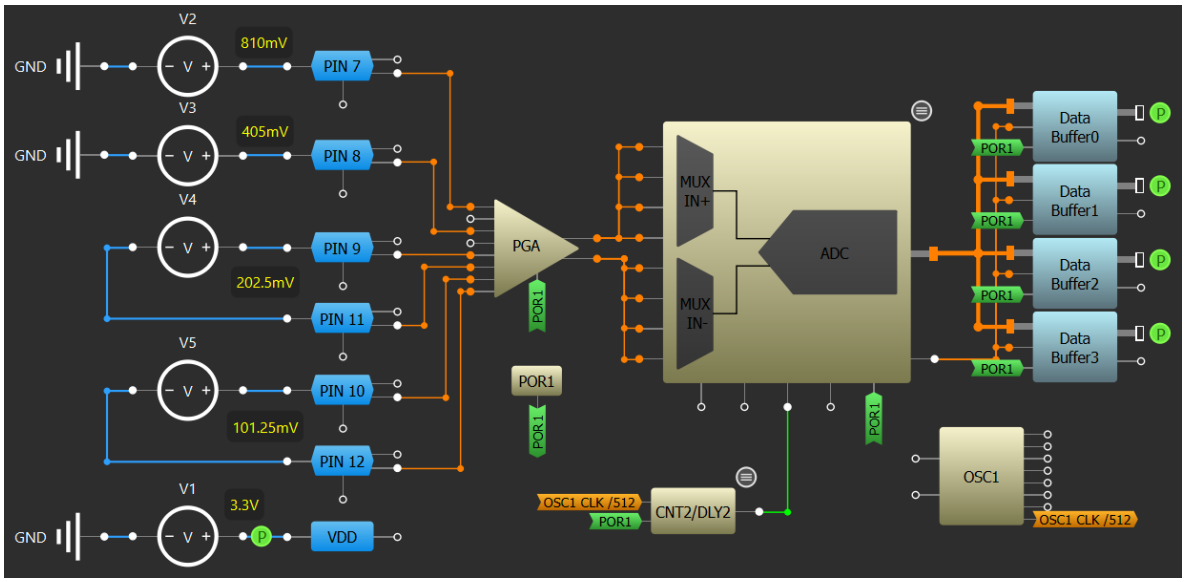


Figure 8: Project Modification for Simulation, Go Configure Screenshot

To be able to see the simulation result, probes must be added to V1 and every Data Buffer output. Since conversion starts after a 10 ms delay, the simulation Ending time should be at least 20 ms, Maximum time step – 400 us. For the simulation result see Figure 9. As can be seen, the conversion starts after 10 ms as expected. Also, we can observe an averaging process of the Data Buffers. Each Data Buffer output is presented as a step-

like line consisting of 8 steps showing an average of 8 words. So, the correct output data should be considered after at least 8 words or 20 ms in this case.

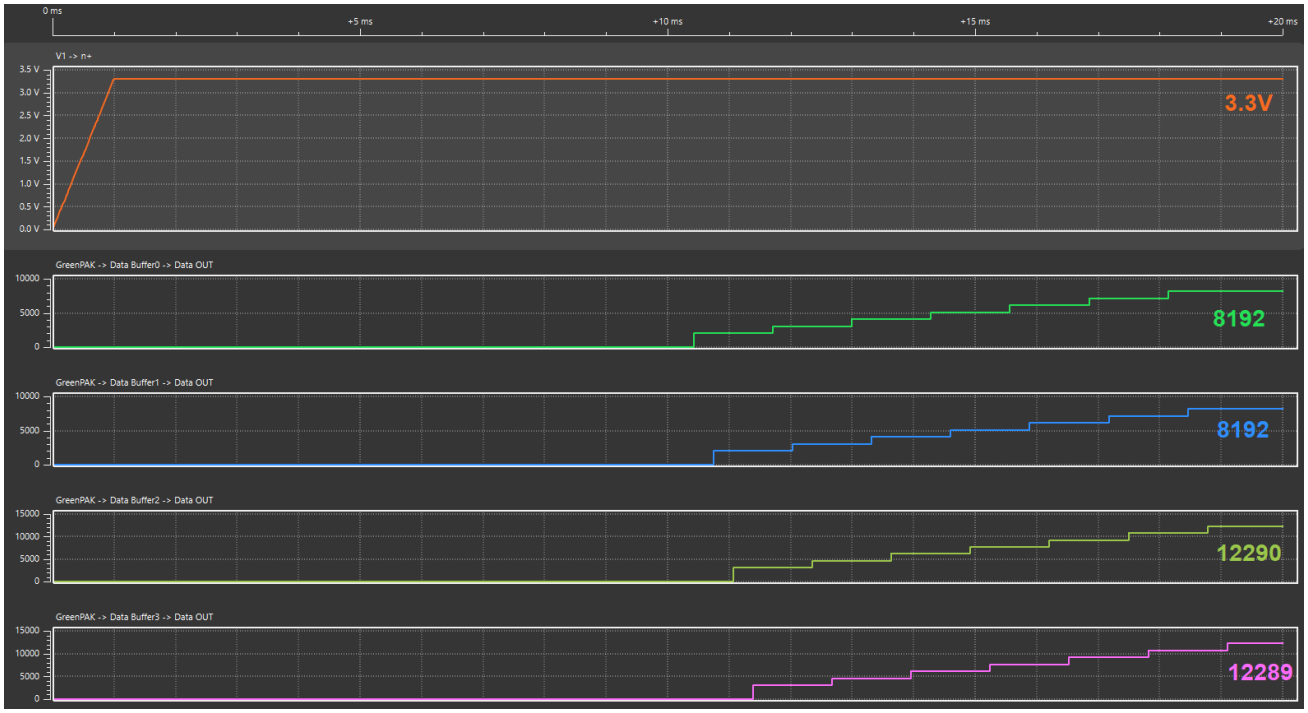


Figure 9: Simulation Result, Go Configure Screenshot

6.4 Output Data Interpretation

To accurately interpret output data, two formulas should be used, for single-ended and differential inputs respectively.

$$Xse = \frac{data,dec \times Vref,mV}{14\ bit \times Gain}$$

$$Xdiff = \frac{(data,dec - 8192) \times Vref,mV}{14\ bit \times Gain}$$

So, for each channel, we get:

$$Xch0 = \frac{8192 \times 1620}{16383 \times 1} = 810\ (mV)$$

$$\boldsymbol{Xch1 = \frac{8192 \times 1620}{16383 \times 2} = 405\ (mV)}$$

$$\boldsymbol{Xch2 = \frac{(12290 - 8192) \times 1620}{16383 \times 4} = 101.3\ (mV)}$$

$$\boldsymbol{Xch3 = \frac{(12289 - 8192) \times 1620}{16383 \times 8} = 50.6\ (mV)}$$

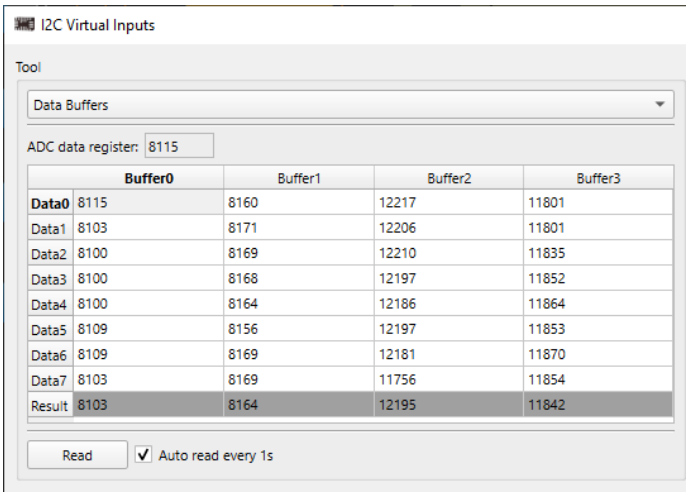
As we see from the calculations, the result is accurate.

6.5 Real-life Testing

To test the design in real-life conditions the **GreenPAK Advanced Development Platform** was used. Instead of the virtual voltage sources, a built-in voltage generator was used for channels 0 and 1, and an external power supply for channels 2 and 3 was used. The voltages are 810 mV, 404 mV, 101.2 mV, and 50,6 mV respectively. Measurements were made using ProsKit MT-1710 multimeter which has an accuracy of ±(0.5%+4). This should be kept in mind when comparing the results.

To read the results start emulation and click on the **I2C Virtual Outputs** button on the upper tool panel, then select Data Buffers and click Read. To read the data periodically, check the **Auto read every 1s** box.

By default, the data is presented in hex, but if right-click on any data a selection window will appear where a decimal data presentation can be chosen, see Figure 10.



	Buffer0	Buffer1	Buffer2	Buffer3
Data0	8115	8160	12217	11801
Data1	8103	8171	12206	11801
Data2	8100	8169	12210	11835
Data3	8100	8168	12197	11852
Data4	8100	8164	12186	11864
Data5	8109	8156	12197	11853
Data6	8109	8169	12181	11870
Data7	8103	8169	11756	11854
Result	8103	8164	12195	11842

Figure 10: Simulation Result, Go Configure Screenshot

The measured voltage is:

$$Xch0 = \frac{8103 \times 1620}{16383 \times 1} = 801.2\ (mV)$$

$$\boldsymbol{Xch1 = \frac{8164 \times 1620}{16383 \times 2.02} = 399.6\ (mV)}$$

$$\boldsymbol{Xch2 = \frac{(12195 - 8192) \times 1620}{16383 \times 4.01} = 98.7\ (mV)}$$

$$\boldsymbol{Xch3 = \frac{(11842 - 8192) \times 1620}{16383 \times 7.99} = 45.2\ (mV)}$$

Note: Gain values in the equations above were taken from the datasheet.

To calculate error relative to full scale, the formula below should be used:

$$\delta ch = \frac{|V - Xch|}{Vref} \times 100\%$$

So, the error for each channel is:

$$\delta ch0 = \frac{|V2 - Xch0|}{Vref} \times 100\% = \frac{|810 - 801.2|}{1620} \times 100\% = 0.5\%$$

$$\delta ch1 = \frac{|V3 - Xch1|}{Vref} \times 100\% = \frac{|404 - 399.6|}{1620} \times 100\% = 0.3\%$$

$$\delta ch2 = \frac{|V4 - Xch2|}{Vref} \times 100\% = \frac{|101.2 - 98.7|}{1620} \times 100\% = 0.15\%$$

$$\delta ch3 = \frac{|V5 - Xch3|}{Vref} \times 100\% = \frac{|50.6 - 45.2|}{1620} \times 100\% = 0.33\%$$

However, there are methods that allow decreasing the error significantly by compensating for the PGA input offset voltage and system noise. Such methods are explained in the next chapter.

7. Error Sources and Methods of Increasing Accuracy

The main error sources are:

- PGA output headroom
- System noise
- PGA input offset voltage
- PGA gain error

7.1 Dealing With Headroom

According to the datasheet, the PGA linear output range starts from ~35 mV. So, when measuring small signals, it is not recommended to use a Single-ended input mode. The Differential input mode (Vref/2 biased diff. in, s/e out) handles near GND without any issues.

Also, in the Instrumentation amplifier mode, output headroom should be considered. One should keep in mind that the PGA in this mode has a differential output that operates relative to ADC_Vref / 2. Meaning, that the voltage on one output increases (going to ADC_Vref) while on the other decreases (going to GND).

For any input mode when choosing gain, saturation should be avoided.

7.2 Dealing With System Noise

Filtering out the noise can be achieved by using Data Buffers in Moving Average mode. It is possible to connect up to four buffers in series, see Figure 11.

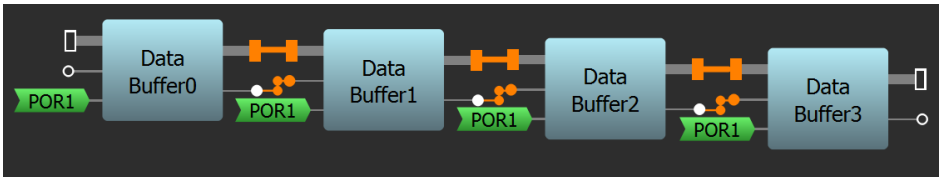


Figure 11: Data Buffers Connected in Series, Go Configure Screenshot

7.3 PGA Input Offset Compensation

The ADC has a System calibration function that allows compensating for the input offset in differential mode. For this purpose, Channel 0 can be used. Channel 0 and Channel 1 must both be configured to differential input with the same settings. Connect both Channel 0 inputs with the non-inverting input of Channel 1 and apply to them a common mode voltage (external or from built-in DAC). The input voltage source should be connected to Channel 1 inputs see Figure 12.

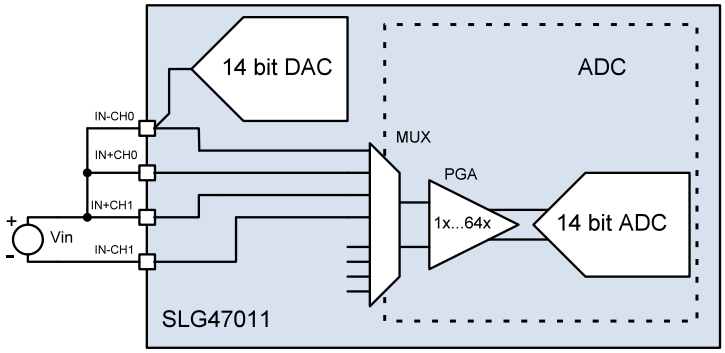


Figure 12: PGA Connection for Input Offset Compensation

To trigger the process of System calibration, the **Start conversion** input should be low and a short high-level signal must be applied to the **Calibration start** input (rising edge sensitive). Right after that, a high-level signal should be applied to **Start conversion** input again. This process can be repeated periodically using additional CNT/DLYs and other logic macrocells thus, keeping the device always calibrated regardless of power supply, temperature, and other factor fluctuations.

The same method can be applied to Channels 2 and 3.

7.4 PGA Gain Error Compensation

As can be seen from the datasheet, the gain differs from the ideal value. However, it can be compensated using the MathCore macrocell by multiplying the ADC data by a constant value. In addition, the Right shift function allows to multiply the data by a fractional number. Right shift data by N equals data divided by 2^N.

For example, if we need to multiply data by 1.03:

$$data \times 1.03 = \frac{\text{data} \times 33751}{32768} = data \times 33751 \gg 15$$

Additionally, it should be noted that for differential input modes, gain compensation by using the multiply MathCore function also requires memory table correction by constant C to achieve the best accuracy.

$$\boldsymbol{C = \frac{ADCresolution}{2} \times (1 - \frac{Gain_{typ}}{Gain_{real}})},$$

Where:

$$\boldsymbol{ADCresolution = \frac{16383}{2} = 8192} \text{ for 14-bit}$$

7.5 General Data Acquisition Recommendations

Input Recommendations

- Consider GPIO input leakage current. It may cause an additional voltage drop across the external components
- Consider PGA input resistance (modes 4, 5a, and 5b, see Figure 2)
- Use anti-aliasing filters. Use differential filters in case of differential input. Choose small resistor values, see Figure 13
- Use PGA in Buffer mode to measure the internal temperature sensor voltage

Sampling Recommendations

- Use as small sampling rate as possible for the application
- Consider PGA closed loop bandwidth (GBWP/Gain) to choose a proper "delay between channels" value. PGA output needs some time to settle down when switching between channels.

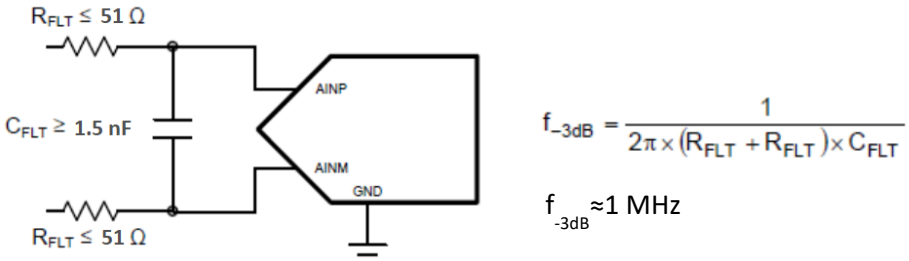


Figure 13: PGA Input Offset Filter

8. Conclusions

This application note shows practical use cases of using the ADC along with its PGA. It explains all nuances for every input mode, considers error sources and gives recommendations on error compensation methods and techniques.

9. Revision History

Revision	Date	Description
1.00	Sep 24, 2024	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.